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Physics-Based DC Compact Modeling of Schottky Barrier and Reconfigurable Field-Effect Transistors

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***Abstract*—A closed-form and physics-based compact model is presented for calculating the DC characteristics of Schottky barrier field-effect transistors and dual gated reconfigurable field-effect transistors. The given model calculates the charge-carrier injection over the Schottky barriers. This current is separated into a field emission current, given by charge carriers tunneling through the Schottky barriers and a thermionic emission current, given by charge carriers overcoming the Schottky barriers. The model verification is done by comparing the model results to measurements and TCAD simulations.**

***Index Terms*—SBFET, RFET, compact modeling, closed-form, Schottky barrier, thermionic emission, field emission, tunneling current**

I. Introduction

THE reconfigurable field-effect transistor (RFET) technology that has been demonstrated in [1] gained attention, because of the application possibilities which differ from regular metal oxide semiconductor field-effect transistors (MOSFETs). Those devices come with an additional gate, which is used to control the device's polarity, leading to an increased device functionality, and can potentially reduce the complexity of electronic circuits [1]–[3]. The given RFET devices rely on the same charge carrier injection principle over Schottky barriers as Schottky barrier field-effect transistors (SBFETs) [4]. However, with the two gates of those devices, where one gate covers the source-channel sided and the other gate covers the drain-channel sided Schottky junction, the charge carrier injection at both contacts can be controlled individually, so one gate - the program gate (PG) - can be used to determine the polarity of the device, while the other gate - the control gate (CG) - controls the actual current flow like in regular MOSFET [1], [5]. The possibility of changing the device's polarity, which means switching between n- and p-type characteristics by changing the PG's bias, enables their usage in reconfigurable logic circuits, like those shown in [2], [3].

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The demand for a compact model, which consists of simple and numerically efficient equations while providing a good fit to measured device characteristics, arises from the need of circuit simulations in a SPICE environment featuring RFET devices. In [6] we introduced the basics of a closed-form and physics-based compact model that fulfills the given conditions and is applicable to SBFETs and configured RFETs. This work gives a more detailed view of the model derivation, provides extensions regarding a consistent modeling of the transistor's output characteristics, and shows additional results for the application of this model.

In order to validate the compact model, based on the measurements from [7], Technology Computer-Aided Design (TCAD) simulations are done with TCAD Sentaurus [8]. These simulations, that use the parameters from [9], are used to simulate the device under various bias conditions. Section II gives a quick overview of the covered device structure. Section III shows the derivation of the compact model and section IV the results, followed by a conclusion in section V.

II. Devices

The presented model works uniformly on SBFET and RFET devices. These devices are usually omega-shaped gate or

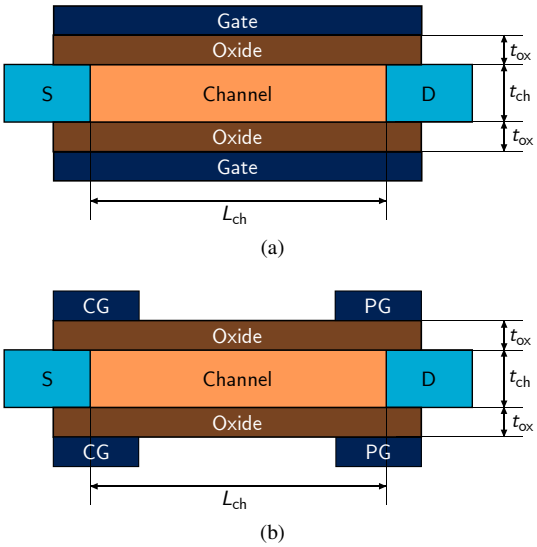

Fig. 1. Schematic cross-section of (a) an SBFET and (b) an RFET with the relevant geometric parameters for the compact model. Typical geometric parameters are shown in table I.

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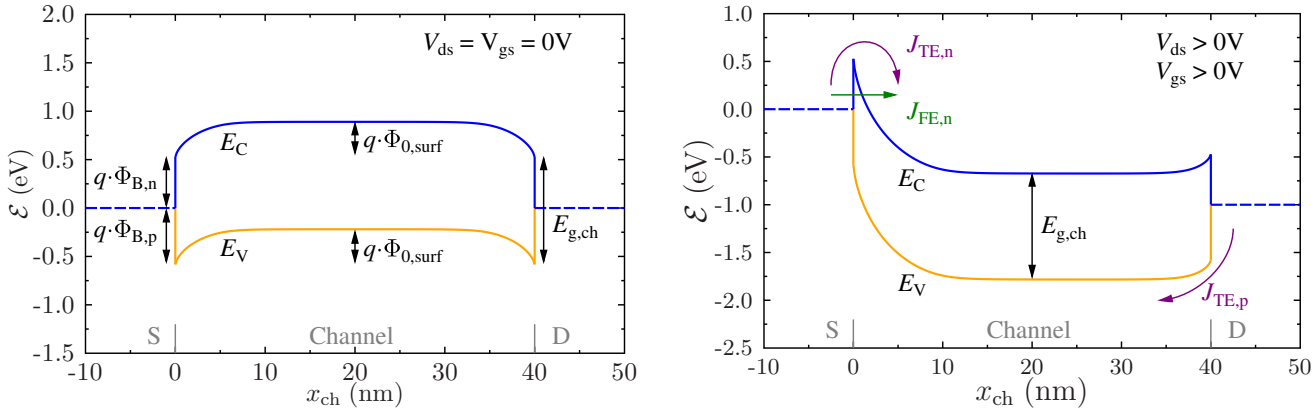


(a) (b)

Fig. 2. Example band diagrams of an SBFET device. (a) band diagram in the device's off-state with the relevant band diagram parameters for the compact model. The parameter $\Phi_{0,\mathrm{surf}}$ determines an initial band bending caused by the work functions of the materials and is compensated in the model by a flatband voltage V_{fb}. (b) on-state band diagram with the current contributions, considered in the compact model.

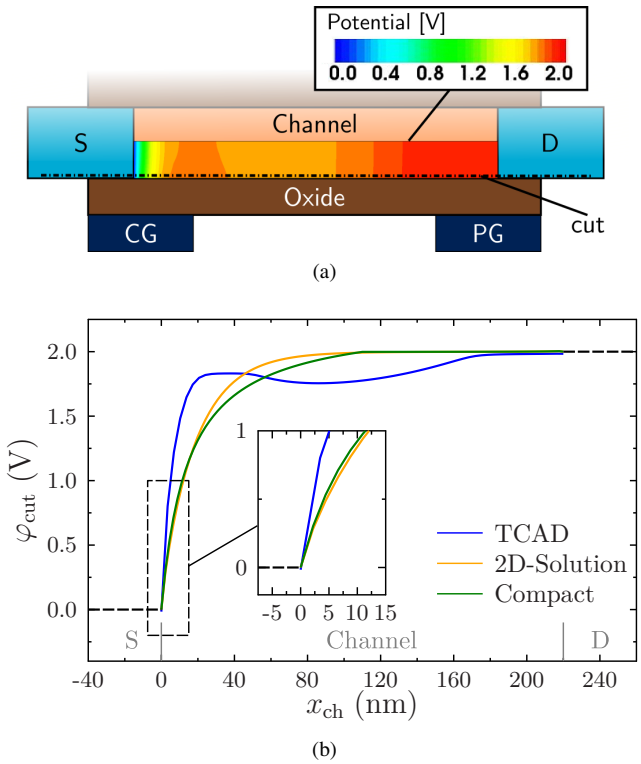
gate-all-around nanowire or nanosheet structures, where the nanowire channel consists of a semiconductor that is attached to the metallic source and drain regions [1], [5], [10]–[13]. The metal-semiconductor junctions form Schottky barriers, that block a charge-carrier current flow in the device's off-state. While the SBFET consists of one gate area covering the entire device, the RFET has two independently controllable gate contacts, each covering one Schottky junction. A cross-section of those devices is shown in Fig. 1. Typical device parameters used with this model are shown in table I. Figure 2 demonstrates the basic working principle of those devices (in this case of an SBFET). While Fig. 2a shows the important band diagram parameters used in the compact model, Fig. 2b shows the device in the on-state with the associated current contributions, that are explained in the next section.

III. Modeling Approach

The current characteristics of the devices under investigation is mainly dominated by the Schottky barriers, which means that in the device's off-state the Schottky barriers at the source and drain junctions block the current flow, while in the on-state the Schottky barriers are permeable for charge carriers. The current over the Schottky barriers is separated into two different types of current. The current which is dominant in the device's off-state is the thermionic emission (TE) current, given by charge carriers that are able to overcome the Schottky barrier [14]. The dominating current contribution in the on-state is the field Emission (FE) current, which is given by the charge carriers tunneling through the Schottky barriers [14]. Those contributions are shown as an example in the energy band diagram in Fig. 2b as FE current for electrons ($J_{\mathrm{FE,n}}$), as well as TE current for electrons ($J_{\mathrm{TE,n}}$) and holes ($J_{\mathrm{TE,p}}$). The compact model, that is introduced in this paper, is based on the charge carrier injection through Schottky barriers and uses both types of current contribution in order to calculate the total device current. Therefore, it is valid as long as the Schottky barriers are the dominant current blocking mechanisms in the device, compared to the device's channel resistance, which is usually given for devices with a channel length smaller than one micrometer.

A. Potential Model

In a first step, the electrostatic potential in the device's channel region is calculated and thereto the band diagram and the electric field close to the junctions. The determination



(a) (b)

Fig. 3. Electrostatic potential of the device from section IV at $V_{\mathrm{ds}} = V_{\mathrm{pg}} = V_{\mathrm{cg}} = 2\,\mathrm{V}$. (a) device structure with the simulated 2D potential along the channel. The 2D potential was simulated using TCAD Sentaurus. (b) potential along the cut line shown in (a) and comparison of the TCAD simulated value (blue) to the result of the 2D analytic closed-form potential model (orange) and the compact potential solution (green) from (2). The dashed box shows a zoom of the potential at the Schottky barrier.

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of the potential is split into two steps. First, an adapted version of the 2D analytical closed-form potential model from [15], [16] is used to calculate the electrostatic potential at some auxiliary points close to the Schottky junctions and in the middle of the channel. This model uses the Schwarz-Christoffel transformation method to calculate the potential inside a double-gate field-effect transistor structure, like the one shown in Fig. 1 [15], [16]. However, this potential model does not consider accumulated charges in the channel at higher gate-source voltages V_{gs}. In order to increase the accuracy of this calculation even for higher V_{gs}, an effective gate-source voltage V'_{gs} is calculated, which shall include the effect of accumulated charges in the device's channel. For this effective gate-source voltage $V_{\mathrm{gs,TFET}}$ is adapted, which is used in the tunnel field-effect transistor model from [17]. However, compact model comparisons to measurements and TCAD simulations showed that $V'_{\mathrm{gs}} = V_{\mathrm{gs,TFET}}$ is not applicable on the tested RFET devices for all used bias conditions. Therefore, an empirical equation was included, given by

$$V'_{\mathrm{gs}} = [\alpha \cdot V_{\mathrm{gs,TFET}} + (1-\alpha) \cdot V_{\mathrm{gs}}] - V_{\mathrm{fb}}\,, \tag{1}$$

where α is a fitting parameter to increase or reduce the effect of the V'_{gs} saturation and V_{fb} is the flatband voltage which is a fitting parameter that compensates the band bending at $V_{\mathrm{gs}} = 0\,\mathrm{V}$. The later can be induced by the gate material's work function.

With the auxiliary points from the 2D analytical closed-form potential model, similar to [17], in a second step a compact analytical expression (φ_{comp}) for the potential along the channel is introduced:

$$\varphi_{\mathrm{comp}}(x) = \frac{k}{x-l} + m\,. \tag{2}$$

This expression is evaluated at the oxide-channel interface and in the middle of the channel for each Schottky junction (source and drain), where the x-direction is the source-drain direction. k, l and m are the reconstructed parameters by auxiliary points calculated in the first step. With this expression for the compact potential, it is possible to calculate the electric field along the channel by

$$E_{\mathrm{x}}(x) = -\frac{d\varphi_{\mathrm{comp}}(x)}{dx} \tag{3}$$

and the band diagram by adding or subtracting the band parameters $\Phi_{\mathrm{B,n}}$ or $\Phi_{\mathrm{B,p}}$. Figure 3b shows the 2D analytical closed-form potential model as well as the compact potential compared to TCAD Sentaurus simulations at the given bias conditions for the device from section IV. This comparison shows that both potential models have a deviation compared to the TCAD simulation between the source-channel junction and the control gate, which is most likely caused by the influence of the accumulated charges in the channel at the given bias condition, due to their empirical consideration. However, the most important part is close to the source-channel junction in order to estimate the Schottky barrier thickness correctly for the tunneling process. In this region the potentials calculated by the compact model show an acceptable agreement to the TCAD simulation.

B. Field Emission Current

The FE current is given by charge carriers tunneling through the Schottky barriers. For this case the bands have to be sufficiently bent so the thickness of the barrier becomes small enough, as it is shown in Fig. 2b. In order to find a way to describe the FE current density (J_{FE}) analytically, an approach from [4] is used. In this approach the equation

$$J_{\mathrm{FE}} = \frac{q\mu_{\mathrm{tn}}N_{\mathrm{C}}}{k_{\mathrm{b}}\vartheta} \cdot \int_{\mathcal{E}_{\mathrm{min}}}^{\mathcal{E}_0} f_{\mathrm{m}}(\mathcal{E})[1-f_{\mathrm{ch}}(\mathcal{E})] \times |\vec{E}(\mathcal{E})| \cdot T(\vec{E},\mathcal{E}) \cdot d\mathcal{E}\,, \tag{4}$$

that describes the tunneling process through the Schottky barrier, but is not solvable analytically, is approximated by

$$J_{\mathrm{FE}} \approx \frac{q\mu_{\mathrm{tn}}N_{\mathrm{C}}}{k_{\mathrm{b}}\vartheta} \cdot \int_{\mathcal{E}_{\mathrm{min}}}^{\mathcal{E}_0} \frac{1}{4}\exp(-a(\mathcal{E}-E_{\mathrm{f}})^2) \times b \cdot \exp(-c(\mathcal{E}_0-\mathcal{E})) \cdot d\mathcal{E}\,, \tag{5}$$

where q is the elementary charge, N_{C} is the effective density of states in the conduction band (for tunneling holes the effective density of states in the valence band N_{V} is used), k_{b} is the Boltzmann constant and ϑ is the temperature. The mobility μ_{tn} for electrons (or μ_{tp} for holes) is an adjustable fitting parameter of the model, which is part of (4), because this equation combines tunneling with drift-diffusion effects [4]. The first part of the integral in (4) is the product of the Fermi functions and represents the occupation probability $f_{\mathrm{m}}(\mathcal{E})$ for electrons in the source region at energy epsilon and $[1-f_{\mathrm{ch}}(\mathcal{E})]$ for holes in the channel region [4], [14]. In the approximation from (5) this first part is approximated by a Gaussian distribution function $\frac{1}{4}\exp(-a(\mathcal{E}-E_{\mathrm{f}})^2)$, where E_{f} is the Fermi energy level [4]. The second part of the integral in (4) is the electric field multiplied with the tunneling probability $|\vec{E}(\mathcal{E})| \cdot T(\vec{E},\mathcal{E})$, which is approximated by an exponential function $b \cdot \exp(-c(\mathcal{E}_0-\mathcal{E}))$ in (5) [4]. The Fermi energy level E_{f} used for the tunneling calculation is the Fermi level of the

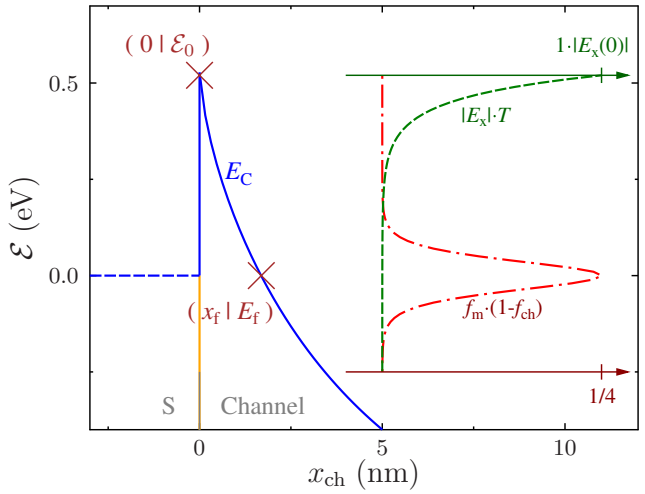

Fig. 4. Visualization of the tunneling equation components at the source-side Schottky barrier for tunneling of electrons. The figure shows some important variables of the compact model, as well as the components of (4) as a function of the energy $\mathcal{E}$, which are the electric field multiplied with the tunneling probability (green) and the product of the Fermi functions (red).

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metal. The x-position where the bent conduction band E_C (or the valence band E_V in case of tunneling holes) reaches the metal's Fermi level is called x_f. This position is estimated to have the highest FE-current contribution per energy level, as shown in Fig. 4. The relation between E_f and x_f is expressed by using (2) as

$$E_\mathrm{f} = -q \cdot \varphi_\mathrm{comp}(x_\mathrm{f}) + q \cdot \Phi_\mathrm{B,n}\,, \tag{6}$$

in case of tunneling of electrons where the conduction band is bent below E_f. For tunneling of holes the valence band is relevant for the tunneling process and $-q \cdot \Phi_\mathrm{B,p}$ is used in (6) instead of $+q \cdot \Phi_\mathrm{B,n}$. If the conduction band is not bent below the metal's Fermi level, x_f will be limited to $l_\mathrm{ch}/2$. The upper boundary of the integrals ($\mathcal{E}_0$), is the highest energy value where tunneling can occur, which is the top of the Schottky barrier (see also $\mathcal{E}_0$ in Fig. 4). The lower limit of the integrals in (4) and (5) is positioned in the middle of the channel, so that $\mathcal{E}_\mathrm{min} = -q \cdot \varphi_\mathrm{comp}(l_\mathrm{ch}/2) + q \cdot \Phi_\mathrm{B,n}$. This lower boundary is the lowest energy value where tunneling charge carriers are theoretically possible. However, due to the increasing tunneling lengths, the tunneling current contributions lower than E_f are decreasing rapidly, so that $\mathcal{E}_\mathrm{min}$ is a formal minimum. a, b and c of (5) are energy independent coefficients, which are reconstructed like shown in [4] and given by

$$a = \gamma_\mathrm{n} \cdot \frac{\pi}{16 \cdot (k_\mathrm{b}\vartheta)^2}, \tag{7}$$

$$b = E_\mathrm{x}(0) \cdot T(0) \tag{8}$$

and

$$c = \ln\left(\frac{1}{b} \cdot E_\mathrm{x}(x_\mathrm{f}) \cdot T(x_\mathrm{f})\right) \cdot \frac{1}{(E_\mathrm{f} - \mathcal{E}_0)} \tag{9}$$

$E_\mathrm{x}(x)$ is the compact electric field in x-direction from (3) and $T(x)$ is the tunneling probability at position x [4]. The fitting parameter γ_n for electrons (or γ_p for holes) is in the range of $0 \ldots 1$ and shall compensate the error for low V'_gs caused by the Gaussian approximation from (5). The tunneling probability $T(x = 0)$ must be 1, because $x = 0$ is exactly the top of the barrier where the tunneling thickness is zero. The tunneling probability at $x = x_\mathrm{f}$, which is at the peak of the Gaussian distribution (see Fig. 4), is calculated by a modified version of the Wentzel-Kramers-Brillouin approximation for triangular tunneling barrier shapes [4], that is given by

$$T(x_\mathrm{f}) = \exp\left(-\frac{4}{3} \cdot \frac{\sqrt{2qm^*} \cdot (\Delta\Phi(x_\mathrm{f}))^{3/2}}{\hbar \cdot |E_\mathrm{x}(0)|}\right). \tag{10}$$

$\hbar$ is the reduced Planck's constant and m^* is either the electron ($m_\mathrm{n} \cdot m_0$) or the hole ($m_\mathrm{p} \cdot m_0$) tunneling mass, which are both used as fitting parameters in the compact model. The parameter $\Delta\Phi$ is the height of the barrier to be tunneled through by charge carriers, which is either given as the potential difference $\Delta\Phi(x_\mathrm{f}) = \varphi_\mathrm{ch}(x_\mathrm{f}) - \varphi_\mathrm{ch}(0)$, in case $\Delta\Phi(x_\mathrm{f})$ is bigger than $\Phi_\mathrm{B,n}$, or it is fixed to $\Phi_\mathrm{B,n}$ otherwise.

Finally, with the equations (7)-(10) the FE current density J_FE can be calculated. As it is demonstrated in [4], (5) can be solved to

$$J_\mathrm{FE} \approx \frac{q\mu_\mathrm{tn}N_\mathrm{C}}{8k_\mathrm{b}\vartheta} \cdot \frac{b\sqrt{\pi}}{\sqrt{a}} \cdot \exp\left(c(E_\mathrm{f} - \mathcal{E}_0) + \frac{c^2}{4a}\right) \times \left[j_\mathrm{erfc}(\mathcal{E}_0) - j_\mathrm{erfc}(\mathcal{E}_\mathrm{min})\right], \tag{11}$$

with

$$j_\mathrm{erfc}(\mathcal{E}) = \mathrm{erfc}\left(\frac{-2a(\mathcal{E} - E_\mathrm{f}) + c}{2\sqrt{a}}\right), \tag{12}$$

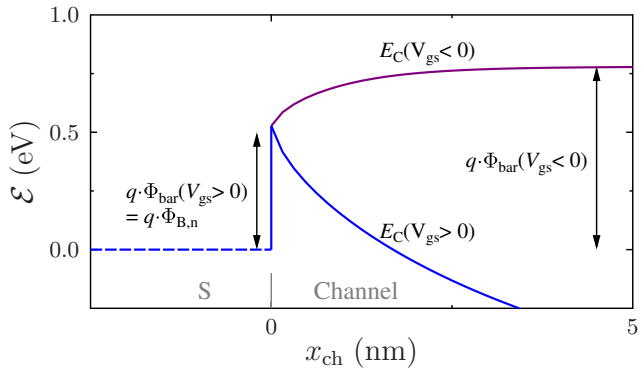

Fig. 5. Energy barriers for the electron TE current at the source-side Schottky barrier. The blue line shows the device in the on-state. In this state, Φ_bar is as high as the Schottky barrier height. The purple line shows the device with negative gate bias. In this state Φ_bar equals the highest potential in the channel.

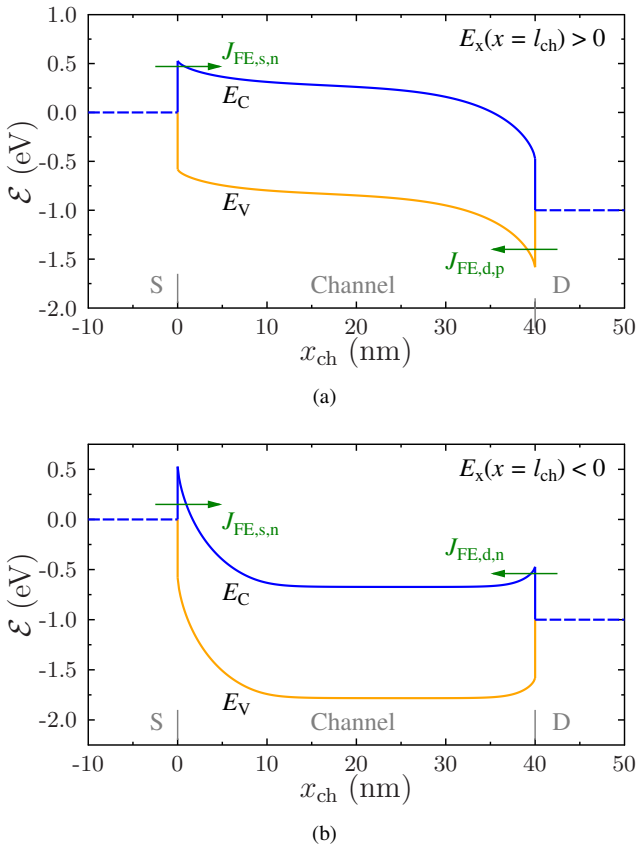

Fig. 6. Example band diagrams at different bias conditions to demonstrate the total FE current calculation. (a) device state that allows an electron FE current ($J_\mathrm{FE,s,n}$) at the source side and a hole FE current ($J_\mathrm{FE,d,p}$) at the drain side. Both currents are contributing to the total FE current ($J_\mathrm{FE,tot}$). (b) device state with a Schottky barrier for electrons on both sides. In the compact model a virtual drain-side FE current ($J_\mathrm{FE,d,n}$) is calculated and subtracted from the source-side injection current ($J_\mathrm{FE,s,n}$), to calculate the total FE current ($J_\mathrm{FE,tot}$).

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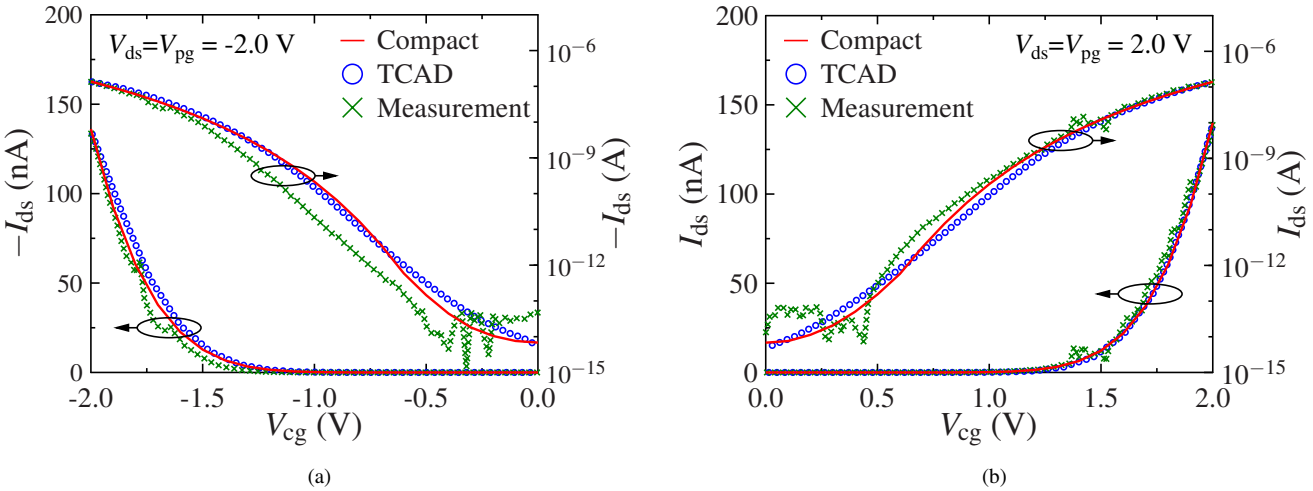

Fig. 7. Transfer characteristics of an RFET device calculated from the compact model (red) compared to TCAD simulations (blue) and measurements (green) from [7] in linear (left axis) and logarithmic (right axis) scale. (a) p-type operation mode ($V_{\mathrm{ds}} = V_{\mathrm{pg}} = -2\,\mathrm{V}$). (b) n-type operation mode ($V_{\mathrm{ds}} = V_{\mathrm{pg}} = 2\,\mathrm{V}$).

where $\mathrm{erfc}(x)$ is the complementary error function. This equation for the FE current density is valid for electrons, tunneling through Schottky barriers at the conduction band. The FE current density for holes works similarly, but with different parameters.

C. Thermionic Emission Current

The TE current consists of the charge carriers which overcome the energy barriers, instead of tunneling through them. In case of electrons it is calculated by

$$J_{\mathrm{TE}} = A^* \vartheta^2 \cdot \exp\left(-\frac{q\Phi_{\mathrm{bar}}}{k_{\mathrm{b}}\vartheta}\right) \cdot \left[1 - \exp\left(-\frac{qV_{\mathrm{ds}}}{k_{\mathrm{b}}\vartheta}\right)\right], \quad (13)$$

where A^* is the effective Richardson constant and Φ_{bar} is the calculated barrier height that charge carriers have to overcome [4], [14]. The gate voltage in (13) is considered in terms of the parameter Φ_{bar}, as demonstrated in Fig. 5. If a Schottky barrier forms where the charge carriers can tunnel through, the barrier height Φ_{bar} will be given by $\Phi_{\mathrm{B,n}}$ itself (see $q \cdot \Phi_{\mathrm{bar}}(V_{\mathrm{gs}} > 0)$ in Fig. 5). In case of a reversed electric field at the interface, it is given by the potential barrier in the channel (see $q \cdot \Phi_{\mathrm{bar}}(V_{\mathrm{gs}} < 0)$ in Fig. 5), calculated with the 2D closed-form potential model from section III-A. For the TE current of holes an equation similar to (13) is defined.

D. Total Current

The so far described current components (FE and TE current) are both contributing to the total device current (I_{ds}). While the previous sections mainly focused on the FE and TE current calculations at the source junction, those currents also appear at the drain junction. In n-type operation mode there is an electron current at the source side and a hole current at the drain side of the device and vice versa for p-type operation mode. While the TE current, given by (13), depends on the drain-source voltage V_{ds}, the FE current according to (5) is independent of V_{ds}. This means that even for low V_{ds} high FE currents would be possible, in case of high gate voltages V_{gs}. In order to prevent this effect and bring a V_{ds} dependency into the expression for the FE current, a current balancing model is included at the drain side. In case that the drain potential is bigger than the potential in the middle of the channel (see Fig. 6a), both FE current contributions are included regularly into the total current. In case that the potential in the channel of the device is bigger than the drain potential, a virtual FE current is calculated which gets subtracted from the source current (see Fig. 6b). So if $V_{\mathrm{ds}} = 0$ and a gate voltage was applied, the source FE current and the virtual drain FE current would be equally high and cancel out each other. For the total FE current density of the device this results in

$$J_{\mathrm{FE,tot}} = \begin{cases} J_{\mathrm{FE,s,n}} - J_{\mathrm{FE,d,n}}, & E_{\mathrm{x}}(x = l_{\mathrm{ch}}) < 0 \\ J_{\mathrm{FE,s,n}}, & E_{\mathrm{x}}(x = l_{\mathrm{ch}}) = 0 \\ J_{\mathrm{FE,s,n}} + J_{\mathrm{FE,d,p}}, & E_{\mathrm{x}}(x = l_{\mathrm{ch}}) > 0 \end{cases} \quad (14)$$

in the n-type operation mode and the on-state and similarly for other operation modes. $E_{\mathrm{x}}(x = l_{\mathrm{ch}})$ is the electric field in x-direction at the drain-channel junction.

The total TE current density is calculated with the TE current contributions from electrons and holes, given by

$$J_{\mathrm{TE,tot}} = J_{\mathrm{TE,n}} + J_{\mathrm{TE,p}}. \quad (15)$$

Considering both total current densities from (14) and (15) the total drain current of the device is calculated by

$$I_{\mathrm{ds}} = W_{\mathrm{ch}} \cdot t_{\mathrm{ch}}(J_{\mathrm{FE,tot}} \cdot t_{\mathrm{eff,FE}} + J_{\mathrm{TE,tot}} \cdot t_{\mathrm{eff,TE}}), \quad (16)$$

where W_{ch} is the channel width and t_{ch} is the channel thickness of the DG structure (see Fig. 1). The channel width W_{ch} is needed, because the used potential model from section III-A works with a 2D planar structure. Therefore, instead of calculating a nanowire structure, the model calculates the currents inside the planar structure from Fig. 1, which gets stretched in the third dimension by W_{ch}. To consider the fact that the FE current is the main on-current where the current flow is mostly located at the channel-oxide interface and the TE current flows mainly in the center of the device, two effective thicknesses ($t_{\mathrm{eff,FE}}$ and $t_{\mathrm{eff,TE}}$) are introduced in

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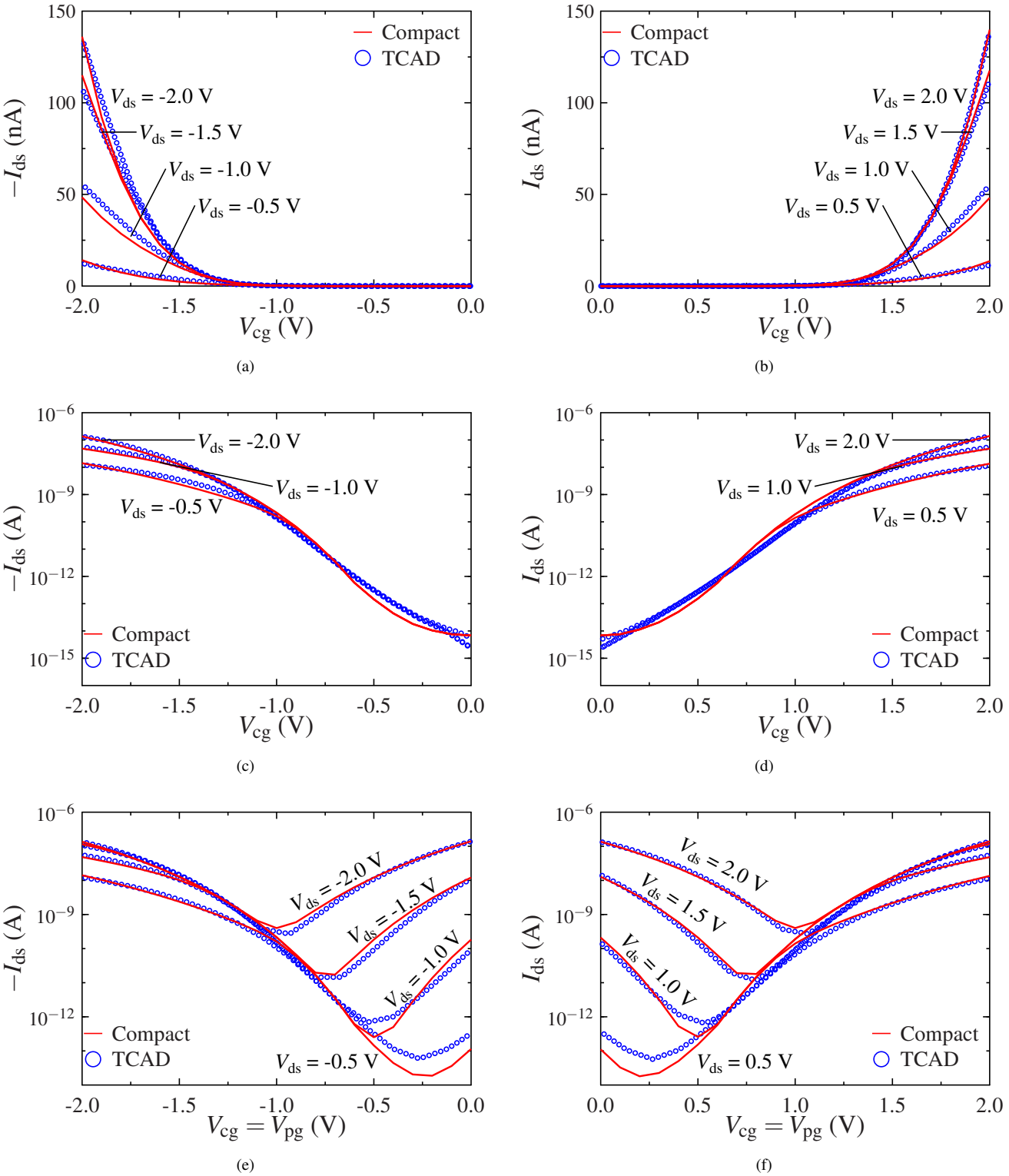

Fig. 8. Transfer characteristics calculated from the compact model (red) compared to TCAD simulations (blue). (a) p-type operation mode with $V_{pg} = -2\,V$ and (b) n-type operation mode with $V_{pg} = 2\,V$ in linear scale. (c) and (d) results from (a) and (b) in logarithmic scale. (e) transfer characteristics for various negative drain voltages and (f) transfer characteristics for various positive drain voltages, while the device is driven in SBFET mode, in logarithmic scale.

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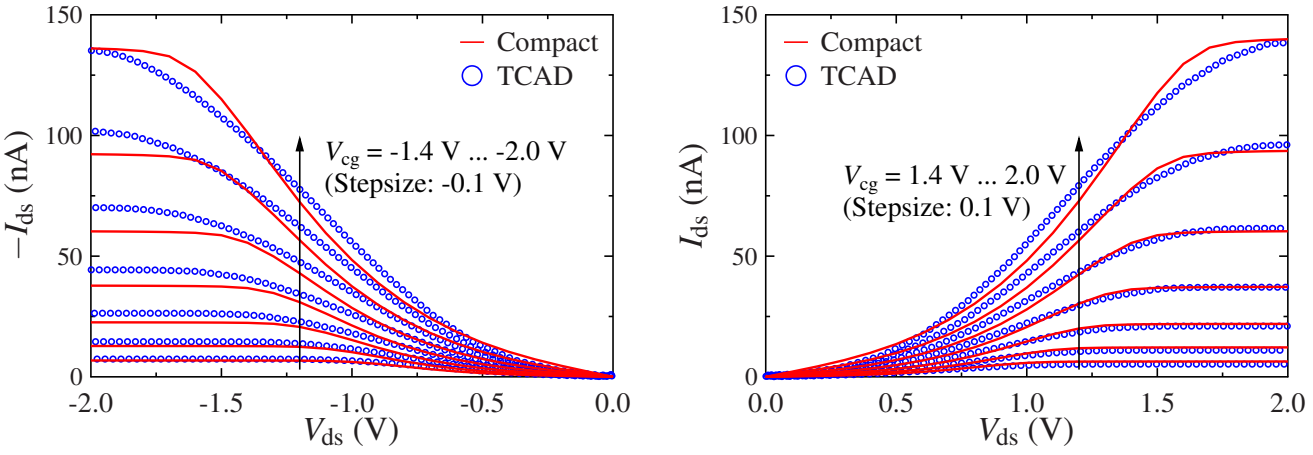

(a) (b)

Fig. 9. Output characteristics calculated from the compact model (red) compared to TCAD simulations (blue). (a) p-type operation mode for various CG voltages with $V_{\mathrm{pg}} = -2\,\mathrm{V}$. (b) n-type operation mode for various CG voltages with $V_{\mathrm{pg}} = 2\,\mathrm{V}$.

(16), each in the range of $0 \ldots 1$. Equation (16) leads to the total drain current which is valid for SBFET devices.

In order to make the model applicable to RFETs, that have been configured as n-type or p-type, one of the two charge carrier types get suppressed in the FE current calculation, depending on the PG bias. In case of $V_{\mathrm{pg}} \gg 0$ the FE current density for holes $J_{\mathrm{FE,p}}$ is set to 0 and in case of $V_{\mathrm{pg}} \ll 0$ the FE current density for electrons $J_{\mathrm{FE,n}}$ is set to 0.

IV. Model Results and Verification

The model verification is done by TCAD simulations and measurements. Therefore, the measurement of the device from [7] is used. In order to obtain additional results, the TCAD simulation from [9] is used to simulate the device with various bias conditions. Table I shows the geometric and material parameters and table II shows the fitting parameters that are used for the compact model. While the real and the simulated structures are gate-all-around nanowire structures, the compact model calculates a double gate structure. Therefore, in the model a channel width W_{ch} is used which is in the same order of magnitude than the nanowire's diameter. The discrepancy between those two structures is compensated by the model's fitting parameters.

TABLE I
Device geometries and material parameters of the device under investigation in Fig. 7-9

Parameter	Value
L_{ch} [nm]	220
W_{ch} [nm]	12
t_{ch} [nm]	12
t_{ox} [nm]	8
$t_{\mathrm{eff,FE}}$ [-]	0.2
$t_{\mathrm{eff,TE}}$ [-]	0.8
$\epsilon_{\mathrm{r,ox}}$ [-]	3.9
$\epsilon_{\mathrm{r,ch}}$ [-]	11.7
$E_{\mathrm{g,ch}}$ [eV]	1.1696
$\Phi_{\mathrm{B,n}}$ [V]	0.5800
$\Phi_{\mathrm{B,p}}$ [V]	0.5896

TABLE II
Fitting parameters used in the compact model of the device under investigation in Fig. 7-9

Parameter	Value
V_{fb} [V]	0.0
α [-]	0.5
μ_{tn} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	59.78
μ_{tp} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	43.59
m_{n} [-]	0.10
m_{p} [-]	0.09
γ_{n} [-]	0.2
γ_{p} [-]	0.2

Figure 7 shows the device transfer characteristics with the actual measurement, the corresponding TCAD fit and the model fit, in linear and logarithmic scale. Figure 7a shows the p-configured version with a program gate voltage of $V_{\mathrm{pg}} = -2\,\mathrm{V}$ and a drain voltage of $V_{\mathrm{ds}} = -2\,\mathrm{V}$. Figure 7b shows the n-configured version with a program gate voltage of $V_{\mathrm{pg}} = 2\,\mathrm{V}$ and a drain voltage of $V_{\mathrm{ds}} = 2\,\mathrm{V}$. The model shows a good agreement compared to the TCAD simulation results. There are slight deviations in the p-type characteristics, because of the unsteadiness in the measured curve. Figure 8 and 9 depict various TCAD simulation scenarios compared to the model. Figure 8a to 8d show the same transfer characteristics as Fig. 7, but with additional drain voltages. Figure 8e and 8f show the results of the SBFET calculation. In these two simulations the PG was not fixed, but biased similarly to the CG ($V_{\mathrm{pg}} = V_{\mathrm{cg}}$), which leads to a device behavior like an SBFET. Figure 9 shows one simulated output characteristics per operation mode (with a fixed PG voltage). Although the model shows some deviations in the curvature, which may be attributed to the neglected effect of current control by the channel conductivity, the overall behavior is well captured by the compact model.

V. Conclusion

In this paper a physics-based compact model that is applicable uniformly on SBFETs and RFETs in a fixed configuration

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is derived and presented. The model, which is based on the current injection at the Schottky barriers and applicable on devices with a negligible channel resistance influence, can be switched between SBFET-, p- or n-type operation mode easily. Additionally, with a set of analytical closed-form equations and a total number of eight fitting parameters, the model can be implemented and used in circuit simulation tools for time-efficient simulations of this technology. Finally, the functionality of the model has been demonstrated by comparisons with measurements and TCAD simulations, which show good agreement.

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