COMPACT MODELING OF GATE TUNNELING LEAKAGE CURRENT IN ADVANCED NANOSCALE SOI MOSFETS

Ghader Darbandy

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Compact Modeling of Gate Tunneling Leakage Current in Advanced Nanoscale SOI MOSFETS

Ghader Darbandy

Doctoral Thesis

2012

Universitat Rovira i Virgili
Department of Electronic
Electrical and Automatic
Control Engineering

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Ghader Darbandy

Compact Modeling of Gate Tunneling Leakage Current in Advanced Nanoscale SOI MOSFETs

Doctoral thesis supervised by
Professor Benjamin Iñiguez

Department of Electronic, Electrical and Automatic Control Engineering

Tarragona
2012

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UNIVERSITAT
ROVIRA I VIRGILI
ESCOLA TÈCNICA SUPERIOR D'ENGINYERIA
DEPARTAMENT D'ENGINYERIA ELECTRONICA, ELÈCTRICA I AUTOMÀTICA

Avinguda dels Països Catalans, 26
Campus sescelades
43007 Tarragona
Tel. (977) 55 96 10
Fax (977) 55 96 05
e-mail: secelec@etse.urv.es
http://www.etse.urv.es/DEEEA/

I STATE that the present study, entitled "**Compact Modeling of Gate Tunneling Leakage Current in Advanced Nanoscale SOI MOSFETs**", presented by Ghader Darbandy for the award of the degree of the Doctor, has been carried out under my supervision at the Department of Electrical, Electronic and Automatic Control Engineering of this university, and that it fulfils all the requirements to be eligible for the European Doctorate Award.

Doctoral Thesis Supervisor

Prof. Benjamin Iñiguez

Tarragona, October 2012

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Acknowledgements

I would like to express my deepest appreciation to all those who have made this thesis to be materialized. First of all, I am grateful to my master Prof. Benjamin Iñiguez for his invaluable and endless advice and support. He directed me to interesting topics of research and at the same time permitted me to follow my own ideas. He has not only taught me about compact modeling, but he has also taught how to stay confident, how to have a positive attitude and ….

I would like to express my greatest appreciation to Prof. Antonio Cerdeira, Prof. Magali Estrada and Prof. Jamal Deen for their discussions and advices. Prof. Lluis Marshal, the head of the Department of Electronic, Electric and Automatic Engineering and all personnel of "the department" are sincerely acknowledged for their warm and helpful collaborations.

I would also like to thank Dr. Thomas Gneiting for giving me the opportunity for my six months research stage in his company (AdMOS). My special thanks go to all of my friendly colleagues at AdMOS Company in Germany.

To all my friends, especially Francois Lime, Muthupandian Cheralathan, Alejandra Castro Carranza, Mike Schwarz, Thomas Holtij and in particular Maria Mendez Malaga for the helps (who introduced me to the Spanish language and culture) thanks for your excellent company and making the enjoyable atmosphere. And Kaveh Yalfani, Zahra Tabookht, and Sara Hajian, thank you for being close to me and supporting me all this time.

I would like to thank my friend of life Elham, who started the life journey with me and gave me the best gift so far, our lovely and sweet son Artin. I deeply appreciate my family and kind brothers for their support and helping me all the difficult times.

… and many others…

Tarragona, Spain,

October, 2012.

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It's our attitude more than our aptitude that makes our altitude.

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…to the memory … of my wonderful parents

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2) **Ghader Darbandy**, Romain Ritzenthaler, Francois Lime, Ivan Garduño, Magali Estrada, Antonio Cerdeira and Benjamin Iñiguez, "Analytical modeling of direct tunneling current through SiO2/high-k gate stacks for the determination of suitable high-k dielectrics for nanoscale double-gate MOSFETs", *Semicond. Sci. Technol.* **26** 045002, (2011).

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Introduction

Transistor is the fundamental building block of modern electronic devices. It is a semiconductor device used to amplify and switch electronic signals and electrical power. The transistor is the key active component in practically all modern electronics. Many consider it to be one of the greatest inventions of the 20th century [1].

The first Silicon transistor was produced by Gordon Teal at Texas Instruments in 1954 [2, 3]. The first Metal Oxide Semiconductor (MOS) transistor actually built was by Kahng and Atalla at Bell Labs in 1960 [4]. Transistors are now part of almost every person's daily life. These devices with a majority of cell phones, laptops, iPods, players and desktop computers have become popular. Users are using such devices for a variety of functions, including internet, email, music, games and video.

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1) Transistor Scaling and its Challenges

One of the main challenges in the MOS transistor is the reduction of device dimension. The main concern is to predict the device performance and how the transistors work and behave as the size of device shrinks down.

"Scaling" refers to reduction of the lateral geometric dimensions of MOSFET devices. In 1965, Gordon Moore (later a founder of Intel Corporation) published his famous observation regarding to the evolution of the transistor density in Integrated Circuits (IC) exponentially over time. "Moore's law" says that the number of transistors on a chip wills approximately double every 18 months [5]. This prediction has been the case for many years and remarkably followed by the semiconductor industry for the last forty years (Figure 1). But even in this early work, there was question of how long this scaling trend could continue [6].

Only the rate of increase in transistor density has been described by Moore's Law, while the reduction of the physical MOS device dimensions has improved both circuit speed and enabled cheaper ICs. In fact, scaling allows for the manufacturing of more devices for the same price [7].

Since the early 1990's semiconductor companies and academia decided to predict the future of semiconductor device industry more precisely. This initiative gave birth to the International Technology Roadmap for Semiconductor (ITRS) organization [8]. The ITRS issues a report every year that serves as a bench mark for the semiconductor industry. The reports represent the best opinion on the directions of research into the type of technology, design tools, equipment and metrology tools that have to be developed in order to keep pace with the exponential progress of semiconductor devices predicted by Moore's law, including time-lines up to about 15 years into the future [6]. Figure 1 shows the evolution of the transistors per chip (Moore's law) predicted by the ITRS 2005 for memory and microprocessor.

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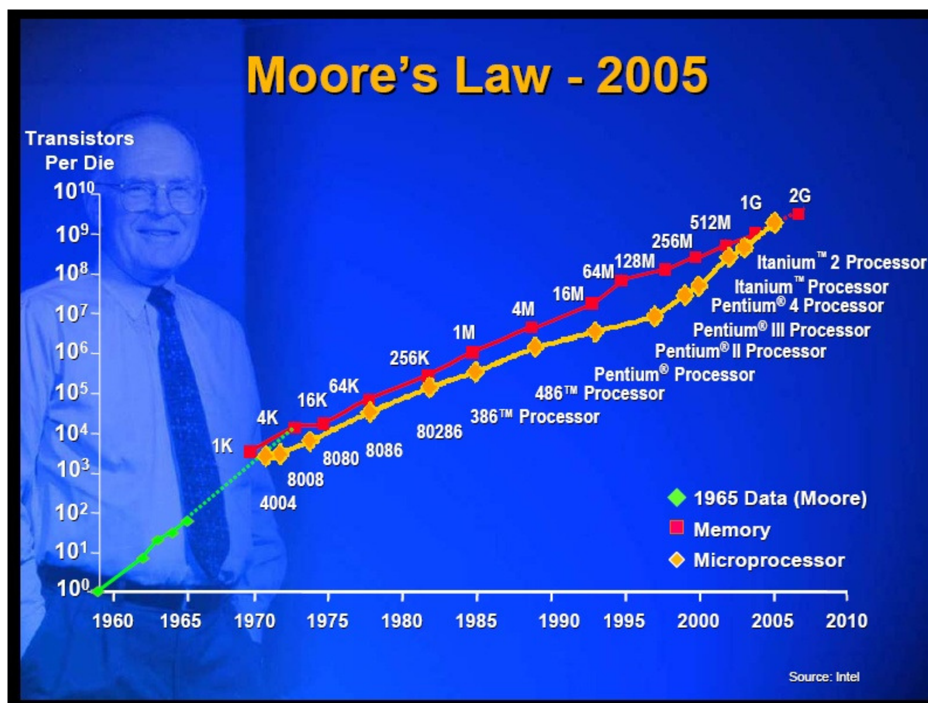

Figure 1: Evolution of the number of transistors per chip (Moore's law) predicted by the ITRS 2005 for memory and microprocessor [Intel Corporation].

2) Compact Analytical Models

The compact model is the heart of circuit simulations. Electronic engineers (device engineers and circuit designers) need device models for both design and simulation of electronic systems. Physically-based compact modeling of electron devices applicable to many electron devices is crucial for accurate circuit design and simulation. Actually, one of the main limitations to the use of novel device structures in circuit design is the lack of appropriate compact models. On the other hand, compact models are also useful to easily predict the performance of new device technologies.

In fact, in the process of development of new semiconductor devices, different types of simulations are required. In order to represent the electrical behavior of semiconductor devices we need semiconductor device simulation. Circuit simulation is essential to understand and predict the behavior of an electrical circuit with different

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device interconnected. For virtual fabrication of semiconductor devices, semiconductor process simulations are required. All of these simulations require models which we have developed and studied part of such models in this thesis. Modeling of nanoscale multiple-gate MOSFET in particular the gate tunneling current have been developed and verified by numerical simulations and experimental measurements. All of the considered simulations require models and the models require their own parameter values.

The downscaling of CMOS technologies has led to a reduction in gate length and a corresponding reduction in gate oxide thickness. For instance in 1970 the gate length was around 10,000 nm and the gate oxide thickness was 100 nm while in 2012 the gate length became 20 nm and the oxide thickness became smaller than 1 nm. One of the key concerns arising from downscaling the gate oxide thickness (ultra-thin SiO_2 gate oxide materials) is dramatically increasing the gate leakage current flowing through gate oxide materials by a quantum mechanical tunneling mechanism [9, 10]. In order to reduce and suppress the gate leakage current, high-k gate dielectrics are expected to replace SiO_2 in future CMOS generations. Alternative gate oxide materials with high dielectric constant candidates for coming CMOS generations are one of the most challenging problems in the continuous development of electronics [11].

3) Parameter Extraction

The parameter extraction techniques are another important aspect in the process of device modeling and circuit simulations. It plays an important role in bridging the communities between chip fabrication and integrated circuit (IC) design. In fact for the design of systems on a chip, realistic analogue simulation models are necessary. Additionally, the accuracy of the circuit simulations not only depends on an accurate model (correct mathematical description), but also on a parameter extraction techniques in order to determine accurate value of the model parameters [12, 13].

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The commercial package (IC-CAP) is used to apply automatic parameter extraction techniques and simulating our models which is coded in Verilog-A. The Verilog-A language is a source code of the compact model and one of the best tools for compact modeling which is actually compatible with IC-CAP (program of Agilent). Automatic parameter extraction routines provide an effective way to calculate the model parameters to minimize discrepancies between measured and model calculations.

4) Thesis Organization

This thesis is aimed to present the novel high-k dielectric materials that can work as gate oxides in Double Gate (DG) device structures for the 22 nm low standby power applications. A guideline for the determination of the suitable high-k candidate is reported in the case of ideal interface (one layer gate oxide material) and in the case of a SiO_2/high-k gate stack in a nanoscale single gate and DG MOSFETs. The effect of interfacial layer thickness is studied in order to select the most promising high-k candidates for different values of the Equivalent Oxide Thickness (EOT) and SiO_2 interfacial layer thicknesses.

A compact gate leakage current partitioning model is presented for nanoscale DG MOSFETs, using analytical models of the direct tunneling gate leakage current. Temperature dependent analytical models of the direct tunneling gate leakage current in inversion region and the Trap Assisted Tunneling (TAT) current in subthreshold regime have been developed for DG FinFET with a two dielectric layers gate stack such as $SiON/SiO_2$. As the last part, we studied the parameter extraction relies on a commercial software package (IC-CAP) allowing automatic parameter extraction routines and provides an effective way to calculate the model parameters to minimize discrepancies between measured and modeled data for reliable circuit simulation.

Additionally, each chapter of this thesis is subjected to the following objectives:

Chapter 1: Analytical modeling of the gate tunneling leakage for the determination of adequate high-k dielectrics in double-gate SOI MOSFETs at the 22 nm node. A

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theoretical study to the ideal interface between high-k material and Si substrate without any interfacial layer is presented [14].

Chapter 2: Analytical modeling of the direct tunneling current through gate stacks for the determination of suitable high-k dielectrics for nanoscale double-gate MOSFETs. A guideline for the determination of the suitable high-k candidate was reported in the case of a SiO_2/high-k gate stack in a nanoscale DG MOSFET. The models demonstrate that the materials such as La_2O_3, HfO_2, $LaAlO_3$ and Pr_2O_3 in the hexagonal phase would fulfill the considered requirements [15].

Chapter 3: Study of potential high-k dielectric for UTB SOI MOSFETs using analytical modeling of the gate tunneling leakage. The most important criteria for selecting alternative dielectrics (maximum gate leakage current, EOT, electron effective mass, dielectric constant k-value, barrier height and SiO_2 thickness as an interfacial layer) were taken into account to determine the suitability of the gate oxide materials [16].

Chapter 4: Gate leakage current partitioning in nanoscale DG MOSFETs, using compact analytical model. A model of the partitioning of the gate to channel tunneling leakage current into the source and drain components is developed. The influence and impact of the thickness of the interfacial SiO_2 layer on the gate-drain and gate-source components has been shown [17].

Chapter 5: Temperature dependent compact analytical modeling of gate tunneling leakage current in DG MOSFETs is studied. The gate leakage current measurements at different temperatures show two different transport mechanisms, DT gate leakage current in the strong inversion regime and TAT current in the sub-threshold regime [18].

Chapter 6: Automatic parameter extraction techniques in IC-CAP for compact DG MOSFET model are studied. We have developed automatic parameter extraction techniques for our explicit compact model in DG MOSFET suitable for design and circuits simulation based on surface potential including short channel effects [19].

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Chapter 7: Automatic Direct Tunneling and TAT Gate Leakage Current Parameter Extraction Techniques and Parameters Correlations in Double Gate MOSFET. The commercial package IC-CAP is used to simulate our leakage current model coded in Verilog-A, and comparing with gate leakage measurements in order to obtain parameters and study parameters correlations [20].

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Chapter 1

Analytical Modeling of Gate Tunneling Leakage for the Determination of Adequate High-k Dielectrics in Double-Gate SOI MOSFETs at the 22 nm node

The gate leakage current in metal-oxide-semiconductor (MOS) junctions/devices/or transistors is modeled and studied in order to find promising materials for double gate (DG) MOSFETs at 22 nm node by considering analytical models of the direct tunneling current (based on a proper calculation of the WKB tunneling probability in the gate oxide). We present a theoretical study to find the most promising gate oxide materials for the 22 nm technological node with the predicted maximum value of leakage current (10^{-2} [A/cm^2]) that is tolerable for that node, according to the ITRS roadmap. The effects of electron effective mass, dielectric constant k value and barrier height on the ΔE_c-k permitted values have been studied.

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1) Introduction

Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide gate dielectric thickness below 2 nm. Finding an alternative gate material with high dielectric constants for coming CMOS generations is one of the most challenging problems in the continuous development of microelectronics [1]. In order to reduce the gate leakage current, high-k gate dielectrics are expected to replace SiO_2 in future CMOS generations. Introducing a physically thicker high-k material can reduce the leakage current to the acceptable limit. Keeping at the same time a high enough value of the drain current in On-state (because of the higher dielectric constant).

Two of the most elementary quantities that need to be considered are the dielectric constant k and the energy band-offset values ΔE_c between the conduction band of the oxide materials and the silicon substrate [2]. It is not straightforward to replace SiO_2 with an alternative gate dielectric. The required properties of gate dielectrics should be systematically considered to provide the key guidelines for selecting an alternative gate dielectric.

The k of candidate oxides tends to vary inversely with the band gap, so we must accept a not too high-k value [3]. There are of course oxides with extremely large k values, such as ferroelectrics like $BaTiO_3$ but these have too low band gap. In fact, a huge k is undesirable in CMOS design because they cause undesirably strong fringing fields at source and drain electrodes [4]. Since the key motivation for replacing SiO_2 with high-k materials is leakage reduction, accurate modeling of the leakage current is necessary to understand the scaling limits and ensure that the selected materials are highly scalable and usable for many future generations of technology. In this work, we suppose that direct tunneling is the dominant conduction mechanism.

Due to the excellent control of short channel effects, Double-Gate (DG) MOSFET has emerged as one of the most promising devices for circuit design in sub-32 nm regime. However as explained before, the gate direct tunneling current is becoming a major source of leakage with aggressive scaling of oxide thickness [5, 6]. Therefore, it is necessary to analyze the gate leakage in sub-32 nm DG MOS devices.

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The better gate control reduces the vertical electric field, and as a consequence, the gate leakage in a DG MOSFET is lower than in its bulk-CMOS counterpart at the same bias conditions [7]. In [8] an expression of the direct-tunneling current density for an oxide voltage drop smaller than the barrier height is given.

The tunneling electron effective mass m_{ox} increases while decreasing the oxide thickness T_{ox} and m_{ox} for V_{ox} >1.5 V is about a factor of 0.8 times smaller than m_{ox} for V_{ox}<1.5 V. It was reported that the apparent increase of the conduction band effective mass in ultra thin SiO_2 with decreasing T_{ox} is consistent with a narrowing of the energy bands due to the decreased dimensionality [9].

Accurate simple and improved models for the direct tunneling current through high-k gate dielectrics adapted to DG MOSFETs are presented. We present a theoretical study to the ideal interface between high-k material and Si substrate without any interfacial layer, using these models, three of the most fundamental quantities that are needed: the dielectric constant (k), the energy band-offset values (ΔE_c) between the conduction band of the oxide and the silicon substrate, and electron effective mass to determine promising gate oxide materials for further DG MOSFETs technologies [10]. Our goal is to make the study of the best possible case (ideal device without interfacial layer).

2) Simple Analytical Model

In the case of the 22 nm node, for low standby power operation, an oxide EOT of about 0.5nm is required with a leakage target at 1 V of about 10^{-2} [A/cm^2] [11, 12]. A simplified estimate of the corresponding requirements for k and ΔE_c can be done by assuming that the most severe leakage mechanism for this case is direct tunneling from the silicon conduction band to the conduction band of the dielectric.

Our analysis applies to the ideal case of direct tunneling in high-k dielectric films and ideal interface without trap assisted tunneling [13], which may be present at low electric fields (low gate voltage) in these dielectrics (especially if the quality of the

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interface is not very good [14]). Additionally, we have made our analysis at V_g=1V which is well above the threshold voltage and therefore Direct Tunneling is clearly dominant over TAT [15, 16].

We have adapted to the DG MOSFET structure a relatively simple analytical model for the gate direct tunneling leakage (assumed to be the main gate leakage component) [12, 17], incorporating it to our previous compact model for the potential and drain current of a DG MOSFET [18, 19]. The direct-tunneling current density for an oxide voltage smaller than the barrier height can be simply expressed as:

$$J_n = A \times (\frac{\Delta E_C}{V_{ox}}) \times (\frac{2\Delta E_C}{V_{ox}} - 1) \times E_{ox}^2 \times \exp\{\frac{-B.[1-(1-\frac{V_{ox}}{\Delta E_C})^{\frac{3}{2}}]}{E_{ox}}\} \quad (1)$$

where; $A = \frac{q^3}{8\pi h \Delta E_C}$, $B = \frac{8\pi\sqrt{2m_{ox}}\Delta E_C^{\frac{3}{2}}}{3hq}$ and $E_{ox}=V_{ox}/T_{ox}$

where ΔE_c is the conduction band offset for a dielectric material, q is the electron charge, T_{ox} is the oxide thickness, h is the Planck constant, m_{ox} correspond to the electron tunneling effective mass in the dielectric layer, and V_{ox} is the voltage across the material which for the tunneling it was suggested [8, 20].

The voltage across the gate dielectric layer V_{ox} is given by the relation:

$$V_{ox} = V_g - V_{FB} - \psi_s \quad (2)$$

where V_g is the applied gate voltage, V_{FB} is flat band voltage; ψ_s is the band bending at the interface (surface potential). This surface potential is obtained using our previous compact model for the potential of a DG MOSFET [18, 19].

The functions ΔE_c = f(k_h) as given by Eq. (1) are plotted for the different cases together with the data points in the figures and considered as borders for estimating the relations between band offset values and dielectric constants for the low standby power requirements of the 22 nm node.

Results with our model suggest alternative dielectric materials such as Ce_2O_3 and $LaAlO_3$ in the most aggressive gate dielectric scaling scenario for low standby power

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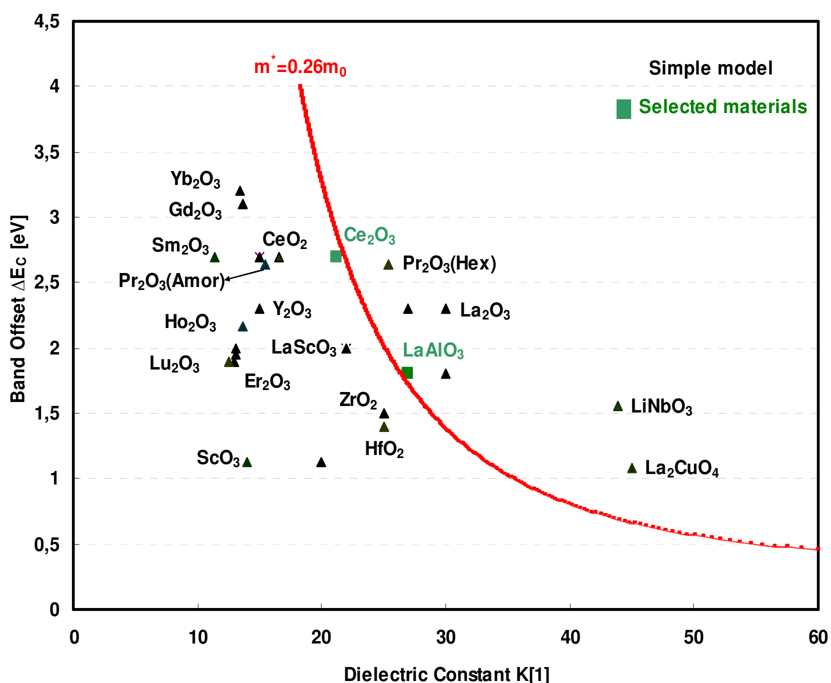

Figure 1: Band offset between conduction bands for different oxides and silicon as a function of k-value, for an oxide EOT of 0.5nm, $m^*=0.26m_0$, $V_g=1V$ with a leakage current about 10^{-2} [A/cm^2], using the simple analytical model.

technology requirements. It has been demonstrated that, for EOT=0.5nm and $m^*=0.26m_0$ [10], Ce_2O_3, and $LaAlO_3$ in Figure1 give a leakage current of about 10^{-2} [A/cm^2] at 1 V with a transport mechanism assumed to be direct tunneling as the most important component from simple model. Ce_2O_3 and $LaAlO_3$ have particularly large potential barrier offsets which mean that they could be the next generation high-k oxides with the required leakage currents.

Figure 2 shows the results for the minimum ($m^*=0.20m_0$) and maximum value ($m^*=0.50m_0$) of the electron effective mass for various dielectric materials taken from the literature [11, 21, 22]. It is remarkable that there is a strong dependence on the electron effective mass that is used and that it should be taken into account when evaluating new dielectric materials as a gate oxide. Therefore, it is necessary to accurately know the value of the electron effective mass in any new gate dielectric.

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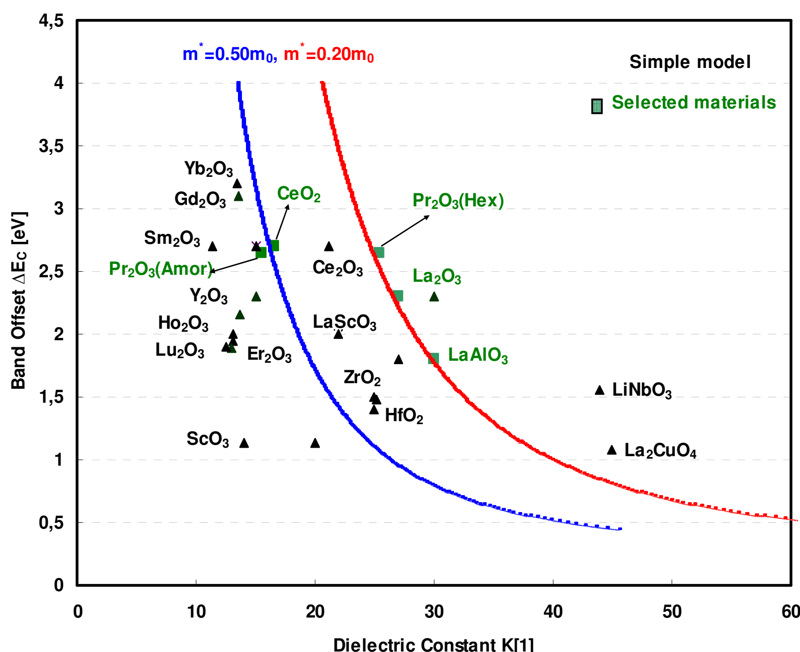

Figure 2: Band offset between conduction bands for different oxides and silicon as a function of k-value, for an oxide EOT of 0.5nm, V_g=1V, J=10^{-2} [A/cm^2], with effective mass $m^*=0.20m_0$ and $m^*=0.50m_0$, using the simple analytical model.

For EOT=0.5nm, Pr_2O_3 in the hexagonal phase as well as La_2O_3 and $LaAlO_3$ are suitable dielectrics which give the required leakage current with $m^*=0.20m_0$. When changing the effective mass to $m^*=0.50m_0$, the suitable materials then change to CeO_2, and Pr_2O_3 in the amorphous phase (see Figure 2).

Additionally Figure 2 shows the effect of changing the value of the electron effective mass in a range from $m^*=0.20m_0$ to $m^*=0.50m_0$, because this parameter almost changes in wide range [22]. The materials such as Ce_2O_3, $LaScO_3$, $DyScO_3$, $GdScO_3$, ZrO_2, and HfO_2 could be possible from the point of view of the barrier height, dielectric constant-k, and electron effective mass for EOT=0.5nm, V_g=1V, and leakage current J=0.01 [A/cm^2].

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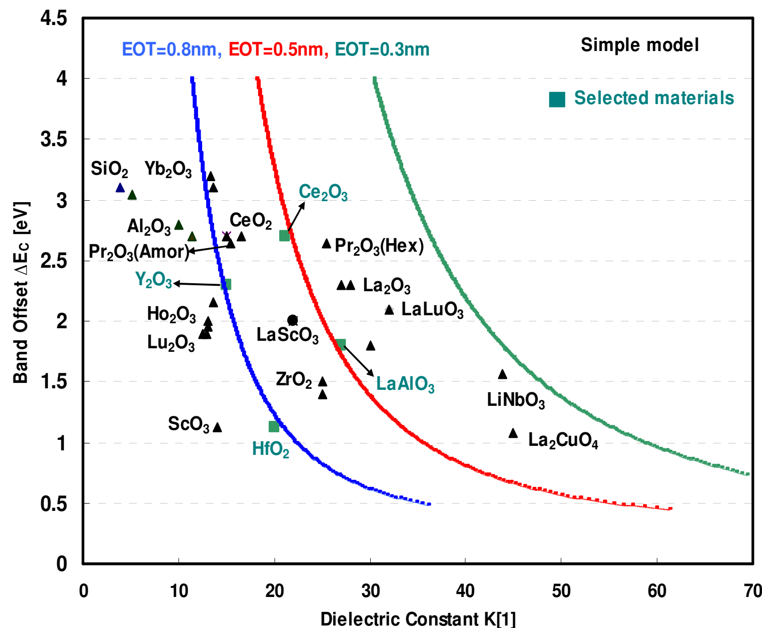

Figure 3: Band offset of the conduction band between different oxides and silicon as a function of k-value, for EOT=0.3, 0.5, and 0.8 nm, V_g=1V, J=10^{-2} [A/cm^2], and effective mass m^*=0.26m_0, using the simple analytical model.

According to different electron effective mass values in the HfO_2, in a range from m^*=0.1m_0 to m^*=0.7m_0 [22], HfO_2 appears to be one of the best candidates for the 22 nm node DG MOSFET requirements. Anyway, it is evident that the electron effective mass plays an important role and affects the overall analysis.

Figure 3 predicts the alternative gate oxide materials for different EOT values using our simple analytical model. It shows that the suitable high-k dielectrics from the barrier height point of view strongly depend on the EOT values. For EOT=0.8nm, materials with low dielectric constant are acceptable. By changing EOT value to 0.5nm, the barrier height versus dielectric constant curve shifts toward high-k materials. For EOT=0.3nm there are no suitable dielectrics to be used as gate oxides for identified parameters.

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3) Improved Analytical Model

The simple model expression includes a number of approximations that can lead to inaccuracies. The finite density of electrons or energy states in the semiconductor needs to be accounted for. The assumption of a constant effective mass for all energies (all locations at any oxide thickness and gate bias) is not accurate either. Furthermore, as oxide becomes thinner, the quantization effects in the semiconductor have to be considered in order to obtain the oxide potentials as an accurate function of the gate voltage [23, 24].

Because of these reasons, the simple analytical model falls short of a complete description of the tunneling current and is unable to fit the tunneling current for the entire range. A correction function is needed in order to cover the second-order effects listed above.

We used for the DG MOSFET structure a more complex and accurate analytical model for the direct tunneling gate current [25] that was adapted to the DG MOSFET [26] and presented in [18, 19]. The current density due to direct tunneling is expressed as follows

$$J_n = \frac{A}{\varepsilon_i}.EC.\exp\{-\frac{B.t_{ph}}{|V_{ox}|}[1-(1-\frac{|V_{ox}|}{\Delta E_C})^{\frac{3}{2}}]\} \quad (3)$$

where ε_i is the gate dielectric constant, V_{ox} is the voltage drop across the gate dielectric, ΔE_c as previously said is the conduction band offset for a dielectric material and t_{ph} is the physical dielectric thickness as:

$$t_{ph} = (\frac{k_{High-k}}{k_{SiO_2}}) \times EOT$$

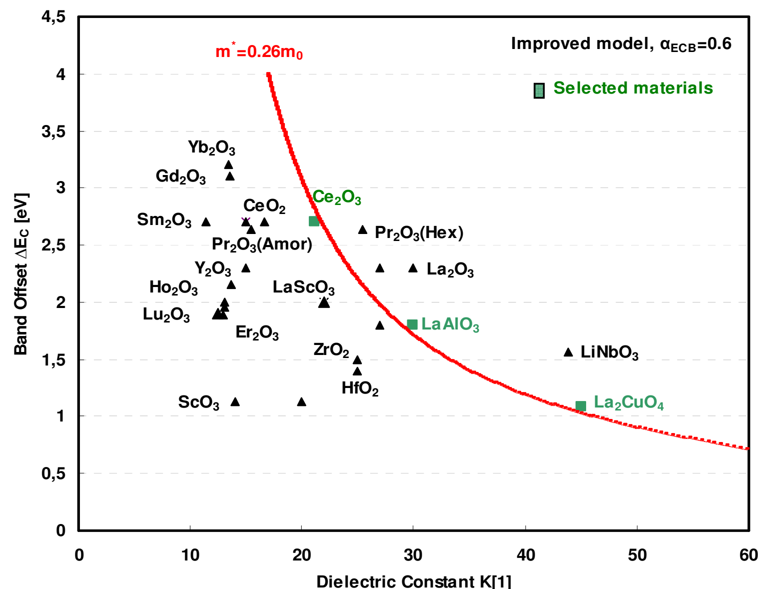

Figure 4: Band offset of the conduction band between different oxides and silicon as a function of k-value, for an oxide EOT of 0.5nm, m^*=0.26m_0, V_g=1V, α_{ECB}=0.6 with a leakage current 10^{-2} [A/cm^2], using the improved analytical model.

Factors A and B is expressed as:

$$A = \frac{q^3}{8\pi h \Delta E_C}\text{, and }\quad B = \frac{8\pi\sqrt{2m_{ox}}\Delta E_C^{\frac{3}{2}}}{3hq}$$

Expression (3) includes the empirical correction function EC described by

$$EC = \frac{V_G \pm \Delta V_G}{t_{ph}} \times N_T \times \exp\{\frac{20}{\Delta E_C}(\frac{|V_{ox}| - \Delta E_C}{\phi_0} + 1)^{\alpha_{ECB}} \times (1 - \frac{|V_{ox}|}{\Delta E_C})\} \qquad (4)$$

Where V_G is the applied gate voltage, ΔV_G is a fitting parameter to adjust the origin of the I-V characteristic to coincide with the modeled and the experimental curve. The value ϕ_0 is only slightly different from ΔE_c; therefore we can assume $\Delta E_c = \phi_0$, α_{ECB} is fitting parameter depending on the tunneling process and α_{ECB} =0.6 provides the overall best fit for EC [25].

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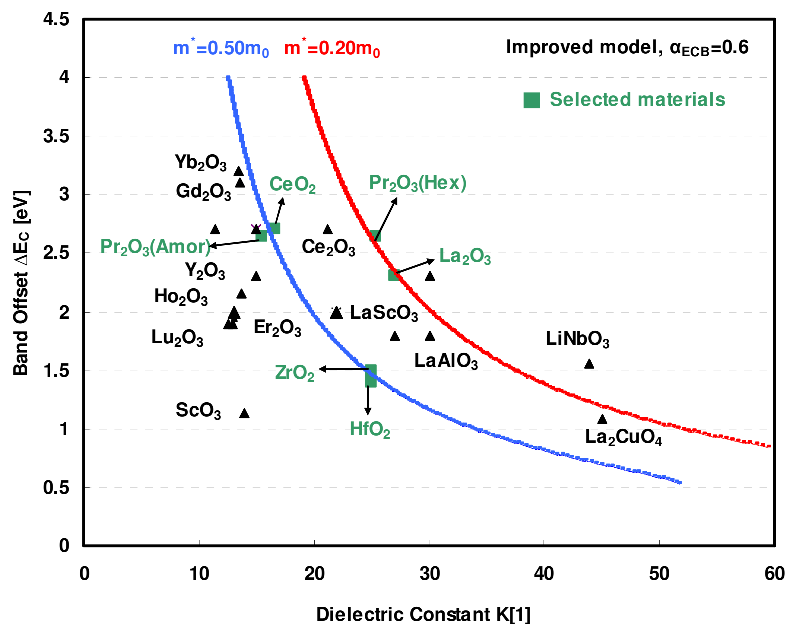

Figure 5: Band offset of the conduction band between different oxides and silicon as a function of k-value, for an oxide EOT of 0.5nm, V_g=1V, J=10^{-2} [A/cm^2], with effective mass $m^*=0.20m_0$ and $m^*=0.50m_0$, using the improved analytical model.

It is not a very sensitive parameter since even for α_{ECB} = 0.6 $\pm$0.3 we obtained very small affects on the ΔE_c-k plots, which means that with the improved model we can select the same materials as a gate oxide dielectric than with the α_{ECB} =0.6 case. N_T represents the behavior of density of carriers in the MOS structure [18, 19].

We have demonstrated that the potential barrier, dielectric constant value and the electron effective mass variation are quite important when studying the gate material that can be used. Figure 4 and Figure 5 show the guidelines for the selection of alternative gate dielectrics by using our improved analytical model for high-performance and low-operating-power logic technology requirements, assuming direct tunneling current as a dominant current at an applied gate voltage of 1V, materials as CeO_2, $LaAlO_3$, and La_2CuO_4 will be usable for EOT=0.5nm, leakage current J=0.01 [A/cm^2], and $m^*=0.26m_0$.

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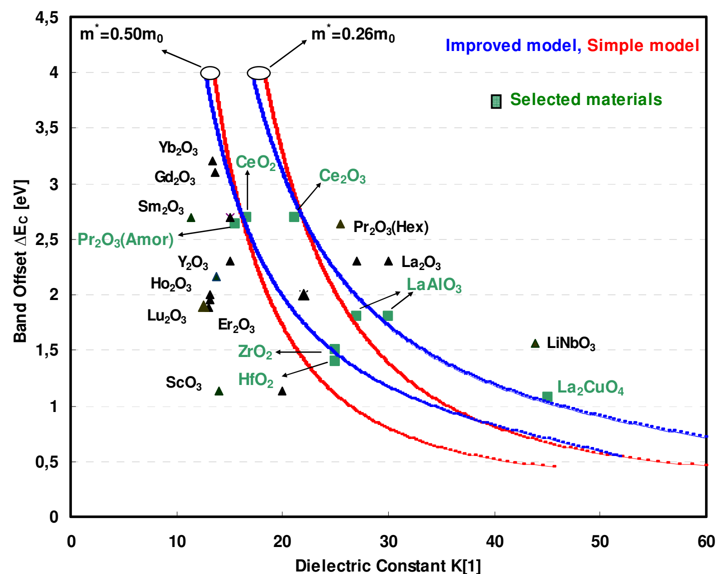

Figure 6: Band offset of the conduction band between different oxides and silicon as a function of k-value, for an oxide EOT of 0.5nm, V_g=1V, J=10^{-2} [A/cm^2], with effective mass $m^*=0.26m_0$ and $m^*=0.50m_0$, using the simple and improved analytical models.

As seen in Figure 6, the comparison the results between the simplified and the improved models show that both models predict the same materials as suitable gate dielectrics in the higher energy offset region.

Under the same conditions the acceptable dielectric materials in the higher energy offset region are Ce_2O_3 and $LaAlO_3$ from the two models. In the lower energy offset region the improved model suggests the La_2CuO_4 as a possible gate oxide material with higher dielectric constant, which give a leakage current of about 10^{-2} [A/cm^2] at 1V with $m^*=0.26m_0$, although the simple model does not suggest any acceptable materials in this region. As shown in Figure 6 for an electron effective mass equal to $m^*=0.50m_0$ the suitable dielectric materials determined by improved model are CeO_2, Pr_2O_3 in the amorphous phase, ZrO_2, and HfO_2. For the same conditions with $m^*=0.50m_0$ the simple model predicts only CeO_2, and Pr_2O_3 in the amorphous phase as proper dielectrics, but according to the improved model ZrO_2, and HfO_2 with higher dielectric constant can also be used.

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Actually, the improved model compare to the simple model gives additional acceptable dielectric materials with higher dielectric constant for same conditions (see in Figure 6).

4) Conclusion

We have developed analytical models for the gate tunneling leakage, adapted to DG MOSFETs. Using the new models, we have estimated the novel high-k dielectric materials that can work as gate oxides in DG device structures. Finally we have presented guidelines for finding an appropriate material for the 22 nm low standby power applications.

The simulations are based on two direct tunneling models of different complexity in order to determine suitable new oxide materials for 22 nm with the conditions EOT=0.5nm, J=0.01 [A/cm^2] for gate leakage current at a gate voltage of 1V. However both models give almost identical predictions in the range of k-values of interest.

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Chapter 2

Analytical Modeling of Direct Tunneling Current through Gate Stacks for the Determination of Suitable High-k Dielectric for Nanoscale Double-Gate MOSFETs

Gate-leakage current reduction is the key motivation for the replacement of SiO_2 with alternative gate dielectrics. In this chapter, a guideline for the determination of the suitable high-k candidate was reported in the case of a SiO_2/high-k gate stack in Nanoscale Double-Gate (DG) MOSFET. Analytical models of the direct tunneling gate leakage current with SiO_2 as an interfacial layer have been considered. Using these models the most promising high-k materials for different conditions were predicted, considering the effects of Equivalent Oxide Thickness (EOT), gate leakage current, electron effective mass, dielectric constant-k value, barrier height and interfacial oxide thickness.

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1) Introduction

Alternative gate oxide materials with high dielectric constant candidates for coming CMOS generations are one of the most challenging problems in the continuous development of electronics [1]. Accurate characterization and modeling of the tunneling current through gate stacks is essential to understand the scaling limitations of gate dielectrics. Analytical models of the direct tunneling assumed to be main component of the leakage current [2] through a trapezoidal barrier were considered to study proper high-k candidates to meet the gate leakage requirements [3, 4].

In our previous work [5], the suitability of high-k dielectric for DG MOSFET at 22 nm technological node requirements was studied, assuming the ideal case without interfacial layer between the dielectric and the Si body. However, in order to maintain a good interface and to prevent mobility degradation, it is desirable to have a thin layer of SiO_2 between the bulk and the high-k dielectric [6, 7].

In this chapter, accurate simplified and improved models for the direct tunneling current through SiO_2/high-k gate stacks are presented for the determination of suitable high-k dielectrics for Nanoscale DG MOSFETs. The direct tunneling models are adapted to our previous DG MOSFET compact model for the potential and drain current [8, 9]. Using these models, the most important parameters like: gate leakage current, EOT, electron effective mass, dielectric constant-k value, energy band-offset values between the conduction band of the oxide and the silicon substrate (barrier height) and interfacial oxide thickness are studied. Then, the most promising gate oxide materials for further DG MOSFETs technologies are highlighted from considered parameters point of view.

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2) Double Gate MOSFET Structure

Double Gate MOSFET structure under analysis with the oxides (Figure 1.a) and assumed potential profile (Figure 1.b) are shown in Figure 1, where ϕ_{B1} is the barrier height to the carrier for SiO_2 layer, ϕ_{B2} is the barrier high to the carrier for high-k layer, V_{ox1} is the voltage drops across the SiO_2 and V_{ox2} is the voltage drop across the high-k dielectric oxide layer.

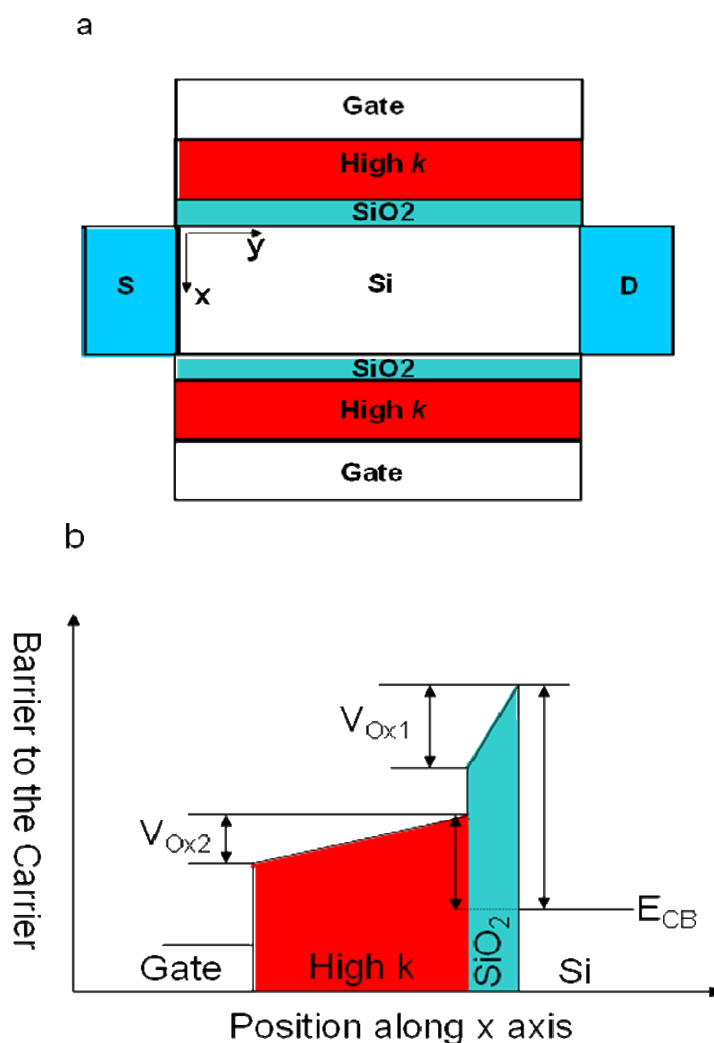

Figure 1: Schematic representation of: (a) Double gate MOSFET structure with gate stack; (b) Potential profile analyzed.

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The electric field at the surfaces of the Si-SiO_2 and SiO_2-high-k materials is needed in order to model gate leakage tunneling current for DG MOSFET structure. In our previous works an explicit compact model for the surface potential and drain current including short channel effects for DG MOSFET transistor was developed [8, 9]. Using this potential model in order to model gate leakage current, the electric field at the surface of the Si-SiO_2 (E_S) was calculated using Poisson's equation. The following expression was obtained for E_S as a function of the potential at the surface ϕ_S and at the center of the Si film ϕ_o [8, 9]:

$$E_S = \sqrt{\frac{2qN_a\phi_t}{\varepsilon_s}} \times \sqrt{(\frac{\phi_S - \phi_O}{\phi_t}) + (1 - e^{-(\frac{\phi_S - \phi_O}{\phi_t})}) \times e^{(\frac{\phi_S - 2\phi_F - V}{\phi_t})}} \quad (1)$$

where $\phi_t = KT^{'}/q$ is the thermal potential, K is the Boltzmann constant, q is the electron charge, $T^{'}$ is the temperature in Kelvin, N_a is the uniform acceptor concentration in the silicon layer, ϕ_{Fp} is the quasi Fermi level for holes in the P-type silicon layer, and ϕ_{Fn} is the quasi Fermi level for electrons. The potential along the channel is $V = \phi_{Fn} - \phi_{Fp}$, and ϕ_{Fp} is renamed as ϕ_F [8, 9].

Figure 2 shows surface potential at the Si-SiO_2 interface obtained from the model of [8, 9] are in a good agreement with those obtained from ATLAS numerical simulations for DG MOSFET structure.

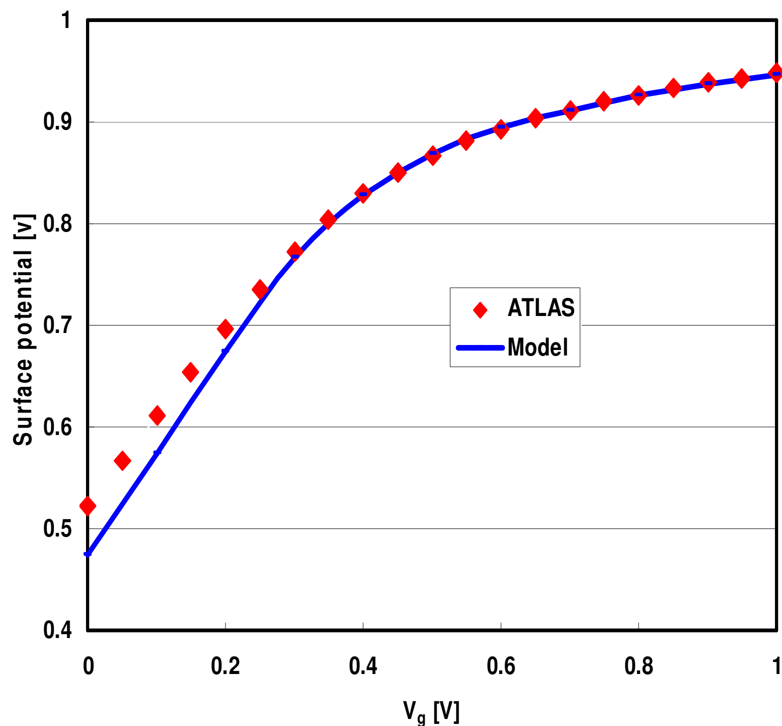

Figure 2: Model and ATLAS simulation of the surface potential at the Si-SiO_2 interface as a function of gate voltage at $V_d = 0V$.

The electric field at the surface of the Si-SiO_2 into SiO_2 using Eq. (1) and ATLAS simulations are displayed in Figure 3. The electric field at the surface of the SiO_2-high-k material into high-k material (assuming HfO_2 as an example of high-k dielectrics) are shown in Figure 4 obtained from the model and ATLAS simulations. There is a very good agreement between the model and numerical simulations in the above threshold region, which is the region of interest for this study and where direct tunneling dominates.

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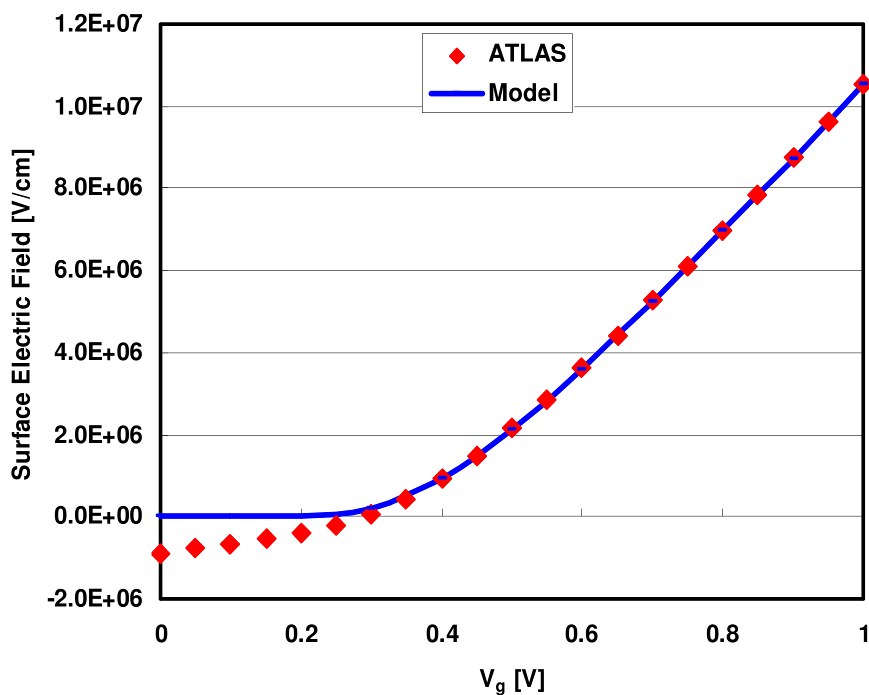

Figure 3: Model and ATLAS simulation of the surface electric field at the Si-SiO_2 interface into SiO_2 as a function of gate voltage at $V_d = 0V$.

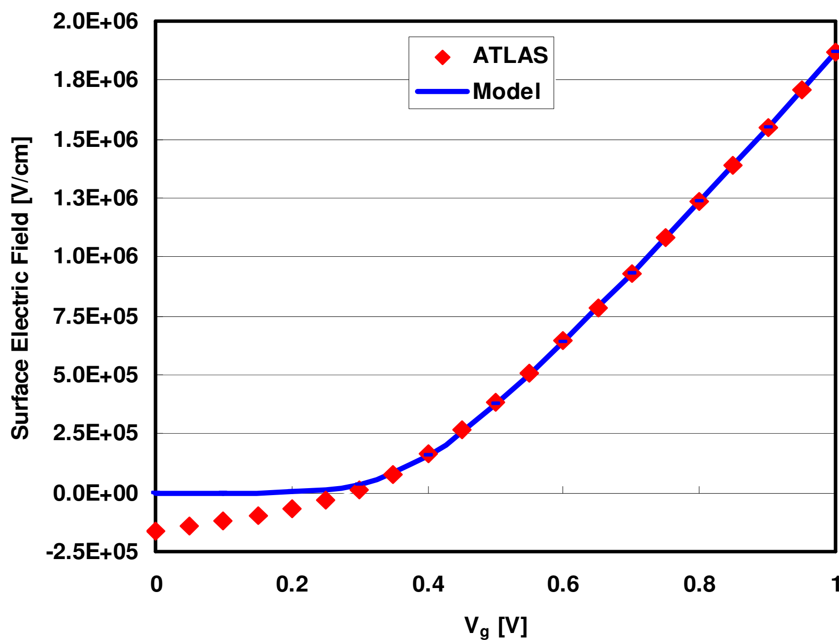

Figure 4: Model and ATLAS simulation of the surface electric field at the SiO_2- HfO_2 interface into HfO_2 as a function of gate voltage at $V_d = 0V$.

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3) Tunneling Probability Approximation (WKB)

The tunneling current models are based on the use of the well-known Wentzel-Kramers-Brillouin (WKB) approximation [10]. The WKB approximation is used to calculate the tunneling probability of a carrier through an energy band diagram for the MOSFET structure with two gate oxide layers as shown in Figure 1.

The tunneling probability for the two layers gate oxide (T), assuming direct tunneling through gate stack is given [11] by:

$$T = \exp\left\{\frac{8\pi}{3h}\frac{k_1 d_2 + k_2 d_1}{V_{ox} k_2}\sqrt{2 m_1 q}\,[\phi_{B1}^{\frac{3}{2}} - (\phi_{B1} - fV_{ox})^{\frac{3}{2}}]\right\}$$
$$\times \exp\left\{\frac{8\pi}{3h}\frac{k_1 d_2 + k_2 d_1}{V_{ox} k_1}\sqrt{2 m_2 q}\,[(\phi_{B2} - fV_{ox})^{\frac{3}{2}} - (\phi_{B2} - V_{ox})^{\frac{3}{2}}]\right\} \quad (2)$$

where h is Planck's constant, k_1 is representing first layer dielectric constant, k_2 is representing second layer dielectric constant, d_1 and d_2 are the physical thickness of first and second layers, m_1 is the effective mass of carrier in the first layer, q is the electron charge, f is EOT fraction of the first layer (SiO_2 thickness divided by EOT value), V_{ox} is the voltage drop across the gate stack and m_2 is the effective mass of carrier in the second layer.

It is clear from the last term of Eq. (2); in order to achieve the real part or non imaginary values of the tunneling probability for the carriers through the gate oxide, the values of ϕ_{B2} must be bigger than V_{ox}. In this case (Figure 1), electrons can move from Si substrate to the gate or inverse depending on the applied gate voltage only by tunneling directly the entire oxide thickness by tunneling the trapezoidal potential barrier between gate and Si substrate.

The WKB approximation is used to model the tunneling probability. The tunneling current density through the gate oxide can be calculated in all cases by changing the tunneling probability function accordingly.

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4) Simple Analytical Model

A simplified analytical model for the gate direct tunneling leakage through a two-layer stack [5, 12] based on the WKB approximation is developed for DG MOSFET structure (Figure 1). The incorporation of the model to our previous compact model for the potential and drain current [8, 9] is discussed in section two.

In our analysis, only the direct tunneling mechanism is considered as it is the main contribution to the tunneling current for a gate voltage equal to 1V in strong inversion [4, 10]. We consider the ideal case (best possible scenario) and, therefore, the interface trap charge is neglected as well as the gate oxide charges in the gate dielectric [13, 14].

A modified direct tunneling model based on the WKB approximation for SiO_2 as an interfacial layer and different high-k materials for two layer stack can be formulated:

$$\begin{aligned} J &= \frac{q^3}{8\pi h\phi_{B1}}\left(\frac{\phi_{B1}}{V_{ox1}}\right)\left(\frac{2\phi_{B1}}{V_{ox1}}-1\right)\frac{V_{ox1}}{d_1} \\ &\times \exp\left\{\frac{8\pi}{3h}\frac{k_1 d_2 + k_2 d_1}{V_{ox} k_2}\sqrt{2m_1 q}\,[\phi_{B1}^{\frac{3}{2}} - (\phi_{B1} - fV_{ox})^{\frac{3}{2}}]\right\} \\ &\times \exp\left\{\frac{8\pi}{3h}\frac{k_1 d_2 + k_2 d_1}{V_{ox} k_1}\sqrt{2m_2 q}\,[(\phi_{B2} - fV_{ox})^{\frac{3}{2}} - (\phi_{B2} - V_{ox})^{\frac{3}{2}}]\right\} \end{aligned} \quad (3)$$

where V_{ox1} is the voltage across the first layer (SiO_2) gate oxide.

The applied gate voltage will partly drop over the interfacial layer and the high-k, whereas the distribution depends on the physical layer thicknesses and the k-values. The applied bias (gate voltage) V_g relates to the voltage drop across the stack V_{ox} through the potential balance equation [15] by $V_g = V_{FB} + V_{ox} + \phi_S$ where $V_{ox} = V_{ox1} + V_{ox2}$, V_{FB} is flat band voltage and the voltage across the ith dielectric is given [15] by the relation:

$$V_{oxi} = \frac{\frac{d_i}{\varepsilon_i}}{\sum_{j=1}^{N}\frac{d_j}{\varepsilon_j}} V_{ox} \quad (4)$$

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ε_i being the permittivity of the ith gate dielectric layer.

The considered direct tunneling model is used to study the most interesting high-k dielectric candidates for gate leakage requirements.

5) Improved Analytical Model

The simple model expression includes a number of approximations that lead to inaccuracies (e.g., the assumption of a constant effective mass for all energies). As the oxide becomes thinner, the quantization effects in the semiconductor have to be considered in order to obtain the oxide potentials as an accurate function of the gate voltage [16, 17]. Therefore, a correction function (C) is needed in order to cover these effects in an analytical model. This leads to an improved analytical model [12, 18].

An improved analytical model based on the proper WKB approximation in order to accurately model the direct tunneling gate leakage current, by considering semi empirical correction function, can be proposed:

$$J = \frac{q^3}{8\pi h\phi_{B1}}\frac{C}{\varepsilon_1}\exp\left\{\frac{8\pi}{3h}\frac{k_1 d_2 + k_2 d_1}{V_{ox}k_2}\sqrt{2m_1 q}[\phi_{B1}^{\frac{3}{2}} - (\phi_{B1} - fV_{ox})^{\frac{3}{2}}]\right\}$$
$$\times\exp\left\{\frac{8\pi}{3h}\frac{k_1 d_2 + k_2 d_1}{V_{ox}k_1}\sqrt{2m_2 q}[(\phi_{B2} - fV_{ox})^{\frac{3}{2}} - (\phi_{B2} - V_{ox})^{\frac{3}{2}}]\right\} \quad (5)$$

where ε_1 is SiO_2 permittivity and C is the semi empirical corrections function:

$$C = \frac{V_g \pm \Delta V_g}{d_1}.N_T.\exp\{\frac{20}{\phi_{B1}}(\frac{|V_{ox1}| - \phi_{B1}}{\phi_0} + 1)^{\alpha_{ECB}} \times (1 - \frac{|V_{ox1}|}{\phi_{B1}})\} \quad (6)$$

ΔV_G is a fitting parameter to adjust the origin of the $I-V$ characteristic to make the modeled curve coincide with the experimental curve [12], its value is the same in all calculations. The value ϕ_0 is only slightly different from ϕ_{B1} ($\phi_0 \approx \phi_{B1}$), α_{ECB} is a fitting

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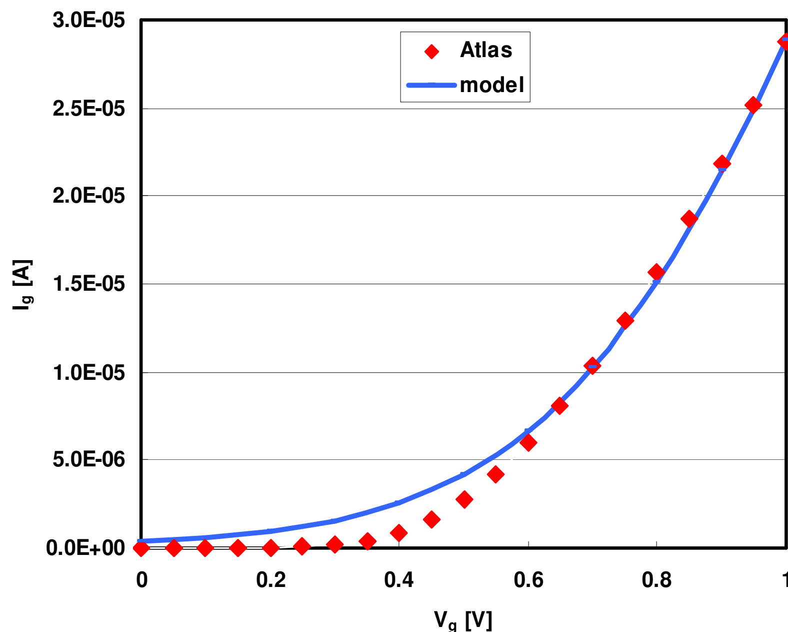

Figure 5: Analytical model and ATLAS simulations for the gate leakage tunneling current for DG MOSFET with EOT=0.5nm, $V_d = 0V$, interfacial layer (SiO_2) thickness of 0.2nm and HfO_2 as an oxide material.

parameter depending on the tunneling process and N_T represents the density of carriers for depletion, inversion and accumulation regimes in the injecting electrode [12, 18].

Figure 5 demonstrates the accuracy of the direct tunneling gate leakage current as function of gate voltage at $V_d = 0$ obtained by the model and ATLAS simulation. There is a very good agreement at high gate voltage (maximum gate leakage current).

6) Results and Discussion

Modified simple and improved direct tunneling models based on the WKB approximation are used to study the k_2, ϕ_{B2}, EOT, d_1, and m_2 dependence of the gate leakage current in order to study suitability of high-k materials while $\phi_{B1} = 3.2$ eV and $m_1 = 0.50 m_0$ (m_0 is the free electron mass) [7]. To select the alternative materials, it is

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important to notice that as the dielectric constant of the material increase, the band gap decreases and therefore higher k dielectrics tend to have a lower barrier height [19, 20]. Using the models, the optimum candidates are shown for each condition in order to meet the gate leakage requirements (ϕ_{B2} is shown as a band offset ΔE_C in the figures).

A) Simple Model

In order to study the effect of EOT and interfacial oxide thickness on the gate oxide materials, we have carried out the calculation by varying the EOT and SiO_2 thickness while maintaining the same leakage current ($J = 10^{-2}[\frac{A}{cm^2}]$) and gate voltage 1V for the device. Figure 6 and Figure 7 illustrate, with decreasing of EOT and SiO_2 thickness, the gate oxide materials change.

The proposed model determines the suitable dielectric materials as a gate oxide for the two layers case with EOT=0.6nm, $m_2 = 0.26m_0$, $V_g = 1V$, the gate leakage current $J = 10^{-2}[\frac{A}{cm^2}]$, two different SiO_2 thicknesses as $d_1 = 0.2nm, d_1 = 0.3nm$ for the nanoscale DG MOSFETs requirement parameters regarding to the low standby power application (Figure 7). The curve is plotted for different SiO_2 thickness and it shows the trend of the curves with interfacial layer thickness. The comparison can theoretically help to select available high-k dielectrics and suitable interfacial layer thickness.

It is found that Ce_2O_3 and $LaAlO_3$ are suitable gate oxides for EOT = 1 nm with a SiO_2 thickness equal to 0.5 nm (Figure 6) and that the use of La_2O_3 and $LaLuO_3$ dielectric materials leads to good results for EOT = 0.8 nm and $d_1 = 0.4nm$ (Figure 6). Moreover, $LiNbO_3$ is found to be a suitable gate oxide for EOT=0.6nm with a SiO_2 thickness equal to 0.2 nm (Figure 7). On the other hand, for EOT = 0.6 nm and SiO_2 thickness equal to 0.3 nm (Figure 7), no suitable dielectric materials are found using the simplified model. Additionally, it can be noticed (Figs. 6 and 7) that when decreasing the EOT and the SiO_2 interfacial thickness, the suitable gate oxide materials zone changes drastically due to the total physical thickness change.

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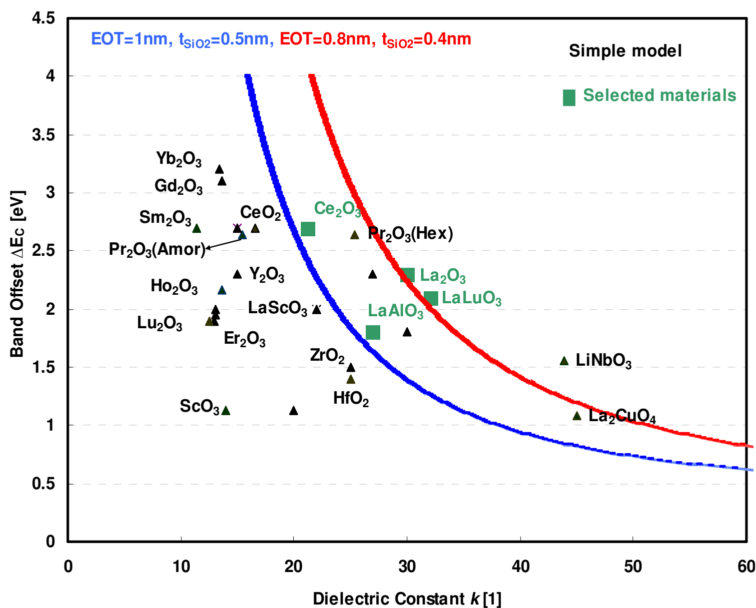

Figure 6: Band offset ΔE_C as a function of k-value for EOT=1nm with t_{SiO2}=0.5nm, EOT=0.8nm with t_{SiO2}=0.4nm, $m_2 = 0.26 m_0, V_g = 1V$ and leakage current $J = 10^{-2} [\frac{A}{cm^2}]$ using the simplified model.

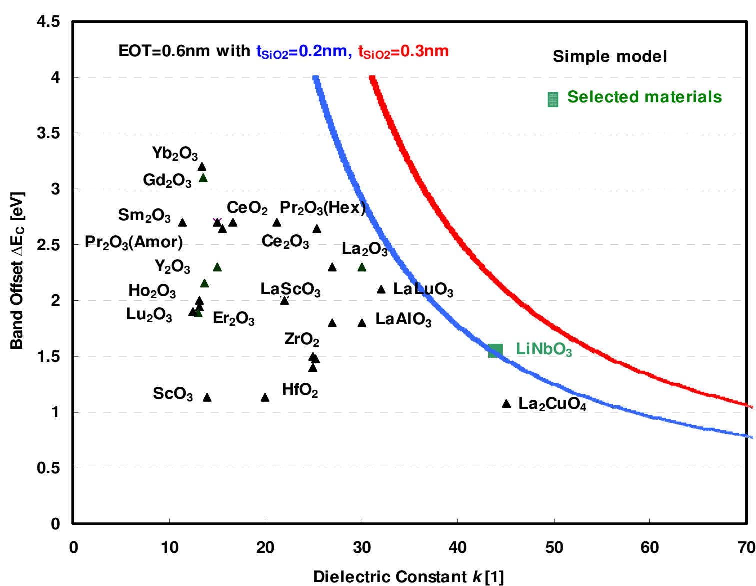

Figure 7: Band offset ΔE_C as a function of k-value for EOT=0.6nm (with t_{SiO2}=0.2nm and t_{SiO2}=0.3nm), $m_2 = 0.26 m_0$, $V_g = 1V$ and leakage current $J = 10^{-2} [\frac{A}{cm^2}]$ using the simplified model.

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It was reported that the tunneling electron effective mass m_2 increases while the oxide thickness decrease [21]. Figure 8 shows the plots of band offset versus k for higher electron effective mass which can change in a wide range [22], and for two different values of interfacial layer thickness. It is obvious that the electron effective mass plays an important role and strongly affects the plots of band offset versus k values.

For the case where EOT=0.6nm with $d_1 = 0.3nm$ as interfacial layer, $m_2 = 0.70m_0$, $V_g = 1V$, the gate leakage current $J = 10^{-2}[\frac{A}{cm^2}]$, the simple model indicated that materials such as Pr_2O_3 in hexagonal phase, La_2O_3, $LaAlO_3$ and La_2CuO_4 could be possible candidates as high-k dielectrics. Using the same conditions and $m_2 = 0.26m_0$, no suitable dielectric materials are found (Figure 7).

B) Improved Model

We considered and studied stacks with different EOT, and interfacial SiO_2 layer thickness by using the improved analytical model in the two layers case.

Figure 9 shows the result for a gate stack with EOT =1 nm, and $d_1 = 0.5nm$. The suitable materials are $LaScO_3$, ZrO_2, and HfO_2. Changing the value to EOT = 0.8 nm, and $d_1 = 0.4nm$ from improved model the promising dielectric materials change to Pr_2O_3 in the hexagonal phase, La_2O_3, $LaAlO_3$ and La_2CuO_4 which give a leakage current of about $J = 10^{-2}[\frac{A}{cm^2}]$ at $V_g = 1V$ with $m_2 = 0.26m_0$.

Figure 10 shows the results of our model calculations with an EOT of 0.6 nm, a thickness of the SiO_2 interface of 0.2 nm, and a leakage current density of $J = 10^{-2}[\frac{A}{cm^2}]$ at a gate voltage of 1 V. The promising gate oxide materials for these requirements with $m_2 = 0.26m_0$ are La_2O_3, and $LaLuO_3$.

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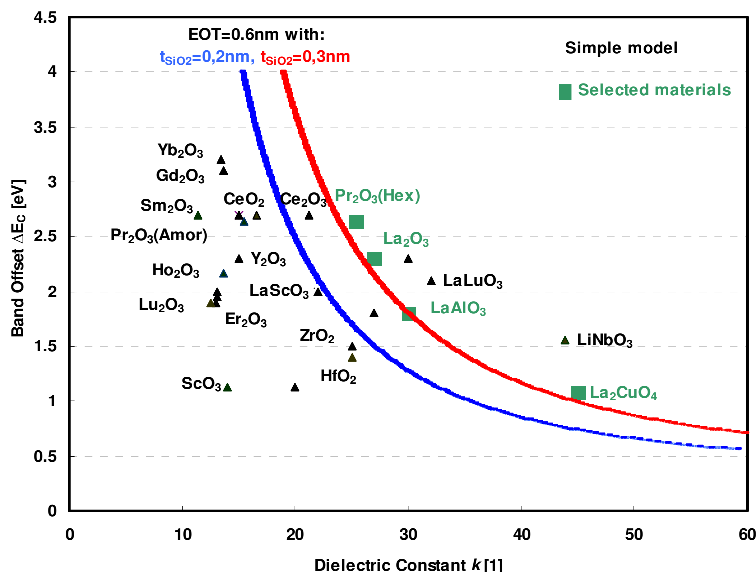

Figure 8: Band offset ΔE_C as a function of k-value for EOT=0.6nm with t_{SiO2}=0.2nm, and t_{SiO2}=0.3nm as an interfacial layer, $m_2 = 0.70 m_0$, $V_g = 1V$ and leakage current $J = 10^{-2}[\frac{A}{cm^2}]$ using the simplified model.

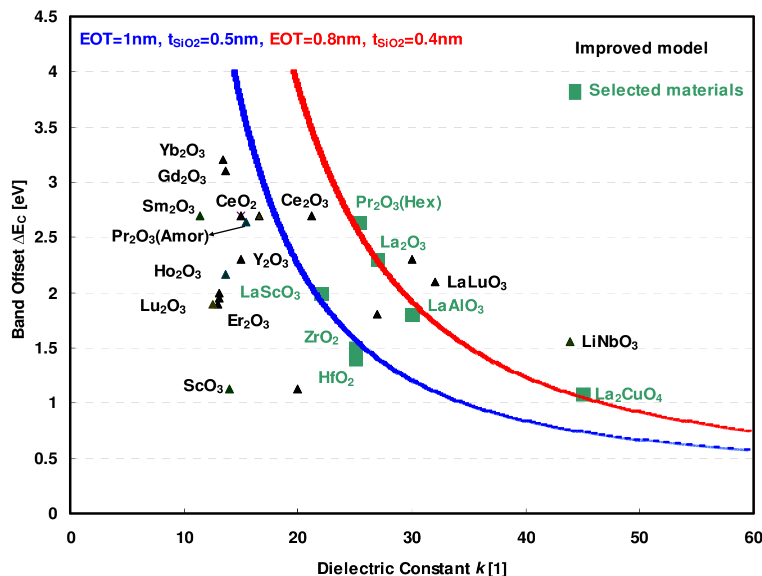

Figure 9: Band offset ΔE_C as a function of k-value for EOT=1nm with t_{SiO2}=0.5nm, EOT=0.8nm with t_{SiO2}=0.4nm, $m_2 = 0.26 m_0$, $V_g = 1V$ and leakage current $J = 10^{-2}[\frac{A}{cm^2}]$ from improved model.

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Increasing the thickness of the SiO_2 interface from 0.2 nm to 0.3 nm using the same parameters, there is no suitable gate dielectric material for the considered conditions. As it was found for the simple model, increasing the electron effective mass causes the band offset versus k curve to shift toward low k dielectric candidates (Figure 11).

Figure 10 shows that when increasing the thickness of the SiO_2 interface from 0.2 nm to 0.3 nm for $m_2 = 0.26m_0$, there is no dielectric material possibility as a gate oxide for the considered conditions. But increasing the electron effective mass from $m_2 = 0.26m_0$ to $m_2 = 0.70m_0$, while keeping the same values as before for all the other parameters, shifts the band offset versus k curve ($\Delta E_c - k$) toward low dielectric k value as it can be seen in Figure 11. For gate stacks with EOT = 0.6 nm and SiO2 thickness equal to 0.3 nm, the suitable high-k materials are $LaAlO_3$ and Ce_2O_3 (giving a leakage current of about $J = 10^{-2}[\frac{A}{cm^2}]$ at $V_g = 1V$ with $m_2 = 0.70m_0$).

As we have seen, simple and improved models showed that they are quite sensitive to the electron effective mass value. When the effective mass is increased, the band offset versus k graphs shift toward the low dielectric k values. In particular, when we decrease the EOT value or increase the SiO_2 layer thickness as an interfacial layer, the models does not give any suitable dielectrics (Figure 7 and Figure 10) but when the electron effective mass increases (Figure 8 and Figure 11), the graphs shift and then some possible choices appear. Therefore it is obvious that the electron effective mass plays an important role in the selection of suitable high-k dielectric as a gate oxide. Figure 8 and Figure 11 show that there is a strong dependence on the electron effective mass that is used. The results from two models in the figures show that the materials like La_2O_3, HfO_2, $LaAlO_3$ and Pr_2O_3 in the hexagonal phase are the best gate dielectric candidates from the considered conditions point of view.

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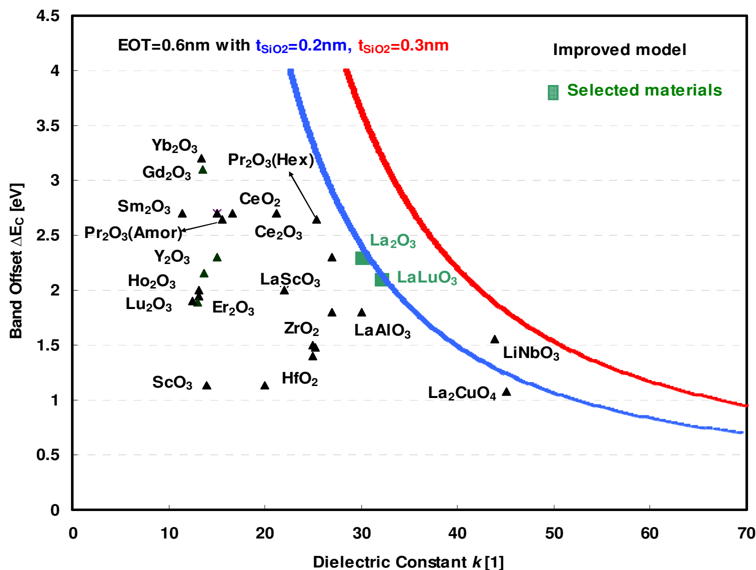

Figure 10: Band offset ΔE_C as a function of k-value for EOT=0.6nm with t_{SiO2}=0.2nm, and t_{SiO2}=0.3nm as an interfacial layer, $m_2 = 0.26m_0$, $V_g = 1V$ and leakage current $J = 10^{-2}[\frac{A}{cm^2}]$ from improved model.

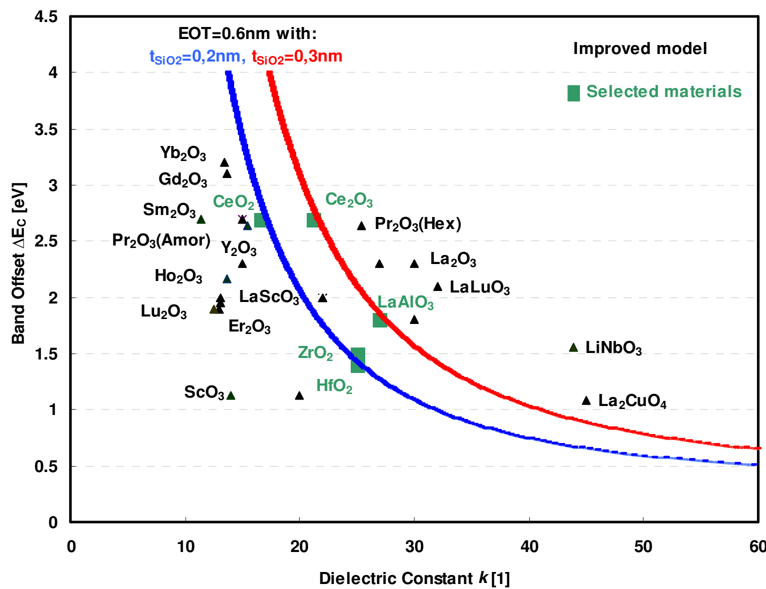

Figure 11: Band offset ΔE_C as a function of k-value for EOT=0.6nm with t_{SiO2}=0.2nm, and t_{SiO2}=0.3nm as an interfacial layer, $m_2 = 0.70m_0$, $V_g = 1V$ and leakage current $J = 10^{-2}[\frac{A}{cm^2}]$ using the improved model.

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7) Conclusion

Analytical models for the direct tunneling current flowing between gate and channel, based on the modified WKB tunneling probability approximation through the gate stack have been developed. The models have been used to study the impact of parameters in the leakage current equations in order to find guidelines for the search of an appropriate dielectric in Nanoscale DG MOSFET structure.

It should be noted that the EOT, barrier height, dielectric constant-k value, interfacial layer thickness and electron effective mass strongly affect the direct tunneling current and they should be considered together in determining the suitable dielectrics. The models show the most promising high-k candidates for different values of EOT and SiO_2 interfacial layer thickness, satisfying the gate leakage requirements. They demonstrate that the materials like La_2O_3, HfO_2, $LaAlO_3$ and Pr_2O_3 in the hexagonal phase would fulfill the considered requirements.

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Chapter 3

Study of Potential High-k Dielectric for UTB SOI MOSFETs Using Analytical Modeling of the Gate Tunneling Leakage

In this chapter, we use analytical models of the direct tunneling gate leakage current to determine the high-k dielectric suitable for the nanoscale UTB SOI MOSFETs structure with the predicted Equivalent Oxide Thickness (EOT) and the maximum value of the gate leakage current according to the requirements of the latest ITRS roadmap for three technological nodes. The most important criteria for selecting alternative dielectrics (maximum gate leakage current, EOT, electron effective mass, dielectric constant-k value, barrier height and SiO_2 thickness as an interfacial layer) were taken into account to determine the suitability of the gate oxide materials. In the ideal case without an interfacial layer, HfO_2 and Lu_2O_3 were found to be the best gate oxide materials for the 17nm, 15nm and 14nm technological node requirements.

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1) Introduction

The downscaling of CMOS technologies has led to a reduction in gate length and a corresponding reduction in gate oxide thickness. One of the problems arises from downscaling the thickness of the silicon dioxide layer is that the gate leakage current flowing through the gate oxide increases.

High-k materials are essential to the successful scaling of silicon-based MOSFETs. In fact, gate leakage can be suppressed if appropriate high-k dielectric materials are used. In ultra thin SiO_2 gate layers, charge carriers can flow through the gate dielectric by a quantum mechanical tunneling mechanism [1, 2]. In addition, the tunneling probability using a simple Wentzel-Kramers-Brillouin (WKB) approximation [3] is exponentially dependent on EOT, so it increases as the EOT decreases [1, 4].

In our previous papers we studied the suitability of high-k materials in Double-Gate SOI MOSFETs to meet the 22 nm node requirements in the case of one layer gate oxide [5] and SiO_2 as an interfacial layer [6]. We ignored trap assisted tunneling (TAT) [7, 8] because direct tunneling dominates TAT at Vg = 1V [9, 10] and we considered an ideal interface (without interface states) in two cases: first a high-k material directly on Si substrate without an interfacial layer, and the case with the SiO_2 as an interfacial layer. Due to the process induced presence of a silicon dioxide interfacial layer in the gate stacks, it is desirable to have a thin layer of SiO_2 between the silicon and the high-k dielectric to maintain a good interface and prevent mobility degradation. A high-k dielectric suffers from stronger remote soft optical phonons that degrade the mobility [11-13] and, normally, the higher the dielectric constant, the stronger the remote phonons.

In this chapter, we develop analytical models for the direct tunneling current [14, 15] through gate stacks (considering a proper WKB tunneling probability adapted to the UTB SOI MOSFETs structure) and incorporate them into our new compact model for the potential and drain current of a UTB SOI MOSFET [16].

Gate oxide candidates must meet a set of criteria if they are to perform well. The main parameters to take into account are EOT, gate leakage current, electron effective mass, dielectric constant-k value, barrier height and SiO_2 thickness as an interfacial layer if we are to determine suitable gate oxide candidates [17, 18] for different conditions.

These conditions are drawn from the specifications of the latest International Technology Roadmap for Semiconductors (ITRS) [19]. The next generations of Si-based MOSFETs will require gate dielectrics with an EOT equal to 0.90 nm, 0.85 nm or 0.8 nm for low standby power (LSP) logic applications and acceptable gate leakage current limits of 0.19 [A/cm^2] , 0.21 [A/cm^2] and 0.23 [A/cm^2], respectively.

According to the ITRS, low standby power devices technical requirements are more strict than the case of high performance (HP) device technical requirements (with an EOT equal to 0.88nm or 0.75nm, acceptable gate leakage current limits of 900 [A/cm^2] and 1000 [A/cm^2]), and low operating power (LOP) requirements (with an EOT equal to 0.8nm or 0.7nm, acceptable gate leakage current limits of 180 [A/cm^2] and 200 [A/cm^2]). Then, the determination of suitable high-k materials for ultra-nanoscale nodes is more critical in LSP than in HP and LOP´s requirements.

2) UTB SOI MOSFET Structure

The ultra-thin body SOI transistor structure under analysis is shown in Figure 1. In order to determine the high-k materials that are most promising as gate insulators in the UTB SOI MOSFETs structure, we have used gate leakage current analytical models that have been adapted to an ideal interface between the high-k material and Si substrate with no interfacial layer (Figure 1a) and with a thin layer of SiO_2 between the silicon and high-k dielectric (Figure 1b). As discussed below, using those leakage current models adapted to the UTB SOI MOSFET structures shown in Figure 1 and bearing in mind the application requirements, we can plot various barrier heights as a function of the dielectric constants of specific technological node requirements to optimize the choice of the potential candidate materials.

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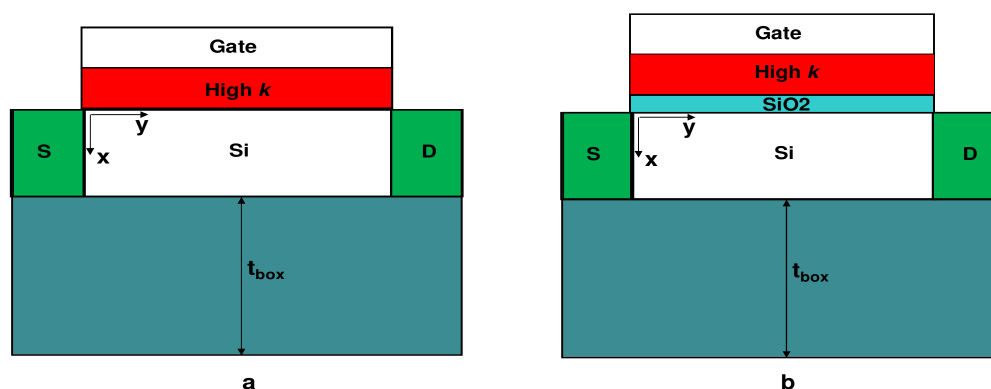

Figure 1: Schematic representation of a single gate UTB SOI MOSFET structure: (a) One-layer oxide; (b) Two-layer oxides (SiO_2 as an interfacial layer).

A new compact charge-based model for the potential, consisting of relatively simple equations for fully depleted UTB SOI MOSFETs, was presented in a previous study (see [16]). Figure 2 shows calculations of the surface potential using our UTB SOI MOSFET model (adapted to our structure and TCAD 2D numerical simulations). The results provided by our model are in good agreement with the results of the numerical simulation.

The strength of the electric field in the gate stack needs to be known in order to calculate the direct tunneling current through the silicon dioxide and high-k material dielectric between the gate and the channel. The electric field in the SiO_2 at the surface of the Si-SiO_2 (Figure 3) and SiO_2-high-k dielectric (pointing towards the HfO_2 and assuming it is a high-k material) are shown using the model and compared with TCAD simulations (Figure 3). The agreement between the model calculations and TCAD numerical simulation results is good enough.

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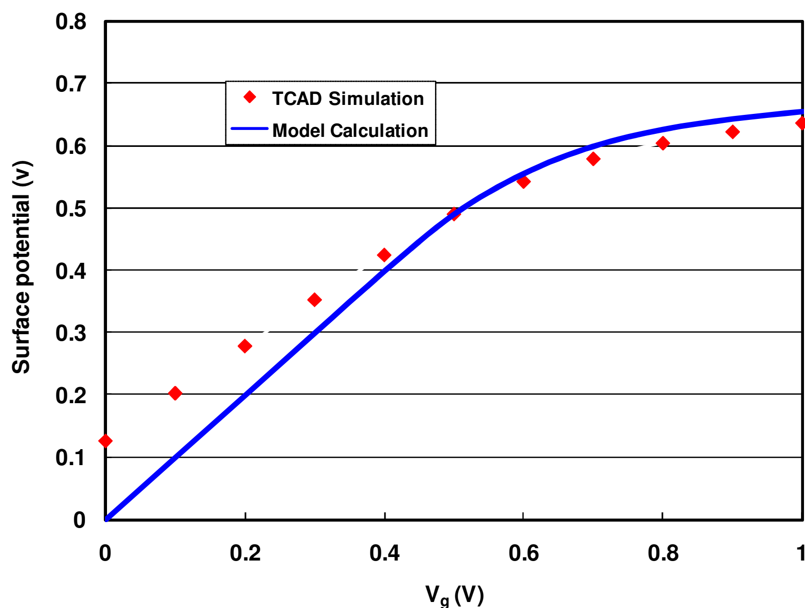

Figure 2: Model calculation and TCAD numerical simulation of the surface potential at the Si-SiO_2 interface as a function of gate voltage at V_d=0V.

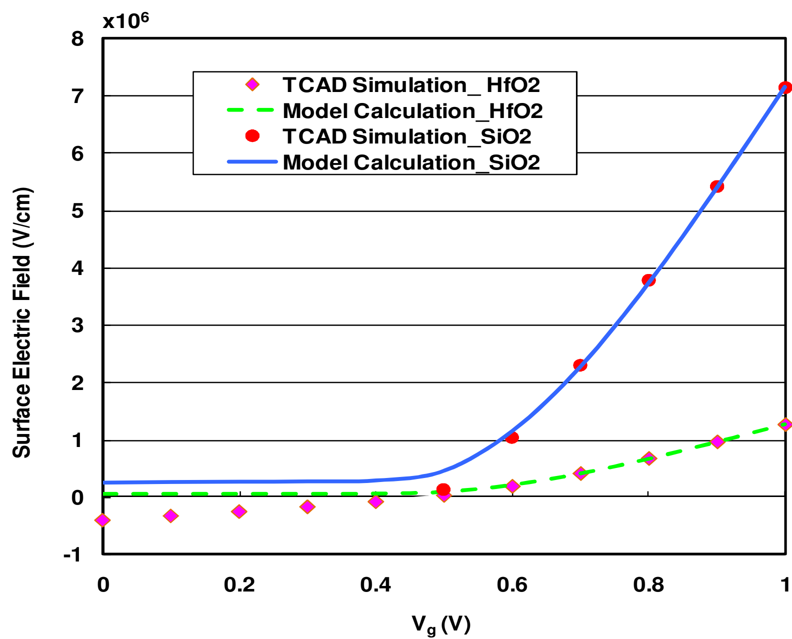

Figure 3: Model calculation and TCAD simulation of the electric field at the SiO_2- HfO_2 interface into HfO_2 and at the Si-SiO_2 interface into SiO_2 as a function of gate voltage at V_d=0V.

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3) Tunneling Probability Approximation (WKB)

We describe a proper Wentzel-Kramers-Brillouin (WKB) approximation for the probability of the tunneling through the gate oxide, which is required to model the direct tunneling current flowing between gate and channel [3, 4].

Using the WKB approach for the one-layer gate oxide for UTB SOI MOSFET, a proper tunneling approximation is:

$$T_{OneLayer} = \exp\{\frac{-\frac{8\pi\sqrt{2m_{High-k}}\phi_{High-k}^{\frac{3}{2}}}{3hq}[1-(1-\frac{V_{ox}}{\phi_{High-k}})^{\frac{3}{2}}]}{E_{High-k}}\} \quad (1)$$

where m_{High-k} is the electron tunneling effective mass in the high-k layer, ϕ_{High-k} is the conduction band offset for dielectric material, q is the electron charge, h is Planck's constant and E_{High-k} is the electric field across the high-k material which was suggested for the direct tunneling [20, 21].

The voltage across the high-k material (V_{ox}) is given by $V_{ox} = V_g - V_{Fb} - \phi_S$ where V_g is the applied gate voltage, V_{Fb} is the flat band voltage, and the potential at the surface (ϕ_S) was obtained using our new compact charge based on the potential of a UTB SOI MOSFET [16].

The tunneling probability for the two layer case [22] modified to the conditions in the UTB SOI MOSFETs structure is given as:

$$T_{TwoLayers} = \exp\left\{\frac{8\pi}{3h}\frac{k_{SiO_2}\times T_{High-k} + k_{High-k}\times T_{SiO_2}}{V_{ox}\times k_{High-k}}\sqrt{2m_{SiO_2}q}[\phi_{BSiO_2}^{\frac{3}{2}} - (\phi_{BSiO_2} - fV_{ox})^{\frac{3}{2}}]\right\}\times$$
$$\exp\left\{\frac{8\pi}{3h}\frac{k_{SiO_2}\times T_{High-k} + k_{High-k}\times T_{SiO_2}}{k_{SiO_2}\times V_{ox}}\sqrt{2m_{High-k}q}[(\phi_{BHigh-k} - fV_{ox})^{\frac{3}{2}} - (\phi_{BHigh-k} - V_{ox})^{\frac{3}{2}}]\right\} \quad (2)$$

where ϕ_{BSiO_2} is the barrier height for the electrons in the SiO_2 layer, f is the EOT fraction of the SiO_2 layer, m_{SiO_2} is the effective mass of carrier in the SiO_2, k_{SiO_2} is the

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SiO_2 dielectric constant, k_{High-k} is the high-k dielectric constant, and T_{SiO_2} and T_{High-k} are the physical thicknesses of SiO_2 and high-k materials.

According to the UTB SOI structure used to model and study the direct tunneling through the gate insulator (and to determine the suitability of high-k materials), a proper WKB approximation is necessary to capture the correct behavior of the leakage current.

4) Gate Direct Tunneling Model in the UTB SOI Structure

A) Simple Model with no Interfacial Layer and with SiO_2 as an Interfacial Layer

We adapted a simple analytical gate leakage current model to a UTB SOI MOSFET structure. This model considers electron energy quantization effect approximations for the direct tunneling current between the gate and the channel as the main gate leakage component [15, 21]. In order to calculate the gate leakage current by the simple model across the oxide materials for the assumed structure, we need to use the value of the electric field across the gate stack which we have obtained using our new charge-based potential compact model [16]. This simple analytical model, which is used to study suitable dielectric materials assuming an ideal interface with no interfacial layer, is given by:

$$J_{S_{OneLayer}} = \frac{q^3}{8\pi h\phi_{High-k}} \times (\frac{\phi_{High-k}}{V_{ox}}) \times (\frac{2\phi_{High-k}}{V_{ox}} - 1) \times E^2_{High-k} \times T_{OneLayer} \qquad (3)$$

The presence of SiO_2 at the interface between the high-k material and the Si substrate is important when studying the suitability of high-k candidates. We considered an interfacial layer in order to maintain the advantages of SiO_2 (large energy band offsets with the conduction and valence bands of silicon, good interface and weak mobility degradation) and because the process can induce SiO_2 as an interfacial

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layer. We should point out that the use of SiO_2 as an interfacial layer will limit the lowest obtainable EOT value [8].

A simple analytical model for the case of an interfacial layer, based on a proper WKB tunneling probability for studying promising gate oxide materials, is given by:

$$J_{S_{TwoLayers}} = \frac{q^3}{8\pi h\phi_{SiO_2}} \times (\frac{\phi_{SiO_2}}{V_{ox}}) \times (\frac{2\phi_{SiO_2}}{V_{ox}} - 1) \times E_{SiO_2}^2 \times T_{TwoLayers} \quad (4)$$

E_{SiO_2} is the electric field across the SiO_2. We used this simple analytical model of the gate tunneling current for the case with no interfacial layer and the case with SiO_2 as an interfacial layer, in order to study high-k materials that were suitable oxide dielectrics according to the latest ITRS low standby power requirements to the incoming UTB SOI MOSFETs.

B) Improved Model with and without an Interfacial Layer

An improved analytical model can be developed from the simple model by using a correction function to include electron energy quantization effects in a more accurate way [23]. It cannot be assumed that the effective mass is constant at all oxide thicknesses and gate biases [24] and, as the oxide becomes thinner, the quantization effects in the semiconductor have to be considered. A correction function is incorporated in order to account for these effects.

The improved analytical model adapted to UTB SOI MOSFET (based on our new compact model of potential [16]) and a proper WKB probability is given by:

$$J_{I_{OneLayer}} = \frac{q^3}{8\pi h\phi_{High-k}} \frac{1}{k_{High-k}\varepsilon_0} C_{OneLayer} T_{OneLayer} \quad (5)$$

ε_0 is the permittivity of free space and the correction function for the ideal interface without any interfacial layer ($C_{OneLayer}$) is given by:

$$C_{OneLayer} = \frac{V_g \pm \Delta V_g}{T_{High-k}} \times N_T \times \exp\{\frac{20}{\phi_{High-k}}(\frac{|V_{ox}| - \phi_{High-k}}{\phi_0} + 1)^{\alpha_{ECB}} \times (1 - \frac{|V_{ox}|}{\phi_{High-k}})\} \quad (6)$$

the ΔV_g is a fitting parameter that adjusts the origin of the I-V characteristic to coincide with the modeled and the experimental curve [25]. The value ϕ_0 is only slightly different from ϕ_{High-k} so we can assume $\phi_{High-k} = \phi_0$, α_{ECB} is a fitting parameter that depends on the tunneling process and α_{ECB} =0.6 provides the best overall fit for $C_{OneLayer}$ [22]. N_T represents the behavior of the density of carriers [25] and its expression was adapted to the UTB SOI MOSFET structure. Figure 4 shows the direct tunneling current as a function of gate voltage with HfO_2 and SiO_2 as a gate dielectric stack at V_d = 0 obtained by our model calculations and TCAD numerical simulations. There is a good agreement between model calculations and simulation results especially in the interesting range of high gate voltage (1V), where the gate leakage current is max. The study to find the proper dielectrics was carried out at V_g = 1V (maximum gate leakage current).

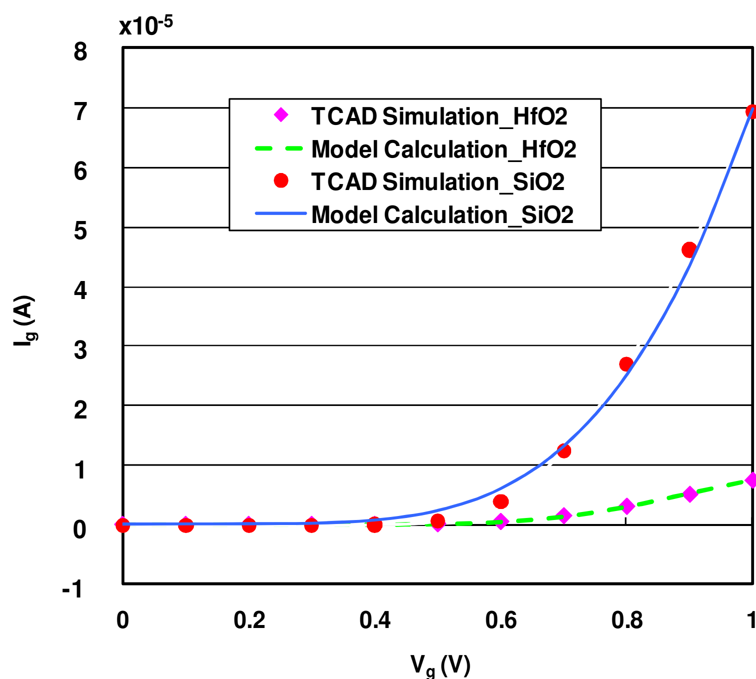

Figure 4: Analytical model calculation and TCAD simulations for the gate leakage tunneling current for UTB SOI MOSFET with HfO_2 and SiO_2 as an oxide material at $V_d = 0V$.

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The improved analytical model for two-layer gate oxide materials with SiO_2 as an interfacial layer, using a proper WKB tunneling probability, is given by:

$$J_{I_{TwoLayers}} = \frac{q^3}{8\pi h\phi_{SiO_2}} \frac{1}{k_{SiO_2}\varepsilon_0} C_{TwoLayers} T_{TwoLayers} \quad (7)$$

The correction function for the two-layer gate oxide structure ($C_{TwoLayers}$) is given by:

$$C_{TwoLayers} = \frac{V_g \pm \Delta V_g}{T_{SiO_2}} \times N_T \times \exp\{\frac{20}{\phi_{SiO_2}}(\frac{|V_{ox1}| - \phi_{SiO_2}}{\phi_0} + 1)^{\alpha_{ECB}} \times (1 - \frac{|V_{ox1}|}{\phi_{SiO_2}})\} \quad (8)$$

V_{ox1} is the voltage across the first gate oxide layer (SiO_2) [6] and $\phi_{SiO_2} = \phi_0$.

5) Results and Discussion

The simple and improved analytical direct tunneling current models are used to study the suitability of the gate insulator candidates for one and two layers in the UTB SOI MOSFETs structure. According to the latest ITRS specifications, the next generations of UTB SOI MOSFETs for the different technological nodes will require EOT = 0.85 nm and EOT = 0.8 nm for the low standby power logic applications and an acceptable gate leakage current will be 0.21 [A/cm^2] and 0.23 [A/cm^2], respectively.

The dielectric candidates required to meet low standby power application requirements depend on the technological node. In addition, the plot of the band offset as a function of dielectric constants, using the gate leakage current calculations (mentioned in section 4) for the specific conditions and requirements, is used to discuss the suitability of the dielectric materials. The curves in graphs 5 to 12 represent a minimum of the band offset required. So, all the materials above the curve could be selected materials, and not only the nearest to the curves. Therefore, when two or more dielectrics satisfy the conditions about tunneling current, one could choose between them according to the technological issues or to the best behavior with respect to the mobility.

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5.1) EOT=0.85nm and J=0.21 [A/cm^2] (15 nm Technological Node)

A) One Layer case

Initially we calculate the gate leakage current for the one-layer case as shown in Figure 1a with no interfacial layer. Figure 5 shows a plot of the barrier height (ΔE_C refers to the dielectric material barrier height in the figures) as a function of the k-value for EOT=0.85 nm, leakage current $J = 0.21[\frac{A}{cm^2}]$, $m^* = 0.26m_0$ and $V_g = 1V$ using the simple (Eq.3) and improved (Eq.5) models for the ideal interface, and with different ΔE_C and k values for metal oxides [26]. As can be seen in Fig 5, of the high-k dielectrics, Sm_2O_3, Er_2O_3, Ho_2O_3 and Lu_2O_3 appear to be promising candidates in the conditions tested for both the simple and the improved models. However, the improved model calculations predict one more appropriate dielectric, HfO_2, for the same application requirements in the case of the one-layer gate oxide (Figure 5).

Using the simple model (Eq.3) the figure of merit showing the suitable dielectrics (band offset versus dielectric constant k values curve) is shown for different values of EOT (EOT=0.85 nm, EOT=0.65 nm and EOT=0.45 nm), $m^* = 0.26m_0, V_g = 1V$ and leakage current $J = 0.21[\frac{A}{cm^2}]$ (Figure 6). The direct tunneling gate leakage current tends to increase as EOT decreases. Figure 6 shows that, depending on the value of EOT, the possible candidates for suitable dielectric materials shift toward higher dielectric constants because the EOT values decrease. The improved model (Eq. 5) shows the same trend in EOT values using the two-layer oxide models (Eq. 4, Eq. 6). In fact the EOT value is an important criterion for finding high-k dielectric materials.

Figure 5: Band offset ΔE_C as a function of the k-value for EOT=0.85 nm with $m^* = 0.26m_0, V_g = 1V$ and gate tunneling leakage current $J = 0.21[\frac{A}{cm^2}]$ using the simple and improved models.

Figure 6: Band offset ΔE_C as a function of the k-value for EOT=0.85 nm, EOT=0.65 nm and EOT=0.45 nm, $m^* = 0.26m_0$, $V_g = 1V$ and gate tunneling leakage current $J = 0.21[\frac{A}{cm^2}]$ using the simple model.

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B) SiO_2 as an Interfacial Layer

Eq.2 shows the exponential dependence of the tunneling probability in the two-layer case on the interfacial layer thickness (T_{SiO_2}); as a result the direct tunneling gate leakage current (Eq. 4 and Eq. 7) also exponentially depends on T_{SiO_2}. We study the suitability of high-k dielectric materials depending on the interfacial layer thickness.

Figure 7 shows the band offset as a function of the k-value for EOT=0.85 nm with two different interfacial layer thicknesses ($T_{SiO_2} = 0.35nm$ and $T_{SiO_2} = 0.55nm$) using the simple (Eq. 4) and improved (Eq. 7) analytical gate leakage current models. We see in Figure 7 that using the improved model (Eq. 7) with $m^* = 0.26m_0$, $V_g = 1V$ and leakage current $J = 0.21[\frac{A}{cm^2}]$, of the high-k gate oxides, the best candidates near the minimum of the band offset, are CeO_2, ZrO_2 and HfO_2. By changing only the interfacial layer (SiO_2) thickness (assuming all other parameters are the same as before) to $T_{SiO_2} = 0.55nm$ the preferred high-k materials near the minimum of the band offset, are Pr_2O_3 in the hexagonal phase, La_2O_3 and La_2CuO_4. In fact, the thickness of SiO_2 (as an interfacial layer) affects which candidates should be chosen to meet the technological node requirements. The same trend is observed when the simple model is used with different thicknesses of the interfacial layer (SiO_2) to select suitable dielectrics (Figure 7).

The tunneling electron effective mass in dielectric materials changes with the oxide thickness and voltage across the oxide materials [24] and the values reported in the literature vary over a wide range [27, 28]. We have shown the role of electron effective mass values and their effect on the determination of suitable dielectrics.

Figure 8 shows the band offset as a function of the k-value for two different values of the tunneling electron effective mass, $m^* = 0.20m_0$ and $m^* = 0.60m_0$ (EOT=0.85 nm with t_{SiO2}=0.55 nm, $V_g = 1V$ and leakage current $J = 0.21[\frac{A}{cm^2}]$) using the simple (Eq.4) and improved (Eq.7) gate leakage current models.

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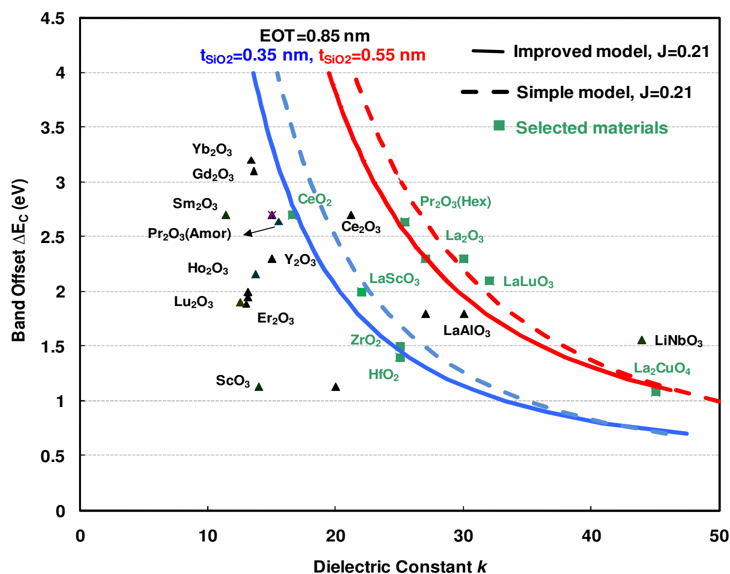

Figure 7: Band offset ΔE_C as a function of the k-value for EOT=0.85 nm (with t_{SiO2}=0.35 nm and t_{SiO2}=0.55 nm), $m^* = 0.26 m_0$, $V_g = 1V$ and gate tunneling leakage current $J = 0.21[\frac{A}{cm^2}]$ using the simple and improved models.

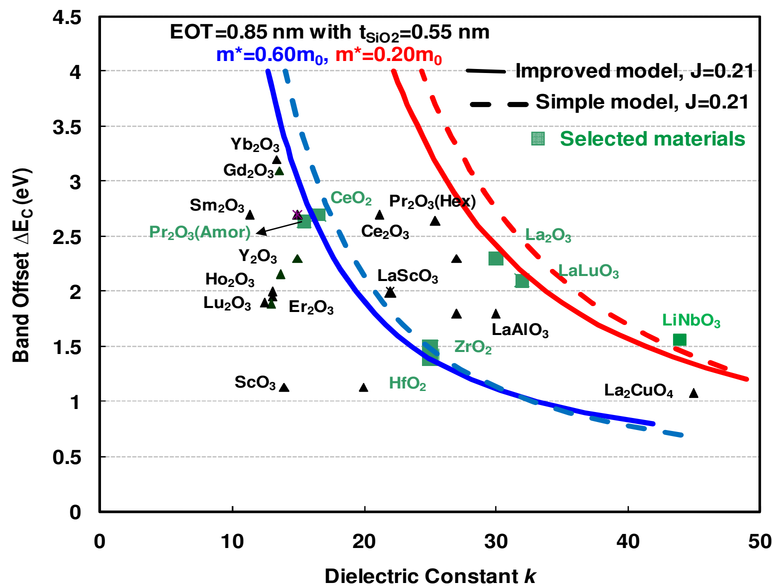

Figure 8: Band offset ΔE_C as a function of the k-value for EOT=0.85 nm with t_{SiO2}=0.55 nm, $m^* = 0.20 m_0$, $m^* = 0.60 m_0$, $V_g = 1V$ and gate tunneling leakage current $J = 0.21[\frac{A}{cm^2}]$ using the simple and improved models.

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As shown by the models, if the electron effective mass value is increased, the guideline (band offset as a function of dielectric constant curves) for finding the suitable high-k materials shifts toward a lower dielectric constant region (Figure 8). In fact the models considered have the ability to take into account (during the determination of suitable high-k materials) the effect of electron effective mass in the calculation of gate leakage current. The results indicate that the exact value of electron effective mass plays an important role in the accurate determination of the favorable dielectric candidates.

5.2) EOT=0.80nm and J=0.23 [A/cm^2] (14 nm Technological Node)

According to the latest ITRS, there are a number of requirements (equivalent oxide thickness and gate leakage current density) for the 14 nm technological node of UTB SOI MOSFETs.

A) One Layer Case

We predicted the suitable alternative high-k gate dielectrics (the optimal k and barrier height values) that fulfill the requirements of low standby power operation for UTB SOI MOSFETs using the simple (Eq. 3) and improved (Eq. 5) gate leakage current models for a one-layer gate oxide (the ideal case with no interfacial layer).

Figure 9 shows the band offset as a function of the k-value for EOT=0.80 nm with $m^* = 0.26m_0$, $V_g = 1V$ and leakage current $J = 0.23[\frac{A}{cm^2}]$ when the simple and improved models of the gate leakage current are used. According to Figure 9, high-k candidates such as Sm_2O_3 and Er_2O_3 fulfill the requirements when the improved model is used (Eq.5). Ho_2O_3 and Lu_2O_3 are the preferred dielectrics, near the minimum of the band offset, predicted by the simple model (Eq.3) for the same technological node requirements. In this technological node, these candidates produce acceptable gate leakage currents (J = 0.23 [A/cm^2]) for the EOT = 0.80 nm. HfO_2 can also be one of the feasible candidates in this case (see Figure 9).

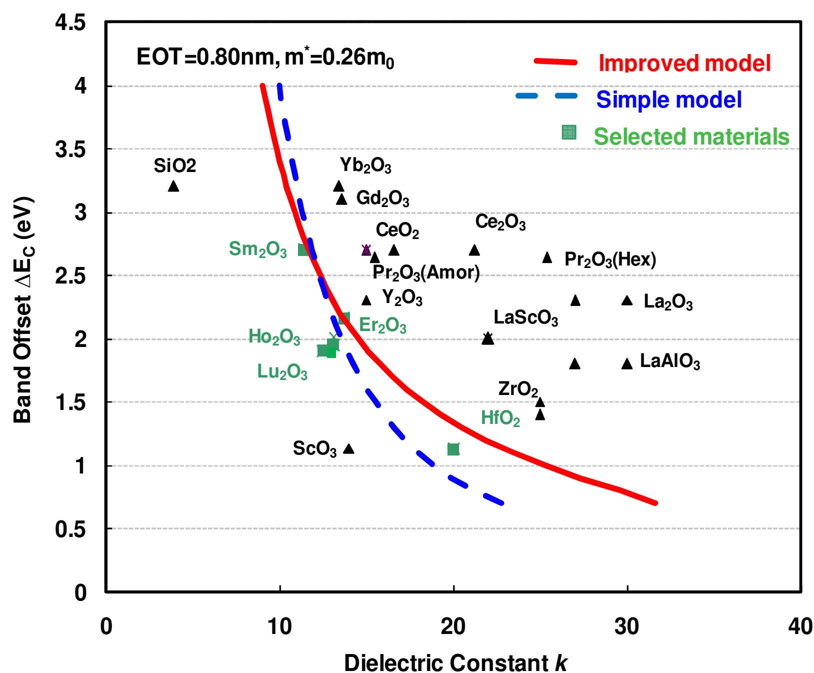

Figure 9: Band offset ΔE_C as a function of the k-value for EOT=0.80 nm with $m^* = 0.26m_0, V_g = 1V$ and gate tunneling leakage current $J = 0.23[\frac{A}{cm^2}]$ using the simple and improved models.

Interestingly, the simple (Eq. 3) and improved (Eq. 5) models lead to very similar results for both technological node requirements (Figure 5 and Figure 9), despite their different gate leakage current density and EOT values for UTB SOI MOSFETs with no interfacial layer.

B) SiO_2 as an Interfacial Layer

Using the simple (Eq. 4) and improved (Eq. 7) gate leakage current models, Figure 10 shows the band offset as a function of the k-value for EOT=0.80 nm, $m^* = 0.26m_0$, $V_g = 1V$ and leakage current $J = 0.23[\frac{A}{cm^2}]$ and two different values of interfacial layer (SiO_2) thicknesses ($T_{SiO_2} = 0.30nm$ and $T_{SiO_2} = 0.50nm$).

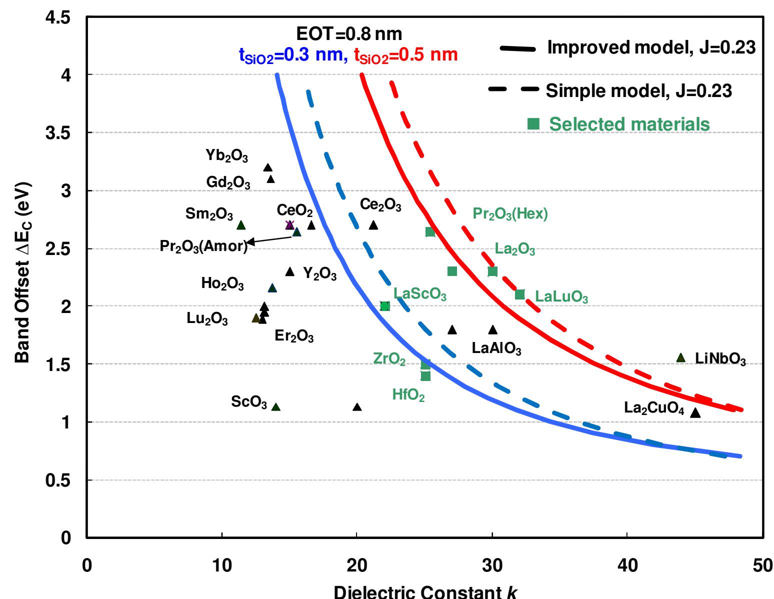

Figure 10: Band offset ΔE_C as a function of the k-value for EOT=0.80 nm (with t_{SiO2}=0.30 nm and t_{SiO2}=0.50 nm), $m^* = 0.26m_0$, $V_g = 1V$ and gate tunneling leakage current $J = 0.23[\frac{A}{cm^2}]$ using the simple and improved models.

For $T_{SiO_2} = 0.30nm$ the dielectrics, near the minimum of the band offset, predicted by the improved model are $LaScO_2$, ZrO_2 and HfO_2. Pr_2O_3 gives an acceptable leakage current (J = 0.23 [A/cm^2]) when the same model and parameters are used for $T_{SiO_2} = 0.50nm$. The simple model predicts $LaScO_2$ for $T_{SiO_2} = 0.30nm$ and La_2O_3 and $LaLuO_3$ for $T_{SiO_2} = 0.50nm$. The results of barrier height calculations show that different interfacial layer thicknesses can draw the curves for the 15 nm node requirements presented in Figure 7 closer to the curves for the 14 nm technological node requirements presented in Figure 10.

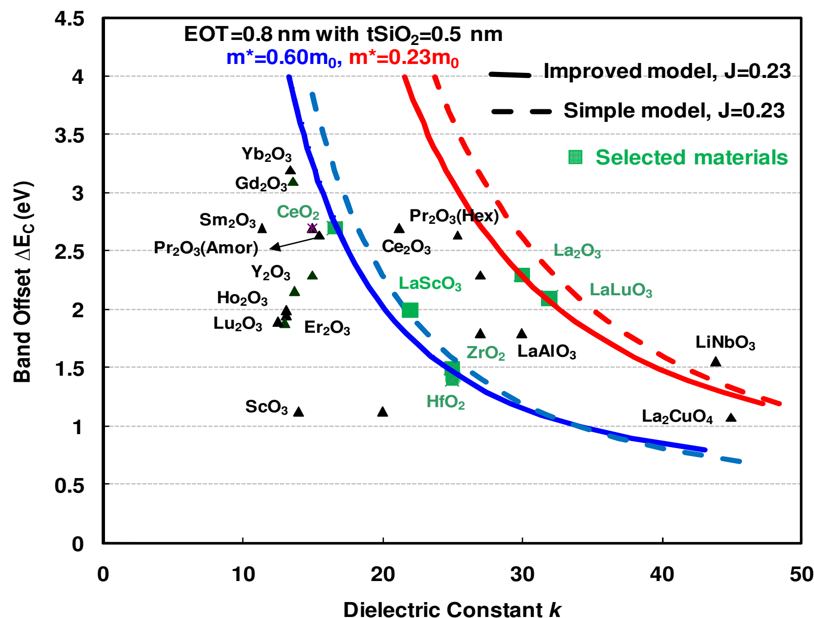

Figure 11: Band offset ΔE_C as a function of the k-value for EOT=0.80 nm with t_{SiO2}=0.50 nm, $m^* = 0.23m_0$, $m^* = 0.60m_0$, $V_g = 1V$ and gate tunneling leakage current $J = 0.23[\frac{A}{cm^2}]$ using the simple and improved models.

Figure 11 shows the band offset as a function of the k-value for EOT=0.80 nm with $T_{SiO_2} = 0.50nm$, $V_g = 1V$ and leakage current $J = 0.23[\frac{A}{cm^2}]$ when the simple (Eq. 4) and improved (Eq. 7) leakage current models are used for two different electron effective mass values ($m^* = 0.23m_0, m^* = 0.60m_0$).

The results show that appropriate oxide materials depend on the value of electron effective mass (all other parameters being the same). Therefore, the electron effective mass value (which is almost a fitting parameter) has an important role in determining suitable dielectric materials. Finally figure 12 shows the possible candidates for EOT=0.90 nm with $m^* = 0.26m_0$, $V_g = 1V$ and leakage current $\mathrm{J} = 0.19\left[\frac{\mathrm{A}}{\mathrm{cm}^2}\right]$ (17nm technological node requirements) using the simple and improved models of the gate leakage current.

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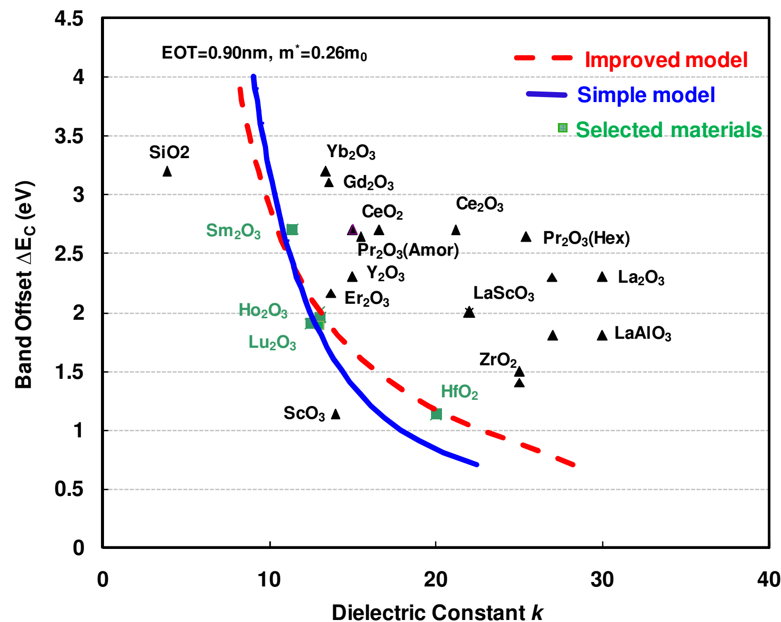

Figure 12: Band offset ΔE_C as a function of the k-value for EOT=0.85 nm with $m^* = 0.26 m_0, V_g = 1V$ and gate tunneling leakage current $J = 0.19\left[\frac{A}{cm^2}\right]$ using the simple and improved models.

The gate leakage direct tunneling current is a highly sensitive function of the oxide thickness, interfacial layer thickness and electron effective mass value. It has been observed that the choice of the suitable dielectric materials is affected by variations in the oxide thickness, interfacial layer thickness or electron effective mass. It should be pointed out that in general the simple and improved model predict similar results and, therefore, for the sake of analytical simplicity the simple model can be used because its accuracy is similar to that of the improved model.

6) Conclusion

Analytical models of the gate tunneling leakage current have been developed and used to identify the most promising high-k candidates for the UTB SOI MOSFETs structure, in cases with no interfacial layer and with SiO_2 as an interfacial layer in order to satisfy the requirements of low standby power applications according to the latest

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ITRS roadmap. The suitability of the materials depends on the technology node requirements and, particularly, EOT, the electron effective mass and interfacial layer thickness can change the choice of the dielectric candidates. It has been found that HfO_2 and Lu_2O_3 are the most promising gate oxide materials for the 17nm, 15nm and 14nm technological node requirements assuming the ideal case with no interfacial layer. This study provides additional insight into choosing the favorable dielectric candidates for the different technological nodes in the future.

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Chapter 4

Gate Leakage Current Partitioning in Nanoscale Double-Gate MOSFETs, Using Compact Analytical Model

This chapter presents a compact gate leakage current partitioning model for nanoscale Double Gate (DG) MOSFETs, using analytical models of the direct tunneling gate leakage current. Gate leakage current becomes important and an essential aspect of MOSFET modeling as the gate oxide thickness is scaled down to 1nm and below in advanced CMOS processes. We considered an ideal interface (ideal case without an interfacial layer) and two layers high-k dielectric materials as gate insulators. In the case of two layers, a thin layer of SiO_2 as an interfacial layer is considered. The results of the gate current partitioning components into drain and source show good agreement with 2D TCAD numerical device simulation (Silvaco ATLAS).

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1) Introduction

The continuous reduction of the gate oxide layer thickness in advanced CMOS devices to 1nm and below causes an increase of the gate leakage current density, due to the increasing carrier direct tunneling and can become an important undesirable effect on the device operation [1, 2]; besides, it increases power dissipation and can deteriorate the device performance and circuit stability [3] for every process generation. Part of the gate leakage current (I_{gc}) is collected by the source (I_{gcs}) while the rest goes to the drain (I_{gcd}). For an accurate characterization and modeling of the tunneling current through high-k gate stacks and its effect on device and circuit performance, it is essential to derive a compact model of the partition of the leakage current flowing between gate and channel into the source (I_{gcs}) and drain (I_{gcd}) components. Several authors have studied and modeled the gate leakage current partition in single gate MOSFET structures [4-6].

The main goal of the present chapter is to develop a compact analytical model of the partitioning of the direct tunneling gate leakage current (I_{gc}) in nanoscale Double-Gate (DG) MOSFETs. This model consists of analytical equations for the gate-source and the gate-drain tunneling components. A gate leakage current model was developed and implemented in our previous surface potential based model [7, 8] which includes short channel effects related to the DG MOSFET structure. We considered an ideal case, with one layer gate insulator, and also the case of a two-layer dielectric stack with a thin layer of SiO_2 (in order to maintain a good interface with substrate) as an interfacial layer with a suitable gate oxide material (HfO_2) are being proposed [9, 10].

In this chapter, in order to derive the gate-source (I_{gcs}) and gate-drain (I_{gcd}) leakage current components, current continuity equation is considered in the presence of gate leakage current as a perturbation for a DG MOSFET at the voltage along the channel as a function of x, which is 0 at the source and L (channel length) at the drain. In fact the main goal of partition modeling is to solve the current continuity equation for the channel current in the presence of the gate leakage. The model is therefore

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based on the underlying physics of the direct gate tunneling current and its components into the source and drain, and has been successfully validated by comparison with 2D TCAD numerical device simulation.

2) Double Gate MOSFET Structure

The double-gate transistor structure under analysis is shown in Figure 1; I_{gc} is the leakage current flowing between gate and channel. I_{gcs} is the part of the gate to channel leakage current collected by the source and I_{gcd} is the rest of the gate to channel leakage current and goes to the drain.

In order to carry out a physical modeling of the gate leakage current flowing between gate and channel, the availability of expressions of the surface potential and the electric field into the gate oxide materials are essential. In our previous works [7, 8] we developed an advanced compact model for the surface potential and drain current which considered short channel effects for a DG MOSFET structure. We show the calculated surface potential at the Si-SiO_2 (or Si-HfO_2) interface using our compact model in inset of Figure 2 as a function of drain voltage (V_{ds}) at gate applied voltage $V_g = 1V$ for the considered structure and parameters according Figure 1. The results from our model for the presented structure are in good agreement with the one obtained from 2D TCAD numerical device simulation.

The surface electric field (E_s) is obtained by using Poisson's equation as a function of the potential at the surface (ϕ_S) and at the center of the Si layer (ϕ_o) [7, 8]:

$$E_s = \sqrt{\frac{2qN_a\phi_t}{\varepsilon_s}} \times \sqrt{(\frac{\phi_S - \phi_O}{\phi_t}) + (1 - e^{-(\frac{\phi_S - \phi_O}{\phi_t})}) \times e^{(\frac{\phi_S - 2\phi_F - V/2}{\phi_t})}} \tag{1}$$

where $\phi_t = \dfrac{kT'}{q}$ is the thermal potential, k is the Boltzmann constant, q is the electron charge and T' is the temperature in K, N_a is the uniform acceptor concentration in-

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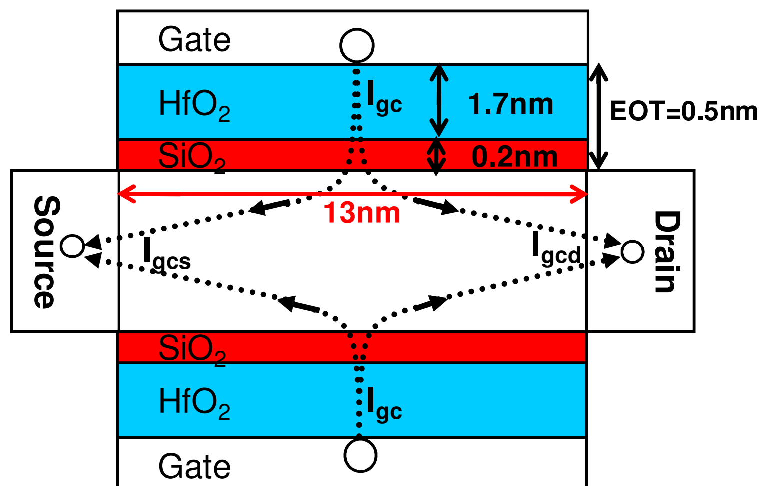

Figure 1: Diagram of a double gate MOSFET structure analyzed. I_{gc} is the gate-to-channel tunneling current. It is partitioned into I_{gcs} and I_{gcd}, which flow to the source and to the drain respectively.

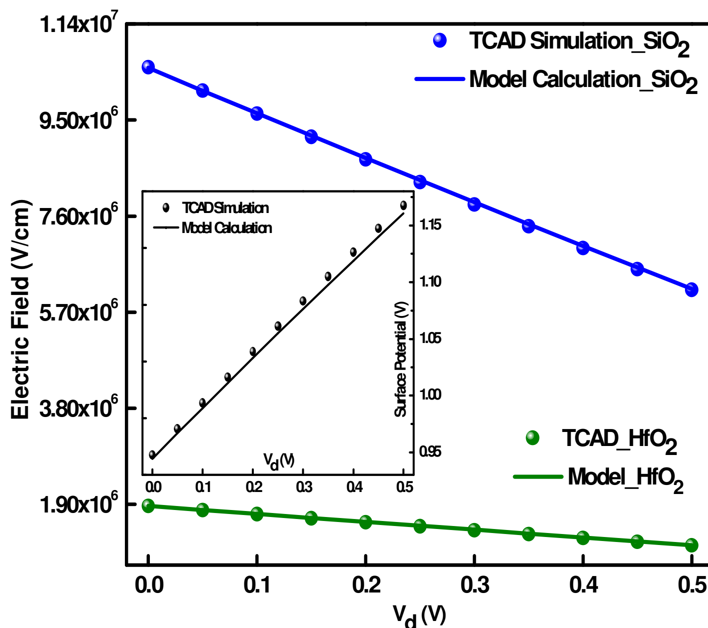

Figure 2: Analytical model calculations and 2D TCAD numerical simulations of the surface electric field pointing at the interfacial layer (SiO_2) at the Si-SiO_2 interface, and at the high-k layer (HfO_2) at the SiO_2-HfO_2 interface, Inset: the surface potential at the Si-SiO_2 (or Si-HfO_2) interface as a function of drain voltage at $V_g = 1V$.

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the silicon layer, ϕ_{Fp} is the quasi Fermi level for holes in the P-type silicon layer and ϕ_{Fn} is the quasi Fermi level for electrons. The potential along the channel is $V = \phi_{Fn} - \phi_{Fp}$, and ϕ_{Fp} renamed as ϕ_F .

Figure 2 shows the comparison between the model calculations (Eq.1) and 2D TCAD numerical device simulations of the electric fields considering materials and conditions as shown in Figure 1. Both the surface electric field as a function of drain voltage at $V_g = 1V$, pointing at SiO_2 at the interface of the Si-SiO_2 (Figure 2) and the surface electric field (pointing at the HfO_2 layer) at the interface of the SiO_2-HfO_2 (Figure 2) using Eq.1 show a good agreement with 2D TCAD simulation results. Using the considered electric fields, the model will be able to calculate the gate leakage current in order to obtain the source and drain components of the gate to channel leakage current.

3) Tunneling Probability Approximation

The tunneling probability depends on the potential barrier shape. Using the Wentzel-Kramers-Brillouin (WKB) approximation, it can be calculated for given conditions (one layer and two layers gate oxide dielectrics) and structures as shown in Figure 1 [11, 12]. A proper WKB approximation method can be used to calculate the tunneling probability of a carrier through the dielectric stack structure. Parameters such as the SiO_2 and dielectric material thicknesses and barrier heights at the various interfaces, dielectric constant and electron effective mass values across the dielectric stacks, have been taken into account.

An approximate expression for the transmission in the case of one layer gate oxide is:

$$T_{1-Layer} = \exp\left\{ \frac{ -\frac{8\pi\sqrt{2m_{High-k}}\,\phi_{High-k}^{\frac{3}{2}}}{3hq}\left[1-\left(1-\frac{V_{Ox}}{\phi_{High-k}}\right)^{\frac{3}{2}}\right] }{E_{High-k}} \right\} \qquad (2)$$

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m_{High-k} is the electron effective mass in the high-k material, $\phi_{BHigh-k}$ is the conduction band offset for the dielectric material, q is the electron charge, h is the Planck's constant. The voltage across the high-k material (V_{ox}) is given by $V_{ox} = V_g - V_{Fb} - \phi_S$ where V_g is the applied gate voltage, V_{Fb} is flat band voltage; on the other hand, using our compact model for the potential of a DG MOSFET, the potential at the surface (ϕ_S) was obtained.

SiO_2 has a low dielectric constant, but in all other aspects remains an excellent insulator [13]. It would be useful to keep the advantages of SiO_2 and at the same time to use a suitable new high-k dielectric in a SiO_2/high-k gate stack. Using SiO_2 as an interfacial layer for the two layer case, tunneling probability for direct tunneling is given by [14]:

$$T_{2-Layers} = \exp\left\{\frac{8\pi}{3h}\frac{k_{SiO_2}\times T_{High-k} + k_{High-k}\times t_{SiO_2}}{V_{ox}\times k_{High-k}}\sqrt{2m_{SiO_2}q}[\phi_{BSiO_2}^{\frac{3}{2}} - (\phi_{BSiO_2} - fV_{ox})^{\frac{3}{2}}]\right\}\times$$
$$\exp\left\{\frac{8\pi}{3h}\frac{k_{SiO_2}\times T_{High-k} + k_{High-k}\times t_{SiO_2}}{k_{SiO_2}\times V_{ox}}\sqrt{2m_{High-k}q}[(\phi_{BHigh-k} - fV_{ox})^{\frac{3}{2}} - (\phi_{BHigh-k} - V_{ox})^{\frac{3}{2}}]\right\} \quad (3)$$

m_{SiO_2} ($m_{SiO_2} = 0.50m_0$) is the electron effective mass in the SiO_2, m_0 is the free electron mass, ϕ_{BSiO_2} ($\phi_{BSiO_2} = 3.2eV$) is the conduction band offset for the SiO_2, f is EOT fraction of the first layer (SiO_2 thickness divided by EOT value), k_{SiO_2} and k_{High-k} are the SiO_2 and high-k dielectric constant, t_{SiO_2} and T_{High-k} are the physical thicknesses of SiO_2 and high-k materials and E_{High-k} is the electric field across the high-k material which was considered in the second section [15, 16].

Once the tunneling probability for the considered conditions and structure was established, the tunneling current can be calculated in all cases considering the tunneling probability function accordingly.

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4) Gate Leakage Current Model and Comparison

Only the direct tunneling mechanism is considered in our analysis, as the main contribution to the tunneling current for high gate voltage ($V_g = 1V$) [15, 18]. The interface trap charge is neglected due to the small interface trap density at the interface [19, 20].

A) One Layer Gate Insulator

Our analytical direct tunneling gate leakage current model is based on a proper WKB electron tunneling probability for one layer gate oxide becomes:

$$J_{1Layer} = \frac{q^3}{8\pi h \phi_{BHigh-k}} \frac{1}{k_{High-k}\varepsilon_0} C_{1Layer} T_{1Layer} \quad (4)$$

where ε_0 is permittivity of free space and the correction function (C_{1Layer}) in the case of ideal interface without any interfacial layer becomes:

$$C_{1Layer} = \frac{V_g \pm \Delta V_g}{T_{High-k}} \times N_T \times \exp\{\frac{20}{\phi_{BHigh-k}}(\frac{|V_{ox}| - \phi_{BHigh-k}}{\phi_0} + 1)^{\alpha_{ECB}} \times (1 - \frac{|V_{ox}|}{\phi_{BHigh-k}})\} \quad (5)$$

ΔV_g is a fitting parameter [21], the value ϕ_0 is only slightly different from $\phi_{BHigh-k}$ therefore we can assume $\phi_{BHigh-k} \approx \phi_0$, α_{ECB} is a fitting parameter depending on the tunneling process and $\alpha_{ECB} = 0.6$ provides the overall best fit for C_{1Layer} [17]. N_T represents the behavior of density of carriers [21] and its expression was adapted to the DG MOSFET structure in Figure 1.

The gate to channel leakage current (I_{gc}) depends on V_{ds}, which controls the position dependence of the Fermi level along the channel, which makes I_{gc} a decreasing function of V_{ds} (see Figure 3).

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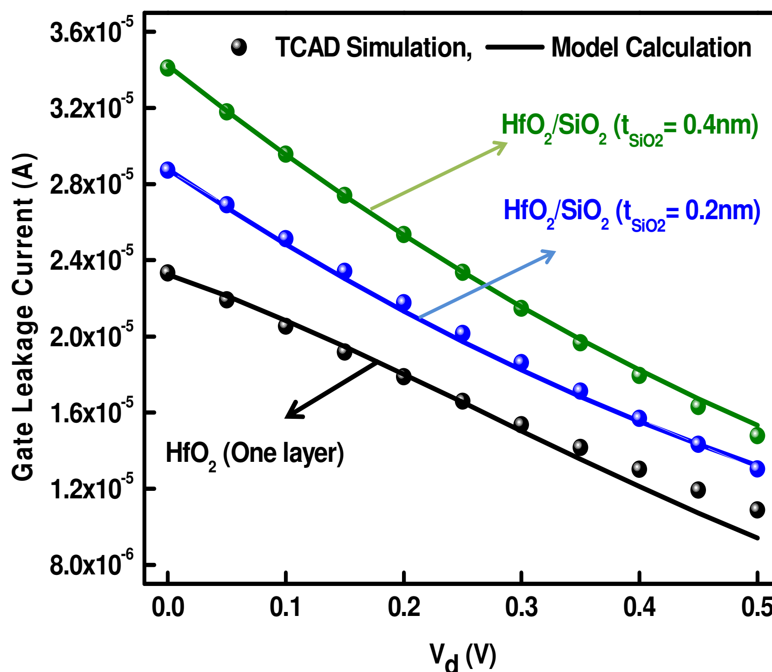

Figure 3: Analytical model and 2D TCAD numerical simulations of the direct tunneling gate leakage current in the case of one layer gate oxide (HfO_2), and two layer case with interfacial layer (SiO_2) thickness equal to 0.2 nm, 0.4 nm and HfO_2 as a high-k material versus drain voltage with EOT=0.5 nm, $V_g = 1V$ for a DG MOSFET.

First of all, we developed a gate leakage current model without interfacial layer (ideal case) based on a compact analytical model for the electric potential. Figure 3 shows the behavior of the direct tunneling gate to channel leakage current as a function of drain voltage at $V_g = 1V$ obtained by the analytical model calculations (Eq. 4) and 2D TCAD numerical device simulations in the case of one layer gate oxide with EOT=0.5nm and HfO_2 as a high-k material for a DG MOSFET structure. There is a very good agreement especially at low drain voltage where there is a maximum gate leakage current.

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B) Two Layer Gate Insulator

The presence of an interfacial layer (SiO_2) increases the EOT of the gate stack, which should thus be as thin as possible to achieve the EOT value required by the International Technology Roadmap for Semiconductors (ITRS).

An approximate analytical model with a proper WKB electron tunneling probability for two layers gate oxide was proposed in [14, 17]:

$$J_{2_{Layers}} = \frac{q^3}{8\pi h \phi_{BSiO_2}} \frac{1}{k_{SiO_2}\varepsilon_0} C_{2Layers} T_{2Layers} \qquad (6)$$

The correction function $(C_{2Layers})$ for the two layer gate oxide (SiO_2-HfO_2) material can be expressed as:

$$C_{2Layers} = \frac{V_g \pm \Delta V_g}{t_{SiO_2}} \times N_T \times \exp\{\frac{20}{\phi_{BSiO_2}}(\frac{|V_{ox1}| - \phi_{BSiO_2}}{\phi_0}+1)^{\alpha_{ECB}} \times (1 - \frac{|V_{ox1}|}{\phi_{BSiO_2}})\} \qquad (7)$$

An applied gate voltage will partly drop over the interfacial layer and the high-k material, whereas the distribution depends on the physical layer thicknesses and the k-values. The applied bias V_g is related to the voltage drop across the stack (V_{ox}) through the potential balance equation and $V_{ox} = V_{ox1} + V_{ox2}$ where the V_{ox1}, V_{ox2} are the voltages across the first (SiO_2) and second gate oxide layers respectively. The voltage across the ith dielectric is given by the relation [22]:

$$V_{oxi} = \frac{\frac{d_i}{\varepsilon_i}}{\sum_{j=1}^{N} \frac{d_j}{\varepsilon_j}} V_{ox} \qquad (8)$$

where d_i and ε_i are the thickness and permittivity of the ith gate dielectric layer. The changes in voltage across dielectrics by a change in gate voltage are taken into account.

This expression has been adapted to the DG MOSFET structure in Figure 1 with SiO_2 as an interfacial layer and HfO_2 as a high-k material (two layers gate stack), and incorporated to our advanced surface potential based compact MOSFET model for the potential and drain current including short channel effects.

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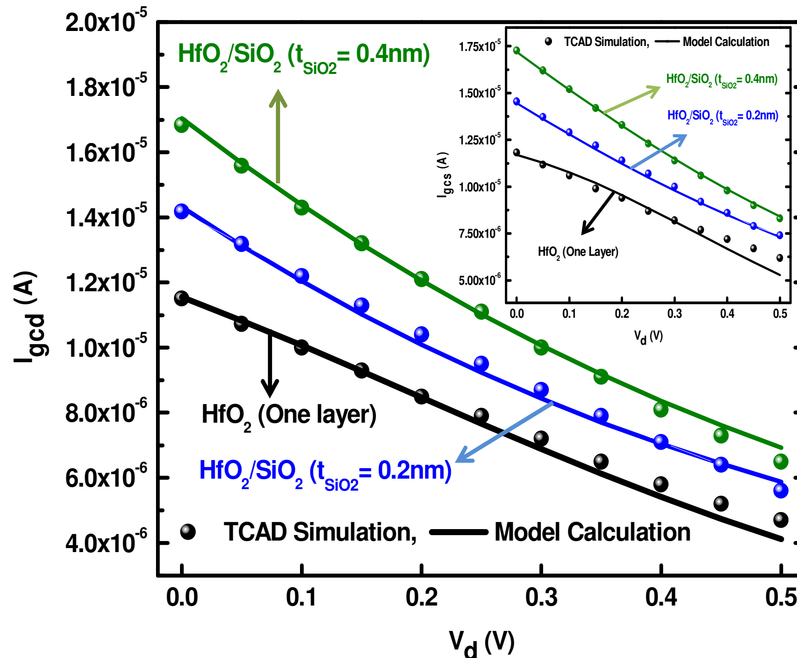

Figure 4: Analytical model and 2D TCAD simulations of the direct tunneling gate-drain (Inset: gate-source) leakage current component, in the cases of one layer gate oxide (HfO_2) and two layer gate insulator (HfO_2/SiO_2) with an interfacial layer (SiO_2) thickness equal to 0.2 nm, 0.4 nm and HfO_2 as an oxide material with EOT=0.5 nm and $V_g = 1V$ for a DG MOSFET structure as a function of drain voltage.

Figure 3 shows the direct tunneling current as a function of the drain voltage with HfO_2 and SiO_2 as a gate oxide stack at V_g = 1 obtained by our model calculations (Eq.6) and TCAD numerical simulations. There is a good agreement between the analytical model calculations and 2D TCAD numerical device simulations. It can be seen in Figure 3, that by increasing the interfacial layer thickness (t_{SiO2}) for the same EOT value (EOT=0.5nm), the gate leakage current and accordingly gate-drain and gate-source components of the leakage current will be increased (as shown in Figure 4).

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5) Gate Leakage Partition Model and Validation

In this section, the gate leakage partition model based on the considered analytical gate leakage current models for the one and two layer gate insulators is developed and analyzed for a DG MOSFET structure. In order to obtain the gate current partition, current continuity equation in the presence of the gate leakage current is necessary to solve.

We have adapted to a DG MOSFET structure the gate leakage model with source-drain partitioning that was derived for single gate MOSFET [4]. Using the drift equation, the drain current for a DG MOSFET structure is given by:

$$I_x = 2\mu C_{ox}(V_{gs} - V_{th} - V)\frac{dV}{dx} \qquad (9)$$

The current continuity equation for DG MOSFET structure is introduced:

$$2\times\frac{d\left[\left(V_g - V_{th} - V\right)\frac{dV}{dx}\right]}{dx} + \frac{J_g(x)}{\mu C_{ox}} = 0 \qquad (10)$$

V_{th} is the threshold voltage, V is the channel potential reference to the source, μ is the mobility, C_{ox} is the oxide capacitance and $J_g(x)$ is the gate current density as a function of channel location.

The current continuity equation assumed for DG MOSFET is solved without gate leakage current ($J_g(x) = 0$). This assumption leads to exactly the same condition and results of single gate MOSFET:

$$V_0(x) = V_g - V_{th} - \sqrt{(V_g - V_{th})^2 - 2(V_g - V_{th} - \frac{V_{ds}}{2})V_{ds}\frac{x}{L}} \approx (V_g - V_{th} - \frac{V_{ds}}{2})\frac{V_{ds}}{(V_g - V_{th})}\frac{x}{L} \qquad (11)$$

where $V_0(x)$ is the solution of Eq. (10) without gate leakage current.

The inclusion of the gate leakage current causes the change of channel potential along the channel $V(x) = V_0(x) + V_1(x)$, assuming the gate leakage current is much smaller than the drain current, the gate leakage current perturbation on $V(x)$ is small

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and $V_0(x) \gg V_1(x)$ is the approximation that leads to obtain analytical solution for the leakage current perturbation:

$$(V_{gs}-V_0)\frac{d^2V_1}{dx^2}-\frac{V_1 d^2V_0}{dx^2}-\frac{2dV_0}{dx}\frac{dV_1}{dx}+\frac{J_{g0}e^{-\beta V_0}}{2\mu C_{ox}}=0 \quad (12)$$

J_{g0} is the gate leakage current density with $V_{ds}=0$ which can be modeled by equation (4) and (6), $\beta = 8\pi\frac{\sqrt{2qm_{ox}\phi_b^3}}{3h}\frac{T_{ox}}{V_g^2}P$. Note that P is a model parameter added for flexibility with a default value of one.

Based on the boundary condition $V_1(0)=V_1(L)=0$, assuming that the gate leakage current is much smaller than the drain current and $V_0 \gg V_1$, the analytical solution of V_1, can be presented by:

$$V_1 = -\frac{J_{g0}\left[(e^{-\beta Kx}-1)+\frac{x}{L}(1-e^{-\beta KL})\right]}{2\mu C_{ox}\beta^2 K^2 (V_{gs}-Kx)} \quad (13)$$

where $K=(V_g-V_{th}-\frac{V_{ds}}{2})\frac{V_{ds}}{(V_g-V_{th})L}$

The gate to channel tunneling leakage current partition between the channel and the source (I_{gcs}) becomes:

$$I_{gcs}=2\mu C_{ox}(V_{gs}-V_{th})W\frac{dV_1}{dx}\Big|_{x=0}=\frac{J_{g0}WL(\beta KL+e^{-\beta KL}-1)}{2\beta^2K^2L^2} \quad (14)$$

Using the gate to channel direct tunneling current density calculations from the expressions (4 and 6), the gate-to-source component is determined based on expression (14). In the case of one layer gate oxide (HfO_2) and two layer gate insulator (HfO_2/SiO_2) with an interfacial layer (SiO_2) thickness equal to 0.2 nm, 0.4 nm and HfO_2 as an oxide material with EOT=0.5nm and $V_g = 1V$ for a DG MOSFET structure, the source component of gate leakage current as a function of drain voltage is shown in the inset of Figure 4. Considering two different thickness of the interfacial

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layer (t_{SiO2}=0.2nm and t_{SiO2}=0.4nm) we can see in Figure 4 the influence and impact of the thickness of the intermediate SiO_2 layer. It is shown in the inset of Figure 4, that the gate-source component of the leakage current increases with the interfacial layer thickness while keeping the same EOT value. The comparison with the 2D TCAD numerical device simulations shows a very good agreement with the analytical model as shown in Figure 4.

The drain component of the gate to channel tunneling leakage current (I_{gcd}) can be obtained as:

$$I_{gcd} = -2\mu C_{ox}(V_{gs} - V_{th} - KL)W \frac{dV_1}{dx}\Big|_{x=L} = -\frac{J_{g0}WL(\beta KLe^{-\beta KL} + e^{-\beta KL} - 1)}{2\beta^2 K^2 L^2} \quad (15)$$

The direct tunneling gate to drain current described by an analytical model (Eq.15) is used to calculate the drain component of the gate leakage current (Figure 4). The comparison with 2D TCAD numerical device simulations is shown in the cases of one layer gate oxide (HfO_2) and two layer gate insulator (HfO_2/SiO_2) with an interfacial layer (SiO_2) thickness equal to 0.2 nm, 0.4 nm and HfO_2 as an oxide material with EOT=0.5nm and $V_g = 1V$ for a DG MOSFET structure as a function of drain voltage. According to Figure 4 the impact of SiO_2 layer as an interfacial layer has been shown and as it is expected the gate-drain component of the leakage current increase by increasing interfacial layer thickness for the same EOT value.

Therefore, we have obtained the components of the gate to channel leakage current that go to the source and to the drain in terms of the drain voltage. When V_{ds} equals zero as it is expected the gate leakage current is equally divided between source and drain (50/50 partition). As V_{ds} increases the ratio of current goes to the source increases, accompanied by a decrease the ratio of current goes to the drain.

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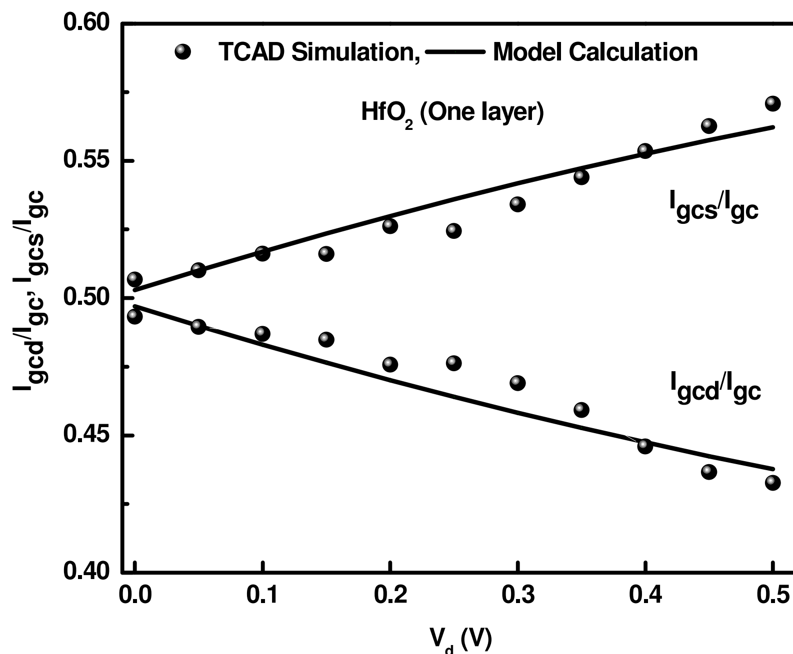

Figure 5: Analytical model and 2D TCAD simulation of the direct tunneling gate leakage current partitioning ratios ($\frac{I_{gcs}}{I_{gc}}$ and $\frac{I_{\text{gcd}}}{I_{gc}}$) in the cases of one layer gate oxide (HfO_2) with EOT=0.5nm and $V_g = 1V$ for a DG MOSFET structure as a function of drain voltage.

To consider the drain bias effect, I_{gc} is split into two components such as I_{gcs} and I_{gcd} that is $I_{gc} = I_{gcs} + I_{\text{gcd}}$, then the gate leakage current as a function of drain voltage can be easily calculated as:

$$I_{gc} = \frac{J_{g0} WL(1 - e^{-\beta KL})}{2\beta KL} \tag{16}$$

The analytical model calculations of the direct tunneling gate leakage current partition into the source/drain (Eqs. 14 and 15) and the source/drain component ratio ($\frac{I_{gcs}}{I_{gc}} / \frac{I_{\text{gcd}}}{I_{gc}}$) of the gate to channel leakage current (Eq. 16) are shown in Figure 4 and Figure 5.

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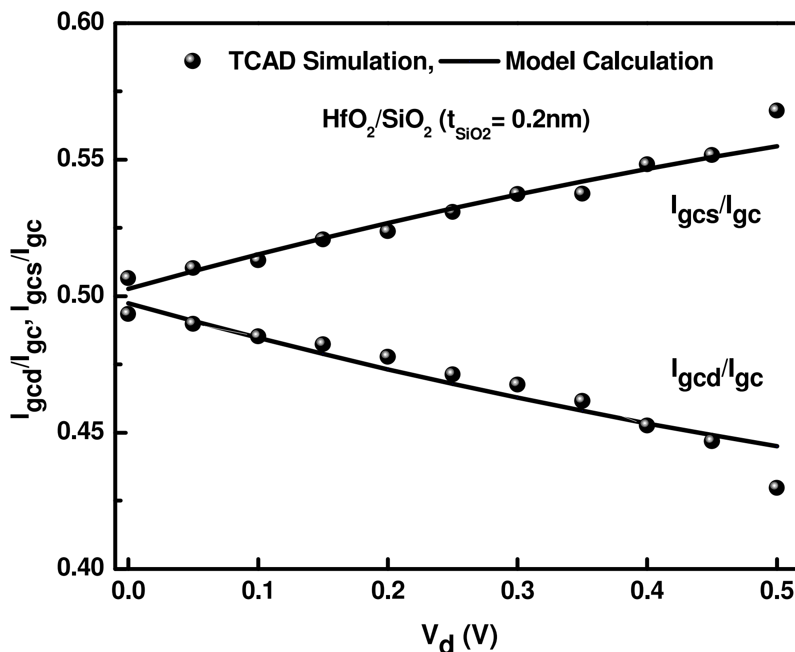

Figure 6: Analytical model and 2D TCAD numerical simulations of the direct tunneling gate leakage current partitioning ratios ($\frac{I_{gcs}}{I_{gc}}$ and $\frac{I_{\text{gcd}}}{I_{gc}}$) in the case of two layer gate insulator (HfO_2/SiO_2) with an interfacial layer (SiO_2) thickness equal to 0.2 nm and HfO_2 as an oxide material with EOT=0.5 nm and $V_g = 1V$ for a DG MOSFET structure as a function of drain voltage.

The comparison of the results obtained from the analytical models and 2D TCAD numerical device simulations in the case of one layer gate oxide (HfO_2) with EOT=0.5nm and $V_g = 1V$ for a DG MOSFET structure as a function of drain voltage shows that both models are accurate enough.

Figure 6 shows our analytical model calculations (Eqs.14 and 15) and 2D TCAD numerical device simulations of the direct tunneling gate leakage current partitioning ratios ($\frac{I_{gcs}}{I_{gc}}$ and $\frac{I_{\text{gcd}}}{I_{gc}}$) in the case of two layer gate insulator (HfO_2/SiO_2) with an interfacial layer (SiO_2) thickness equal to 0.2nm and HfO_2 as an oxide material with EOT=0.5nm and $V_g = 1V$ for a DG MOSFET structure as a function of drain voltage.

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There is a good agreement between the results from our analytical model and 2D TCAD numerical device simulations. Figure 5 and Figure 6 show the gate leakage current split equally between source and drain for drain voltage equal to 0 (V_d=0), while the ratio of the leakage current that goes to the source increase by drain voltage, and at the same time the ratio of the gate current goes to the drain decrease. In fact increasing the ratio of the source component exactly is compensated by decreasing the ratio of drain component in terms of drain voltage.

6) Conclusion

In this study we presented a model of the partitioning of the gate to channel tunneling leakage current into the source and drain components based on a recently developed, complete, surface potential-based compact MOSFET model and a compact analytical gate leakage current model for a nanoscale DG MOSFETs structure. The influence and impact of the thickness of the interfacial SiO_2 layer on the gate-drain and gate-source components has been shown. The model works well from the numerical simulation point of view (Silvaco Atlas). The proposed model provides additional insight into the gate leakage components and can be very useful to address the impact of the gate leakage current on DG MOSFET device and circuit performance.

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Chapter 5

Temperature Dependent Compact Modeling of Gate Tunneling Leakage Current in Double Gate MOSFETs

The temperature dependence of the gate leakage current has been developed for Double Gate (DG) MOSFETs. This model is compared with experimental data measured in Trigate MOSFETs at various temperatures with SiON as a dielectric material and SiO_2 as an interfacial layer. The gate leakage current measurements at different temperatures show two different transport mechanisms, direct tunneling (DT) gate leakage and Trap-Assisted-Tunneling (TAT) current. Our analysis based on leakage current measurements in the above threshold regime for different temperatures shows that the DT current is clearly dominant over the TAT, while the opposite happens below threshold. Our model is able to explain the gate tunneling current in terms of gate voltage for different temperatures. The results of the DT current in the strong inversion regime and TAT in the subthreshold regime show good agreement with temperature dependent measurements.

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1) Introduction

The scaling down of gate oxide thickness in advanced CMOS technology causes an increase of gate leakage current due to the increasing carrier tunneling between gate and channel [1, 2]. Understanding the gate current transport mechanisms is important in order to develop accurate design-oriented models.

The temperature dependence of the surface potential induces a decrease of the threshold voltage with increasing temperature. As a result, an increase of the carriers in the channel takes place with temperature. Besides, the barrier height between gate and channel decreases with temperature. Therefore, the gate leakage current increases at higher temperatures [3, 4]. It causes undesirable effects on the device performance [5, 6]; it increases power dissipation and deteriorates the circuit stability [7]. Temperature dependent measurements of the gate leakage current have been used to study and understanding carrier transport through different gate dielectric materials [8, 9].

The high-k dielectric materials are alternative gate oxide materials [10, 11] for the coming nanoscale CMOS generations in order to suppress the gate leakage current. Analytical expressions are presented to model the gate leakage current as a function of applied gate and drain voltages for DG MOSFETs [12]. The presence of electron trap levels in SiON can result in a significant leakage current at low electric field (subthreshold regime) in which electrons gain sufficient energy to tunnel through the oxide material [13]. In this chapter we present the incorporation of the temperature dependence for the DT and TAT in FinFETs (modeled as DG MOSFETs) assuming a two dielectric layer gate stack (being SiO_2 as an interfacial layer). Furthermore, for that purpose, we have extended the gate current models to the case of a two dielectric layer gate stack. The comparison between our model calculations demonstrates that the model can accurately reproduce the gate leakage current behavior through $SiON/SiO_2$ gate oxide for different temperatures.

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2) DG FinFET Structure and Temperature Effects

The DG FinFET structure under analysis and related potential profile showing DT and TAT mechanisms through SiON/SiO_2 as gate oxide materials are shown in Figure 1. The effect of temperature has been taken into account by considering its dependence on the thermal voltage, flat band voltage, carrier concentration, Fermi level and the Si-SiO_2 barrier height of the carriers [14, 15].

A) Thermal Voltage

The thermal voltage ($\phi_t = \frac{KT}{q}$) at room temperature is equal to 0.026 (V) where q is the electronic charge, T is temperature in Kelvin and K is Boltzmann constant. Higher thermal energy gives electrons more energy for jumping from the valence into the conduction band. Thus, the number of carriers of an intrinsic semiconductor increases with temperature which is taken into account by thermal voltage.

B) Carrier Concentration and Fermi Level

The electron concentration and the Fermi potential in the case of an n-type semiconductor are calculated:

$$n = n_i \times e^{\frac{-q\times\phi_F}{KT}} \qquad (1)$$

The Fermi potential becomes:

$$\phi_F = \frac{-KT}{q} \times Ln\left(\frac{n}{n_i}\right) = \frac{-KT}{q} \times Ln\left(\frac{N_a}{n_i}\right) \qquad (2)$$

where n_i is the intrinsic carriers (electrons) concentration at T and is a function of temperature and N_a is the acceptor atoms concentration. Hence the Fermi potential is calculated using (2) and will be shifted with the temperature.

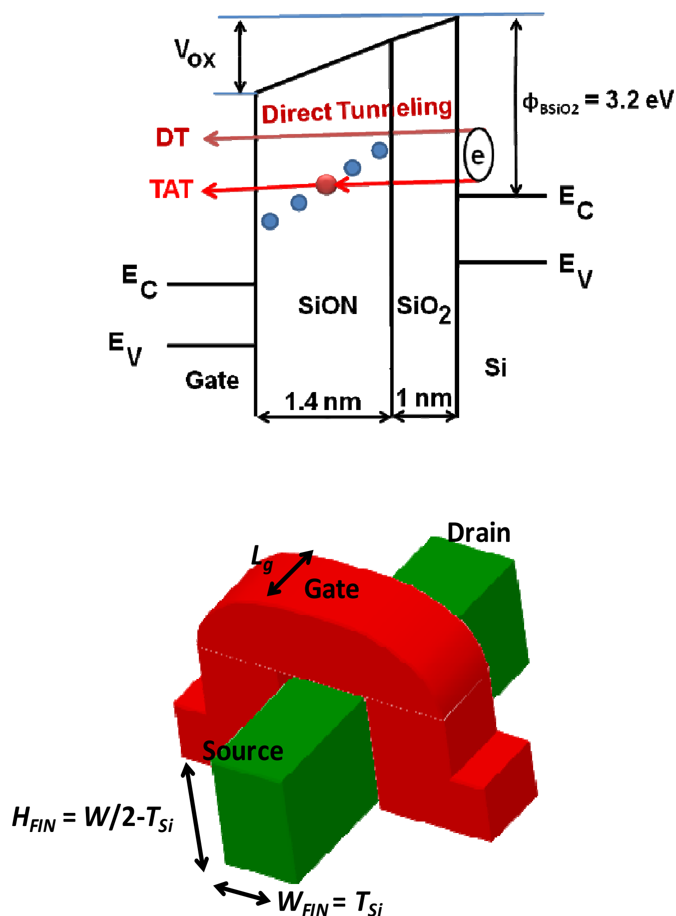

Figure 1: Schematic representation of the potential profile (showing direct tunneling and TAT mechanisms through $SiON/SiO_2$ as gate oxide materials) and a DG FinFET structure under analysis.

C) Flat Band Voltage Calculation

The flat band voltage (V_{FB}) is determined by the work function difference between gate and semiconductor and charge at the oxide-semiconductor interface which is represented in the model by an effective charge ($Q_0 = q \times N_{ss}$) where N_{ss} is the interface states. The dependence of the flat band voltage on the temperature comes mostly from the work function difference between gate and semiconductor.

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The flat band voltage considering the effects of the effective charge and work function difference between gate and semiconductor as a function of temperature becomes:

$$V_{FB}(N_a,T,EOT)=\phi_{MS}(N_a,T)-\frac{Q_0}{C_{OX}(EOT)} \tag{3}$$

where $\phi_{MS}(N_a,T)$ is the work function difference between gate and Si, *E*quivalent *O*xide *T*hickness is EOT and C_{OX} is the oxide capacitance.

D) Dielectric-Semiconductor Barrier Height

We extracted the Si-SiO_2 barrier height to the carrier (ϕ_{BSiO2}) at different temperatures. We observed that it shows a linear decrease of ϕ_{BSiO2} with temperature. As a result, an expression of the ϕ_{BSiO2} accounting for the observed linear dependence with temperature can be incorporated into our temperature dependent model.

3) Direct Tunneling Gate Leakage Current

We developed a temperature dependent analytical model of the direct tunneling gate leakage current based on a proper WKB approximation for DG MOSFETs, using our previous compact model for the potential and drain current [16, 17]. It was demonstrated that this model can also be applied to sufficiently narrow FinFETs. We derived the following gate tunneling leakage current expression [11, 12] for two dielectric layer gate stacks (in our case, $SiON/SiO_2$):

$$J_{GDT}=\frac{F_A}{k_{SiO2}\times\varepsilon_0}\times\left(\frac{V_g-V_{fbp}(N_a,T,EOT)-\frac{1}{2}\times V_{def}}{T_{SiO2}}\times Q_{gm}\right)\times$$
$$\exp\left\{-\left[\frac{8\pi}{3h}\times10^{-2}\times\frac{k_{SiO2}\times T_{SiON}+k_{SiON}\times T_{SiO2}}{k_{SiON}\times V_{im}}\times\sqrt{2\times m_{SiO2}\times q}\right]\times\left[\left(\frac{\phi_{BSiO2}}{q}\right)^{\frac{3}{2}}-\left(\frac{\phi_{BSiO2}-Fraction\times q\times V_{im}}{q}\right)^{\frac{3}{2}}\right]\right\}\times$$
$$\exp\left\{-\left[\frac{8\pi}{3h}\times10^{-2}\times\frac{k_{SiO2}\times T_{SiON}+k_{SiON}\times T_{SiO2}}{k_{SiO2}\times V_{im}}\times\sqrt{2\times m_{SiON}\times q}\right]\times\left[\left(\frac{\phi_{BSiON}-Fraction\times q\times V_{im}}{q}\right)^{\frac{3}{2}}-\left(\frac{\phi_{BSiON}-q\times V_{im}}{q}\right)^{\frac{3}{2}}\right]\right\} \tag{4}$$

where k_{SiO2} is SiO_2 dielectric constant, the permittivity of vacuum is ε_0, V_g is the applied gate voltage, V_{fbp} is the flat band voltage corresponding to the channel region, V_{def} is effective drain voltage [16, 17], T_{SiO2} is the SiO_2 thickness, h is the Plank`s

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constant, T_{SiON} is the $SiON$ thickness, k_{SiON} is $SiON$ dielectric constant, m_{SiO2} is electron effective mass in SiO_2, *Fraction* is equal to $\frac{T_{SiO2}}{T_{SiON}}$, m_{SiON} is electron effective mass in $SiON$ and the barrier height to the carrier for $SiON$ is ϕ_{BSiON}. The V_{im} is the voltage through the oxide materials considered as:

$$V_{im} = \phi_t \times \left(\frac{q_s + q_d}{2} + \frac{q_b}{2} \right), \; F_A = \frac{q^3}{8\pi h\sqrt{2\times\phi_{BSiO2}}} \tag{5}$$

where q_s is the normalized charge concentration at the source and q_d is the normalized charge concentration at the drain and q_b is the total normalized depletion charge in the Si body film [17].

The Q_{gm} is the total charge in the channel [11]:

$$Q_{gm} = \frac{\left[\frac{q_s^3 - q_d^3}{3} + \left(q_s^2 - q_d^2\right) - q_b \times \left(q_s - q_d\right) + q_b^2 \times Ln\left(\frac{q_s + q_d}{q_d + q_b}\right) \right]}{\left[\frac{q_s^2 - q_d^2}{2} + 2\left(q_s - q_d\right) - q_b \times Ln\left(\frac{q_s + q_d}{q_d + q_b}\right) \right]} \tag{6}$$

The developed temperature dependent DT model is used to calculate and evaluate the DT gate leakage current at different temperatures when the gate voltage increases, and allows a better understanding of the carrier transport mechanism through $SiON/SiO_2$ with respect to the temperature. We will show that the DT current is dominant above threshold voltage for the considered range of temperatures.

4) Trap Assisted Tunneling Current

The TAT current through the gate oxide materials is caused by defects and disadvantages in the high-k dielectric materials [18, 20]. A temperature dependent analytical TAT current model through two layer potential barriers (as shown in Figure 1) has been modified and developed.

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We have developed the following expression for the TAT current corresponding to the source-channel overlap for a two dielectric layer gate stack. We use a similar procedure for the tunneling probability that was applied in [11] for the case of direct tunneling current through two oxide layers:

$$J_{GTATS} = \left(\frac{2 \times C_{Trap} \times N_{Trap} \times \phi_{Trap} \times q}{3 \times 10^{4} \times V_{IappGS} \times \left[(T_{SiO2} + T_{SiON}) \times 10^{-2} \right]^{-1}} \right) \times \exp\left\{ -\left[\frac{8\pi}{3h} \times 10^{-2} \times \frac{k_{SiO2} \times T_{SiON} + k_{SiON} \times T_{SiO2}}{k_{SiON} \times V_{IappGS}} \times \sqrt{2 \times m_{SiO2} \times q} \right] \times \left[\left(\frac{\phi_{BSiO2}}{q} \right)^{\frac{3}{2}} - \left(\frac{\phi_{BSiO2} - Fraction \times q \times V_{IappGS}}{q} \right)^{\frac{3}{2}} \right] \right\} \times \exp\left\{ \frac{F_B \times (\phi_{Trap})^{\frac{3}{2}}}{V_{IappGS} \times \left[(T_{SiO2} + T_{SiON}) \times 10^{-2} \right]^{-1}} \right\} \quad (7)$$

where ϕ_{Trap} is the trap energy, the trap states density is N_{Trap} and

$$C_{Trap} = \left(\frac{m_0}{m_{SiON}} \right)^{\frac{5}{2}} \times \left(\frac{16\pi \sqrt{\phi_e^3}}{3h \sqrt{\phi_{Trap} - \phi_e^3}} \right) \quad (8)$$

where m_0 is the free electron mass and ϕ_e is the total energy of electrons considered equal to 0.2 (eV). $V_{IappGS} = V_g - V_{FBn} - V_s$, $F_B = \frac{8\pi}{3h} \sqrt{2 \times q \times m_{SiON}}$ where V_{FBn} is the flat band voltage corresponding to the source and drain regions of overlap.

Similarly, the TAT current corresponding to the drain-channel overlap becomes:

$$J_{GTATD} = \left(\frac{2 \times C_{Trap} \times N_{Trap} \times \phi_{Trap} \times q}{3 \times 10^{4} \times V_{IappGD} \times \left[(T_{SiO2} + T_{SiON}) \times 10^{-2} \right]^{-1}} \right) \times \exp\left\{ -\left[\frac{8\pi}{3h} \times 10^{-2} \times \frac{k_{SiO2} \times T_{SiON} + k_{SiON} \times T_{SiO2}}{k_{SiON} \times V_{IappGD}} \times \sqrt{2 \times m_{SiO2} \times q} \right] \times \left[\left(\frac{\phi_{BSiO2}}{q} \right)^{\frac{3}{2}} - \left(\frac{\phi_{BSiO2} - Fraction \times q \times V_{IappGD}}{q} \right)^{\frac{3}{2}} \right] \right\} \times \exp\left\{ \frac{F_B \times (\phi_{Trap})^{\frac{3}{2}}}{V_{IappGD} \times \left[(T_{SiO2} + T_{SiON}) \times 10^{-2} \right]^{-1}} \right\} \quad (9)$$

where $V_{IappGD} = V_g - V_{FBn} - V_D$ and the total TAT overlap current (J_{GTAT}) is:

$$J_{GTAT} = J_{GTATS} + J_{GTATD} \quad (10)$$

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The tunneling probability of carriers is exponentially dependent on the barrier height that they have to cross through the dielectric layers. The presence of the trap inside the dielectric materials splits the energy barrier in two parts. An increasing temperature will also decrease the barrier height, whereas increasing exponentially the probability of the total tunneling current. Once the transition probabilities of the carriers are known, the trap-assisted tunneling current can be obtained. The model calculations at different temperatures give the precise gate leakage at low electric field.

5) Results and Discussion

The device structure under analysis and potential profile showing the DT and TAT mechanisms through two layer oxide materials ($SiON/SiO_2$) is shown in Figure 1. The DT gate leakage current calculations for different temperatures (using our model) in strong inversion as well as TAT in the subthreshold regime has been compared with experimental measurements. The temperature dependent $Si\text{-}SiO_2$ barrier height to the carrier (ϕ_{BSiO2}) was extracted and it resulted a linear decrease of ϕ_{BSiO2} with temperature. Therefore, an expression of the ϕ_{BSiO2} giving the observed linear dependence with temperature is incorporated into our model. The measurements have been performed on FinFET devices with an EOT equal to 1.9nm through $SiON/SiO_2$ as a gate oxide material for different bias and temperatures.

A) Direct Tunneling Gate Leakage Current

The model calculations (4) and experimental measurements of the DT current as a function of applied gate voltage for different temperatures are shown in Figure 2 with channel length (L_G) equal to 10 micrometer (u) at V_D=0.05(V) and V_D=1(V). As can be seen in Figure 2, the gate leakage current will increase with increasing temperature, which is attributed to the increase of carriers in the channel and the decrease of the barrier height. We have considered a linear decrease of the barrier height for the carriers through the gate oxide materials with temperature.

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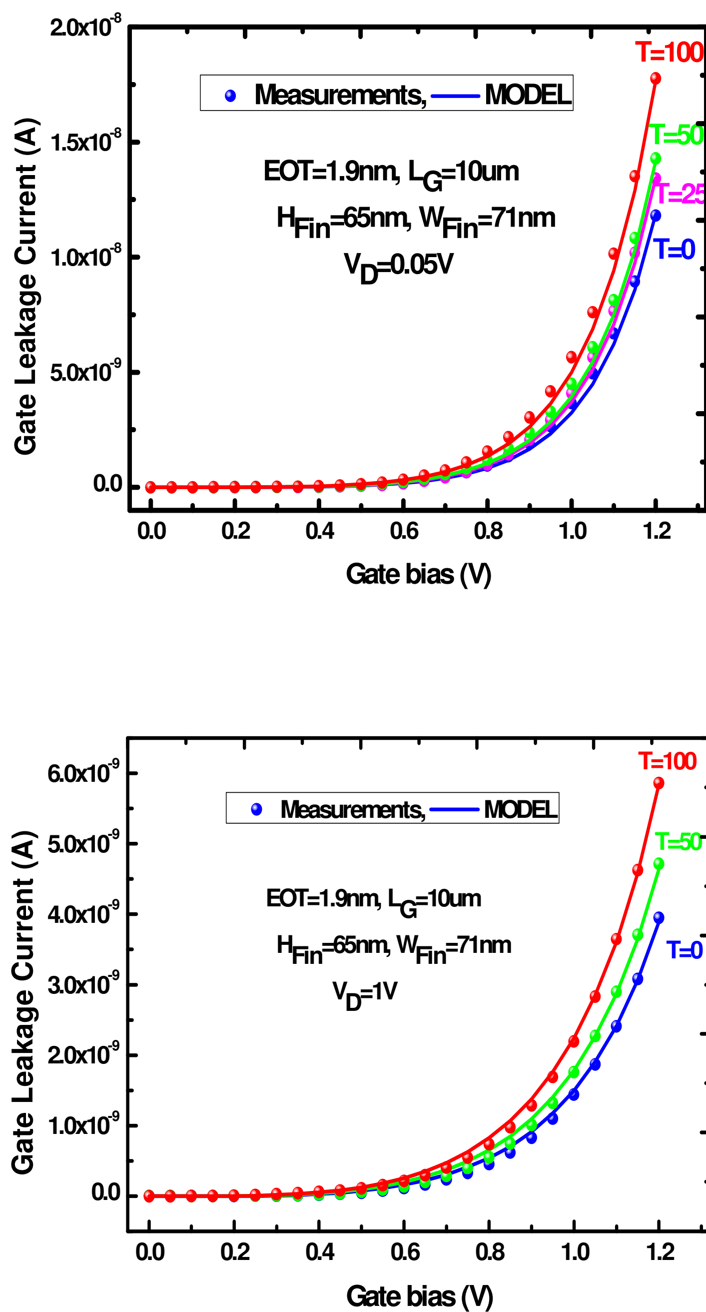

Figure 2: Model calculations and experimental measurements of the gate leakage current as a function of gate voltage for a DG FinFET with L_{Ch}=10u at V_D= 0.05 (V) and V_D= 1 (V) for different temperatures (T= 0, 25, 50, and 100 ºC).

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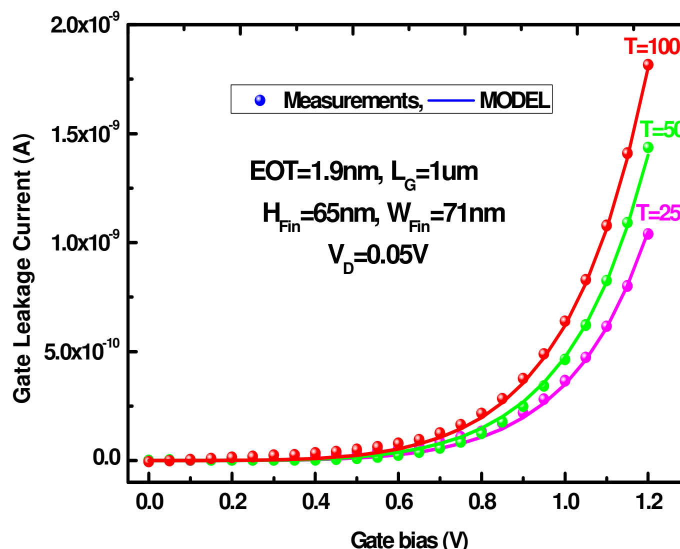

Figure 3: Model calculations and experimental measurements of the gate leakage current as a function of gate voltage for a DG FinFET with L_{Ch}=1u at V_D= 0.05 (V) for different temperatures.

In Figure 3 the model calculations and experimental measurements of the DT current as a function of the gate voltage with L_G=1 (u) are shown at V_D=0.05 (V) for different temperatures (T=25, 50, and 100 ºC). It is shown that our direct tunneling current model (4) with a temperature dependence of the surface potential accurately reproduces the experimentally observed temperature sensitivity of the direct tunneling current through $SiON/SiO_2$. Figure 4 to Figure 6 show comparisons between model calculations and measurements of the DT current in linear and log scales. The results indicate that the DT current (4) for different temperatures is dominant in the above threshold regime and it is negligible in the subthreshold regime. The temperature dependent DT model shows a very good agreement with experimental gate leakage current and it works well from the experimental point of view.

B) Trap Assisted Tunneling Current

The results show that the DT model for different temperatures works well in the strong inversion regime.

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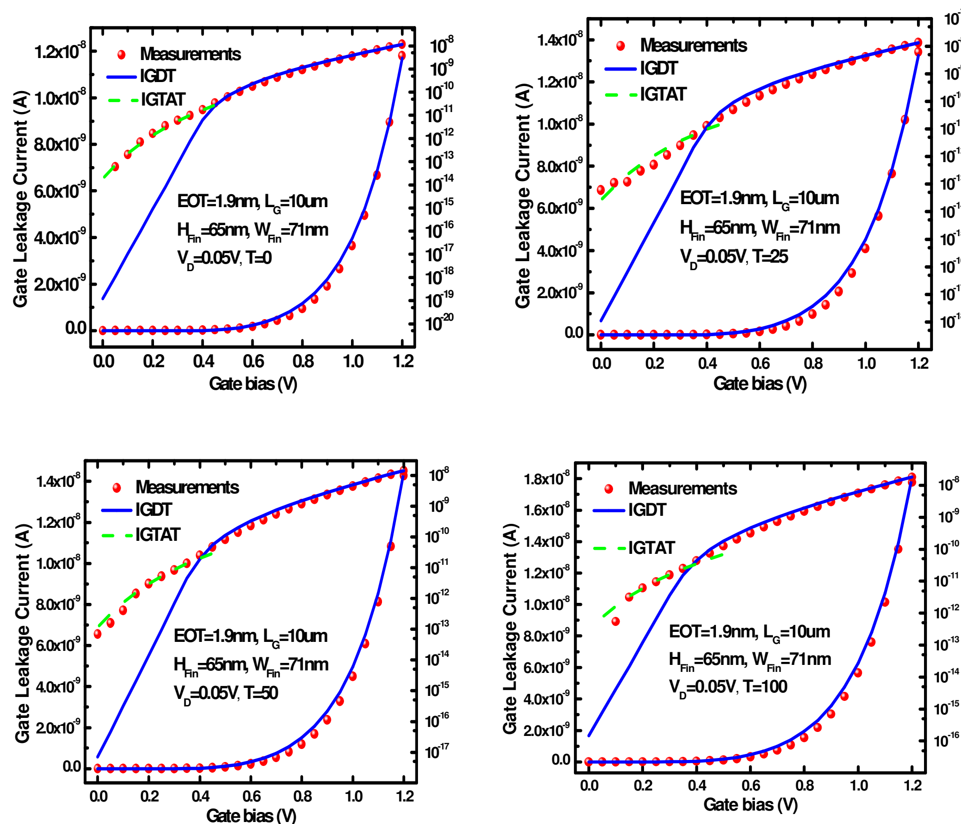

Figure 4: Model calculations and experimental measurements of the gate leakage current as a function of gate voltage for a DG FinFET with L_{Ch}=1u at V_D= 0.05 (V) for different temperatures.

The carriers do not have enough energy in order to tunnel directly from silicon body to the gate through oxide materials at below threshold voltage. The TAT calculations of our model (10) for different temperatures are compared with experimental measurements in the subthreshold regime (see Figure 4 to Figure 6) at low and high drain voltages. Comparison between model (10) calculations and experimental measurements at different temperatures shows that the TAT currents play major role at below threshold voltage and the DT current is negligible (see Figure 4 to Figure 6). Our analysis in the subthreshold regime at different temperatures shows that the TAT is dominant over the DT current and a good agreement in all cases is observed in the subthreshold regime.

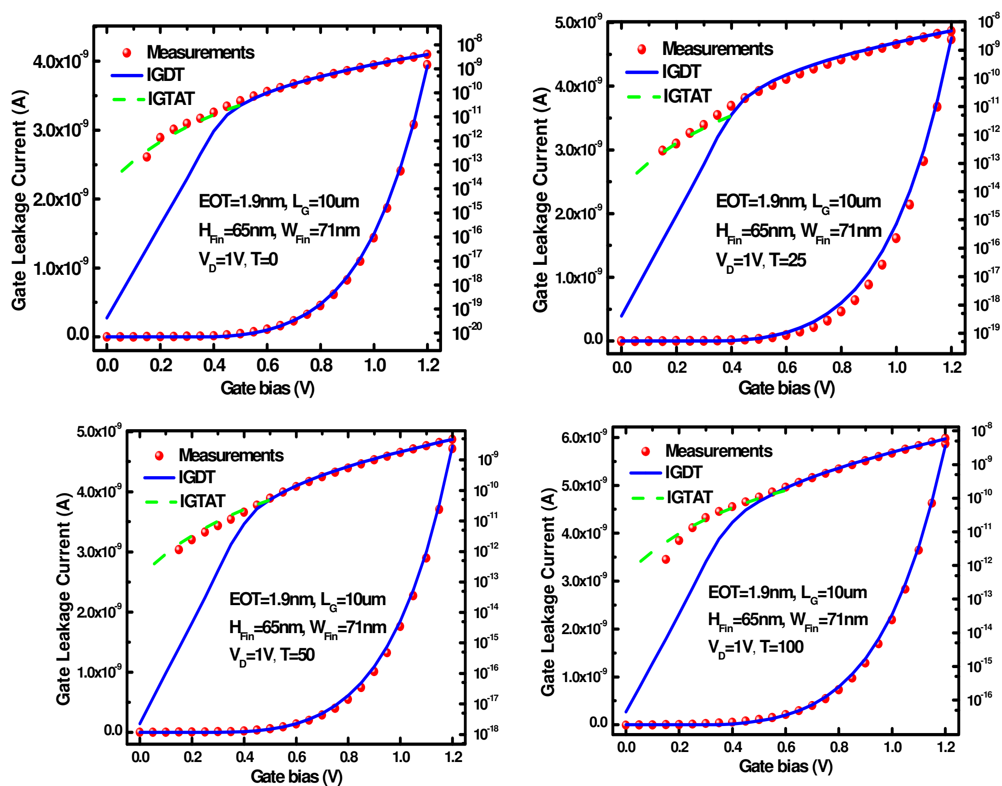

Figure 5: Gate leakage current including DT and TAT currents as a function of gate voltage for a DG FinFET with L_G=10u at V_D= 1 (V) in linear (Left) and logarithmic (right) scales at T=0, 25, 50, and 100 ºC.

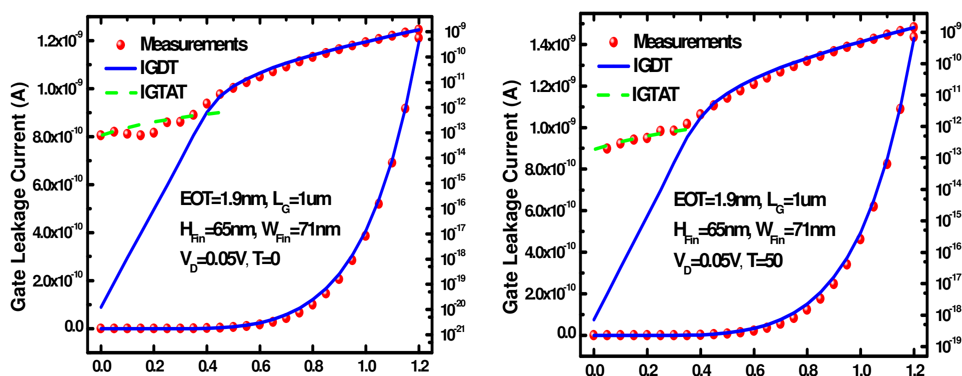

Figure 6: Gate leakage current including DT and TAT currents for a DG FinFET with L_G=1u at V_D= 0.05 (V) as a function of gate voltage in linear (Left) and logarithmic (right) scales at T=0 and 50 ºC.

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The results show that the temperature dependent of DT and TAT currents (4 and 10) have to be taken into account for a precise modeling of the total gate leakage current through the gate dielectric materials in both the strong inversion and the subthreshold regimes at different temperatures.

6) Conclusion

Temperature dependent analytical models of the DT current in inversion region and the TAT current in subthreshold regime have been developed for DG FinFET with a two dielectric layers gate stack such as $SiON/SiO_2$. The comparison between the model calculations and experimental measurements for different temperatures shows that the DT current is clearly dominant over TAT above threshold voltage, whereas it is negligible below threshold voltage and TAT becomes dominant. The temperature dependence of the gate current has been accurately modeled in both the strong inversion and the subthreshold regimes and shows good agreement with the experimental measurements.

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Chapter 6

Automatic Parameter Extraction Techniques in IC-CAP for Compact Double-Gate MOSFET Model

The goal of this work is to present development and implementation of automatic parameter extraction techniques for an explicit compact model (in Verilog-A code) which is developed based on a surface potential model. This explicit model includes short channel effects (SCEs), allows accurate simulations of the device characteristics, and has been adapted to FinFET and Trigate MOSFETs (modeled as DG MOSFETs). The parameter extraction relies on a commercial software package (IC-CAP) allowing automatic parameter extraction routines and providing an effective way to calculate the model parameters, minimizing discrepancies between measured and modeled data, for reliable circuit simulation. The results are compared with measured data for different devices and the related extracted parameters show good agreement with measured transistor characteristics under different conditions and through all operating regimes. The second derivative of the drain current with respect to the source-gate potential is also verified and results to be accurate and continuous though the different operating regimes.

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1) Introduction

The downscaling of CMOS technologies has generated the need for accurate MOSFET compact models as well as suitable parameter extraction methods, in order to be used by circuit designers. Compact device modeling bridges the communities between chip fabrication and integrated circuit (IC) design [1]. In fact, for the design of systems on a chip, realistic analog simulation models are necessary to simulate circuit performance with a sufficient degree of accuracy. In the process of device compact modeling, the strategy for parameter extraction is a necessary task. The accuracy of the circuit simulations not only depends on an accurate model (correct mathematical description), but also on the used parameter extraction techniques [2, 3]. Parameter extraction methods have been studied by several authors in different devices [4-7].

The goal of the parameter extraction techniques is to find a set of model parameters valid for a given technology. We presented an analytical compact model in double gate (DG) MOSFETs including short channel effects (channel length modulation, DIBL, carrier velocity saturation, threshold voltage roll-off and series resistance), verified by numerical simulations [8]. The main details of this model have been described in [9, 10]. The model has been implemented in Verilog-A. The Verilog-A language provides a source code of the compact model and is one of the best tools for compact modeling. It is actually compatible with the IC-CAP software of Agilent (a simulator running a Verilog-A). The Verilog-A also supports conservative and signal flow descriptions and the solution of analog behavior is obtained by applying Kirchhoff's and potential laws. In addition, some commercial circuit simulation programs allow the introduction of models described in this language [11, 12].

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In this chapter automatic parameter extraction techniques for our compact modeling are presented in order to extract the related model parameters. Our model is coded in Verilog-A [13], and could be linked through a Verilog-A capable simulator (IC-CAP program of Agilent) to the parameter extraction software in a very early stage of the model development. The measurements carried out in Trigate MOSFETs and also used in the automatic parameter extraction techniques for verification of simulated and measured data. The results of our model implemented in IC-CAP as a commercial circuit simulator for circuit design show good agreement with measurements.

2) Model and Structure

We have adapted our developed compact model for the potential, threshold voltage [9] and currents in short channel symmetric DG MOSFETs [10] to a new device (Trigate MOSFET) structure as we have shown in Fig. 1. The model core is physics-based (including SCEs) in order to accurately simulate the electrical behavior of DG MOSFETs.

A) Structure

The DG MOSFET structure under analysis and experimental data measured in Trigate MOSFETs are shown in Figure 1, where T_{Si} is silicon thickness and SiO_2 is an interfacial layer with thickness of 1 nm and SiON is a dielectric material with thickness equal to 1.4 nm. The measurements were carried out on Trigate MOSFET with an Equivalent Oxide Thickness (EOT) equal to 1.9nm and SiON/SiO_2 as a gate oxide material for different conditions.

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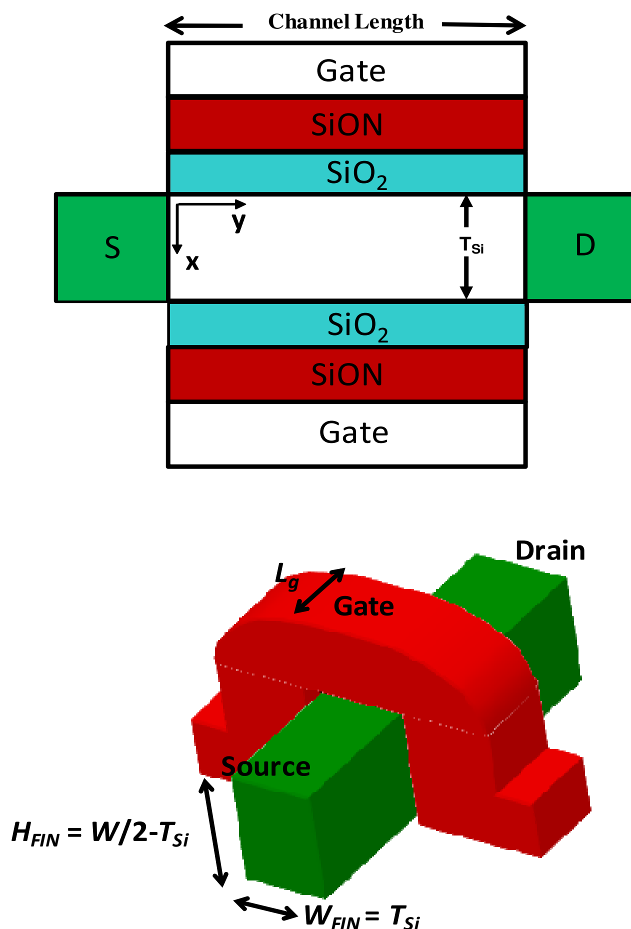

Figure 1: Schematic representation of (a) the Double Gate MOSFET structure modeled and (b) Trigate MOSFET used for the experimental measurements.

B) Electric Field

The electric field at the surface of the Si-SiO$_2$ (E_S) was calculated using Poisson's equation. The electric field as a function of the potential at the surface (ϕ_S) and at the centre of the Si film (ϕ_o) is obtained as [9, 10]:

$$E_S = \sqrt{\frac{2qN_a\phi_t}{\varepsilon_s}} \times \sqrt{(\frac{\phi_S - \phi_O}{\phi_t}) + (1 - e^{-(\frac{\phi_S - \phi_O}{\phi_t})}) \times e^{(\frac{\phi_S - 2\phi_F - V}{\phi_t})}} \qquad (1)$$

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where $V = \phi_{Fn} - \phi_{Fp}$ is the potential along the channel, N_a is the uniform acceptor concentration in the silicon layer, $\phi_t = KT'/q$ is the thermal potential, K is Boltzmann constant, q is the electronic charge, T' is temperature in Kelvin, ϕ_{Fp} is the quasi Fermi level for holes in the P-type silicon layer, and ϕ_{Fn} is the quasi Fermi level for electrons. Fig. 2 shows the verification and validation of the obtained electric field (1) into the dielectric materials (SiO_2 as an interfacial layer and SiON as a dielectric material). The model calculations are in a good agreement with those obtained from ATLAS (Silvaco) numerical simulations.

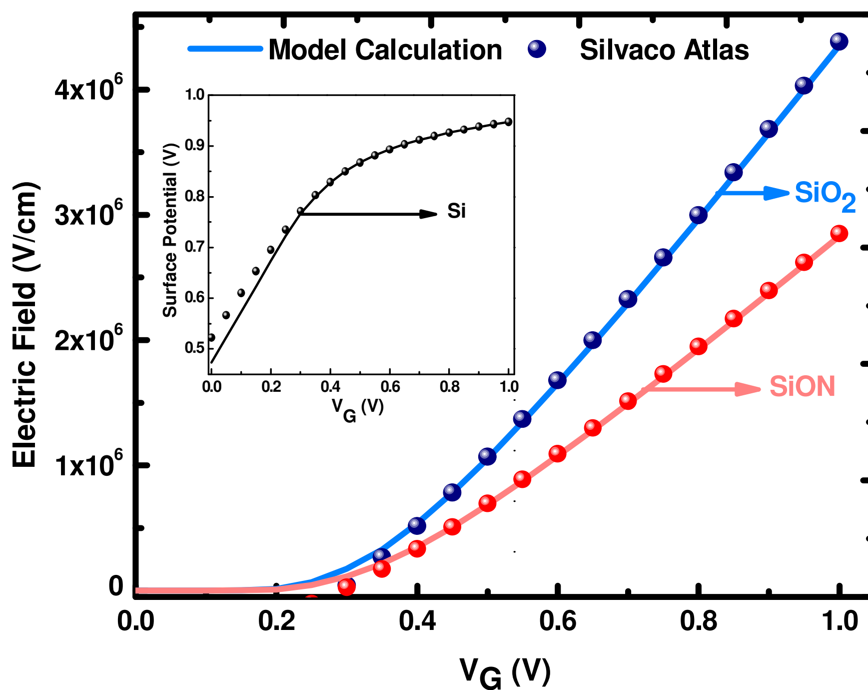

Figure 2: Model calculation (lines) and Silvaco Atlas numerical simulation (symbols) of the surface potential of the channel (Inset), and the surface electric field into the dielectric materials as a function of gate bias at V_D=0.

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C) Surface Potential of the Si Layer

Using the principal branch of Lambert function, the surface potential of the Si layer corresponding to the below threshold condition [9]:

$$\phi s_{BT} = V_G - V_{FB} - \phi_t \times LambW\left(\frac{q_b}{4} \times \exp\left(\frac{V_G - V_{FB} - 2\phi_F - \phi_t \times \frac{q_b}{2}}{\phi_t}\right)\right) \quad (2)$$

The surface potential of the Si layer corresponding to the above threshold condition [9]:

$$\phi s_{AT} = V_G - V_{FB} - 2\phi_t \times LambW\left(\frac{1}{2} \times \sqrt{\frac{q_b}{2} \times \frac{1}{\gamma}} \times \sqrt{1 - \exp(-\alpha)}\exp\left(\frac{V_G - V_{FB} - 2\phi_F - V}{2\phi_t}\right)\right) \quad (3)$$

Merging the solutions for the surface potential in the below and above threshold regimes the surface potential in all regions becomes:

$$\phi s = \phi s_{BT} \times \frac{1}{2} \times \{1 - \tanh[20 \times (V_G - V_T)]\} + \phi s_{AT} \times \frac{1}{2} \times \{1 + \tanh[20 \times (V_G - V_T)]\} \quad (4)$$

where V_G is applied gate bias, V_{FB} is flat band voltage, q_b is normalized total fixed charge in the silicon layer and normalized potential difference is α. The surface potential at the Si-SiO_2 interface calculated using the model (4) are in good agreement with that obtained from ATLAS numerical device simulations as we have shown in inset of Figure 2.

D) Current Model

The total drain current considering both surfaces (gate) is obtained from:

$$I_{DS} = 2 \times \frac{W}{L} \times \mu \times C_{ox} \times \phi_t \times \int_{V_S}^{V_D} q_n(V)\, dV \quad (5)$$

where W is the channel width, L is the channel length, V_S and V_D are the channel potential at the source and drain respectively, μ is the electron mobility.

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In the case of long channel device with constant mobility and neglecting SCEs and calculation of the integral gives [10]:

$$I_{DS}=\left(2\times\frac{W}{L}\times\mu_0\times C_{ox}\times\phi_t^2\right)\times\left[\frac{q_{ns}^2-q_{nd}^2}{2}+2\times\left(q_{ns}-q_{nd}\right)-q_b\times\ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right] \quad (6)$$

where C_{ox} is the gate capacitance per unit area, μ_0 is the maximum constant mobility, q_{ns} is the normalized mobile charge at source as function of V_G at V_D=0V, the normalized mobile charge at drain as a function of V_G is q_{nd} and V_{Deff} is the effective voltage [10].

In the case of short channel device, SCEs become important and they should be considered in order to accurately model the device behavior. In our model the SCEs included are velocity saturation, DIBL, V_T roll-off, channel length shortening and series resistance. The total drain current expression including SCEs in order to calculate drain current and extract the model parameters becomes [10]:

$$I_D=\frac{\left(2\times\frac{W}{L}\times\mu_0\times C_{ox}\times\phi_t^2\right)\times\left[\frac{q_{ns}^2-q_{nd}^2}{2}+2\times\left(q_{ns}-q_{nd}\right)-q_b\times\ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right]}{\left(1-\frac{\Delta L}{L}\right)\times\left\{\left[1+\left(\frac{E_{MS}}{E_1}\right)^{P_1}+\left(\frac{E_{MS}}{E_2}\right)^{P_2}\right]\times\sqrt{1+\left(\frac{\mu_s\times V_{Def}}{V_{Sat}\times L}\right)^2}+2\times\frac{W}{L}\times\mu_0\times C_{ox}\times R\times\left|V_{GT}-\beta\times V_{Def}\right|\right\}} \quad (7)$$

where ΔL is the channel shortening, E_{MS} is the average electric field, V_{Sat}, E_1, E_2, P_1 and P_2 are adjusting parameters, μ_s is surface mobility, R is series resistance and V_{GT} is V_G - V_T. The description of the drain current expression as well as SCEs in details can be found in detail in [10].

In order to calculate the drain current using our model (7) there is a need to know the model related parameters. The technological parameters of the model are L and W, silicon layer thickness (T_{Si}), doping concentration (N_a), EOT and metal work function which are obtained from the laboratory or factory which produces the transistors. Model parameters are extracted from the measured current voltage characteristics: transfer characteristic, output characteristic, the first and second order derivatives of the drain current with respect to the gate voltage as a function of gate bias.

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3) Model Implementation and Automatic Parameter Extraction Techniques

Our model is coded in Verilog-A language in order to implement and use automatic parameter extraction techniques compatible with IC-CAP. It can be used directly in circuit simulators as well as in parameter extraction software, which provides methods for handling measured data. The sub-circuit modeling environment, the multiple plot function and the piped simulation mode is making the quick setup of tests and measurements followed by automatic parameter extraction routines and easy use for the new devices when the models have many parameters and parameters have a complex dependence on fields and voltages.

In order to have a best optimization with the highest accuracy, we have prioritized the model parameters into the several groups and the extraction procedure begins from the most important parameters and continues to fix other parameters (less important ones). At the beginning, parameter extraction will use the initial values (best guess) as a default value of the parameters, and then the optimization steps will be used in order to fit simulation to measurements. The improvement of the fitting quality will be achieved using the optimization steps. Parameter extractions are organized in an extraction flow and the extraction steps can be selected from available functions in order to apply direct extractions, optimizers and manual tuners.

4) Results and Discussion

The accuracy of the simulations as using our compact model with the extracted parameters is verified by comparison with measurements.

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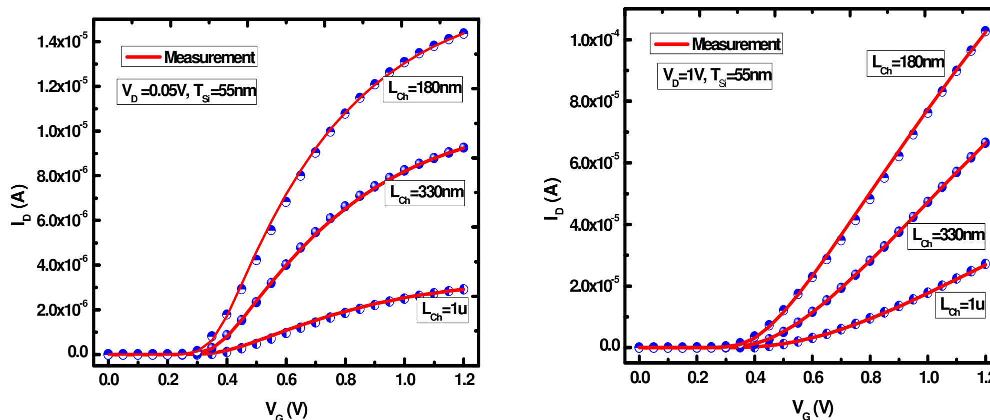

Figure 3: Comparison between simulated drain current as a function of gate bias characteristics after optimization (using the values of extracted parameters) and measurements at V_D=0.05 and V_D=1V.

We use the measured transistor characteristics of the Trigate MOSFETs for three different channel lengths (1000nm, 330nm and 180nm) and two different Si thicknesses (W_{Fin}=55nm and W_{Fin} =71nm).

The transfer characteristics were obtained for gate voltage varying from 0 V to 1.2 V, while the drain voltage was fixed at 0.05 V and 1 V for the linear and saturation regimes respectively. The output characteristics were obtained for different V_{GS} values in order to verify the abilities of the model and results of transistor simulation.

The surface potential of the channel and surface electric field into the dielectric materials as a function of gate bias are shown in Figure 2, using our model and numerical simulation (Silvaco ATLAS) at V_D=0. Comparison between our model (7) calculations and measured data of the drain current for different channel lengths (Figure 3) and Si thicknesses (Figure 4) are shown at V_D=0.05 and V_D=1V.

The transconductance (g_m) at a particular bias point is the slope of the tangent of the transfer characteristic curve at that point. We plotted the first derivative of the drain current with respect to the gate voltage (transconductance) as a function of gate bias at V_D=0.05 and V_D=1V for different channel lengths (Figure 5) and Si thickness (Figure 6).

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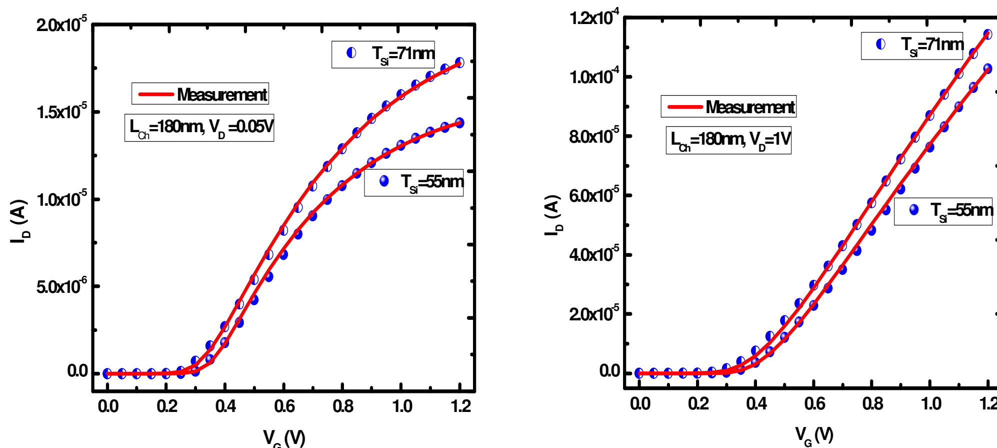

Figure 4: Comparison between simulated I_D-V_G characteristics (symbols) and measurements (lines) for our model with extracted parameters at V_D=0.05 and V_D=1V for different Si thickness.

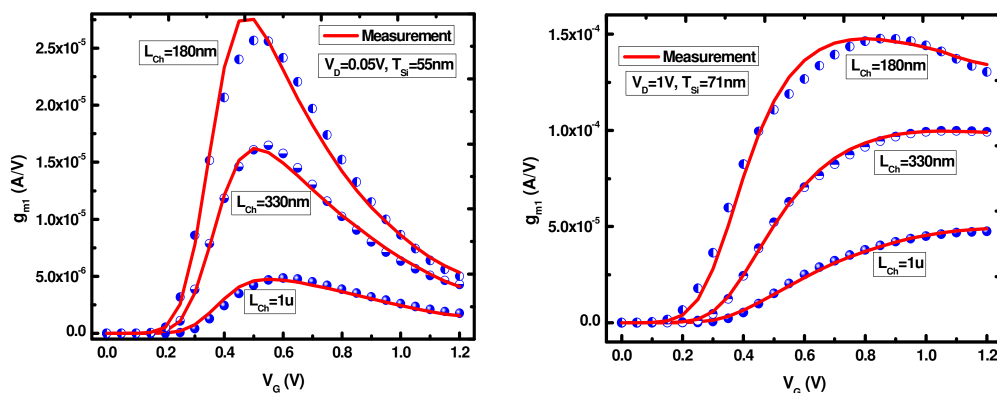

Figure 5: Modeled and experimental first derivative of I/V (transconductance) for different channel lengths at V_D=0.05 and V_D=1 V.

The second order derivatives of the drain current with respect to the gate voltage (g_{m2}) are analyzed as a function of gate bias for different channel lengths (Figure 7) and Si thicknesses (Figure 8) at V_D=0.05 and V_D=1V. Continuity of the second derivative of the drain current is obtained as shown in Figure 7 and Figure 8. A lack of continuity of the second derivative could originate convergence problems of the model when used in circuit simulation.

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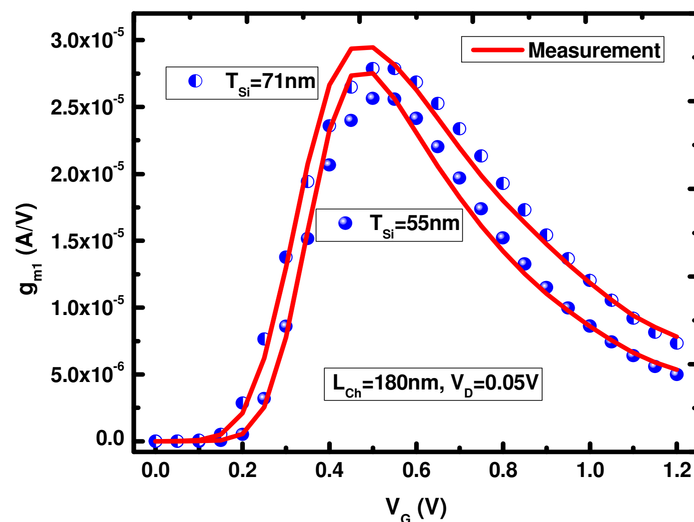

Figure 6: A Comparison of modeled and measured of transconductance for two different Si thicknesses at V_D=0.05 V.

Table I: The model extracted parameters according to the automatic parameter extraction techniques

L_{Ch}	1u	1u	330nm	330nm	180nm	180nm
$T_{Si}= W_{Fin}$	55nm	71nm	55nm	71nm	55nm	71nm
MWF	4.715	4.68	4.69	4.69	4.65	4.63
MM_0	2k	2k	2k	2k	2k	2k
E_1	370k	380k	630k	630k	320k	650k
E_2	1.7MEG	730k	1MEG	1.02MEG	970k	1.01MEG
$E_{2\upsilon}$	0.001	0.001	0.5	0.5	0.8	0.5
FDVT0	1	5	0.3	0.3	5	5
λ	1	1	0.5	0.5	1	1
δ	1	1	0.2	0.1	1	1
V_{Sat}	2.3MEG	2.08MEG	4.75MEG	4.9MEG	7MEG	7 MEG
θ	1.5	1.5	1.5	1.5	1.4	1.4

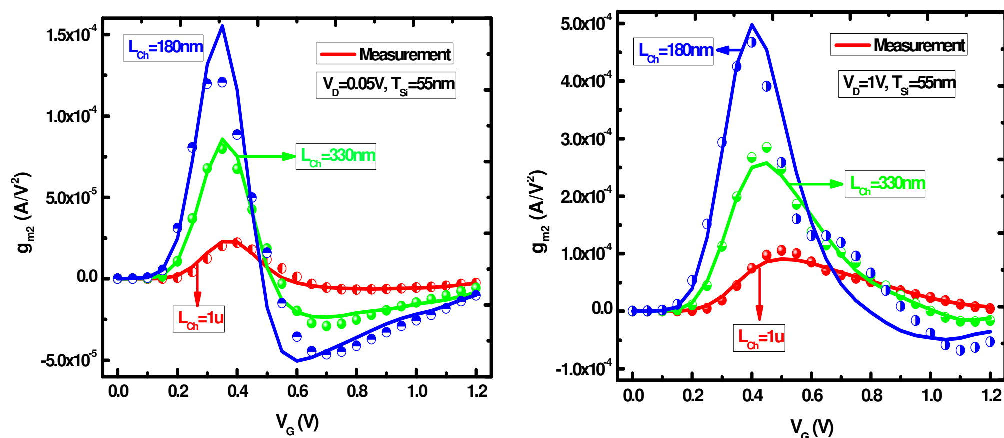

Figure 7: Model and experimental second derivative of I/V as a function of gate bias for different channel lengths at V_D=0.05 and V_D=1 V.

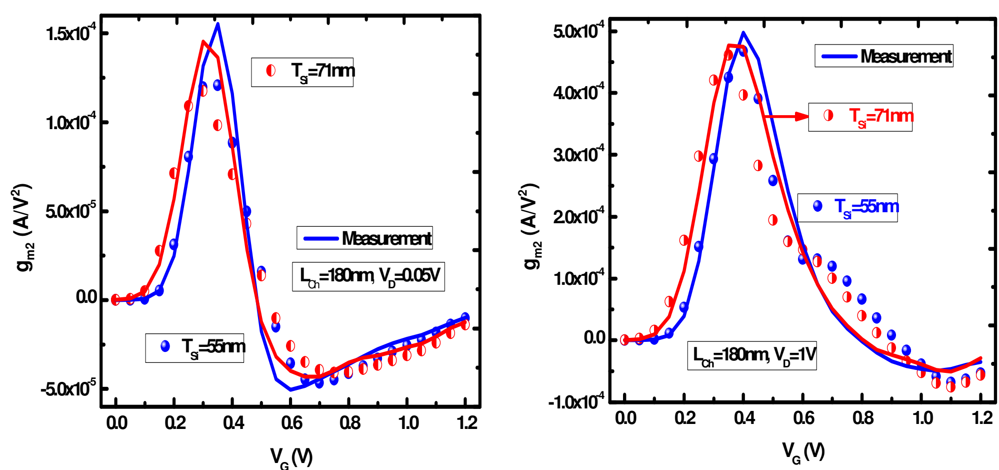

Figure 8: A comparison of modeled and experimental second derivative of I/V as a function of gate bias for two different Si thicknesses at V_D=0.05 and V_D=1V.

The observed continuity obtained from our model will contribute to avoid convergence problems. Table I summarizes the entire number of the model corresponding extracted parameters according to the automatic parameter extraction techniques.

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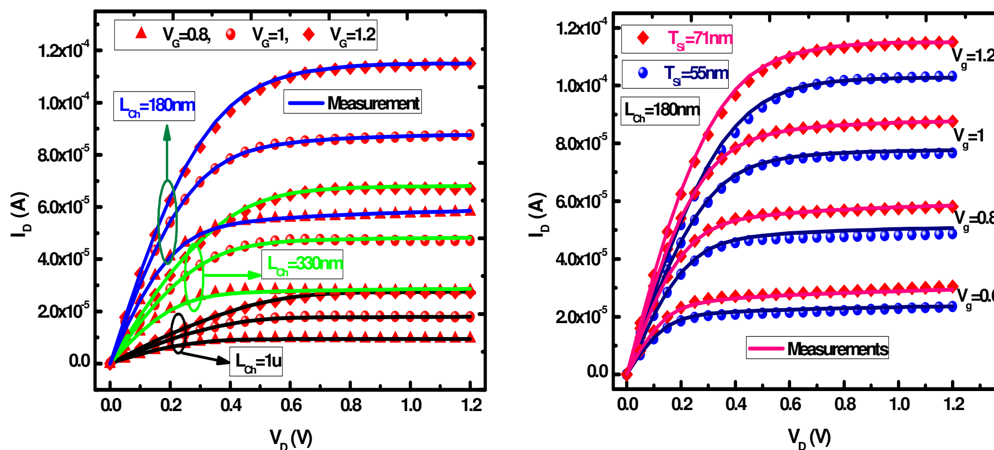

Figure 9: Comparison between simulated drain current as a function of drain bias (using the values of extracted parameters) and measurements at (a) different channel lengths and (b) different Si thickness.

Figure 9 shows the model fitting to the output characteristics for different channel lengths, Si thicknesses and different gate bias. Parameters E_1, E_2, P_1 and P_2 are functions of the channel length and V_{Deff}. The P_1 and P_2 dependencies on channel length in Trigate MOSFETs based on the extracted parameters (Table I) and experimental data measured in Trigate MOSFETs become:

$$P_1 = 0.85 - \frac{0.05}{L(\mu)} \text{ and } P_2 = 1.5 - \frac{0.05}{L(\mu)}.V_{Deff}\,. \qquad (8)$$

The extraction program has been tested on several n channel transistors of varying geometric dimensions. A good agreement between simulations with the extracted model parameters and measurements is achieved. It is evident that high accuracy of the extracted parameters is essential in order to describe the Trigate MOSFET device performance precisely using our model calculations. The model successfully described the measured drain currents, their first and second derivatives for different device geometry.

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5) Conclusion

We have developed automatic parameter extraction techniques for our explicit compact model in DG MOSFET suitable for design and circuits simulation, based on a surface potential model including short channel effects (channel length modulation, DIBL, carrier velocity saturation, threshold voltage roll-off and series resistance). The P_1 and P_2 parameters dependencies on the channel length are investigated and shown for Trigate MOSFETs based on measured data and extracted parameters. The continuity of the second derivative of the drain current with respect to the gate bias is verified and evaluated by plotting the derivatives at different conditions. The simulated I-V characteristics in linear and saturation regions and the first and second derivatives of the drain current using the extracted parameters show good agreement in all operating regions when compared to available measured data for Trigate MOSFETs with different geometry size.

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Chapter 7

Automatic Parameter Extraction Techniques and Parameters Correlations of Gate Leakage Current Model in Double-Gate MOSFETs, with IC-CAP

Direct Tunneling (DT) and Trap Assisted Tunneling (TAT) gate leakage current parameters have been extracted and verified considering automatic parameter extraction approaches. The commercial package IC-CAP is used to simulate our leakage current model coded in Verilog-A, and comparing with the measurements in order to obtain model parameter values and study parameters correlations. The model and parameter extraction techniques have been used to study the impact of parameters in the gate leakage current based on our developed compact analytical model and experimental data. It is shown that the gate leakage current depends on interfacial barrier height more strongly than barrier height of the dielectric layer. There is almost same scenario with respect to the carrier effective masses into the interfacial layer and dielectric layer. The comparison of the simulated results shows good agreement with available gate leakage current measured transistor characteristic in Trigate MOSFET.

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1) Introduction

With the downscaling of CMOS technologies, many MOSFET models have been developed in order to accurately describe gate leakage current and new physical phenomena in the device behavior [1-3]. Accurate model expressions are necessary to achieve the correct physical and real device/circuit behavior. Additionally, high precise parameter extraction is another important aspect of device and circuit simulation to ensure that the extracted parameters are an accurate reflection of the effects and performances [4-7]. Automatic parameter extraction techniques are an alternative to optimize the model parameters for the determination of model parameter values in comparison with measured data [8].

The commercial parameter extraction package (IC-CAP) is used to apply automatic parameter extraction techniques and simulating our gate leakage current models which is coded in Verilog-A. IC-CAP provides extraction routines for industry standard and supports the use of models in Verilog-A and wide range of customer requirements. IC-CAP uses different optimization algorithms and combination of those algorithms can be a main advantage of parameter extraction [9, 10]. Parameter extractions are organized in an extraction flow and extraction steps can be selected from available functions in order to apply direct extraction, optimizers and manual tuners.

In this work we have applied compact analytical gate leakage current models in the DT regime and TAT regime for the prediction of gate leakage current. We have developed and implemented automatic parameter extraction strategies for DT and TAT current models in the available parameter extraction system (IC-CAP). These techniques have been applied to the gate leakage current measurements in Trigate MOSFET and have given successfully results. We have shown parameters correlations based on our developed gate leakage current models, automatic parameter extraction techniques and measured gate leakage current data in Trigate MOSFET.

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The analyzed correlations of parameters provide knowledge of the sensitivity of the model parameters and an insight into the gate leakage current model available for circuit simulation. Comparison between simulated leakage current (using related extracted model parameters) show good agreement with the gate leakage current measurements in Trigate MOSFET with different geometries.

2) Device Structure and Gate Leakage Current Models

Figure 1 shows structure of the device under analysis which it is modeled as DG MOSFETs, as well as Trigate MOSFET structure which the gate leakage current measurements carried out. The DT and TAT current mechanisms have been developed and implemented in Verilog-A code for accurate simulation of the gate leakage current through two layer gate oxide materials (SiON/SiO_2 stack). The gate leakage current is calculated based on the proper tunneling probabilities through two layers gate oxide material such as SiON/SiO_2 with EOT=1.9nm. To achieve good performance we need to have accurate models and find techniques to extract model parameter values with high accuracy. The extraction techniques are based on the measurements and our developed model equations (4, 10) to ensure that a good representation of the device characteristics will be achieved.

A) Structure

The gate leakage current measurements carried out on Trigate MOSFET (Fig 1b) with T_{SiO2}=1nm, T_{SiON}=1.4nm (EOT=1.9nm), channel length equal to 1µm and 10 µm, H_{Fin}=65nm and W_{Fin}=55nm through SiON/SiO_2 gate oxide materials in terms of gate bias. The TAT current is dominant in subthreshold regime while above threshold voltage the DT is dominant and TAT is negligible [11].

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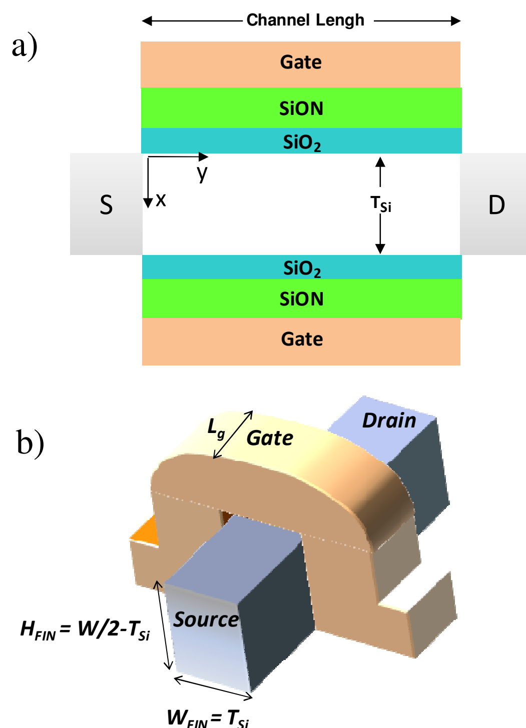

Figure 1: Structure of the device under analysis which it is modeled (a) as DG MOSFETs, (b) Trigate MOSFET structure which the gate leakage current measurements carried out.

B) Direct Tunneling Current

The direct tunneling current through SiON/SiO_2 is used to fit the gate leakage current measurements above threshold voltage in order to extract model parameters and study parameters correlations. The tunneling probability through SiO_2 (P_{SiO_2}) as an interfacial layer becomes [11]:

$$P_{SiO_2} = e^{-\left[\frac{8\pi}{3h}\times\frac{k_{SiO2}\times T_{SiON}+k_{SiON}\times T_{SiO2}}{k_{SiON}\times V_{im}}\times\sqrt{2\times m_{SiO2}\times q}\right]\times\left[\left(\frac{\phi_{BSiO2}}{q}\right)^{\frac{3}{2}}-\left(\frac{\phi_{BSiO2}-\frac{T_{SiO2}}{T_{SiON}}\times q\times V_{im}}{q}\right)^{\frac{3}{2}}\right]} \quad (1)$$

where h is the Plank`s constant, k_{SiO2} is SiO_2 dielectric constant, T_{SiON} is the $SiON$ thickness, k_{SiON} is $SiON$ dielectric constant, T_{SiO2} is the SiO_2 thickness, m_{SiO2} is electron

effective mass in SiO_2, q is the electronic charge and ϕ_{BSiO2} is the barrier height to the carrier for SiO_2. The V_{im} is the voltage through the oxide materials considered as:

$$V_{im} = \phi_t \times \left(\frac{q_s + q_d}{2} + \frac{q_b}{2} \right) \qquad (2)$$

The tunneling probability through SiON (T_{SiON}) becomes:

$$P_{SiON} = e^{-\left[\frac{8\pi}{3h} \times \frac{k_{SiO2} \times T_{SiON} + k_{SiON} \times T_{SiO2}}{k_{SiO2} \times V_{im}} \times \sqrt{2 \times m_{SiON} \times q}\right] \times \left[\left(\frac{\phi_{BSiON} - \frac{T_{SiO2}}{T_{SiON}} \times q \times V_{im}}{q}\right)^{\frac{3}{2}} - \left(\frac{\phi_{BSiON} - q \times V_{im}}{q}\right)^{\frac{3}{2}}\right]} \qquad (3)$$

where m_{SiON} is electron effective mass in $SiON$ and ϕ_{BSiON} is the barrier height to the carrier for $SiON$. Once the tunneling probabilities of the carriers through gate oxide materials are known, the DT current become:

$$J_{GDT} = \frac{q^3}{8\pi h \sqrt{2 \times \phi_{BSiO2}}} \times \frac{1}{k_{SiO2} \times \varepsilon_0} \times \left(\frac{V_g - V_{fbp} - \frac{1}{2} \times V_{def}}{T_{SiO2}} \times Q_{gm} \right) \times P_{SiO_2} \times P_{SiON} \qquad (4)$$

where ε_0 is the permittivity of vacuum, V_g is the applied gate voltage, V_{fbp} is the flat band voltage corresponding to the channel region, V_{def} is effective drain voltage [12, 13]. The Q_{gm} is the total charge in the channel [14]:

$$Q_{gm} = \frac{\left[\frac{q_s^3 - q_d^3}{3} + \left(q_s^2 - q_d^2 \right) - q_b \times \left(q_s - q_d \right) + q_b^2 \times Ln\left(\frac{q_s + q_d}{q_d + q_b} \right) \right]}{\left[\frac{q_s^2 - q_d^2}{2} + 2\left(q_s - q_d \right) - q_b \times Ln\left(\frac{q_s + q_d}{q_d + q_b} \right) \right]} \qquad (5)$$

where q_s is the normalized charge concentration at source and q_d is the normalized charge concentration at drain and q_b is the total normalized depletion charge in the Si body film. Comparison of the model calculation with experimental measurements shows DT is negligible in subthreshold regime. The model links process technology and circuit design and maintain balance between accuracy and simplicity.

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C) Trap Assisted Tunneling Current

The TAT current is becoming important and dominated in subthreshold regime where the DT is negligible. The proper tunneling probabilities through SiO_2 corresponding to the Source/Drain side`s cannel overlap ($PTAT_{SiO_2S/D}$) become:

$$PTAT_{SiO_2S/D} = e^{-\left[\frac{8\pi}{3h}\times\frac{k_{SiO2}\times T_{SiON}+k_{SiON}\times T_{SiO2}}{k_{SiON}\times V_{IappGS/GD}}\times\sqrt{2\times m_{SiO2}\times q}\right]\times\left[\left(\frac{\phi_{BSiO2}}{q}\right)^{\frac{3}{2}}-\left(\frac{\phi_{BSiO2}-\frac{T_{SiO2}}{T_{SiON}}\times q\times V_{IappGS/GD}}{q}\right)^{\frac{3}{2}}\right]} \quad (6)$$

where $V_{IappGS/GD} = V_g - V_{FBn} - V_{S/D}$. The proper tunneling probabilities through SiON corresponding to the Source/Drain side`s cannel overlap ($PTAT_{SiONS/D}$) become:

$$PTAT_{SiONS/D} = e^{\left(\frac{\frac{8\pi}{3h}\sqrt{2\times q\times m_{SiON}}\times(\phi_{Trap})^{\frac{3}{2}}}{V_{IappGS/GD}\times\left[(T_{SiO2}+T_{SiON})\right]^{-1}}\right)} \quad (7)$$

where ϕ_{Trap} is the trap energy. Using the considered tunneling probabilities through $SiON/SiO_2$, the TAT current corresponding to the source/drain side`s cannel overlap become:

$$J_{GTATS/D} = \left(\frac{2\times C_{Trap}\times N_{Trap}\times\phi_{Trap}\times q}{3\times10^4\times V_{IappGS/GD}\times(T_{SiO2}+T_{SiON})^{-1}}\right)\times PTAT_{SiO_2S/D}\times PTAT_{SiONS/D} \quad (8)$$

where N_{Trap} is the trap states density and

$$C_{Trap} = \left(\frac{m_0}{m_{SiON}}\right)^{\frac{5}{2}}\times\left(\frac{16\pi\sqrt{\phi_e^3}}{3h\sqrt{\phi_{Trap}-\phi_e^3}}\right) \quad (9)$$

where ϕ_e is the total energy of electrons considered equal to 0.2 (eV). The total TAT current ($J_{GTATTOT}$) corresponding to the both sides of source and drain channel overlap become:

$$J_{GTATTOT} = J_{GTATS} + J_{GTATD} \quad (10)$$

We have implemented the developed DT and TAT current in automatic parameter extraction techniques using Verilog-A language in commercial IC-CAP package.

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3) Model Implementation in Verilog-A and Parameter Extraction inside IC-CAP

The implementation of the developed DT and TAT compact model is presented in Verilog-A code which is simulated in IC-CAP as a commercial package for parameter extraction. Verification of the extracted parameters and parameters correlations is performed against the gate leakage current measurements in Trigate MOSFET. The gate leakage current models are coded in verilog-A which makes it applicable to other simulators and industry IC design tools.

We present experimental study of the gate leakage tunneling current parameters correlations in Trigate MOSFET. In order to show the correlation between two parameters we have fixed one of the parameters in different values and we have tried to extract the other parameter by fitting simulated leakage current with those obtained from measurements.

4) Experimental Results and Discussion

The extraction techniques have been applied on n channel Trigate MOSFET with $SiON/SiO_2$ as gate dielectric stacks. Comparison of the simulation calculations to the measured data of the gate leakage current on Trigate MOSFETs allows obtaining DT and TAT current parameter values. Automatic parameter extraction techniques have been used to extract the model parameters and to illustrate parameters correlations for two sample device geometries. In the automatic parameter extraction routines a set of gate leakage current as a function of gate bias is used for each transistor and then optimizations are performed for the parameters in different group based on their important and priorities.

Table I, lists the corresponding parameter values of the TAT current and DT current based on experimental measurements. Figure 2 shows a good agreement between simulated plots from the application of DT (4) model and TAT (10) model using the extracted parameters (Table I) and measured data.

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Table 1: Extracted gate leakage current parameter values for an N-channel Tri-gate MOSFET for two different channel lengths.

L_G	1u	10u
EOT	1.9nm	1.9nm
H_{Fin}	65nm	65nm
W_{Fin}	71nm	71nm
V_D	0.05V	0.05V
m_{SiO2}	0.4	0.4
m_{SiON}	0.155	0.155
Φ_{SiO2}	3eV	3eV
Φ_{SiON}	2eV	2eV
ELEC	0.2eV	0.2eV
BTAT	300 MEG	3.5G
ATAT	1e15	8.2e20

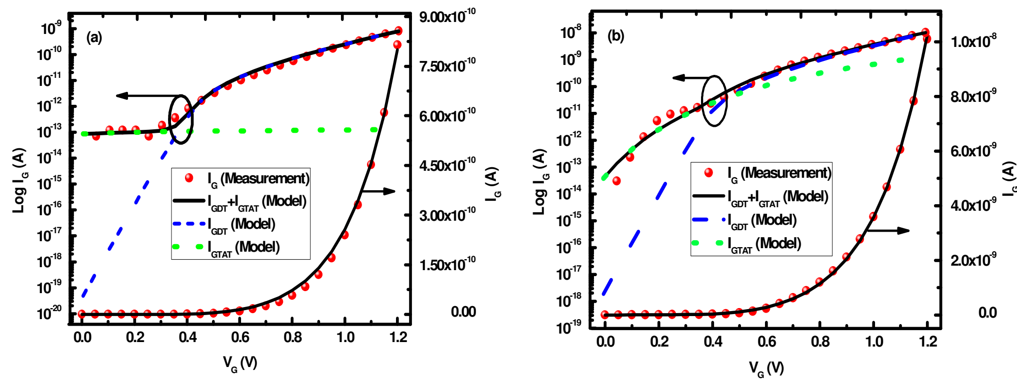

Figure 2: Model calculations and experimental measurements of the direct tunneling and TAT current as a function of gate voltage for a DG FinFET with extracted parameters for (a) channel length equal to 1µm and (b) channel length equal to 10µm.

The correlation between the gate leakage current and barrier height of the interfacial layer and dielectric layer as extracted parameters indicating further analysis of those parameters and providing additional insight into the gate leakage current. The experimental data for Trigate MOSFET, demonstrate that the gate tunneling leakage current is more strongly correlated to the barrier height of interfacial layer than barrier height of dielectric layer. Figure 3 shows the extracted correlation between the gate leakage current and barrier height of the interfacial layer and dielectric layer in the same device and conditions. The change in the leakage current due to the decreasing of barrier height in interfacial layer is much higher than the change due to the barrier height of dielectric layer.

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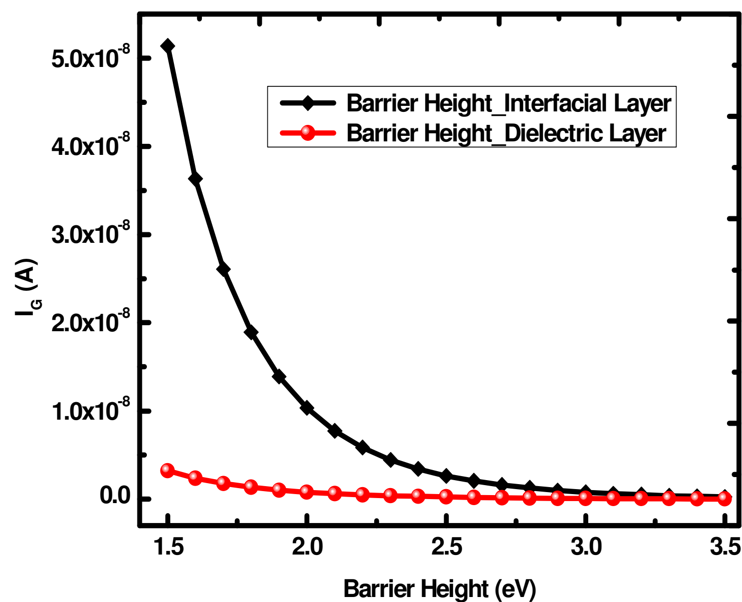

Figure 3: The gate leakage current as a function of barrier height of interfacial layer and dielectric material for a DG FinFET with extracted parameters.

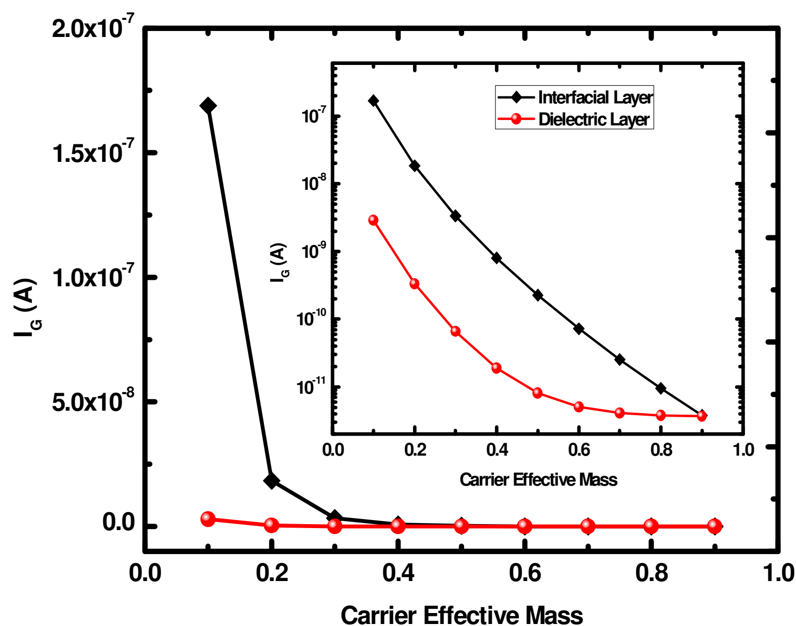

Figure 4: The gate tunneling leakage current as a function of carrier effective mass of interfacial layer and dielectric material for a DG FinFET with extracted parameters.

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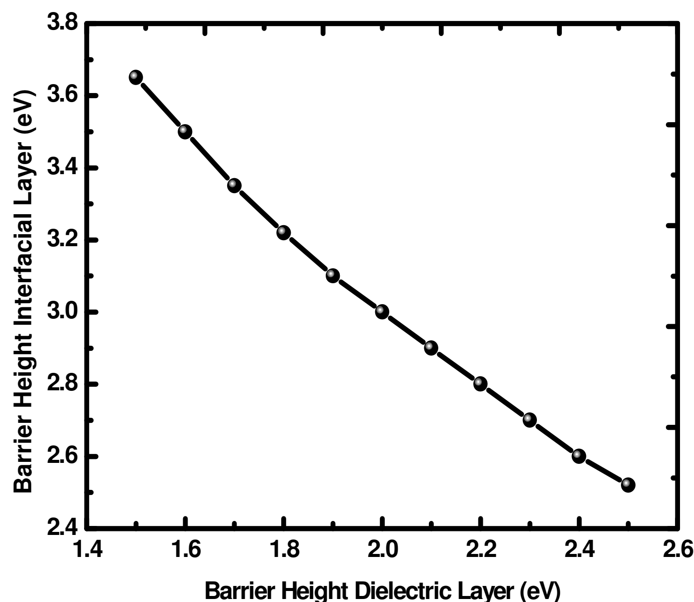

Figure 5: Correlation between barrier heights of interfacial layer as a function of barrier height of dielectric layer.

The correlation between the gate leakage current and carrier effective mass of interfacial layer and dielectric layer has been shown in Figure 4 in linear and log scale (inset figure). It is showing exact dependency of the gate leakage current in terms of carrier effective mass of the interfacial layer and dielectric layer. According to the Figure 4 the gate leakage current has a high sensitivity to the electron effective mass in interfacial layer rather than the electron effective mass in dielectric layer.

The gate leakage current measurements for the devices with channel length equal to 1µm and 10µm is used to verify correlation between barrier heights and carrier effective masses in interfacial layer and dielectric layer. Figure 5 shows the correlation between barrier heights of interfacial layer as a function of barrier height of the dielectric layer. The correlation between carrier effective mass in dielectric layer as a function of carrier effective mass in interfacial layer has been shown in Figure 6. The correlation between barrier height in interfacial layer and dielectric layer as a function of carrier effective mass in interfacial layer are shown in Figure 7.

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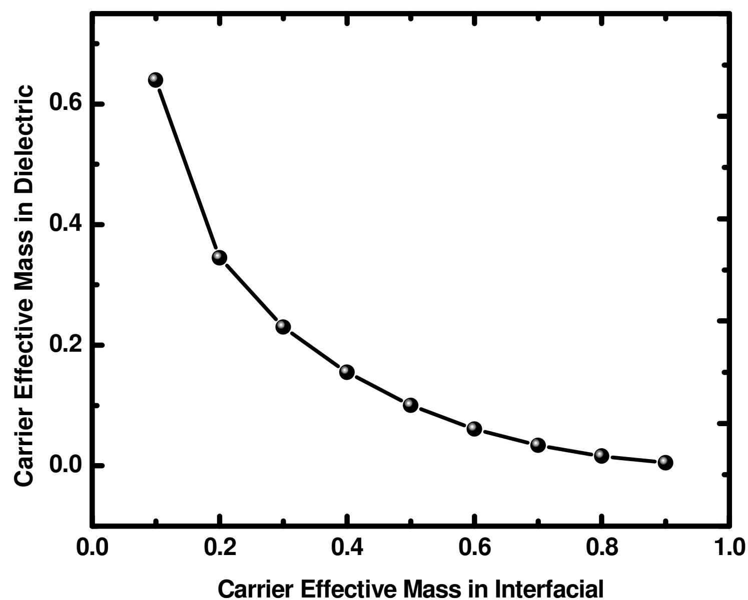

Figure 6: Correlation between carrier effective mass in dielectric layer as a function of carrier effective mass in interfacial layer.

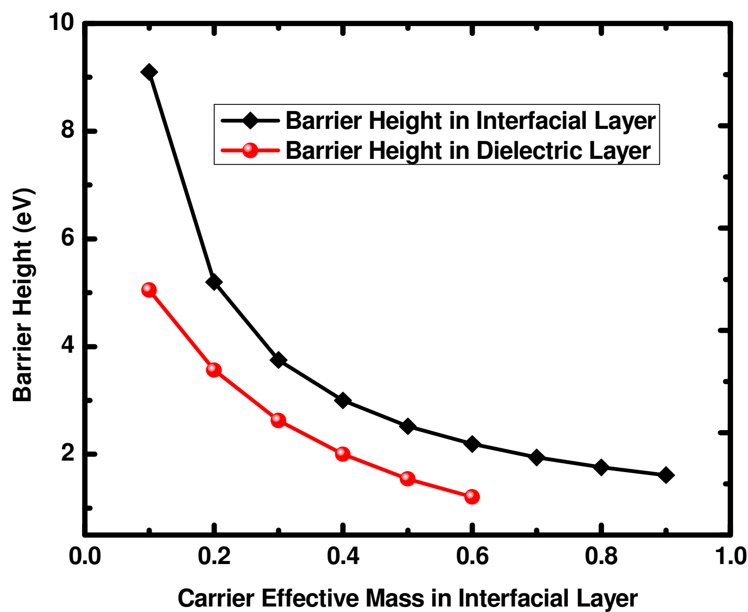

Figure 7: Correlation between barrier height in interfacial layer and dielectric layer as a function of carrier effective mass in interfacial layer.

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5) Conclusion

We have developed automatic parameter extraction techniques in the commercial package (IC-CAP) to obtain gate leakage current parameter values for Trigate MOSFET. The extraction approaches have been applied for various conditions and device geometry and have been found suitable techniques for MOSFET parameter extraction process. The correlation between gate leakage currents, barrier heights and carrier effective messes are analyzed in details based on our DT current and TAT current models, automatic parameter extraction techniques and measured gate leakage current in Trigate MOSFET. The verification of the extraction techniques and gate leakage current parameters correlations are discussed and the results show additional insight into the gate leakage current model and good agreement with the measured data in Trigate MOSFET.

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General Conclusion

1) We have developed simple and improved analytical models for the direct tunneling gate leakage current based on a proper WKB tunneling probability approximation. A theoretical study with only one layer of gate oxide materials has been considered. We have shown guidelines for finding the appropriate high-k dielectric materials for the 22 nm technological node requirements according to the latest ITRS in DG MOSFETs.

2) We have developed simple and improved gate leakage current models for the two layer gate oxide materials in DG MOSFETs. We have shown the most promising high-k candidates for different values of EOT and SiO_2 interfacial layer thickness, satisfying the gate leakage requirements according to the ITRS. They demonstrate that the materials like HfO_2, La_2O_3, $LaAlO_3$ and Pr_2O_3 in the hexagonal phase would fulfill the considered requirements.

3) Analytical models of the direct tunneling gate leakage current are used to determine the high-k dielectric suitable for the nanoscale UTB SOI MOSFETs structure in cases with no interfacial layer and with SiO_2 as an interfacial layer for the 17nm, 15nm and 14nm technological node requirements. In the ideal case without an interfacial layer, HfO_2 and Lu_2O_3 were found to be the best gate oxide materials for the 17nm, 15nm and 14nm technological node requirements.

4) A compact gate leakage current partitioning model has been presented for nanoscale Double Gate MOSFETs, using analytical models of the direct tunneling gate leakage current. The influence and impact of the thickness of the interfacial SiO_2 layer on the gate-drain and gate-source components has been shown. The results of the gate current partitioning components into the drain and source show good agreement with 2D TCAD numerical device simulation.

5) The temperature dependent analytical models of the direct tunneling current in inversion region and the trap assisted tunneling current in subthreshold regime have

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been developed for DG FinFET with a two dielectric layers gate stack such as $SiON/SiO_2$. Our analysis based on the gate leakage current measurements in the above threshold regime for different temperatures shows that the direct tunneling current is clearly dominant over the trap assisted tunneling, while the opposite happens below threshold.

6) We have developed automatic parameter extraction techniques for our explicit compact model in DG MOSFET based on surface potential including short channel effects (channel length modulation, DIBL, carrier velocity saturation, threshold voltage roll-off and series resistance). The second derivative of the drain current with respect to the source-gate potential is verified which is continuous due to a careful mathematical derivation of our model. The P_1 and P_2 parameters dependency on the channel length are investigated and shown for Trigate MOSFETs based on measured data and extracted parameters.

7) Direct Tunneling and Trap Assisted Tunneling gate leakage current parameters have been extracted and verified considering automatic parameter extraction approaches for Trigate MOSFET. The correlation between gate leakage currents, barrier heights and carrier effective messes are analyzed in details based on our DT current and TAT current models, automatic parameter extraction techniques and measured gate leakage current in Trigate MOSFET.

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