Interleaved Digital Power Factor Correction Based on the Sliding-Mode Approach

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Abstract

This study describes a digitally controlled power factor correction system based on two interleaved boost converters operating with pulse width modulation (PWM). Both converters are independently controlled by an inner control loop based on a discrete-time sliding-mode approach that imposes loss-free resistor (LFR) behavior on each cell. The switching surface implements an average current-mode controller so that the power factor is high. The sliding-mode-based digital controller is designed to operate at a constant switching frequency so that the interleaving technique, which is recommended for AC-DC power conversion systems higher than 1 kW, can be readily applied. An outer loop regulates the output voltage by means of a discrete-time PI compensator directly obtained from a discrete-time small signal model of the ideal sliding dynamics. The control law proposed has been validated using numerical simulations and experimental results in a 2 kW prototype.

Keywords: AC-DC power conversion, loss-free resistor, digital control, discrete-time sliding-mode control, power factor correction, interleaving.

I. INTRODUCTION

In recent years, researchers and engineers have been striving to improve power factor correction (PFC) and ensure that the quality of the absorbed grid current complies with the stipulations of standard regulations [1]. Although many switching power converters have been proposed [2] to substitute passive rectifiers, the most popular PFC circuit for applications lower than 1 kW is still configured by a boost converter connected to the grid by a diode bridge. This is because of the intrinsic advantages of this simple stage: i.e., the input current is continuous, the transistor is grounded, and it is simple and highly efficient. For higher power levels and single-phase applications, the interleaving technique is recommended [3-5]. This technique consists of connecting two or more converters in parallel with the same switching frequency and phase-shifting their respective control signals. This operation reduces not only component stress and volume but also EMI generation levels due to the ripple cancellation of inductor currents and output voltage [6, 7].

Various control techniques have been developed to achieve unity power factor in switch-mode AC-DC power supplies. First of all, analog controllers have been widely used in PFC applications because they provide good performance at low cost. An interesting review of PFC analog controllers is presented in [8] for three inductor current conduction modes: namely, continuous conduction mode (CCM), discontinuous conduction mode (DCM) and boundary conduction mode (BCM). Figure 1 shows the classical control strategy for single-phase PFC applications consisting of an inner loop that controls the input current while an outer loop regulates the output voltage [9]. The reference of the inner current loop is obtained by multiplying the output of the outer loop by the sensed input voltage. This is the strategy used in studies that propose a hysteretic current controller as the inner control loop because of its robustness, stability and dynamic response [10-12]. To illustrate this behavior, Fig. 2 shows an inductor current switching in a hysteresis width of $2H$, and the transition to a new equilibrium point caused by a step change at $t=t_1$ of the current reference. Because of these advantages, hysteretic controllers have been used to implement loss-free resistors (LFRs) based on sliding-mode control (SMC) [13] in CCM for both PFC and impedance matching applications [14-17].

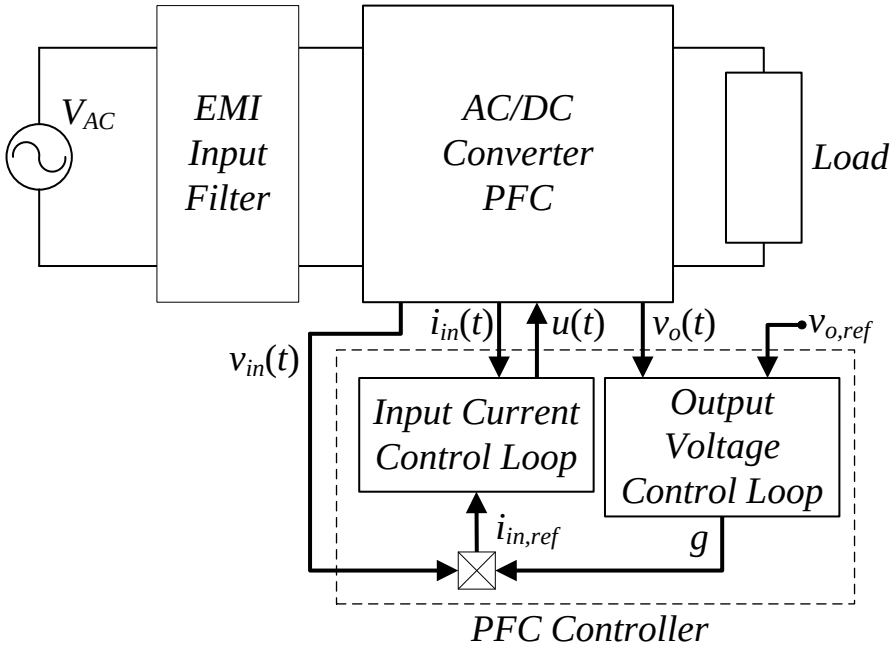


Fig. 1. General block diagram of a classical two-loop control strategy in single-phase power factor correction applications.

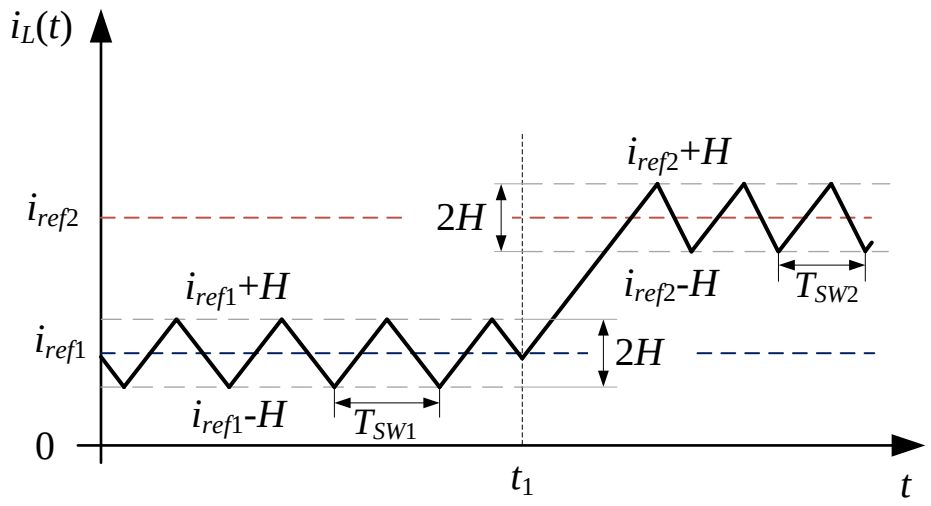


Fig. 2. Inductor current reference step response of a hysteretic controller. T_{SW1} and T_{SW2} are the switching periods for the equilibrium points corresponding to i_{ref1} and i_{ref2} respectively.

Although hysteretic controllers can result in very low distorted input currents, constant-frequency-based current controllers are a more attractive solution in PFC applications since they make it easier to design the EMI input filters. Furthermore, the complex implementation and high cost of analogue circuits that require the use of an external multiplier prompted the development of low-cost single-chips specifically designed for PFC applications [18]. Also, other control strategies such as Non-linear Carrier (NLC) control [19] and One Cycle Control (OCC) [20, 21] were developed in an attempt to avoid the use of an external multiplier. Despite their differences, all

these controllers generate a control signal with a constant switching frequency since they are based on a pulse-width-modulation (PWM) technique [22]. Several studies have proposed sliding-based implementations with constant switching frequency [23-26] the aim of which is to provide a fast dynamic response similar to that provided by hysteretic-based sliding-mode (SM) controllers. In [26], the correspondence between the equivalent control in SM and the zero-dynamics non-linear PWM control is applied to a boost converter behaving like a LFR. However, the drawback of this controller is that it needs an analog divider, which is a bulky component that is difficult to adjust and can be saturated for a zero value of the denominator.

Digital controllers have increasingly been used in switching power converters in the last decade because of the decrease in their cost and size, and the increase in their computation capability with respect to their analog counterparts [27]. These advantages led to digital controllers being used in PFC applications so that the Power Factor (PF) could be increased, the Total Harmonic Distortion (THD) of the input current reduced and the control technique adjusted to the load conditions [28]. Several digital current controllers have been developed to ensure proportionality between input current and input voltage while operating at constant switching frequency. Of these, the average current approach is the most popular. In [29] the input current and output voltage controllers are designed on the basis of the desired time-domain behavior of the corresponding current and voltage loops, so that the associated transfer functions are designed in the s -domain and then discretized. In turn, the strategy in [30] discretizes the continuous-time power stage model so that the current controller can be directly designed in the z-domain. Moreover, the design of the current control loop is calculated from the control-to-inductor current transfer function obtained from the small-signal discrete-time model of the converter. A different procedure has been followed in [31], where the purpose of the digital controller is to emulate the operation of the analog NLC controller presented in [19].

What is more, the improvement in computational capability of digital devices has led to predictive model (PM) current controllers being developed on the basis of the internal model of the converter [32, 33]. A widely used family of constant switching frequency predictive current controllers is presented in [34]. They include valley, peak and average current controllers for the three basic power converters (i.e. boost, buck and buck-boost). These predictive current controllers calculate the duty cycle of the next switching period using the parameters of the plant and the present samples of inductor current, input and output voltages, and duty cycle. As is reported in [35], boost converters working as pre-regulators and managed by predictive current controllers can achieve a

better quality of input current waveform than discrete-time proportional-integral (PI) current controllers because their dynamic response is faster.

In a clear-cut contrast with all previous studies that needed to sense the inductor current, a more recent study has tried to avoid the use of current sensors [36] by using pre-calculated duty cycles to compensate for the absence of the direct measure of the inductor current. The system works well for nominal conditions and in the steady-state regime, but changes in the input voltage and load conditions can reduce the power factor.

A digitally controlled interleaved bridgeless boost converter working as a pre-regulator reported in [37] also avoids the current sensor. The total input current is estimated as a function of the present duty cycle and both the input and output sensed voltages, while the necessary duty cycle of the following switching period is calculated by a predictive controller that takes into account the input current reference, estimated input current, and input and output voltages. However, this approach can increase the line current distortion due to the accumulative error produced by inappropriately estimating the input current. In the same context of digital interleaving for PFC, a discretized average current controller that senses the total input current and both the input and output voltages is reported in [38] to address the current sharing problem between two interleaved boost cells. In [39], a different approach is used: a master-slave strategy based on a transition determined by a current-mode controller aims to achieve zero-current switching in interleaved operation. Finally, a discrete-time energy function is used in [40] to derive the optimal value of the instantaneous duty cycle in two-interleaved boost cells for PFC with output voltage regulation as in the work reported here.

A noteworthy feature of interleaving-based PFC is that not only does it improve the input current quality, it also makes it possible to handle higher power levels by means of the parallel connection of low power converters. This means that the power system can be constructed in modules, each one of which can be standardized and traditional low-power design techniques can be used. The purpose of this study is to design a 2 kW power system with PFC using two interleaved modules of 1kW, each of which employs a control technique similar to the one recently reported in [41]. The valley current-mode controller proposed in [41] was designed following the discrete-time sliding-mode control theory proposed in [13]. It offers a similar fast response to analog hysteretic control systems and is also capable of operating at a constant switching frequency (see Fig. 3). However, if the valley current-mode controller is directly applied for PFC, the amplitude of the input current third harmonic will be as high as when peak current-mode controllers are used [42] because the upper envelope of the inductor current is highly distorted. This phenomenon is illustrated in Fig. 4, where the converter parameters are L=620

µH, C_O=300 µF, g=0.0031 S=Ω^{-1}, V_{AC}=230 V_{rms}, V_O=400 V, F_{SW}=60 kHz and the control algorithm is the one reported in [43].

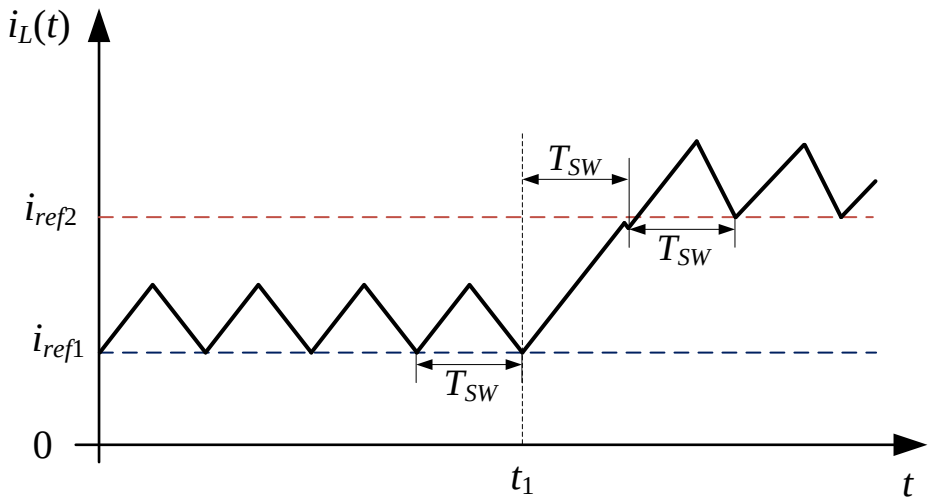
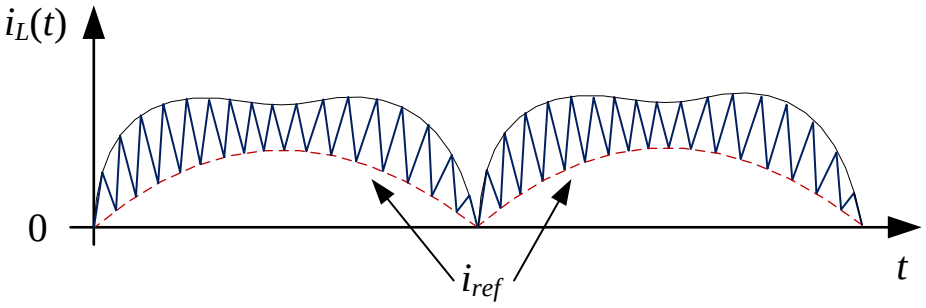


Fig. 3. Inductor current reference step response of the discrete-time sliding-mode valley current-mode controller. T_{SW} is defined as the constant switching period.

a)



b)

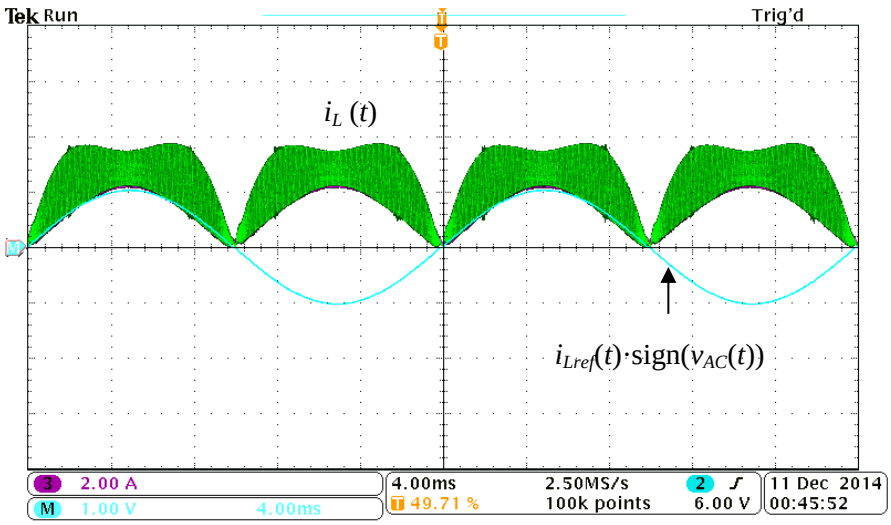


Fig. 4. Inductor current waveform under valley current-mode control: a) expected behavior, b) experimental result.

Therefore, to mitigate the influence of the third harmonic, another current-mode approach has to be considered. This study reports an average current-mode controller based on discrete-time sliding-mode control theory. The controller proposed is expected to have no oscillation issues because the calculated duty cycle is directly applied in the present switching period and does not use information from the previous one. The resulting control law is implemented by means of an inner loop that imposes an LFR behavior to a single converter, which constitutes the basic module. A proportional relation between voltage and current is obtained in this module, which generates a unity power factor. The extension of power factor correction to a higher power system is achieved by the interleaving operation of two modules.

However, it is still not clear how to make sliding-mode control compatible with interleaving. Previous attempts to make it compatible have been limited to specific configurations [7, 44]. The difficulty stems from the fact that sliding-mode controllers are usually implemented with hysteretic comparators, which results in variable switching frequency. In most cases it is not easy to establish an interleaved operation with variable switching frequency. Hence, it makes sense to use sliding-mode controllers operating at constant switching frequency as in [24, 25] or [41]. The procedure used in the latter is the one proposed here. Therefore, the controller reported belongs to the family of sliding-mode-based PWM systems.

The power system is a 2 kW pre-regulator made up of two interleaved boost converters that are independently controlled to ensure correct current sharing. A PI discrete-time controller is also inserted in an outer loop to regulate the output voltage of the system. This outer control loop is designed from the resulting discrete-time small signal model of the ideal sliding dynamics of the inner loop.

The rest of the paper is organized as follows. The system is described in section II, and the design of the digital controller and its stability analysis are presented in section III. Section IV reports the simulations and experimental results of the digitally-controlled power system for PFC applications. It is shown to be feasible and to perform well. Section V presents the final conclusions.

II. SYSTEM DESCRIPTION

The PFC system proposed consists of two interleaved unidirectional boost converters which are regulated by a digital controller (see Fig. 5) so that each boost cell behaves like an LFR.

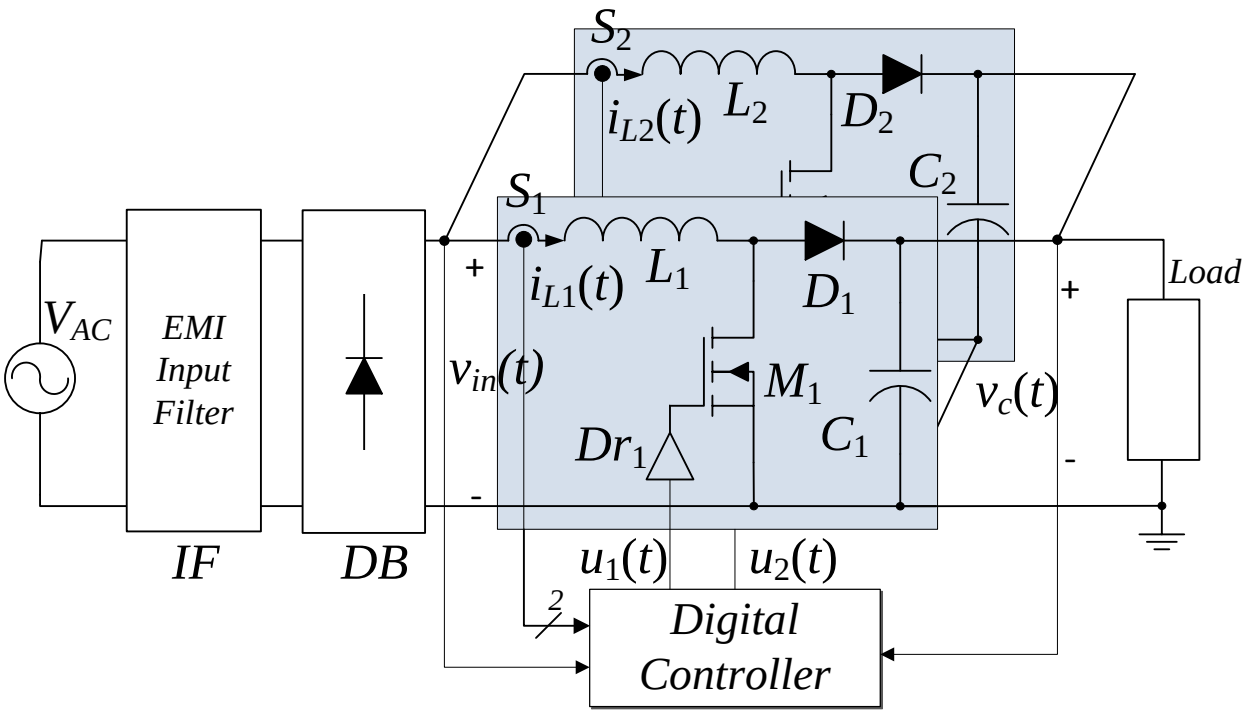


Fig. 5. Scheme of the digitally controlled PFC system based on two interleaved boost converters.

An LFR is a two-port switching structure of the *POPI* type (Power Output = Power Input) [45] because all the power absorbed by the input port (P_{in}) is ideally transmitted to the output port (P_{out}). The second characteristic of an LFR is the proportionality between voltage and current at the input port, which implies a unity power factor. Hence, the steady-state equations of a loss-free resistor are defined as follows

$$V_1 I_1 = V_2 I_2 \tag{1}$$

$$V_1 = r I_1 \tag{2}$$

where V_1, I_1, V_2 and I_2 are the steady-state averaged value of input and output variables, respectively. Parameter r defines the chosen input resistive impedance of the circuit in steady-state. The emulated resistance value is also defined as r=1/G, where G represents the conductance of the LFR.

If the digital controller requires each boost cell to behave like an LFR behavior, the steady-state representation of Fig. 5 can be modeled as in Fig. 6 where two LFRs in parallel. Hence, the total input resistive impedance r corresponds to the equivalent resistance value of the parallel resistors r_1 and r_2 while the total output power P_o becomes the sum of the power delivered by both LFR sources (P_1 and P_2):

$$r = \frac{r_1 \cdot r_2}{r_1 + r_2} \tag{3}$$

$$P_o = P_{o1} + P_{o2} \tag{4}$$

$$P_o = \frac{V_{in}^{\ 2}}{r} \tag{5}$$

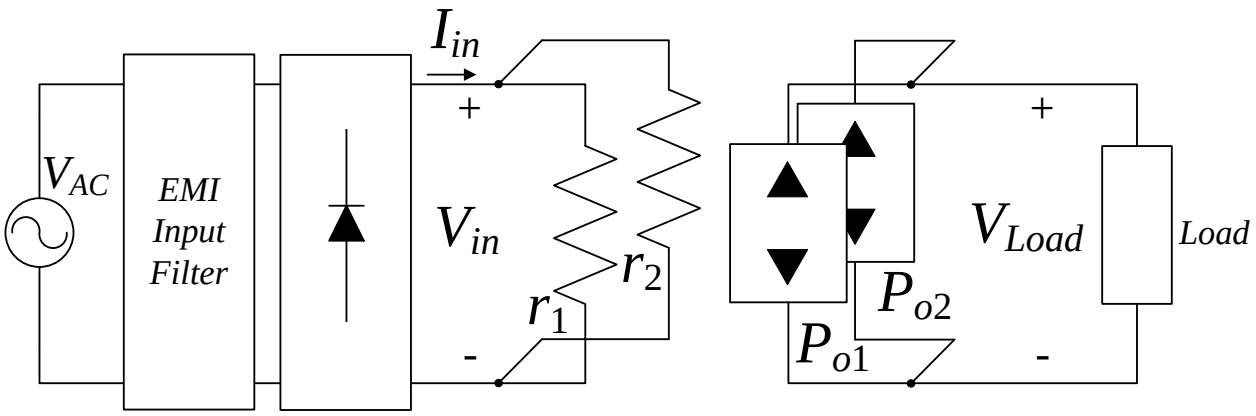


Fig. 6. Equivalent representation of the pre-regulator based on two parallel connected LFRs.

For a proper interleaving operation, the input current I_{in} must be shared equally by each boost converter. This can be ensured by adjusting r_1=r_2, so that each boost cell absorbs half of the input current and delivers half of the total output power (P_{o1}=P_{o2}=P_o/2). This means that both inductor currents must share the same current reference and each boost cell must be controlled independently to ensure that the input current is equally distributed.

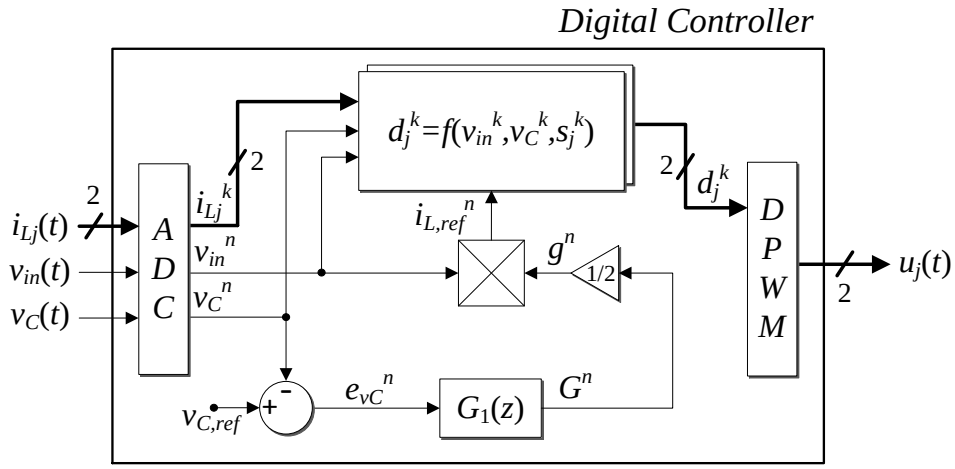


Fig. 7. Block diagram of the digital controller.

Figure 7 illustrates the block diagram of the proposed digital controller. Four different variables of the pre-regulator are sampled: the rectified input voltage $v_{in}(t)$, the output voltage $v_C(t)$ and the inductor currents $i_{Lj}(t)$ where j is 1 and 2 for each boost cell, respectively. Inductor current variables are sampled at the beginning of their respective n^{th} and m^{th} switching periods (see Fig. 8). Index k will be used to describe in compact form the dynamic behavior of both cells whose sampling instants are related by t^m=t^n+T_{SW}/2, where T_{SW} stands for the switching period of each cell. This index will be equal to n for cell 1 and equal to m for cell 2. Since $v_{in}(t)$ and

$v_C(t)$ present slower dynamics than inductor currents, they are only sampled at the beginning of the n^{th} switching period, so that both samples are referred to index *n*.

Both inductor currents are controlled by the inner control loop which is based on the discrete-time non-linear function d_j^k that is obtained from the discrete-time SMC theory. This function represents the calculated duty cycle in the k^{th} switching period defined as

$$d_j^{\,k} = \frac{\tau_j^{\,k}}{T_{SW}} \;, \quad 0 < d_j^{\,k} < 1 \tag{6}$$

where τ_j^k stands for the duration of the conduction state of MOSFET M_j during the k^{th} switching period. Once the duty cycle calculation has finished, the corresponding result is transmitted to the Digital PWM module so that the control signals $u_1(t)$ and $u_2(t)$ can be generated. Besides, the inductor current reference is given by the product of the sampled rectified input voltage $v_{in}^{\,n}$ and parameter g^n, which stands for the computed conductance of each boost cell. The latter parameter is calculated by the outer control loop $G_1(z)$ which regulates the output voltage $v_C(t)$ at the desired reference level given by $v_{C,ref}$.

Figure 8 illustrates the expected interleaving operation with inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ sampled at the beginning of their respective switching periods and whose average values coincide with the current reference $i_{L,ref}^{\,n}$. Note that the current reference is the same for both inductors so that the input current is distributed equally between both cells. Moreover, to obtain a correct interleaving operation, the control signals have to be phase-shifted 360º/*h* where *h* corresponds to the number of interleaved converters or cells, so that the control signals $u_1(t)$ and $u_2(t)$ need to be phase-shifted 180º in the present study.

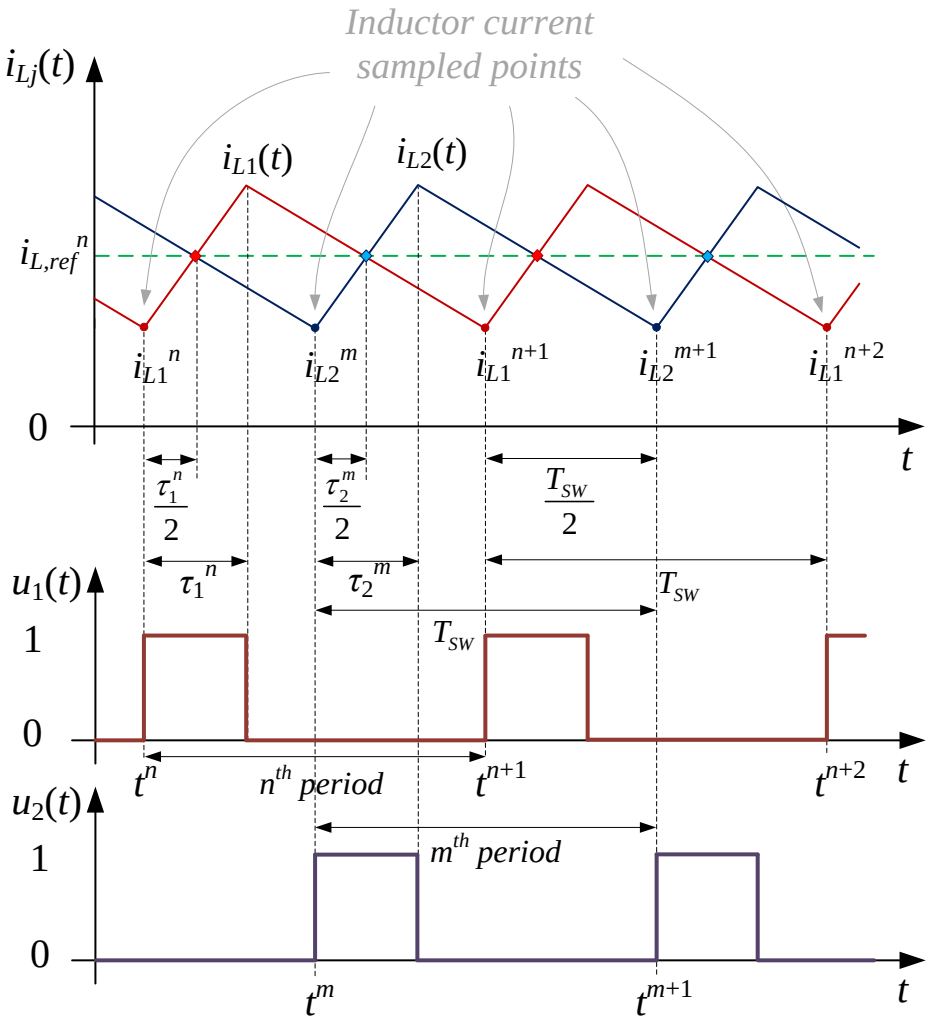


Fig. 8. Expected operation of the interleaved inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ and control signals $u_1(t)$ and $u_2(t)$.

III. DIGITAL CONTROL DESIGN

The design of the digital control algorithm is divided into two parts: the inner control loop for the inductor currents and the outer control loop regulating the DC output voltage.

A. Discrete-time Sliding-Mode Current Control

A discrete-time model of the switching converter is first derived to characterize the dynamic behavior of the power stage.

1) Discrete-time Model of the Power Converter

Assuming that the system operates at a constant swiching frequency and in Continuous Conduction-Mode (CCM), two topologies can be defined for each boost converter depending on the conduction state of their respective MOSFETs. It is considered that control signal $u_j(t)$ will be 1 for ON topology during state conduction

time τ_j^k, and 0 for the rest of the switching period in OFF topology. Hence, the continuous-time dynamics of the state variables are described by the following two linear differential equations

$$\dot{x}_j(t) = A_{1,j}x_j(t) + B_{1,j} \qquad t^k < t \le t^k + \tau_j{}^k \tag{7}$$

$$\dot{x}_j(t) = A_{2,j}x_j(t) + B_{2,j} \qquad t^k + \tau_j{}^k < t \le t^k + T_{SW} \tag{8}$$

where $x_j(t)$ is the state vector of the state variables, the symbol ($\dot{}$) represents the time derivative operation and t^k stands for the moment at which the k^{th} switching period is started so $t^{k+1} = t^k + T_{SW}$. The state vector of each boost cell is defined as follows

$$x_j(t) = \left[i_{Lj}(t) \quad v_C(t) \right]^T \tag{9}$$

where ^{T} indicates the transpose of the vector. Since both converters are connected in parallel, the total output capacitance becomes $C=C_1+C_2$. Considering that both converters are ideal lossless systems and that the output load consists of a resistor of value R_o, the state matrices $A_{1,j}$, $A_{2,j}$, $B_{1,j}$ and $B_{2,j}$ are the following

$$A_{1,j} = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R_o C} \end{bmatrix} \qquad A_{2,j} = \begin{bmatrix} 0 & -\dfrac{1}{L_j} \\ \dfrac{2}{C} & -\dfrac{1}{R_o C} \end{bmatrix} \qquad B_{1,j} = B_{2,j} = \begin{bmatrix} \dfrac{v_{in}(t)}{L_j} \\ 0 \end{bmatrix} \tag{10}$$

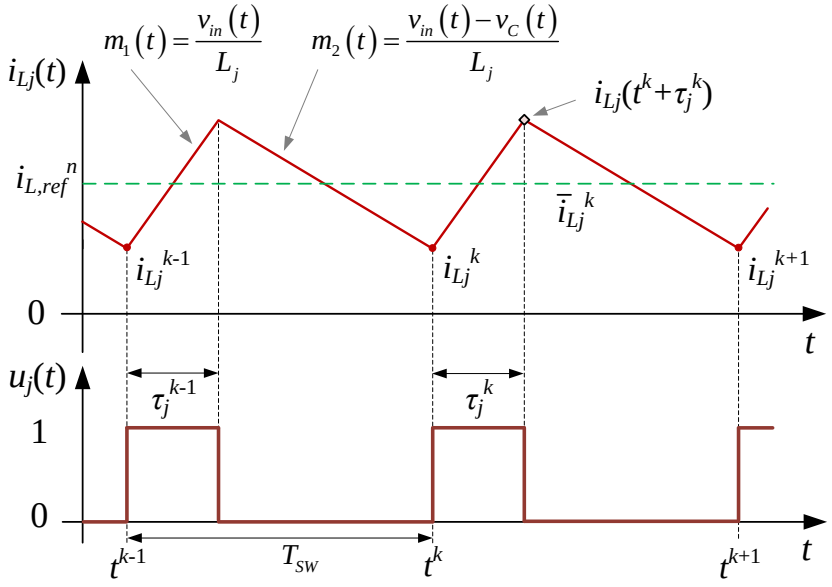


Fig. 9. Theoretical behavior of one cell inductor current. $m_1(t)$ is the inductor current slope for the ON topology and $m_2(t)$ for the OFF topology.

Assuming that input and output voltages do not change in a switching period, it can be easily deduced from Fig. 9 that the theoretical value of inductor current $i_{Lj}(t)$ at $t=t^{k+1}$ can be expressed as follows

$$i_{Lj}\left(t^k+\tau^k\right)=i_{Lj}\left(t^k\right)+\frac{v_{in}\left(t^k\right)}{L_j}\tau_j^{\ k} \tag{11}$$

$$i_{Lj}\left(t^{k+1}\right)=i_{Lj}\left(t^k+\tau_j^{\ k}\right)+\frac{v_{in}\left(t^k\right)-v_C\left(t^k\right)}{L_j}\left(T_{SW}-\tau_j^{\ k}\right) \tag{12}$$

Variables $i_{Lj}(t^k)$ and $i_{Lj}(t^{k+1})$ are redefined as $i_{Lj}^{\ k}$ and $i_{Lj}^{\ k+1}$, respectively, $v_{in}(t^k)$ as $v_{in}^{\ k}$ and $v_C(t^k)$ as $v_C^{\ k}$ in order to simplify the notation.

Substituting (11) in (12) leads to

$$i_{Lj}^{\ k+1}=i_{Lj}^{\ k}+\frac{\left(v_{in}^{\ k}-v_C^{\ k}\right)}{L_j}T_{SW}+\frac{v_C^{\ k}}{L_j}\tau_j^{\ k} \tag{13}$$

where $i_{Lj}^{\ k}$ is the discrete-time representation of inductor current $i_{Lj}(t)$, and $i_{Lj}^{\ k+1}$ describes the discrete-time recurrence of each boost cell.

Note that in steady-state, which means $i_{Lj}^{\ k}= i_{Lj}^{\ k+1}$, the corresponding duration of the ON state time $\tau_{j,ss}^{\ k}$ is

$$\tau_{j,ss}^{\ k}=\left(1-\frac{v_{in}^{\ k}}{v_C^{\ k}}\right)T_{SW} \tag{14}$$

Hence, the steady-state average value of the inductor current $i_{Lj}(t)$ during the k^{th} switching period $\left(\bar{i}_{Lj}^{\,k}\right)$ can be represented as a function of its respective valley current value as

$$\bar{i}_{Lj}^{\,k} = i_{Lj}^{\,k} + \frac{v_{in}^{\,k}}{2L_j}\left(1-\frac{v_{in}^{\,k}}{v_C^{\,k}}\right)T_{SW} \tag{15}$$

The discrete-time dynamics of the average value of the capacitor voltage can be obtained by applying Euler's method to the average representation of the continuous-time description defined in (7) and (8). It should be borne in mind that the equivalent output capacitor receives the sum of both inductor currents. Thus, the discrete-time dynamics of the capacitor voltage can be described as follows

$$v_C^{\,k+1} = v_C^{\,k}\left(1-\frac{T_{SW}}{R_oC}\right)+\frac{2\bar{i}_{Lj}^{\,k}}{C}\left(T_{SW}-\tau_j^{\,k}\right) \tag{16}$$

2) Discrete-time Sliding Control Surface

All sliding-mode controllers are based on a switching surface $s(x)$ that in sliding-mode regime is characterized by $s(x)=0$, thus relating the desired state variable to be controlled and its associated reference [13]. In order to design an average current-mode control such as the one depicted in Fig. 10, the discrete-time sliding control surface is defined as follows

$$s_j^{\,k} = i_{L,ref-valley}^{\,n} - i_{Lj}^{\,k} \tag{17}$$

where $i_{L,ref\text{-}valley}^{\,n}$ corresponds to the valley reference value of the inductor current, which is defined as

$$i_{L,ref-valley}^{\,n} = i_{L,ref}^{\,n} - \frac{v_{in}^{\,n}}{2L_j}\left(1-\frac{v_{in}^{\,n}}{v_C^{\,n}}\right)T_{SW} \tag{18}$$

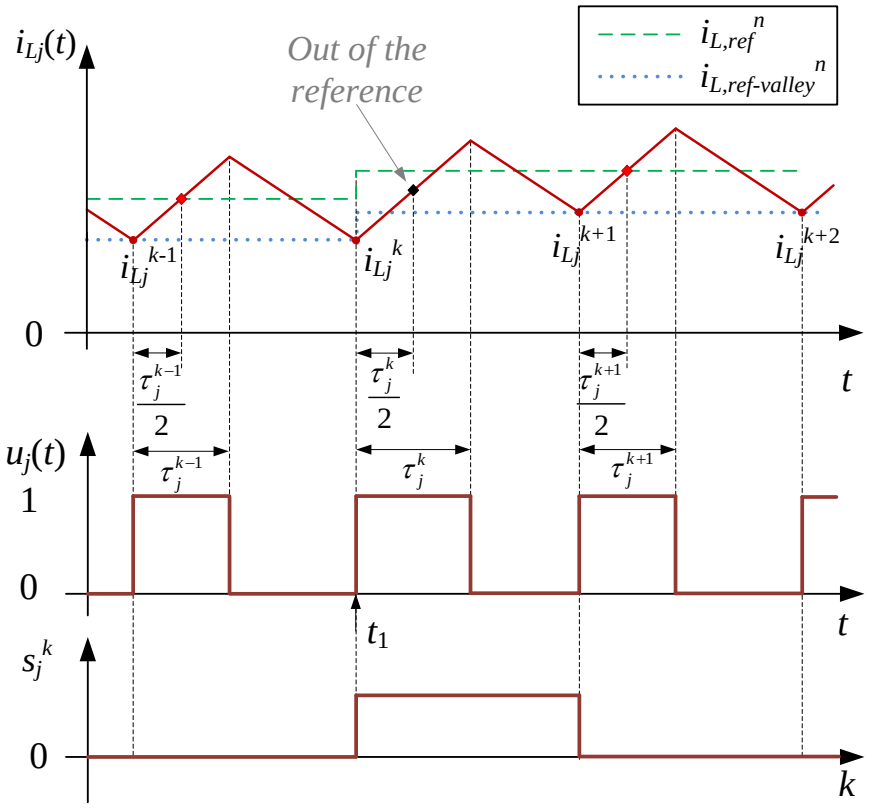


Fig. 10. Inductor current $i_{Lj}(t)$, control signal $u_j(t)$ and sliding surface $s_j^{\ k}$.

Note that the inductor current reference and the input and output voltages are associated to index n while the current variables depend on index k. Note that inducing LFR behavior as in [43] requires the inductor current reference to be defined as $i_{L,ref}^{\ n} = v_{in}^{\ n} g^n$ in order to ensure the proportionality of the input current and input voltage in each boost cell. It can also be observed that the sliding surface depends on the inductor current reference $i_{L,ref}^{\ n}$, the sample of the inductor current $i_{Lj}^{\ k}$ and half of the steady-state peak-to-peak inductor current ripple of the present switching period. When there is a change in the current reference, as depicted in Fig. 10 at t_1, the necessary $\tau_j^{\ k}$ is calculated by applying the sliding-mode existence condition. This means that the sliding control surface has to be equal to 0 in the future switching period [13]:

$$s_j^{\ k+1} = \left(i_{L,ref}^{\ n+1} - \frac{v_{in}^{\ n+1}}{2L_j} \left(1 - \frac{v_{in}^{\ n+1}}{v_C^{\ n+1}} \right) T_{SW} \right) - i_{Lj}^{\ k+1} = 0 \tag{19}$$

In this case, the controller will change $i_{Lj}^{\ k+1}$ to $i_{L,ref\text{-}valley}^{\ n+1}$ in the next switching period as long as variables $i_{L,ref}^{\ n+1}$, $v_{in}^{\ n+1}$ and $v_C^{\ n+1}$ are known. However, it is more common to use their present values – i.e. $i_{L,ref}^{\ n}$, $v_{in}^{\ n}$ and $v_C^{\ n}$– so $i_{Lj}^{\ k+1}$ will become the previous current reference $i_{L,ref\text{-}valley}^{\ n}$. Hence, equation (19) results in

$$s_j^{k+1} = \left({i_{L,ref}}^n - \frac{{v_{in}}^n}{2L_j}\left(1 - \frac{{v_{in}}^n}{{v_C}^n}\right)T_{SW} \right) - i_{Lj}^{k+1} = 0 \tag{20}$$

3) Equivalent control

Substituting (13) in (20) yields the following expression

$$s_j^{k+1} = \left({i_{L,ref}}^n - \frac{{v_{in}}^n}{2L_j}T_{SW}\left(1 - \frac{{v_{in}}^n}{{v_C}^n}\right) \right) - \left({i_{Lj}}^k + \frac{\left({v_{in}}^n - {v_C}^n\right)}{L_j}T_{SW} + \frac{{v_C}^n}{L_j}{\tau_j}^k \right) = 0 \tag{21}$$

The next step is to find the solution to (21) by solving τ_j^k, which is defined as the equivalent control $\tau_{eq,j}^k$ that keeps the controlled variable on the sliding surface $s(x)=0$:

$${\tau_{eq,j}}^k = \frac{L_j\left({i_{L,ref}}^n - {i_{Lj}}^k\right) + T_{SW}\left({v_C}^n - {v_{in}}^n\right)\left(1 - \frac{{v_{in}}^n}{2{v_C}^n}\right)}{{v_C}^n} \tag{22}$$

Hence, in sliding regime, the duration of the MOSFETs' ON state will be $\tau_j^k = \tau_{eq,j}^k$. However, if the controller is not able to reach the sliding surface, the resulting value of τ_j^k has to be theoretically limited as follows

$$0 < {\tau_j}^k < T_{SW} \tag{23}$$

This inequality prevents the loss of the constant switching frequency, because for both limits 0 and T_{SW} the system would not switch. In practice, the minimum applicable ON-state duration will be the time it takes to compute $\tau_{eq,j}^k$ in each switching period, which will depend on the calculation capabilities of the digital controller.

4) Ideal discrete-time dynamics and equilibrium point

Once in sliding regime, the equivalent control ensures that the controlled variable is kept on the surface, which results in a 1st reduced order system. This can be demonstrated by substituting equivalent control (22) in the discrete-time dynamics of inductor currents i_{Lj}^{k+1} defined in (13)

$${i_{Lj}}^{k+1} = {i_{L,ref}}^n - \frac{T_{SW}}{2L_j}{v_{in}}^n\left(1 - \frac{{v_{in}}^n}{{v_C}^n}\right), \tag{24}$$

and ensuring that the average inductor current value $\bar{i}_{Lj}^{\,k}$ coincides with the previous current reference $i_{L,ref}^{n-1}$ as expected.

The reduced discrete-time dynamics of the output capacitor voltage can be obtained if τ_j^k is substituted by $\tau_{eq,j}^k$ and $\bar{i}_{Lj}^{\,k}$ by $i_{L,ref}^{n-1}$ in expression (16).

$${v_C}^{n+1} = {v_C}^n\left(1 - \frac{T_{SW}}{R_o C}\right) + \frac{2{i_{L,ref}}^{n-1}}{C{v_C}^n}\left(L_j\left({i_{L,ref}}^{n-1} - {i_{L,ref}}^n\right) + {v_{in}}^n T_{SW}\right) \tag{25}$$

Taking into account that $i_{L,ref}{}^{n}= v_{in}{}^{n}g^{n}$, equation (25) becomes

$$v_C{}^{n+1} = v_C{}^{n}\left(1-\frac{T_{SW}}{R_oC}\right)+\frac{2v_{in}{}^{n-1}g^{n-1}}{Cv_C{}^{n}}\left(L_j\left(v_{in}{}^{n-1}g^{n-1}-v_{in}{}^{n}g^{n}\right)+v_{in}{}^{n}T_{SW}\right) \tag{26}$$

Since the switching frequency is much higher than the line frequency, we can assume that $v_{in}{}^{n-1}=v_{in}{}^{n}$. In addition, as illustrated in Fig. 7, the computed conductance of the whole PFC is twice the conductance of one boost cell ($G^n= 2g^n$). Hence, equation (26) results in

$$v_C{}^{n+1} = v_C{}^{n}\left(1-\frac{T_{SW}}{R_oC}\right)+\frac{\left(v_{in}{}^{n}\right)^2 G^{n-1}}{Cv_C{}^{n}}\left(L_{eq}\left(G^{n-1}-G^{n}\right)+T_{SW}\right) \tag{27}$$

where L_{eq} is the equivalent value of the parallel connection of L_1 and L_2. Since $L_1=L_2$, then L_{eq} will be given by $L_j/2$.

The previous recurrence describes the discrete-time dynamics of the output voltage when both inductor currents are in sliding mode regime.

At the equilibrium point $X_j^*=[I_{Lj}, V_C]^T$ the following assumptions are taken into account: $v_{in}{}^{n} = V_{in}$ (where V_{in} is the root mean square value of the AC input voltage), $v_C{}^{n} = v_C{}^{n+1}= V_C$ and $G^n = G^{n+1}= G$. Hence, it can be demonstrated that the equilibrium point is given by

$$X_j{}^{*} = \begin{pmatrix} I_{Lj} \\ V_C \end{pmatrix} = \begin{pmatrix} \frac{G}{2}V_{in} \\ V_{in}\sqrt{GR_o} \end{pmatrix} \tag{28}$$

5) Stability analysis of the equilibrium point

Defining

$$\Delta v_C{}^{n} = v_C{}^{n} - v_C{}^{n-1}, \tag{29}$$

introducing (28) into (27), and considering that $v_{in}{}^{n} = V_{in}$, $G^n = G^{n+1}= G$ and $V_{in}{}^2G=V_C{}^2/R_o$ because of POPI conditions, the following recurrence is obtained

$$\begin{aligned} &\Delta v_C{}^{n+1} = v_C{}^{n+1} - v_C{}^{n} = \\ &= \left(1-\frac{T_{SW}}{R_oC}\right)\Delta v_C{}^{n} + \frac{T_{SW}V_{in}^2G}{C}\left(\frac{1}{v_C{}^{n}}-\frac{1}{v_C{}^{n-1}}\right) = \\ &= \left(1-\frac{T_{SW}}{R_oC}-\frac{T_{SW}V_c^2}{R_oCv_C{}^{n}v_C{}^{n-1}}\right)\Delta v_C{}^{n} = k_1\Delta v_C{}^{n} \end{aligned} \tag{30}$$

As depicted in Fig. 11, the stability of the previous recurrence will be ensured if the following conditions are fulfilled

$$-1<1-\frac{T_{SW}}{R_oC}-\frac{T_{SW}V_c^2}{R_oCv_C{}^n v_C{}^{n-1}}<1 \tag{31}$$

From (31), the following inequality is derived

$$0<\left(\frac{T_{SW}}{R_oC}\right)\left(1+\frac{V_C{}^2}{v_c^n v_c^{n-1}}\right)<2 \tag{32}$$

Solving for T_{sw} in (32) leads to

$$0<T_{SW}<\frac{2R_oC}{1+\frac{V_C{}^2}{v_c^n v_c^{n-1}}} \tag{33}$$

Since in a boost converter both $v_C{}^n$ and $v_C{}^{n-1}$ are bigger than V_{in}, the upper bound in (33) yields

$$\frac{2R_oC}{1+\frac{V_C{}^2}{v_c^n v_c^{n-1}}}>\frac{2R_oC}{1+\frac{V_C{}^2}{V_{in}{}^2}}=\frac{2R_oC}{1+GR_o} \tag{34}$$

Therefore, a sufficient condition of stability will be given by

$$0<T_{SW}<\frac{2R_oC}{1+GR_o} \tag{35}$$

Note that the system stability depends on the switching period T_{SW}, which is limited by the load conditions. Observe also that the previous bound corresponds to the interleaved system because G represents the effective input conductance.

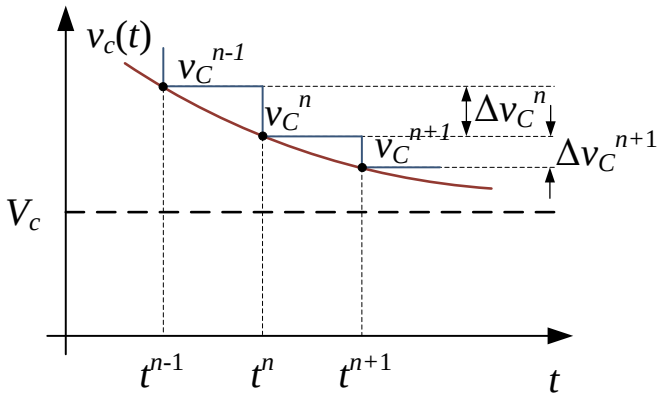


Fig. 11. Representation of $v_C(t)$ evolution towards its equilibrium point V_C in case of accomplishing stability conditions.

B. Proportional-Integral Output Voltage Control Loop

An outer control loop is added to ensure that the output voltage of the PFC system is correctly regulated. This outer control loop computes the corresponding conductance reference G^n that defines the inductor current reference $i_{L,ref}{}^n$ for the inner current control loop. Before designing this control loop in the z-plane, the conductance reference to the output voltage transfer function ($G_{GvC}(z)$) has to be calculated. This transfer function

can be obtained from the reduced order non-linear dynamics of the output voltage defined in (27). Linearizing this expression around the equilibrium point X_j^* and transforming it to the *z*-plane gives

$$G_{GvC}(z)=\frac{v_C(z)}{G(z)}=-\left(\frac{V_C L_{eq}}{R_o C}\right)\frac{\left(z-1-\frac{V_{in}{}^2 T_{SW} R_o}{V_C{}^2 L_{eq}}\right)}{z\left(z-1+\frac{2T_{SW}}{R_o C}\right)} \tag{36}$$

Note that (36) presents two poles, one of which is located in z=0. However, the other one will remain inside the unity circle if $T_{SW}<R_oC$, but this condition is already accomplished by (35). Moreover, transfer function (36) has a zero outside the unit circle, which explains the non-minimum phase characteristic of the control to output voltage transfer function in a boost converter.

The output voltage controller was designed using the nominal power operation conditions in TABLE I.

TABLE I
LIST OF PARAMETER VALUES

Parameter	Value
F_{SW}	60 kHz
L_j	620 µH
L_{eq}	310 µH
C	600 µF
V_{in}	230 V_{rms}
V_{Cref}	400 V
R_o	80 Ω

Taking into account (28) and the parameters in TABLE I, it can be observed that condition (35) is fulfilled since $T_{SW}=1/F_{SW}=16.67$ µs < 23.9 ms.

The *z*-plane transfer function of the proposed PI voltage controller was adjusted as follows

$$G_1(z)=0.0002194\cdot\frac{(z-0.999)}{(z-1)} \tag{37}$$

This compensator presents an integrator and a zero that gives sufficient phase margin to the system (Fig. 12). The proportional term has been calculated to set the cutoff frequency at approximately 9 Hz, sufficiently below the frequency of the grid voltage not to distort the input current.

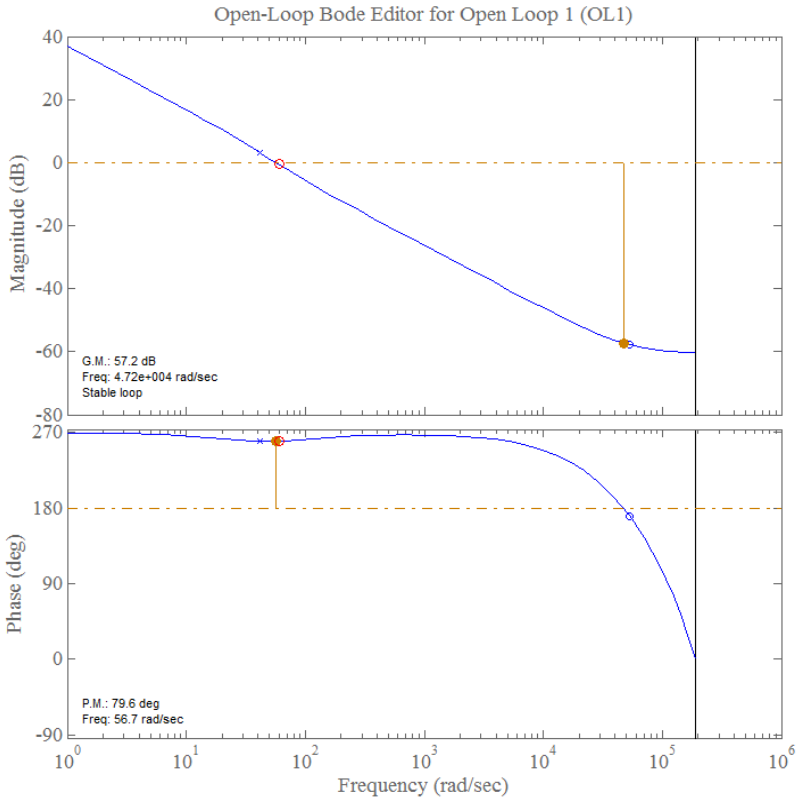


Fig. 12. Magnitude and phase of the power system gain loop.

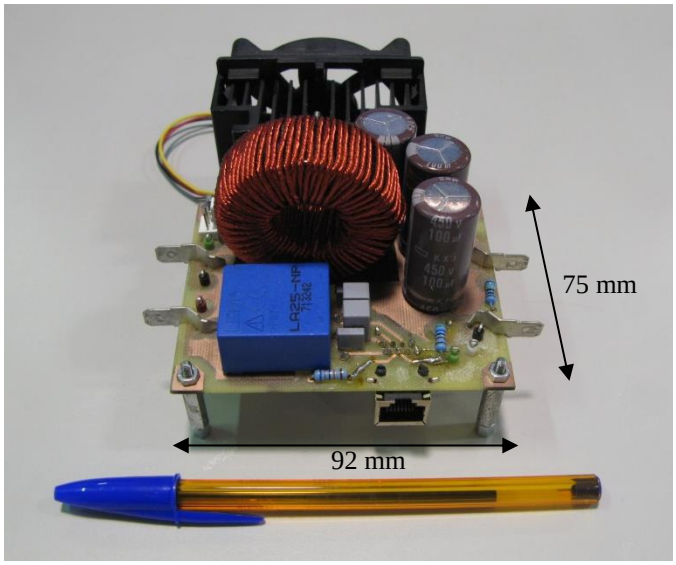
IV. NUMERICAL SIMULATIONS AND EXPERIMENTAL RESULTS

The pre-regulator was simulated using the PSIM package and implemented in an experimental modular prototype (see Fig. 13) to validate the feasibility of the proposed digital control. The prototype consists of an input filter, four regular diodes in bridge configuration and two boost converters connected in parallel. A single boost converter of 1 kW is depicted in Fig. 13.a, and the complete prototype can be observed in Fig. 13.b. The power electronic components are listed in TABLE II. The control algorithm was programmed in a TMS320F28335 Digital Signal Controller (DSC) from Texas Instruments and the switching frequency operation of each boost cell was adjusted to 60 kHz.

TABLE II
POWER ELECTRONIC COMPONENTS OF THE MODULAR PROTOTYPE

Component	Component Reference	Part # / Value	# of devices per cell	Total # of devices
EMI Input Filter	*IF*	SCHURTER 5500.2047	-	1
Regular Diode (Bridge configuration)	*DB*	STTH6004W	-	4
MOSFET	$M_{1,2}$	IPW60R160C6	1	2
SiC Diode	$D_{1,2}$	IDH10SG60C	1	2
Inductor	$L_{1,2}$	77439-A7/ 620 µH	1	2
Capacitor	$C_{1,2}$	EKXJ451ELL101MMP1S / 100 µF	3	6
MOSFET Driver	$Dr_{1,2}$	MCP1407	1	2
Current Transducer	$S_{1,2}$	LA25-NP	1	2

a)



b)

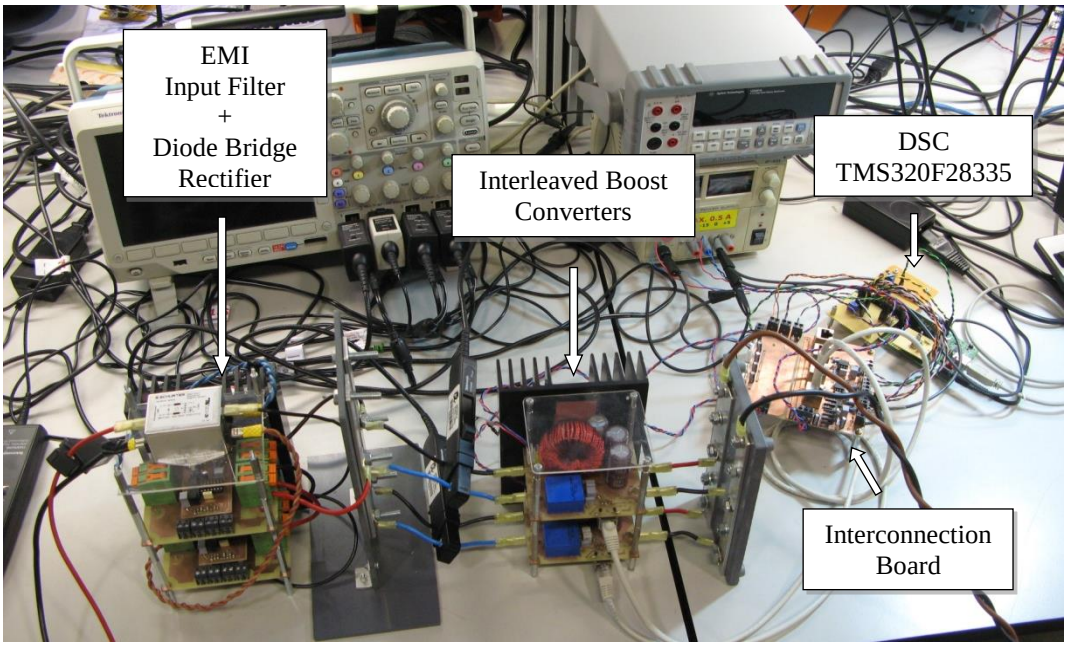
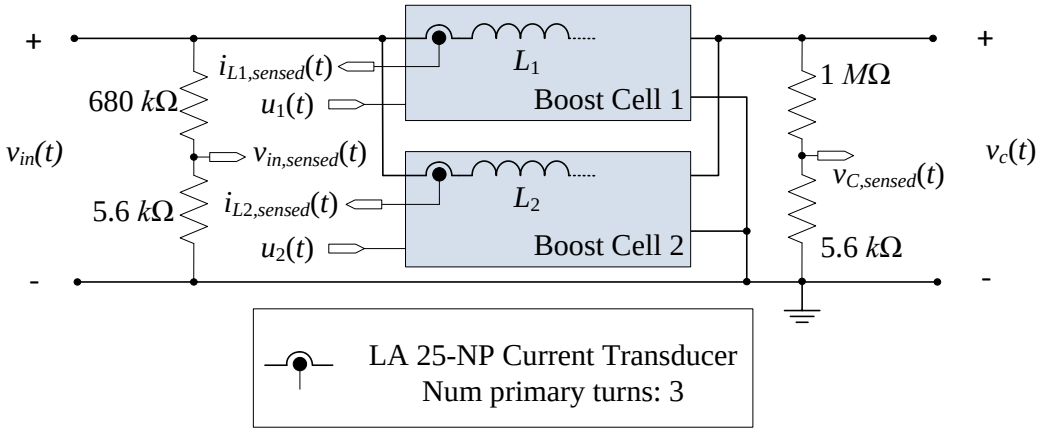


Fig. 13. a) 1 kW single-cell boost converter. b) Complete prototype.

Details about the sensing circuitry and the interconnection board are shown in Fig. 14. Sensed input and output voltage signals are obtained by two voltage dividers while both inductor currents are sensed by two LA25-NP Hall-effect current transducers with three turns in the primary winding. All sensed signals are connected to rail-to-rail operational-amplifiers (OAs) to limit the maximum voltage that can be introduced to the DSC (3.3 V). The OAs' outputs are connected to the four pins of the Analog-to-Digital Converter Input (ADCIN) of the DSC by means of 100 Ω resistors that compensate the low-impedance output of the OAs. Two output pins, managed by the Enhanced Pulse Width Modulators (EPWM) of the DSC, are used to send control signals $u_1(t)$ and $u_2(t)$ to the MOSFETs' drivers.

a)



b)

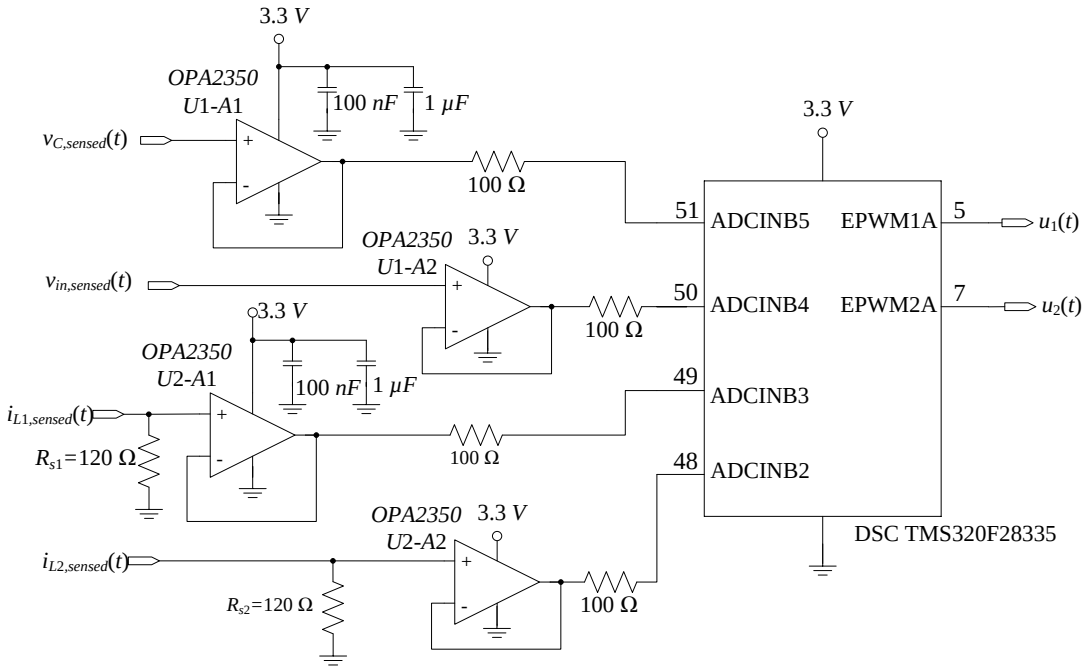


Fig. 14. a) Sensing circuitry. b) Scheme of the intermediate board and its connection to the DSC.

Figure 15 depicts the steady-state response of the system when it operates in the nominal power conditions listed in TABLE III. In particular, figure 15.a shows the PSIM simulation while Fig. 15.b illustrates the experimental results. It can be seen in both figures that input line voltage $v_{AC}(t)$ and current $i_{AC}(t)$ are in phase, so the achieved power factor is high. The resulting low frequency harmonics of the line current $i_{AC}(t)$ under these conditions are depicted in Fig. 16, which also includes the harmonics for low-input voltage. As can be seen, both cases comply with the IEC 61000-3-2 standard regulation limits for Class A equipment.

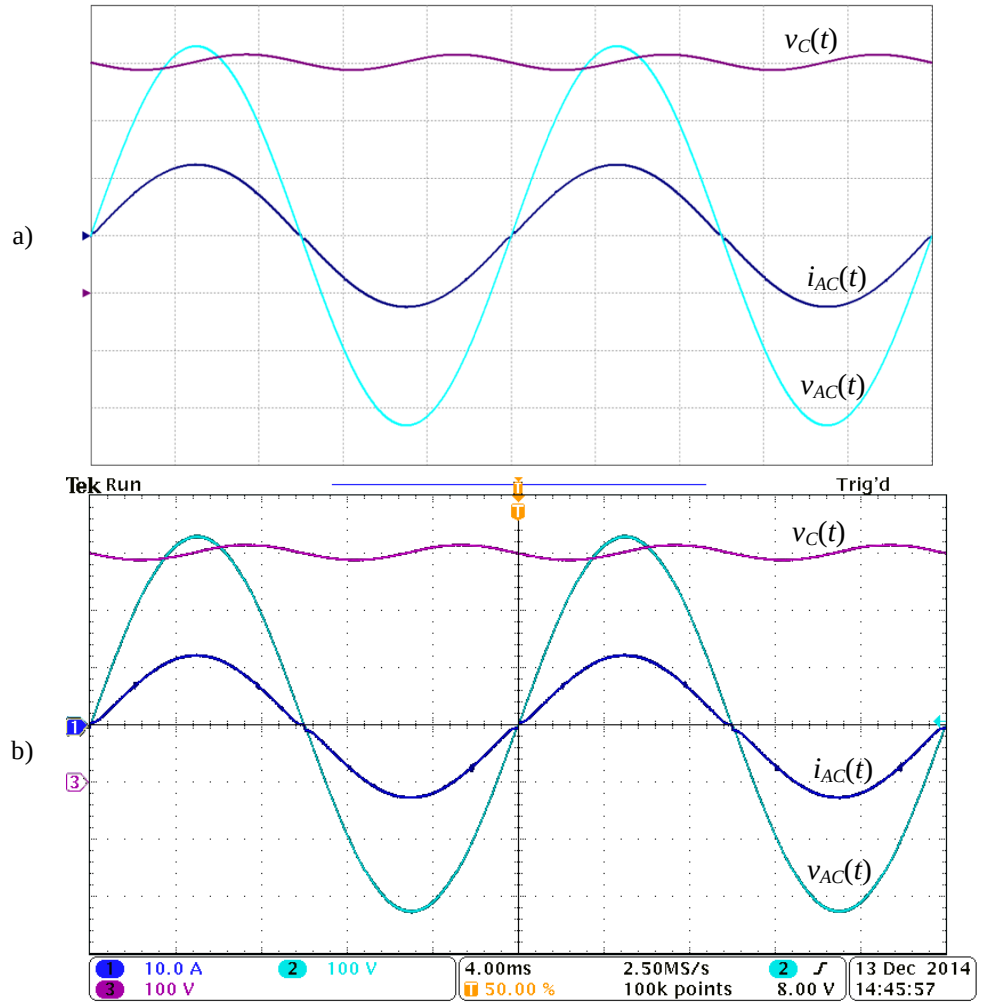


Fig. 15. Steady-state response of the pre-regulator (4 ms/div): a) simulation and b) experimental results. CH1: line current $i_{AC}(t)$ (10 A/div). CH2: line voltage $v_{AC}(t)$ (100 V/div). CH3: output capacitor voltage $v_C(t)$ (100 V/div).

TABLE III
NOMINAL POWER TEST CONDITIONS

Parameter	Symbol	Value
Line voltage	V_{AC}	230 V_{rms}
Line frequency	f_{AC}	50 Hz
Emulated input resistance	$r=1/G$	26.45 Ω
Absorbed input power	P_{in}	2 kW
Output voltage	V_C	400 V (average)
Output load	R_o	82.66 Ω

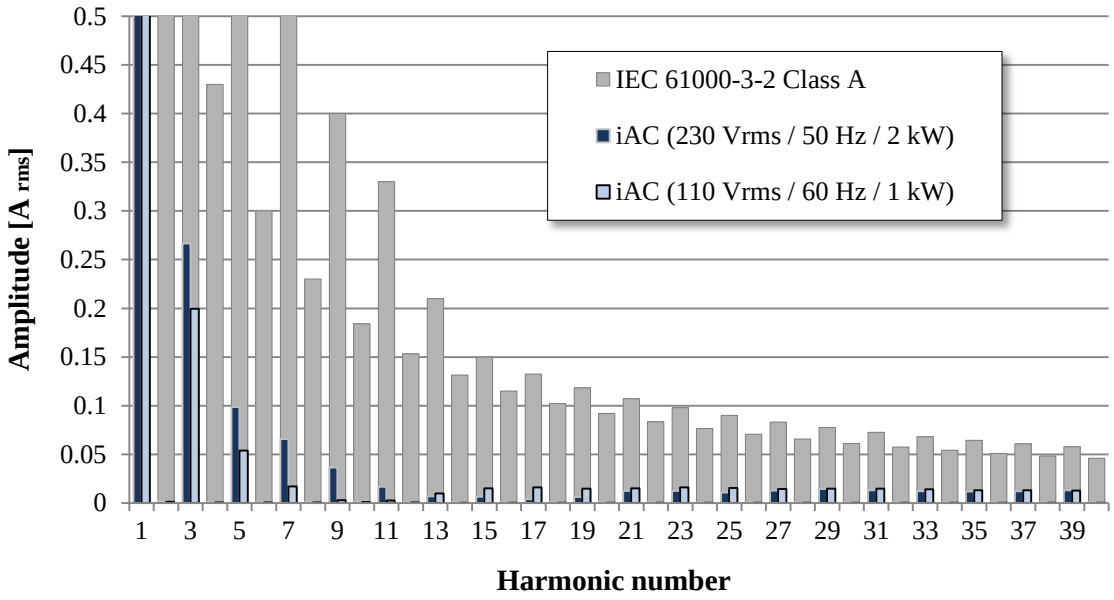
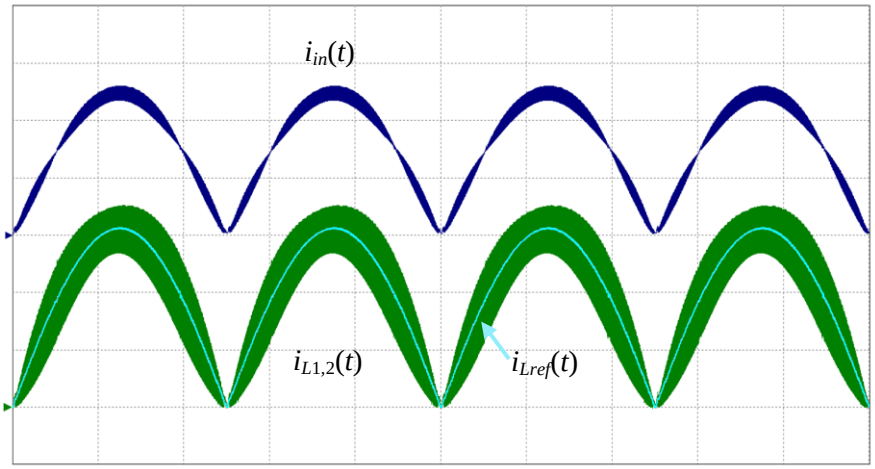


Fig. 16. Experimental low-frequency harmonic spectrum of line current $i_{AC}(t)$ under high and low-input voltage conditions satisfying IEC 61000-3-2 Class A limits.

Besides, Figs. 17.a and 17.b illustrate the perfect tracking of the current reference for both inductor currents in simulated and experimental results, respectively. Similarly, both figures show that the resulting total input current $i_{in}(t)$ has less current ripple than $i_{L1}(t)$ and $i_{L2}(t)$ due to the interleaving operation. The distortion after the zero crossing instant is produced by the parasitic drain-to-source MOSFETs' capacitances (C_{DS}), which affect the inductors' charge in this critical area. Figure 18.a shows a zoom of the simulated steady-state waveforms, and the corresponding experimental results are depicted in Fig. 18.b.

a)



b)

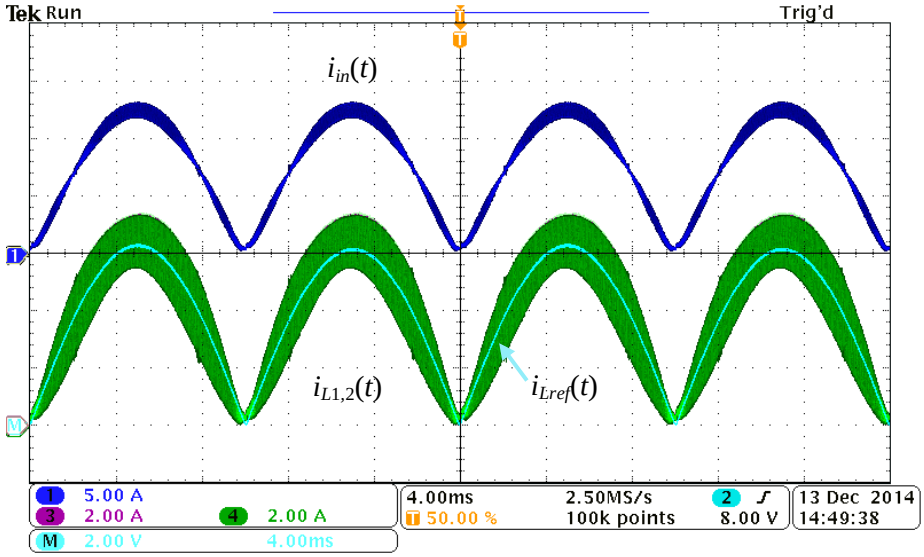
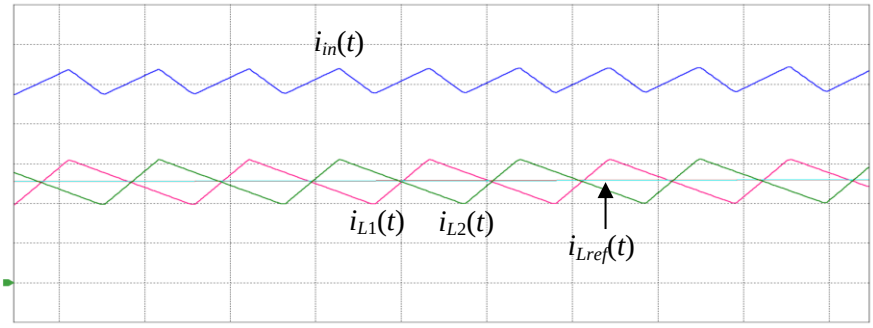


Fig. 17. Steady-state response of the pre-regulator (4 ms/div): a) simulation and b) experimental result. CH1: total input inductor currents $i_{in}(t)$ (5 A/div). CH3: inductor current $i_{L1}(t)$ (2 A/div). CH4: inductor current $i_{L2}(t)$ (2 A/div). CH Math: inductor current reference $i_{Lref}(t)$ (2 A/div).

a)



b)

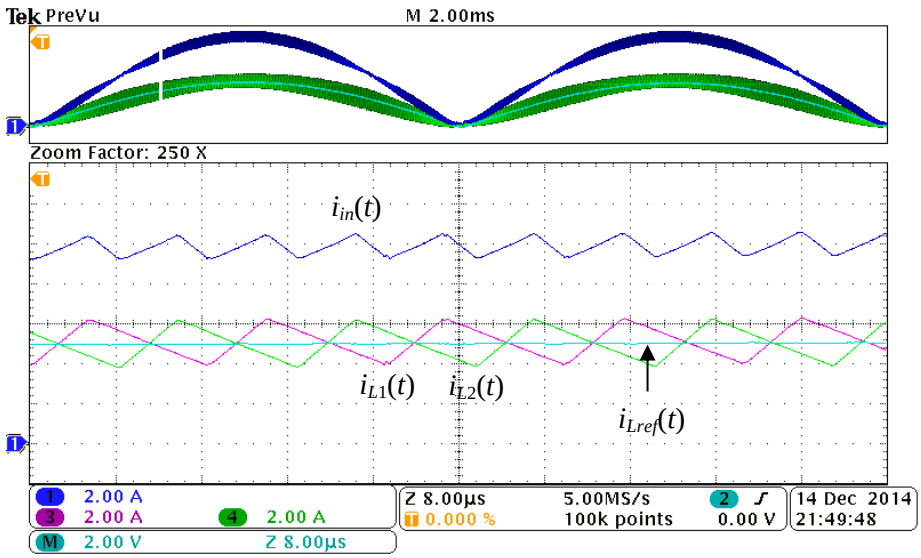
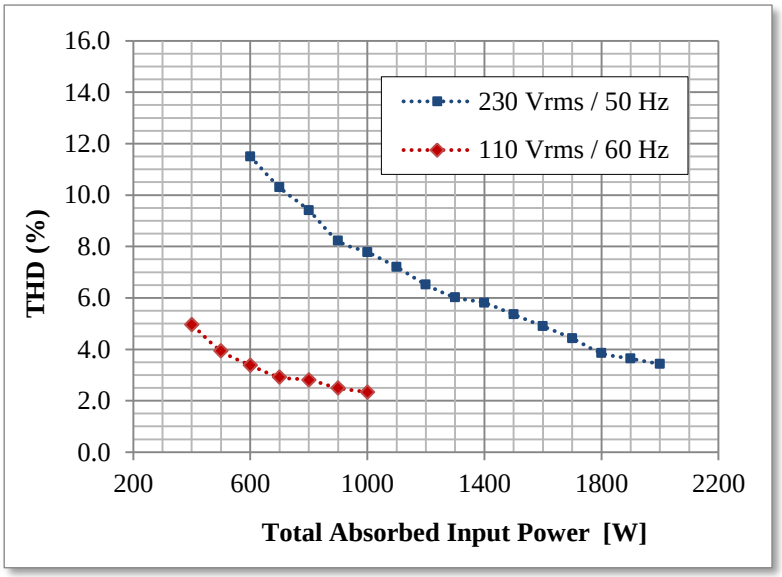


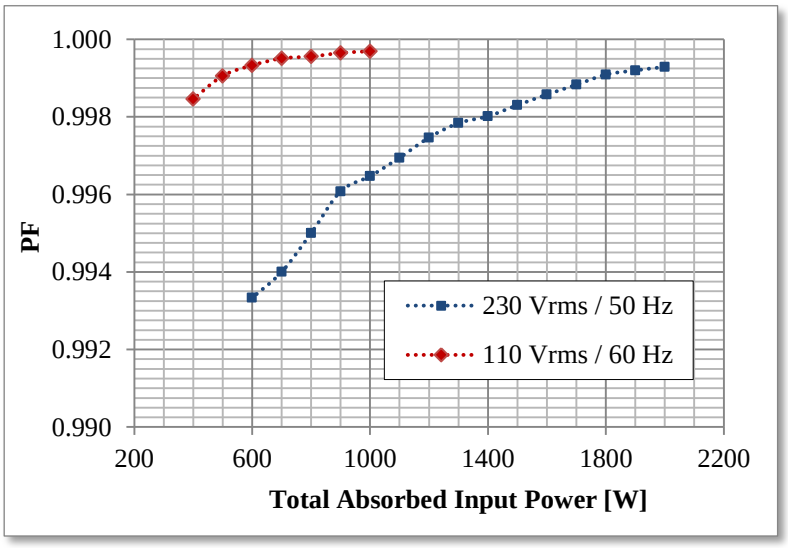
Fig. 18. Zoom of the steady-state response of the pre-regulator (8 µs/div): a) simulation and b) experimental result. CH1: total input inductor currents $i_{in}(t)$ (5 A/div). CH3: inductor current $i_{L1}(t)$ (2 A/div). CH4: inductor current $i_{L2}(t)$ (2 A/div). CH Math: inductor current reference $i_{Lref}(t)$ (2 A/div).

The Total harmonic distortion (THD), the power factor (PF) and the efficiency of the prototype, which did not take into account the power consumption of the controller or driver, were measured with a WT3000 Yokogawa Power Analyzer for different power conditions and a constant output voltage of 400 V_{DC}. Since the total input current is limited to 10 A_{rms}, the experiments were constrained to an upper bound of 1 kW for low-input voltage conditions following a procedure similar to the one reported in [46, 47]. In this context, Fig. 19 compares the THD, PF and efficiency of operating at 230 V_{rms} / 50 Hz and 110 V_{rms} / 60 Hz at approximately the same level of current. It can be observed that the prototype presents a lower THD and higher PF under low line voltage conditions because the third and fifth harmonics are reduced (see Fig. 16). However, the prototype is more efficient at high-input voltage conditions because the system deals with lower levels of current, which reduces the conduction losses.

a)



b)



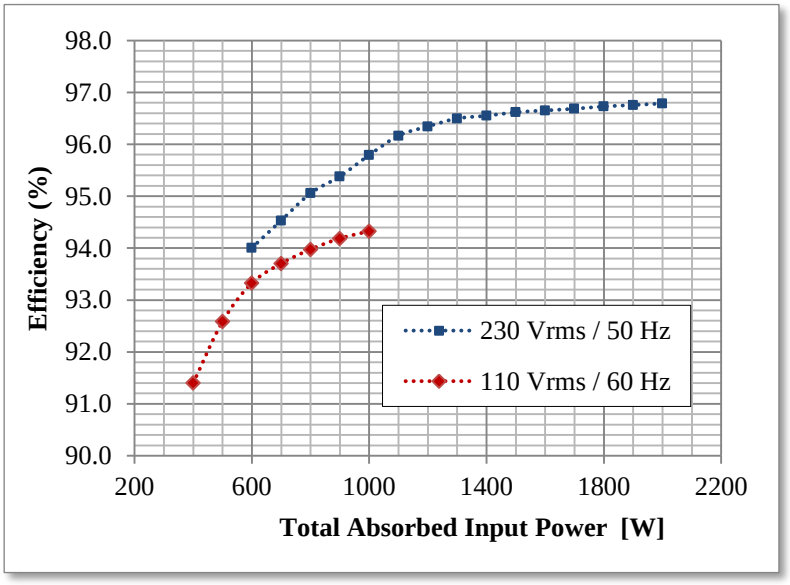
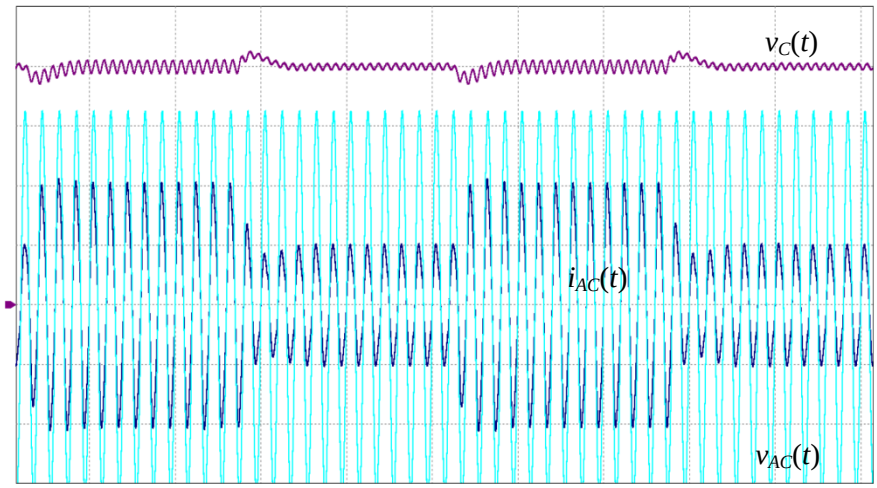


Fig. 19. Measured a) Total Harmonic Distortion (THD), b) Power Factor (PF) and c) efficiency versus total absorbed input power for high and low-input voltage.

Figs. 20.a and 20.b show the simulation and experimental results, respectively, of periodic perturbations of the output load from 100 Ω to 200 Ω every 250 ms. It can be observed that the output voltage is regulated at 400 V_{DC} as desired. The test conditions of this experiment are summarized in TABLE IV. It is worth noting that a change in the load resistance means a change in the power delivered at the output port, which, in turn, changes the power absorbed at the input port. This effect is clearly observed in Fig. 20, where it can be seen that the power system exhibits a perfect output voltage regulation together with an almost unity power factor even during the transient caused by the change of load.

a)



b)

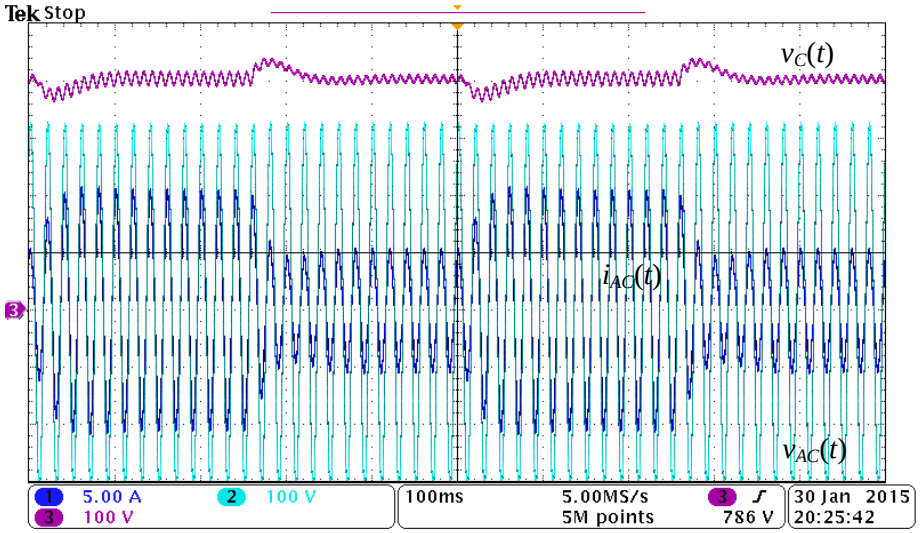


Fig. 20. Transient response of the pre-regulator to periodic perturbations of the output load (100 ms/div): a) simulation and b) experimental results. CH1: $i_{AC}(t)$ (5 A/div). CH2: $v_{AC}(t)$ (100 V/div). CH3: $v_C(t)$ (100 V/div).

TABLE IV
TEST CONDITIONS FOR OUTPUT LOAD PERTURBATIONS

Parameter	Symbol	Value
Line voltage	V_{AC}	230 V_{rms}
Line frequency	f_{AC}	50 Hz
Output voltage reference	V_{Cref}	400 V
Output load	R_{o1}	100 Ω
	R_{o2}	200 Ω
Total output power	P_{o1} (with load R_{o1})	1600 W
	P_{o2} (with load R_{o2})	800 W

V. CONCLUSIONS

This study has described a two-loop digital control that imposes resistive behavior at each input port of two interleaved boost converters. Unlike hysteretic controllers, which yield a variable switching frequency for a sliding-mode regime, the inner loop of the proposed controller induces a sliding-mode operation with constant switching frequency which facilitates the circuit's interleaving tasks. The sliding surface establishes the proportionality between the input voltage and the average input current, which eventually mitigates the third harmonic quite considerably. An outer loop consisting of a PI compensator was also designed to regulate the DC-link output voltage of the two interleaved converters to a desired reference value of 400 V.

A 2 kW prototype was simulated and implemented to demonstrate the feasibility of the proposed digital controller. Finally, TABLE V compares the proposed controller with other controllers for interleaved PFC. It shows that the controller reported in the present study exhibits one of the best PFs and one of the smallest THDs.

The proposed power system also provides one of the highest levels of power in a single module, and is only surpassed by [40] and [46]. However, the power module in [46] is analogically implemented and its PF is slightly lower, while the THD in [40] is clearly higher.

TABLE V
COMPARISON WITH OTHER CONTROLLERS FOR INTERLEAVED PFC

Controller	Type of Controller	Total Power	Input voltage [V_{rms}]	THD	PF
Proposed Controller	Digital	2 kW	230	3.43 %	0.9993
		1 kW	110	2.34 %	0.9997
[37]	Digital	600 W	110	5.4 %	0.999
[38]	Digital	600 W	220	10.4 %	0.994
[39]	Digital	460 W	110	[2.5 %, 3 %]	~ 0.995
[40]	Digital	3.5 kW	210	~ 7%	0.995
			110	-	0.998
[46]	Analog	3.4 kW	240	[3 %, 4 %]	0.996
		1.7 kW	120	~ 3%	0.992

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