# A Compact Explicit DC Model For Short Channel Gate-All-Around Junctionless MOSFETs

François Lime<sup>a,\*</sup>, Fernando Ávila-Herrera<sup>b</sup>, Antonio Cerdeira<sup>b</sup>, Benjamín Iñiguez<sup>a</sup>

<sup>a</sup>Univ. Rovira i Virgili, Department of Engineering in Electronics, Electricity and Automatic, ETSE. Av. Països Catalans, 26. 43007 Tarragona, Spain <sup>b</sup>CINVESTAV-IPN, Dep. Ingeniería Eléctrica, México D.F, Mexico

# Abstract

In this paper we provide solutions to update a long channel model in order to take into account the short channel effects. The presented model is for the junctionless GAA MOSFETs. The resulting model is analytical, explicit and valid for depletion and accumulation regimes, and consists of simple physically based equations, for better understanding of this device, and also easier implementation and better computation speed as a compact model. The agreement with TCAD simulations is very good.

Keywords: Gate-All-Around, cylindrical, MOSFET, junctionless, drain current, compact model, short channel

# 1. Introduction

To overcome the various technological challenges that arise from the continuous scaling of the MOS technology, new architectures are considered. The junctionless transistor is one of those [1, 2]. This multi-gate architecture presents the advantage of removing the need for abrupt source and drain p-n junctions, taking advantage of the very small thickness of the semiconductor film to naturally deplete the doped channel below threshold. Compared to standard junction-based inversion mode devices, it exhibits good subthreshold slope and  $I_{on}/I_{off}$  ratio, as well as similar short-channel effects [3, 4].

Compact models of junctionless devices are needed to be incorporated in circuit simulators, for future use of these devices in integrated circuits. The cylindrical Gate All Around (GAA) case is the ideal one and is sometimes closer to the real device as the fabrication process tends to round up the corners of square FinFETs, which are more easily fabricated [5, 6]. Several models were already presented for Double Gate MOSFETs (DGMOS) [7–14], FinFETs and GAA [15–19]. However, to our knowledge, very few presented a full drain current compact model for the cylindrical junctionless GAA that also takes into account the short channel effects.

The goal of this paper is to present simple modifications to the core long channel model for the GAA [20] that will allow to simulate the effects of the following short channel effects: velocity saturation, Drain Induced Barrier Lowering, series resistances, and the influence of the dopant concentration in the source and drain areas.

# 2. Long channel model

In this paper we will use the long channel model presented in [20]. In that work a simplified compact equation for the drain



Figure 1: Schematic representation of the cylindrical Gate-All-Around MOS-FET.

current was obtained, and is given below for convenience:

$$I_{ds} = 2\pi \frac{R}{L} \mu \phi_T \left( f \left( Q_m \left( 0 \right) \right) - f \left( Q_m \left( V_d \right) \right) \right)$$
(1)

with

$$\begin{split} f\left(Q\right) &= \frac{Q^2}{2Q_{eq}} + 2Q - AQ\ln\left(1 + e^{\frac{Q-Q_{dop}}{2AQ_{cp}}}\right) \\ &+ Q_{dop}\ln\left(\frac{Q-Q_{dop}}{2Q_{cp}\left(e^{\frac{Q-Q_{dop}}{2Q_{cp}}} - 1\right)}\right) \end{split}$$

and A = 1.425.

The mobile charge  $Q_m$  normalized to the channel area is obtained as follows:

$$Q_m = C_{ox}\phi_T LW\left(\frac{Q_{dop}Q_{cp}}{C_{ox}\phi_T}\frac{1 - e^{\frac{Q_{dop}-Q_m^a}{Q_{cp}}}}{Q_m^a - Q_{dop}}e^{\nu}\right)$$
(2)

with

<sup>\*</sup>Corresponding author: Tel: +34 977 25 6190; fax: +34 977 55 9605; francois.lime@urv.cat

$$Q_m^a = Q_{eq} LW\left(\frac{Q_{dop} Q_{cp}}{Q_{eq}} \frac{e^{\frac{Q_m^0}{Q_{cp}}} - e^{\frac{Q_{dop}}{Q_{cp}}}}{Q_m^{a0} - Q_{dop}} e^{\nu}\right),$$
(3)

$$Q_m^{a0} \approx 2C_{ox}\phi_T LW\left(\frac{\sqrt{Q_{cp}Q_{dop}}}{2C_{ox}\phi_T}e^{\frac{v}{2}}\right),\tag{4}$$

where LW stands for the Lambert function. The parameters are defined as  $Q_{cp} = 2\varepsilon_{sc}\phi_T/R$  and  $Q_{dop} = qN_dR/2$ ,  $C_{ox} = \varepsilon_{ox}/R\ln(1+\frac{i\alpha_x}{R})$ ,  $Q_{eq} = Q_{cp}C_{ox}\phi_T/(Q_{cp}+C_{ox}\phi_T)$ , and  $\nu = \left(\frac{V_{gs}-V_{FB}+\frac{Q_{dop}}{C_{ox}}-V}{K_{FB}}\right)/\phi_T$ ,  $V_{FB} = \phi_{ms} + \phi_T \ln(N_d/n_i)$ . The doping impurities concentration in the channel is called  $N_d$  and  $n_i$  is the intrinsic concentration.  $\phi_T = \frac{k_BT}{q}$  stands for the thermal voltage. In the above expressions, all the charges are normalized to the area of the channel.

This long channel model has a lower accuracy around the threshold voltage, for some device structure. So, we made a first modification of the model in order to have more precision in the transition region. This was accomplished by adding an additional iteration injecting (2) into a modified (3), so the final and more accurate expression of the mobile charge density  $Q_m$  is:

$$Q_m = Q_{eq} LW\left(\frac{Q_{dop}Q_{cp}}{Q_{eq}} \frac{e^{\frac{Q_m^2 - Q_{dop}}{Q_{cp}}} - 1}{Q_m^0 - Q_{dop}} \exp\left(\nu + \frac{Q_{dop}}{Q_{cp}f}\right)\right)$$
(5)

with  $f = 1 + 0.2 \frac{Q_m^0}{Q_{dop}} \exp\left(-\frac{Q_m^0}{Q_{dop}}\right)$ .

 $Q_m^0$  is given by (2). *f* and 0.2 are a fitting parameters to adjust the accuracy around the threshold voltage. Putting it to 0 will cancel the adjustment.

In the following, we explain how we modified this model to make it valid for short channel devices.

## 3. Two-dimensional electrostatics

This effect is obtained solving 2D Poisson equation in the channel. For the GAA device, we used cylindrical coordinates, see Fig. 1:

$$\frac{\partial^2 \psi}{\partial r^2} + \frac{1}{r} \frac{\partial \psi}{\partial r} + \frac{\partial^2 \psi}{\partial z^2} = \frac{q N_d}{\varepsilon_{sc}} \left( e^{\frac{\psi - V}{\phi_T}} - 1 \right) \tag{6}$$

where  $\psi(r, z)$  is the potential, and V the quasi-Fermi level. We will simplify the problem by considering that below threshold, the behavior of the device is governed by the point of minimum potential in the channel. As the current below threshold is flowing mainly at the center of the channel, we are considering r = 0 in the following.

Considering a fully depleted device and a parabolic potential along the channel thickness, equation (6) can be simplified as [21]:

$$\frac{\partial^2 \Delta \psi(0,z)}{\partial z^2} = \frac{\Delta \psi(0,z)}{\lambda^2}$$
(7)

with the characteristic length  $\lambda = R \sqrt{\frac{C_{si}}{2C_{ox}} + \frac{1}{4}}$ ,  $C_{si} = \frac{\varepsilon_{sc}}{R}$  and  $\Delta \psi(0, z) = \psi(0, z) - \psi^{lc}(0, z)$ . The potential  $\psi^{lc}(0, z)$  is the potential in the channel for the long channel case, at r = 0.

Considering that  $\Delta \psi_S = \Delta \psi (0, 0)$  is the barrier height at the source side of the channel, and  $\Delta \psi_D = \Delta \psi (0, L)$  the one at the drain side, Eq. (7) has the following solution [22]:

$$\Delta\phi(z) = \frac{\Delta\psi_D \sinh\left(\frac{z}{\lambda}\right) + \Delta\psi_S \sinh\left(\frac{L-z}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \tag{8}$$

The maximum value of this function gives the position of the top of the barrier as:

$$z_{max} = \frac{L}{2} - \frac{\lambda}{2} \ln \left( \frac{\Delta \psi_D - \Delta \psi_S e^{-\frac{L}{\lambda}}}{\Delta \psi_S - \Delta \psi_D e^{-\frac{L}{\lambda}}} \right)$$
(9)

So the change in the threshold voltage of the device  $\Delta V_T = \Delta \phi (z_{max})$  due to the DIBL effect is:

$$\Delta V_T = \frac{\sqrt{\Delta \psi_S e^{\frac{L}{\lambda}} - \Delta \psi_D} \sqrt{\Delta \psi_D - \Delta \psi_S e^{-\frac{L}{\lambda}}}}{\sinh\left(\frac{L}{\lambda}\right)}$$
(10)

The boundary conditions are as follow:

$$\Delta \psi_S = V_{bs} - \varphi_0^{lc} \tag{11}$$

$$\Delta \psi_D = V_{bd} - \varphi_0^{lc} + V_d \tag{12}$$

 $\varphi_0^{lc} = V_g - V_T$  is the long channel value of the potential at the center of the channel, with the threshold voltage  $V_T = V_{fb} - \frac{qN_DR}{4} \left(\frac{R}{\epsilon_{sc}} + \frac{2}{C_{os}}\right)$ .  $V_{bs}$  and  $V_{bd}$  are the effective potential barrier height at the source and drain end of the channel as explained in section 3.1.

It is possible to express (10) in a more physical way, in order to solve the problem that (10) cannot be evaluated outside the subthreshold regime where it is not valid. Considering that the DIBL and subthreshold slope degradation come from a capacitive coupling between the source and drain regions and the virtual cathode,  $C_S$  and  $C_D$ , and that  $\Delta \psi_S$  and  $\Delta \psi_D$  for long and short channels are mostly the same, we can approximate and rewrite (10) as:

$$\Delta V_T = \frac{C_S \Delta \psi_S + C_D \Delta \psi_D}{C_{eq}},\tag{13}$$

with  $\frac{1}{C_{eq}} = \frac{1}{C_{ox}} + \frac{1}{2C_{si}}$ ,  $C_{eq}$  being an equivalent gate capacitance, as seen by the center of the channel, in depletion.

We can obtain an expression for the coupling with the drain as  $C_D = C_{eq} \frac{\partial \Delta V_T}{\partial V_a}$ :

$$C_D = C_{eq} \frac{\Delta \psi_S \cosh\left(\frac{L}{\lambda}\right) - \Delta \psi_D}{\sinh\left(\frac{L}{\lambda}\right) \sqrt{2\Delta \psi_S \Delta \psi_D \cosh\left(\frac{L}{\lambda}\right) - \Delta \psi_S^2 - \Delta \psi_D^2}} \quad (14)$$

Similarly, we can obtain the capacitive coupling with the source as:

$$C_{S} = C_{eq} \frac{\Delta \psi_{D} \cosh\left(\frac{L}{\lambda}\right) - \Delta \psi_{S}}{\sinh\left(\frac{L}{\lambda}\right) \sqrt{2\Delta \psi_{S} \Delta \psi_{D} \cosh\left(\frac{L}{\lambda}\right) - \Delta \psi_{S}^{2} - \Delta \psi_{D}^{2}}$$
(15)

The interest of doing this is that, in (13),  $C_S$  and  $C_D$  vary much slower with  $V_g$  than  $\Delta \psi_S$  and  $\Delta \psi_D$ , so they can be evaluated at a constant gate voltage value below threshold  $V_g^0$ . Changing the value of  $V_g^0$  will not change much the results as long as  $V_g^0$  remains below threshold. For this junctionless device we used the following value:  $V_g^0 = -\frac{qN_DR^2}{4\epsilon_{sc}}$ . We observed that the DIBL and subthreshold slope degradation can be modeled with excellent accuracy considering only the  $V_g$  and  $V_d$  dependence of  $\Delta \psi_S$  and  $\Delta \psi_D$  in (13).

## 3.1. Effective potential barrier at source and drain

Although junctionless devices are supposed to have the same dopant concentration in source and drain as in the channel regions, in fact it might be desirable to have a higher doping to reduce the effect of series resistance. Indeed, a low doping concentration  $N_{SD}$  in the source an drain regions will alter the effective potential barrier at source and drain end of the channel  $V_{bs}$  and  $V_{bd}$ . Ideally, these should be respectively equal to  $V_{bi}$ and  $V_{bi} + V_d$  but are lower in reality. This effect can be modeled as in [23]. In our model, we considered the built-in voltage  $V_{bi}$ of the source drain junctions as a fitting parameter. From [23]:

$$V_{bd} = V_{bi} - \Delta \psi_D^b - \frac{q N_{SD} \lambda}{\varepsilon_{sc}} \left( 1 - \sqrt{1 + 2\varepsilon_{sc} \frac{\Delta \psi_D^b}{q N_{SD} \lambda}} \right) \quad (16)$$

 $\Delta \psi_D^b$  is similar to (12):

$$\Delta \psi_D^b = \phi_T \ln\left(1 + \exp\left(\frac{V_{bi} - \varphi_0^{lc} + V_d}{\phi_T}\right)\right) \tag{17}$$

where  $V_{bi}$  is the equivalent of the built-in voltage of the junction based devices. The function  $\ln (1 + e^x)$  was used to avoid having  $\Delta \psi_D^b < 0$  above threshold. In order to take into account the source and drain doping concentration,  $V_{bi}$  was explicitly written as a function of  $N_{SD}$ :

$$V_{bi} = V_{bi0} - \varphi_F + \phi_T \ln\left(\frac{N_{SD}}{N_d}\right)$$
(18)

where  $\varphi_F = \phi_T \ln \left(\frac{N_d}{n_i}\right)$  is the Fermi voltage in the channel.  $V_{bi0}$  is the barrier height relatively to the intrinsic level at the source side of the channel. It is considered a fitting parameter.  $\varphi_F$  appears here to change the origin of potentials to the intrinsic level at the source side of the channel.

In the same way,  $V_{bs}$  is obtained from (16) considering  $V_d = 0$ .

## 3.2. Incorporation into the long channel model

In this paragraph we also want to ensure that the DIBL expressions previously obtained properly vanish outside the depletion regime. The DIBL effect is included in the long channel model by replacing the v parameter in (2), (3) and (4) with  $v_{dibl}$ :

$$v_{dibl} = v + \frac{C_S^* \Delta \psi_S^* + C_D^* \Delta \psi_D^*}{C_{eq} \phi_T}$$
(19)

with

$$C_{S(D)}^{*} = C_{S(D)} \frac{2 \exp\left(-\frac{Q_m(0)}{\gamma Q_{dop}}\right)}{1 + \exp\left(-\frac{Q_m(0)}{\gamma Q_{dop}}\right)}$$
(20)

 $C_{S(D)}^*$  is in fact  $C_{S(D)}$  multiplied by a screening function, in order to cancel the capacitive coupling above threshold.  $Q_m$  was obtained from the long channel model as defined in (2) and (1) and the parameter  $\gamma$  adjust the smoothness of the transition. We chose  $\gamma = 3.33$ .

In addition, we used the following smoothing function  $\Delta \psi_{S(D)}^* = \phi_T \ln \left(1 + \exp\left(\frac{\Delta \psi_{S(D)}}{\phi_T}\right)\right)$  so that  $\Delta \psi_{S(D)}^*$  do not become negative and cancels to 0 above threshold.

# 4. Modeling of velocity saturation

The velocity saturation was modeled in a similar manner as in [22]. The effects of the velocity saturation on the carrier mobility was described using an effective mobility  $\mu_{eff}$ :

$$\mu_{eff} = \frac{\mu}{\left(1 + \left(\frac{\mu V_{deff}}{v_{sal}(L - \Delta L)}\right)^{\alpha}\right)^{\frac{1}{\alpha}}}$$
(21)

where  $\alpha = 2$  for electrons. For electrons, it can be shown [22, 24] that the saturation voltage can then be obtained as:

$$V_{sat} = \frac{V_s}{\frac{V_s}{V_{max}} + 1}$$
(22)

with  $V_s = \frac{Q_m(0)}{C_{ox}} + \frac{V_{max}}{\frac{V_{max}}{V_{min}} - 1}$ .

We considered a maximum saturation voltage  $V_{max}$  for the drain current, as well as a minimum one below threshold  $V_{min}$ , for numerical reasons. The second term in  $V_s$  corresponds to the classical MOSFET saturation voltage  $V_g - V_T \approx Q_m(0) / C_{ox}$  plus a correction factor to ensure that  $V_{sat}$  will tend to the aforementioned minimal value below threshold. It should be negligible above threshold.  $Q_m$  is the mobile charge density per unit area, given by the long channel model, as the velocity saturation should mainly affects the characteristics above threshold. Considering electron carriers, the maximum and minimum values of the saturation voltage are given as [22]:

$$V_{max} = \alpha \frac{v_{sat}}{\mu} L \tag{23}$$

$$V_{min} = 2\phi_T \tag{24}$$

where  $v_{sat}$  the saturation velocity,  $\mu$  the mobility and *L* is the channel length of the device. We observed that the value of  $V_{min}$  has a low impact on the characteristics of the device. It can then be considered as a fitting parameter.

This effect is included in the core long channel model by substituting the drain voltage  $V_d$  with an effective drain voltage  $V_{deff}$  that saturates at the saturation voltage  $V_{sat}$ . We used the following smoothing function [25]:

$$V_{deff} = V_{sat} - V_{sat} \frac{\ln\left(1 + \exp\left(A\left(1 - \frac{V_d}{V_{sat}}\right)\right)\right)}{\ln\left(1 + \exp\left(A\right)\right)}$$
(25)

where A is a smoothing parameter to ensure a smooth transition from  $V_d$  to its maximum value  $V_{sat}$ . We took A = 3.

The effective reduction in channel length  $\Delta L$  due to the pinch-off effect was obtained by a quasi 2D solving of Poisson equation (6) in the saturation region. In the same way as for the DIBL, considering a parabolic potential, we obtained the same equation as (7), but for the surface potential (r = R):

$$\frac{\partial^2 \left(\psi\left(R,z\right) - \psi\left(R,L - \Delta L\right)\right)}{\partial z^2} = \frac{\psi\left(R,z\right) - \psi\left(R,L - \Delta L\right)}{\lambda^2} \quad (26)$$

with  $\lambda = R \sqrt{\frac{C_{si}}{2C_{ox}}}$ .

Equation (26) is then solved considering that

$$\frac{\partial \psi(R,z)}{\partial z}\Big|_{z=L-\Delta L} = \alpha \frac{v_{sat}}{\mu}$$
(27)

The solution is:

$$\psi(R,z) - \psi(R,L - \Delta L) = \alpha \frac{v_{sat}}{\mu} \lambda \sinh\left(\frac{L - \Delta L - z}{\lambda}\right)$$

Considering that  $\psi(R, L) - \psi(R, L - \Delta L) = V_d - V_{deff}$ , we can obtain  $\Delta L$  [26]:

$$\Delta L = \lambda \ln \left( \frac{\left( V_d - V_{deff} \right) \left( 1 + \sqrt{1 + \left( \frac{\alpha^{\frac{v_{sat}}{\mu}} \lambda}{V_d - V_{deff}} \right)^2} \right)}{\alpha^{\frac{v_{sat}}{\mu}} \lambda} \right) S \qquad (28)$$

The parameter S was added to make  $\Delta L$  tend to 0 below the threshold voltage:

$$S = \sqrt{1 - \frac{1}{1 + \beta \frac{Q_m(0)}{C_{eq}\phi_T}}}$$
(29)

where  $Q_m(0)$  is the mobile charge at the source, given by the long channel model. The parameter  $\beta$  is for adjusting the smoothness of the transition.

Then, the effect of velocity saturation is incorporated in the drain current expression (1), replacing L by  $L - \Delta L$ , and  $\mu$  by  $\mu_{eff}$ .

## 4.1. Series resistance

The electrical resistance  $R_{SD}$  of the source and drain regions will degrade the drain current  $I_{ds}$  above threshold. As a first approximation, its effects can be incorporated in the effective mobility or in the drain current as a function of the drain current without series resistance  $I_{ds0}$  [22, 27]:

$$I_{ds} = \frac{I_{ds0}}{1 + 2\pi \frac{R}{L} \mu_{eff} R_{SD} \left( Q_m(0) - n \left( Q_m(0) - Q_m \left( V_{deff} \right) \right) \right)}$$
(30)

with  $I_{ds0}$  given by (1). The parameter *n* is a fine tunning parameter to take into account the  $V_d$  dependence of the series resistance.  $Q_m(0)$  and  $Q_m(V_{deff})$  are respectively the long channel mobile charges at the source and drain side (pinch-off point) of the channel.



Figure 2:  $I_d(V_g)$  characteristics in logarithmic and linear scale for a short channel Junctionless GAA MOSFET. Lines = model, Symbols=TCAD.



Figure 3:  $I_d(V_d)$  characteristics for a short channel GAA Junctionless MOS-FET. Lines = model, Symbols=TCAD.

#### 5. Results and discussion

The model was validated with TCAD simulations (SILVACO-ATLAS). All the figures present the analytical solution of the model against TCAD simulations. A constant mobility of 100 cm<sup>2</sup>/Vs was considered in order to avoid the use of additional fitting parameters, with the *fldmob* model of ATLAS for the longitudinal dependence of the mobility. A p-type gate was chosen in order to have the highest threshold voltage possible. In fact, the energy difference between the Fermi level of the gate and the intrinsic level of the channel was chosen to be 0.55 eV. The model used the same physical constants values as the TCAD simulator except for the saturation velocity. Indeed, because of the approximations we made to obtain an analytical expression for the saturation voltage  $V_{sat}$ , the velocity saturation has to be considered a fitting parameter: a good agreement with TCAD was found for  $v_{sat} = 2x10^7$  cm/s instead of  $10^7$  cm/s. The simulated structure is shown in Fig. 1. Two silicon radius were used, 10 and 7.5 nm. With typical equivalent oxide thickness,



Figure 4: Dependence on the source and drain doping  $N_{SD}$  of the  $I_d(V_g)$  characteristics. Lines = model, Symbols=TCAD.



Figure 5:  $I_d(V_g)$  characteristics in linear and logarithmic scale for various gate lengths *L* at constant source and drain extensions length  $L_{SD}$ . Lines = model, Symbols=TCAD.

 $t_{ox} = 2$  nm and source/drain extension lengths  $L_{sd}$  of 10 nm. The channel length was scaled down from 30 to 15 nm. Also, structures with  $N_{sd} \ge N_d$  were considered. For the fitting parameters, we used A = 3,  $\gamma = 3.33$ ,  $\beta = 0.25$ . A  $V_{bi0}$  value of 0.6 V was found to give the best results for most of the devices.

Fig.2 and 3 show respectively the transfer and output characteristics. Above threshold, the current characteristics have a decreased drain current due to the combined effects of velocity saturation and series resistances. It can be seen that these effects are correctly accounted for by the model. Below threshold, for low source and drain concentrations, the DIBL effect is reduced due to the effective potential barrier that depends on the source and drain doping level. This effect is illustrated in Fig. 4, that shows the transfer characteristics at  $V_d = 1V$ , for various doping concentration  $N_{SD}$  of the source and drain areas.

In Fig. 4, the variation above threshold is due to  $R_s$  and the velocity saturation, while below threshold, to the effective po-



Figure 6:  $g_d(V_{ds})$  characteristics in logarithmic scale for various  $V_{gs}$ . Lines = model, Symbols=TCAD.



Figure 7:  $g_m(V_{gs})$  characteristics for various  $V_{ds}$ . Lines = model, Symbols=TCAD.

tential barrier. The series resistance  $R_s$  depends of the length of the extensions  $L_{sd}$  as well as its doping level  $N_{sd}$ , so increasing  $N_{sd}$  decreases  $R_s$ , which increases the values of  $I_{ds}$  above threshold where the influence of  $R_s$  is the most important. Below threshold, low values of  $N_{sd}$  means that the potential barrier of the channel will not start at the edges of the channel but inside the source and drain extensions. This in turn will decrease the magnitude of the DIBL, as shown in [23].

Overall, the agreement with TCAD simulations is very good, except for low  $N_{SD}$  at high  $V_{gs}$  values, where the model starts to overestimate the current above  $V_{gs} = 1.5V$ . This discrepancy is due to an effect that is not taken into account by the model, as explained in [28]. In [28], it is said that the mismatch comes from an anomalous distribution of the potential in the source extension, when the gate voltage is superior to 2 V. This phenomenon has not been modeled because the GAA is not supposed to work at such high gate voltage values, so there is little interest in doing it. It can also be seen in Fig. 7. Fig. 5 shows the transfer characteristics for various gate length *L*. The extensions length was kept constant at  $L_{SD} = 10 \text{ nm}$ , so there should be a decreasing influence of the series resistance with the gate length. We can see that the agreement with TCAD is good. For the shortest gate length L = 15 nm, there is a small change of slope in the transition region between sub and above threshold. As it can be seen, this only occurs when the DIBL is very high and is due to the smoothing function (29). This can be improved by adjusting the value of  $\beta$ , but in Fig. 5 we chose to keep it constant for the various gate lengths. Due to the simplifications that were made i.e. the use of a characteristic length, the model should not be valid for very high DIBL, but devices with high DIBL are not practical.

The first derivatives of the current are shown in Fig. 6 and 7. Fig. 6 shows the derivative of the current  $g_d$  for various gate voltages. Again, the agreement with the simulations is very good. In Fig. 7 is shown the derivative of the current  $g_m$  for low and high drain voltages. The agreement is good but again we can see that the model start to diverge from TCAD at high gate and drain voltage, for the reasons explained above.

We also checked (not shown) that the model is continuous at  $V_{ds} = 0$  at least until the third derivative of the current and that our model is in accordance with the simulated GAA of [6].

### 6. Conclusion

We developed an explicit analytical model for short channel Gate-All-Around Junctionless MOSFETs by extending the range of validity of a long channel core model. The modifications to the core model presented in this paper could also be applied to other long channel models.

The complete formulation shares the characteristics of its core model and, as such, presents the advantages of being analytical, explicit, as well as very compact and simple, which makes the model suitable for implementation in design tools. The agreement with TCAD simulations is very good.

# Acknowledgements

This work is supported by the ICREA Academia 2013 from ICREA Institute and the Spanish Ministry of Economy and Competitiveness through project GREENSENSE (TEC2015-67883-R).

#### References

- J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, R. Murphy, Nanowire transistors without junctions, Nat. Nanotechnol. 5 (3) (2010) 225–229.
- [2] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, J. P. Colinge, Junction-less multigate field-effect transistor, Appl. Phys. Lett. 94 (2009) 053511.
- [3] C. W. Lee, I. Ferain, A. Azfalian, R. Yan, N. D. Akhavan, P. Razavi, J. P. Colinge, Performance estimation of junctionless multigate transistors, Solid-State Electronics 54 (2010) 97–103.
- [4] J. P. Colinge, A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Rasavi, Junctionless Nanowire Transistor (JNT): Properties and design guidelines, Solid-State Electronics 65 (2011) 33–37.

- [5] T.-Y. Liu, F.-M. Pan, J.-T. Sheu, Characteristics of Gate-All-Around Junctionless Polysilicon Nanowire Transistors With Twin 20-nm Gates, IEEE Journal of the Electron Devices Society 30 (5) (2015) 405–409.
- [6] D.-I. Moon, S.-J. Choi, J. P. Duarte, Y.-K. Choi, Investigation of Silicon Nanowire Gate-All-Around Junctionless Transistors Built on a Bulk Substrate, IEEE Trans. Electron Dev. 60 (4) (2013) 1355–1360.
- [7] F. Lime, E. Santana, B. Iñiguez, A simple compact model for longchannel junctionless Double Gate MOSFETs, Solid-State Electronics 80 (2013) 28–32.
- [8] J. M. Sallese, N. Chevillon, C. Lallement, B. Iñiguez, F. Prégaldiny, Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors, IEEE Trans. Electron Dev. 58 (8) (2011) 2628–37.
- [9] J. P. Duarte, S. J. Choi, Y. K. Choi, A Full-Range Drain Current Model for Double-Gate Junctionless Transistors, IEEE Trans. Electron Dev. 58 (2011) 4219–4225.
- [10] J. P. Duarte, S. J. Choi, D. I. Moon, Y. K. Choi, Simple analytical bulk current model for long-channel double-gate junctionless transistors, IEEE Electron Device Lett. 32 (2011) 704–706.
- [11] T. Holtij, M. Graef, F. M. Hain, A. Kloes, B. Iñiguez, Compact Model for Short-Channel Junctionless Accumulation Mode Double Gate MOS-FETs, IEEE Trans. Electron Dev. 61 (2014) 288–299.
- [12] A. Cerdeira, M. Estrada, B. Iniguez, R. Trevisoli, R. Doria, M. de Souza, M. Pavanello, Charge-based continuous model for long-channel Symmetric Double-Gate Junctionless Transistors, Solid-State Electronics 85 (2013) 59–63.
- [13] F. Ávila, A. Cerdeira, B. Paz, M. Estrada, B. Iñiguez, M. Pavanello, Compact model for short-channel symmetric double-gate junctionless transistors, Solid-State Electronics 111 (2015) 196–203.
- [14] B. Paz, F. Ávila Herrera, A. Cerdeira, M. Pavanello, Double-gate junctionless transistor model including short-channel effects, Semicond. Sci. Technol. 30 (2015) 055011.
- [15] E. Gnani, A. Gnudi, S. Reggiani, G. Baccarani, Theory of the Junctionless Nanowire FET, IEEE Trans. Electron Dev. 58 (9) (2011) 2903–2910.
- [16] J. Duarte, S.-J. Choi, D.-I. Moon, Y.-K. Choi, A Nonpiecewise Model for Long-Channel Junctionless Cylindrical Nanowire FETs, IEEE Electron Device Lett. 33 (2) (2012) 155–157.
- [17] T.-K. Chiang, A New Quasi-2-D Threshold Voltage Model for Short-Channel Junctionless Cylindrical Surrounding Gate (JLCSG) MOSFETs, IEEE Trans. Electron Dev. 59 (11) (2012) 3127–3129.
- [18] F. Ávila, B. Paz, A. Cerdeira, M. Estrada, M. Pavanello, Charge-based compact analytical model for triple-gate junctionless nanowire transistors, Solid-State Electronics 122 (2016) 23–31.
- [19] R. Trevisoli, R. Doria, M. de Souza, M. Pavanello, Drain Current and Short Channel Effects Modeling in Junctionless Nanowire Transistors, Journal of Integrated Circuits and Systems 8 (2) (2013) 116–124.
- [20] F. Lime, O. Moldovan, B. Iniguez, A Compact Explicit Model for Long-Channel Gate-All-Around Junctionless MOSFETs. Part I: DC Characteristics, IEEE Trans. Electron Dev. 61 (9) (2014) 3036–3041.
- [21] C. P. Auth, J. D. Plummer, Scaling Theory for Cylindrical, Fully-Depleted, Surrounding-Gate MOSFET's, IEEE Electron Device Lett. 18 (2) (1997) 74–76.
- [22] F. Lime, O. Moldovan, B. Iñiguez, A quasi-two-dimensional compact drain-current model for undoped symmetric double-gate MOSFETs including short-channel effects, IEEE Trans. Electron Dev. 55 (2008) 1441– 1448.
- [23] T. Dutta, Q. Rafhay, G. Pananakakis, G. Ghibaudo, Modeling of the Impact of Source/Drain regions on Short Channel Effects in MOSFETs, in: Proceedings of 14<sup>th</sup> International Conference on Ultimate Integration on Silicon (ULIS 2013), 2013, pp. 69–72.
- [24] B. Iñiguez, E. Moreno, An Improved C<sub>∞</sub>-Continuous Small-Geometry MOSFET Modeling for Analog Applications, Analog Integrated Circuits and Signal Processing 13 (1997) 241–259.
- [25] C. C. McAndrews, B. K. Bhattacharyva, O. Wing, A single-piece C<sub>∞</sub>continuous MOSFET model including subthreshold conduction, IEEE Electron Device Lett. 12 (10) (1991) 565–567.
- [26] S. Veeraraghavan, J. Fossum, A physical short-channel model for the thinfilm SOI MOSFET applicable to device and circuit CAD, IEEE Trans. Electron Dev. 35 (11) (1988) 1866–1875.
- [27] A. Cerdeira, F. Ávila, B. Iñiguez, M. de Souza, M. Pavanello, M. Estrada, Compact core model for Symmetric Double-Gate Junctionless Transistors, Solid-State Electronics 95 (2014) 91–97.

# ©2017 This manuscript version is made available under the CC-BY-NC-ND 4.0 license. See the DOI for the published version

[28] A. Cerdeira, F. Ávila Herrera, B. Cardoso Paz, M. Estrada, M. Antonio Pavanello, Role of the extensions in Double-Gate Junctionless MOSFETs in the drain current at high gate voltage, in: Proceedings of the 30<sup>th</sup> Symposium on Microelectronics Technology and Devices (SBMicro) 2015, IEEE, 2015, pp. 1–4.