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Discrete-time sliding-mode based digital PWM control of a boost converter

Enric Vidal-Idiarte[1], Adria Marcos-Pastor[1], Germain Garcia[2], Angel Cid-Pastor[1], Luis Martinez-Salamero[1]

[1]Departament d'Enginyeria Electrònica,Elèctrica i Automàtica, Universitat Rovira i Virgili, Tarragona, SPAIN.

[2]Laboratoire d'Analyse et d'Architecture des Systemes du CNRS (LAAS-CNRS), Toulouse, FRANCE.

E-mail: enric.vidal@urv.cat

Abstract: In this work a non -linear digital control of a boost converter based on a sliding discrete-time approximation is presented. The control strategy follows a classical cascade regulation scheme with the inner loop consisting in a non linear current-control based on discrete-time sliding mode, and the outer one being composed of a simple discrete-time PI controller for output voltage regulation. An analytical expression of the current control law is developed using a simplified discrete-time small signal model of the boost converter. The discrete-time PI compensator is designed from a discrete-time small signal parametric model of the inner loop obtained by linearization around the desired equilibrium point. The proposed method is initially based on the notion of discrete-time sliding motion to eventually derive a PWM controlled system. Thus, the reported approach can be categorized not only as a Direct Digital Design technique for voltage regulation but also as a competitive method to design sliding-mode based PWM controllers. Simulated and experimental results in a boost converter operating in continuous conduction mode verify the theoretical predictions.

1. Introduction

The significant improvement in the computation capability of digital devices during the last decade together with their cost decrease constitute the main reasons of the huge expansion of research works in the field of digital control of DC-DC switching power converters during that period[1]. Basically, most of the reported digital laws have been implemented by means of Digital Signal Controllers (DSC) [4-9],[15-16] or Field Programmable Gate Arrays (FPGA) [2-3][10-14]. The inherent advantages of digital devices such a high noise immunity, absence of ageing effects, ability to implement complex control algorithms and flexibility in changing controller parameters have contributed to establishing digital control strategies as a real and feasible alternative to the classical analogue control techniques applied to switching converters regulation. Another advantage of digital devices is the communication ability that allows them to interface other digital systems as in the battery control system of an electric vehicle [6]. Moreover, two main strategies have been used in order to design the output voltage control loop, namely,

analog-to-digital redesign or direct digital design. In the first case [4-5],[10],[16], the control loop is first designed in the s-domain using traditional techniques, and subsequently a digital controller is obtained using some of the s-domain to z-domain transformation methods. In the direct digital design [2-3],[6-7],[12] the discrete controller is directly designed in the z-plane by using a discrete small-signal model of the converter. In the case of digital current mode control, the most appropriate techniques to avoid the need of continuously sampling the inductor current are of predictive type, irrespective of employing a fixed [7-13] or a variable switching frequency [14-16]. However, in order to achieve output voltage regulation, the design of a second control loop is mandatory and it is realized following one of the previous discrete output voltage control design procedures.

After the pioneer work of Bilalovic et al. on the application of sliding-mode control to the voltage regulation of a buck converter [17], this control technique has gradually become a popular tool among engineers in the design of controllers and in the analysis of the corresponding dynamics of variable structure systems in power electronics and electrical drives. Over the last decade, the amount of works related to sliding-mode applications in this field were still increasing [16-28], where digital control was applied to obtain a digital sliding mode current control implementation [16] or to implement sliding-based fixed frequency switching systems [21-25]. In this context, the design of PWM or fixed frequency switching systems tries to avoid noise filtering problems associated to variable-frequency characteristics and, also, to allow the use of sliding-mode techniques to regulate interleaved converters. In [26], it was obtained a non linear control law which ensured the asymptotic convergence of the average system. A comparison with the equivalent control law obtained from a zero dynamics analysis in sliding- mode revealed that it was mandatory to add an error proportional term to guarantee the surface reaching when the expression of the equivalent control was implemented with a PWM modulator. Indirect Sliding Mode (SM) technique was used in [21-22] to extend the control surface in order to guarantee the error proportional term appearing in the equivalent control expression whereas in [23-24], the application of a Zero Average Dynamics switching surface–based procedure allowed the direct use of sliding-mode design in PWM controlled systems. Recently, a modification of the method presented in [21] which ensures the system approaching asymptotically the sliding surface was developed in [25].

In this work we propose a boost converter Direct Digital Design strategy based on the application of the discrete-time sliding mode concept described in [27]. A simplified discrete-time model of the boost converter is used to develop an analytic expression of a discrete-time control law ensuring that the motion trajectory of the sampled points is confined to a manifold in the state space once the discrete sliding motion is attained. Discrete output voltage regulation is obtained by means of a discrete-time PI control loop designed in the z-domain. This procedure directly establishes a proper design of sliding-mode based PWM controlled systems.

Note that sliding-mode control can be considered as a control in a manifold, in the sense that the desired state trajectory is forced to evolve on the manifold by switching at infinite frequency between two possible states. Classical sliding-mode controllers have been of analogue type, which has implied the use of analogue hysteresis comparators in order to generate switching signals at finite

frequency that could be handled by the semiconductors. As a result, chattering and variable switching frequency are obtained. It has to be pointed out that chattering is not a problem in switching converters because it is inherent to the way these circuits work, i.e., the mechanism of absorbing energy from the input during the on state and transferring it to the output during the off state is the chattering itself. However, the use of switching frequency can be a problem in certain applications that require a reference frequency for synchronization. For that reason, it is advisable to implement sliding-mode algorithms at constant switching frequency. This implementation is simpler in a digital environment than in analogue circuitry. Nonetheless, a digital implementation of sliding-mode controllers employing a digital hysteresis comparator is also possible at the expense of a variable switching frequency and the quasi-sliding phenomenon. In the last case there is no guarantee that the samples of the state trajectory correspond strictly to the samples on the manifold.

The paper is organized as follows. First, a discrete-time model of the boost converter is obtained in section 2. In section 3 the procedure to design a discrete current control law is presented. Also, a parametric discrete current reference to output voltage transfer function of the current controlled boost is derived in this section. The design of a specific output voltage PI control loop together with the corresponding simulation and experimental results are shown and analyzed in section 4. Final conclusions are presented in section 5.

2. Discrete-time model of a boost converter

Fig. 1 shows a schematic representation of a digitally controlled boost converter where $i_L(t)$ and $v_c(t)$ represent respectively the inductor current and the output voltage instantaneous values.

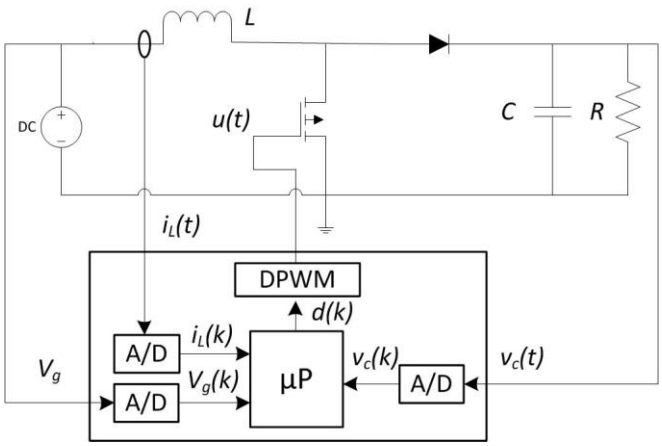


Fig.1: Block diagram of a digitally controlled boost converter

$V_g(t)$ represents the input voltage and u(t) constitutes the control action, which is in the ON-state during $T_{on}(t)$ and in the OFF-state during $T_{off}(t)$ fulfilling $T=T_{on}(t)+ T_{off}(t)$, T being the switching period. Besides, $i_L(k)$, $v_c(k)$ and $v_g(k)$ are the corresponding sampled values of the inductor current, output voltage and input voltage at instant t=kT while $d(k)=T_{on}(k)/T$ represents the computed duty cycle in the k^{th} switching cycle.

The dynamics of a power converter operating in continuous conduction mode at a fixed switching frequency can be represented in the k[th] switching cycle as:

$$\dot{x}(t) = A_1 x(t) + B_1 V_g \qquad kT \le t \le kT + T_{on}(k) \qquad (1)$$

$$\dot{x}(t) = A_2 x(t) + B_2 V_g \qquad kT + T_{on}(k) \le t \le (k+1)T \qquad (2)$$

where $x(t) = \begin{bmatrix} i_L & v_c \end{bmatrix}^T$ represents the state vector of the converter, symbol T means matrix transpose, T is the switching period, kT constitutes the beginning of the switching period, and $T_{on}(k)$ and Vg represent respectively the duration of the conduction state and the input voltage. In case of an ideal boost converter, the state matrices can be represented by

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \qquad (3)$$

Noting that

$$\int_{kT}^{kT+T_{on}(k)} e^{A_1(kT+T_{on}(k)-\tau)} B_1 d\tau = \begin{pmatrix} \frac{T_{on}(k)}{L} \\ 0 \end{pmatrix} \qquad (4)$$

Also, $x(t)$ for t=(k+1)T is given by

$$x(k+1) = e^{A_2 T}\left[e^{-A_2 T_{on}(k)} e^{A_1 T_{on}(k)} x(k) + \right.$$
$$\left. + e^{-A_2 T_{on}(k)} \begin{pmatrix} \frac{T_{on}(k)}{L} \\ 0 \end{pmatrix} V_g + \left(e^{-A_2 T_{on}(k)} - e^{-A_2 T}\right) A_2^{-1} B_2 V_g \right] \qquad (5)$$

where $x(k+1)$ represents $x((k+1)T)$ [28].

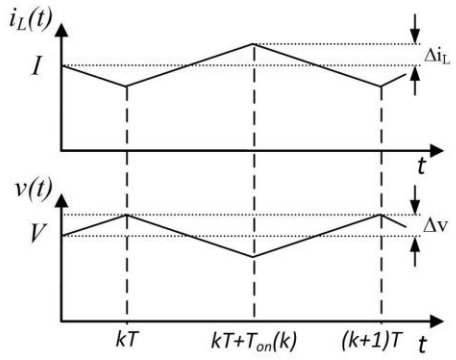


Fig. 2: Inductor current and output voltage waveforms of a boost converter.

We can observe in Fig. 2 that $i_L(k)$ and $v_c(k)$ represent the valley value and the peak value of inductor current and capacitor voltage respectively at t=kT whereas I and V represent their corresponding average values.

Expanding e^{At} in Taylor's series and neglecting the terms of order greater than 1, the following approximate model is obtained:

$$x(k+1) = \left(I + A_2 T + \left(A_1 - A_2\right)T_{on}(k)\right)x(k) + B_2 T V_g = \\ = Hx(k) + Fx(k)T_{on}(k) + G \quad (6)$$

where

$$H = I + A_2 T = \begin{bmatrix} 1 & -\frac{T}{L} \\ \frac{T}{C} & 1 - \frac{T}{RC} \end{bmatrix} \qquad F = \left(A_1 - A_2\right) = \begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix} \qquad G = B_2 T V_g = \begin{bmatrix} \frac{TV_g}{L} \\ 0 \end{bmatrix} \quad (7)$$

3. Discrete-Time Sliding mode control

A. Discrete-Time Sliding Mode Current Control.

In order to reach a desired value of the inductor current $i_L(t)$ at sampling instants t=kT the following condition has to be fulfilled

$$s(t) = I_{ref} - i_L(t) = 0 \quad t=kT \quad k=1,2,3,... \quad (8)$$

which is related to a current control surface, where T is the sampling period and $I_{ref} \geq 0$ is the desired inductor current value at sampling instants.

In a discrete-time representation (8) is defined as

$$s(k) = I_{ref} - C * x(k) \quad (9)$$

where C=[1 0], $s(k)=s(x(k))$ represents the discrete-time sliding mode surface control and $x(k)$ represents the discrete state vector of the converter.

Then, in order to converge to (9), at any k^{th} switching cycle we compute the corresponding control action that brings the system to fulfill [30]

$$s(k+1)=0 \quad (10)$$

which in our case means we are calculating the value of $T_{on}(k)$ that leads the inductor current sampled value to be equal to the reference at the end of the present sampling period, extending the notion of equivalent control to discrete-time systems[30]:

$$T_{eq}(k) = \frac{\left(I_{ref} - i_L(k)\right)L + \left(v_c(k) - V_g\right)T}{v_c(k)} \quad (11)$$

whose value has the following restriction related to the available values of the control action

$$0 \leq T_{eq}(k) \leq T \qquad \forall\ k\ \ kT \geq t_{rch} \quad (12)$$

being t_{rch} the finite time that the system takes to reach the surface from a starting point at t=0. Then, in discrete-time sliding mode regime, the following existence conditions must be satisfied to guarantee (12),

$$v_c(k) \geq V_g \tag{13}$$

$$V_g \geq 0 \tag{14}$$

Condition (13) is the classical existence condition of the corresponding analogue sliding-mode control for a boost converter taking into account that condition (14) is always satisfied.

In some cases, $T_{eq}(k)$ can overpass the range of values of the control action and, as a consequence, $T_{on}(k)$ will be saturated at the nearest limit control value in order to satisfy (12), thus becoming

$$T_{on}(k) = \begin{cases} 0 & T_{eq}(k) < 0 \\ T_{eq}(k) & 0 \leq T_{eq}(k) \leq T \\ T & T_{eq}(k) > T \end{cases} \tag{15}$$

This $T_{on}(k)$ saturation means s(k+1) ≠ 0 and hence, to ensure the existence of discrete-time sliding motion in further cycles, the convergence to the surface must be proved by assuring that ||s(k)|| decreases monotonically until the surface is reached. To verify the system convergence, the following conditions must be satisfied:

$$s(k+1)<0 \text{ and } \Delta s(k+1)>0 \tag{16}$$

$$s(k+1)>0 \text{ and } \Delta s(k+1)<0 \tag{17}$$

where

$$\Delta s(k+1) = s(k+1) - s(k) = \frac{T}{L}\left(v_c(k) - V_g\right) - T_{on}(k)\frac{v_c(k)}{L} \tag{18}$$

In case of $T_{on}(k)$ being saturated to 0, this implies s(k+1)<0 and (18) becomes

$$\Delta s(k+1) = \frac{T}{L}\left(v_c(k) - V_g\right) > 0 \tag{19}$$

To guarantee (19), condition (13) must be used as a reaching condition. If (13) is satisfied then the system will move towards the surface.

When $T_{on}(k)$ is saturated to the highest control value, i.e. $T_{on}(k)$=T, this means $s(k+1)$>0 and, therefore (18) becomes

$$\Delta s(k+1) = -\frac{TV_g}{L} < 0 \tag{20}$$

fulfilling (17) and guaranteeing the system also moves towards the surface.

As it was previously shown, the existence of the discrete-time sliding-mode regime is ensured for constant current surface control (9) and the control action defined by (15).

1) Ideal discrete-time dynamics

Introducing the equivalent control $T_{eq}(k)$ given by (11) in the state space model (6) and assuming sliding-mode operation result

in the following equations

$$i_L(k+1) = I_{ref} \tag{21}$$

and

$$v_c(k+1) = \left(1 - \frac{T}{RC}\right) v_c(k) + \frac{TV_g I_{ref}}{v_c(k)C} \tag{22}$$

(21) and (22) represent the ideal discrete-time sliding dynamics of the controlled boost converter. As we can see, the obtained dynamics of the boost converter is a non-linear function of the capacitor voltage and its order is reduced by one.

At the equilibrium point $i_L(k+1) = i_L(k) = I_e$ and $v_c(k+1) = v_c(k) = V_e$. Then, from (21) and (22) we obtain the following equilibrium point

$$x^* = \begin{pmatrix} I_e \\ V_e \end{pmatrix} = \begin{pmatrix} I_{ref} \\ \sqrt{RV_g I_e} \end{pmatrix} \tag{23}$$

where I_e and V_e are the average values of inductor current and output voltage respectively

Note that (23) can be expected since no losses have been assumed in the analysis and therefore the converter exhibits its POPI nature (DC Power Input equal to DC Power Output) [29].

2) Stability of the equilibrium point

Defining

$$e(k) = v_c(k) - v_c(k-1) \tag{24}$$

and using (23) in (22) yield

$$\begin{aligned} &e(k+1) = v_c(k+1) - v_c(k) = \\ &= \left(1 - \frac{T}{RC}\right) e(k) + \frac{TV_e^2}{RC}\left(\frac{1}{v_c(k)} - \frac{1}{v_c(k-1)}\right) = \\ &= \left(1 - \frac{T}{RC} - \frac{TV_e^2}{RCv_c(k)v_c(k-1)}\right) e(k) \end{aligned} \tag{25}$$

which represents the error dynamics. Therefore, from (13) and (14), a sufficient condition for the stability of the recurrence, i.e., $\lim_{k\to\infty} e(k) \to 0$, is:

$$-1 < 1 - \frac{T}{RC} - \frac{TV_e^2}{RCv_c(k)v_c(k-1)} < 1 \tag{26}$$

This condition is satisfied if

$$T < \frac{2RCV_g^2}{\left(V_g^2 + V_e^2\right)} \qquad (27)$$

which guarantees the stability of the ideal discrete-time sliding dynamics represented by (22) or (24).

Note that expression (27) is consistent with the requirements of a good design i.e., switching period *T* must be significantly smaller than time constant *RC*. Observe also that in case of heavy load and fast dynamics response due to a very small capacitance, the switching frequency would be very high and, consequently, the implementation of a digital control strategy could eventually need the use of a specific ASIC (Application-Specific Integrated Circuit) [30].

B. Current to Output Voltage Discrete Small Signal Model

In order to ensure output voltage regulation, an outer and slower control loop in cascade with the inner current control loop is added. This output voltage control loop is designed in the z-plane, thus implying the existence of a current reference to output voltage discrete transfer function $Gi_{ref}v(z)$ that represents the small-signal dynamics behavior around the equilibrium point, which in this case must be the desired output voltage value V_{ref}. This second control loop computes the corresponding $i_{ref}(k)$ that will lead the system to the desired output voltage and makes the inductor current reference a function of time. Consequently, in order to obtain the current reference to output voltage discrete transfer function for small signal variations around the desired working point (V_{ref}), expression (8) is redefined as

$$s(k) = i_{ref}(k-1) - i_L(k) \qquad (28)$$

Then, applying (10) to (28) equation leads (11) to

$$T_{on}(k) = \frac{\left(i_{ref}(k) - i_L(k)\right)L + \left(v_c(k) - V_g\right)T}{v_c(k)} \qquad (29)$$

Under the assumption of a discrete-time sliding-mode regime it can be written

$$i_L(k) = i_{ref}(k-1) \qquad (30)$$

and introducing (29) and (30) into (6) yields the reduced order dynamics of $v_c(k)$ given by

$$v_c(k+1) = \left(1 - \frac{T}{RC}\right)v_c(k) + \frac{i_{ref}(k-1)}{Cv_c(k)}\left(L\left(i_{ref}(k-1) - i_{ref}(k)\right) + TV_g\right) \qquad (31)$$

Linearizing (31) around the equilibrium point $x^*=[I_e, V_e]^T$ and using (23), the following current reference to output voltage discrete transfer function is obtained.

$$Gi_{ref}v(z) = -\frac{LV_e}{V_g RC}\frac{z-\left(1+\frac{TV_g^2R}{LV_e^2}\right)}{z\left(z+\left(\frac{2T}{RC}-1\right)\right)} \qquad (32)$$

This transfer function represents the discrete-time small-signal model of the output voltage of a boost converter controlled by an inner discrete current control loop based on a discrete-time sliding-mode strategy and it can be used to design a second output voltage discrete control loop in the z plane. Note that (32) has a zero outside the unit circle, which explains the well –known non-minimum phase characteristics of the control to output voltage transfer function in a boost converter. Also, it can be observed that (32) has a pole within the unit circle , which corresponds to a stable system if T<RC, which is ensured by (27).

4. Experimental and simulation Results

Performance and feasibility of the proposed discrete control strategy was first evaluated by means PSIM simulation applied to a boost converter with the following parameters: f_s=100 kHz, T=10^{-5} s, C=200 μF, L=216 μH, R= 44 Ω, V_g= 12 V and V_{ref}= 24 V. Afterwards, a 20 W experimental prototype of a boost converter was developed for the same set of parameters. The control algorithm is implemented using a Digital Signal Controller from Texas Instruments (TMS20F28335) with a sampling frequency exactly equal to the switching frequency.

As it can be observed in Fig. 3, the frequency behavior of the current to output voltage control function $G_{irefvo}(z)$ is compared with the obtained from the current controlled ideal boost converter by means of simulation. Both gain and phase values show a similar behavior up to half of the switching frequency f_s, confirming the feasibility of the model developed in (32).

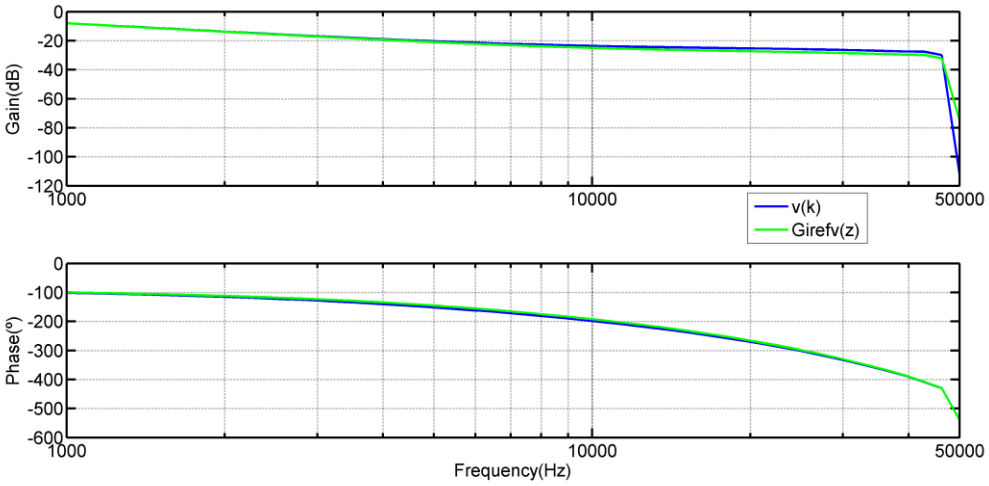


Fig 3: Frequency behavior of $G_{irefv}(z)$

In order to obtain output voltage regulation a Proportional-Integral (PI)-based controller is designed to obtain a phase margin of 40 º and to guarantee zero steady-state error, thus giving

$$G_{PI}(z) = 2.1122\frac{z-0.982}{(z-1)(z-0.5948)} \qquad (33)$$

The controller consists in a pole at z = 1 to achieve zero steady-state error, an additional pole at the same frequency of the non-minimum phase zero, a zero located before the loop gain cross-over frequency and a gain. The zero and the gain were chosen using the Single Input Single Output design tool of Matlab in order to guarantee the desired phase margin.

Fig. 4a depicts the closed-loop poles loci for different values of input voltage and load resistance. It can be observed that the system remains stable for around 25 % variation of the input voltage and 50 % change of the output resistance, the worst case corresponding to Vg= 9 V and R= 22 Ω and being illustrated in the zoom depicted in Fig 4b.

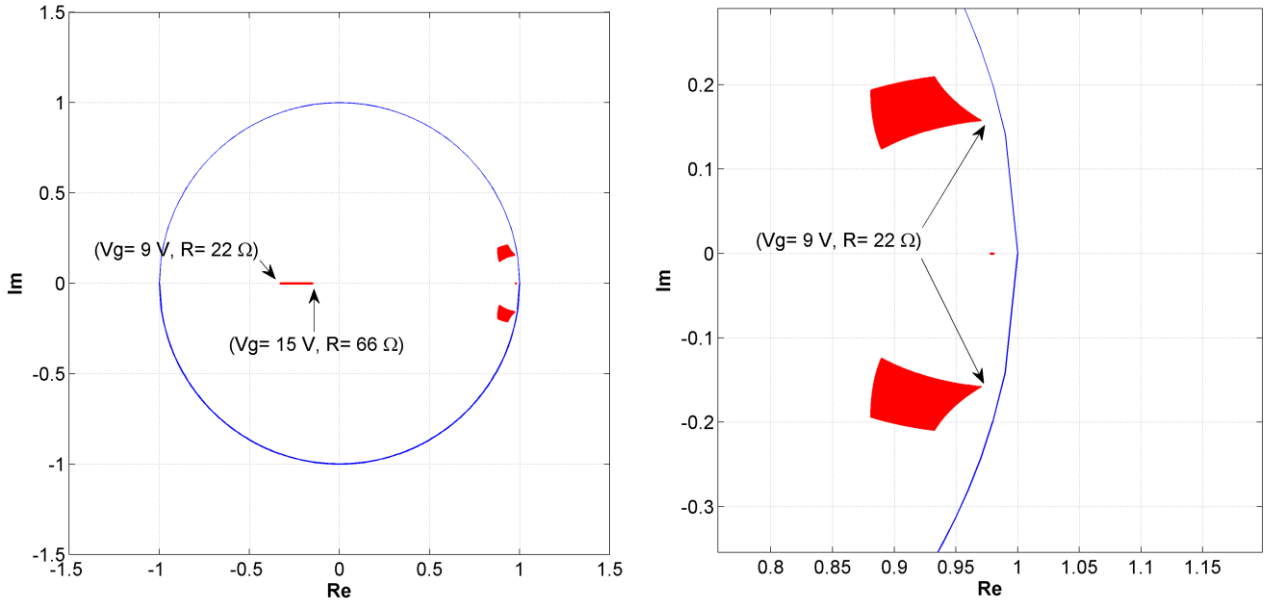
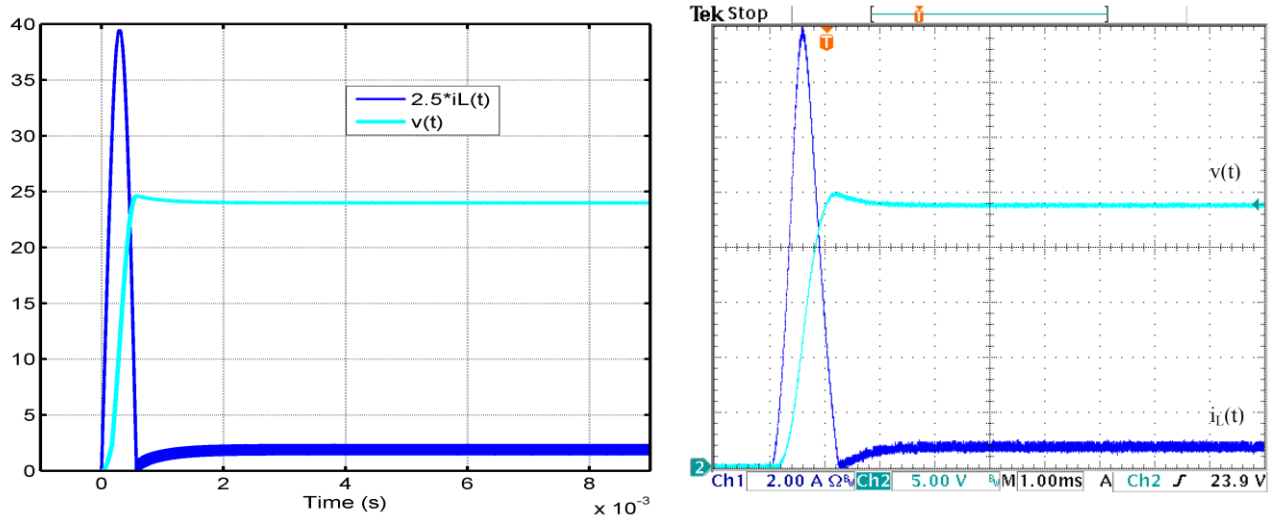


Fig. 4: a) Root Locus LOCI diagram b) zoom

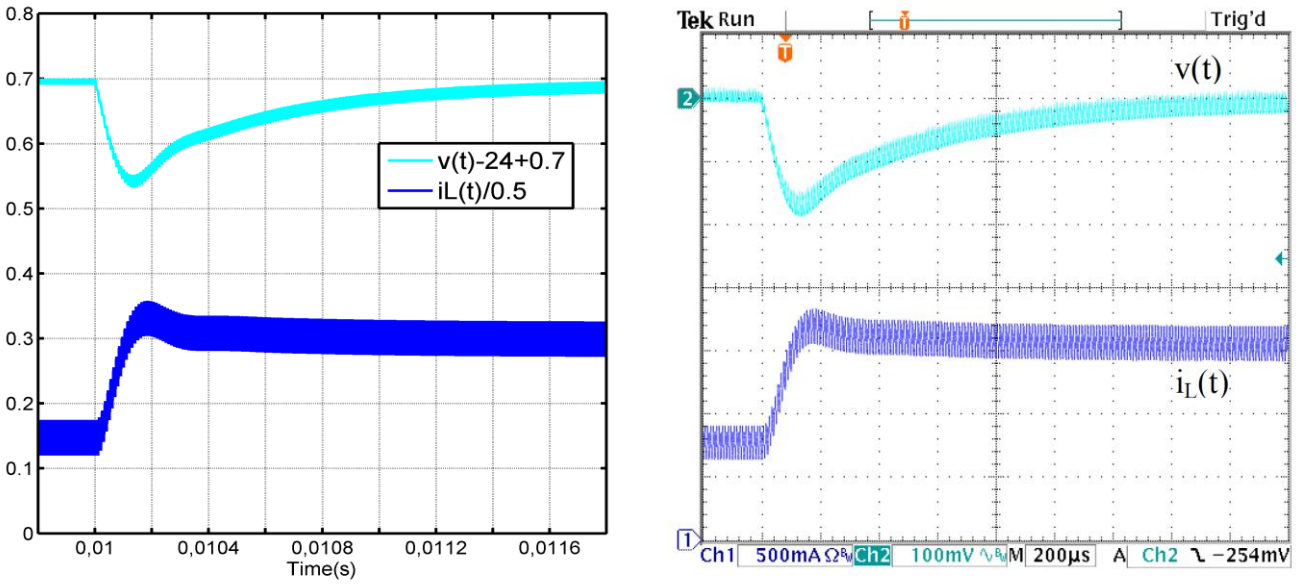
As illustrated in Fig. 5. the system exhibits a good performance and a fast response with very small overshoot of the output voltage in the start-up transient response. In this figure the time response of the inductor current can be also observed. Simulated (Fig. 5a) and experimental (Fig. 5b) responses have a similar dynamic response and show that the system reaches the desired equilibrium point. It has to be pointed out that the inductor current response during start -up exhibits the well-known inrush current problem, which could be minimized using soft-start techniques or ad-hoc control methods [31-32] in case of an eventual commercial development.



(a) (b)

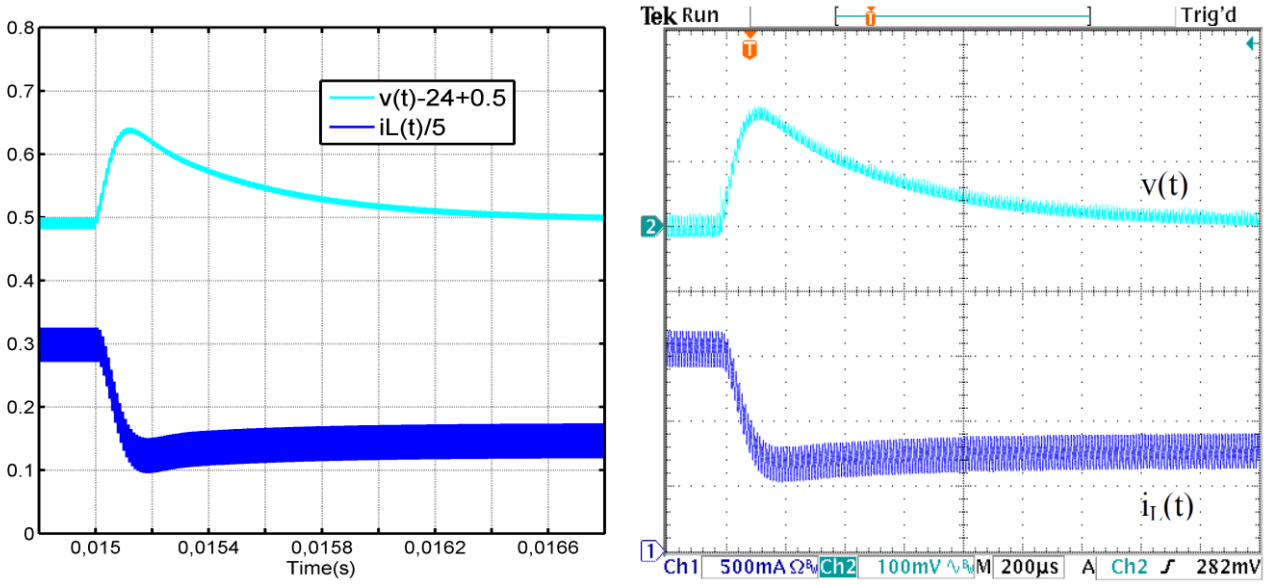
Fig 5.Start-up response: (a) simulated, (b) experimental

The output voltage transient response for load perturbations of 50 % is shown in figures 6 and 7, where it can be verified that simulated results on the left side and experimental results on the right side are in good agreement both showing a fast recovery of the steady-state. Note that Fig. 6 depicts a load decrease while Fig.7 illustrates the return to nominal conditions.



(a) (b)

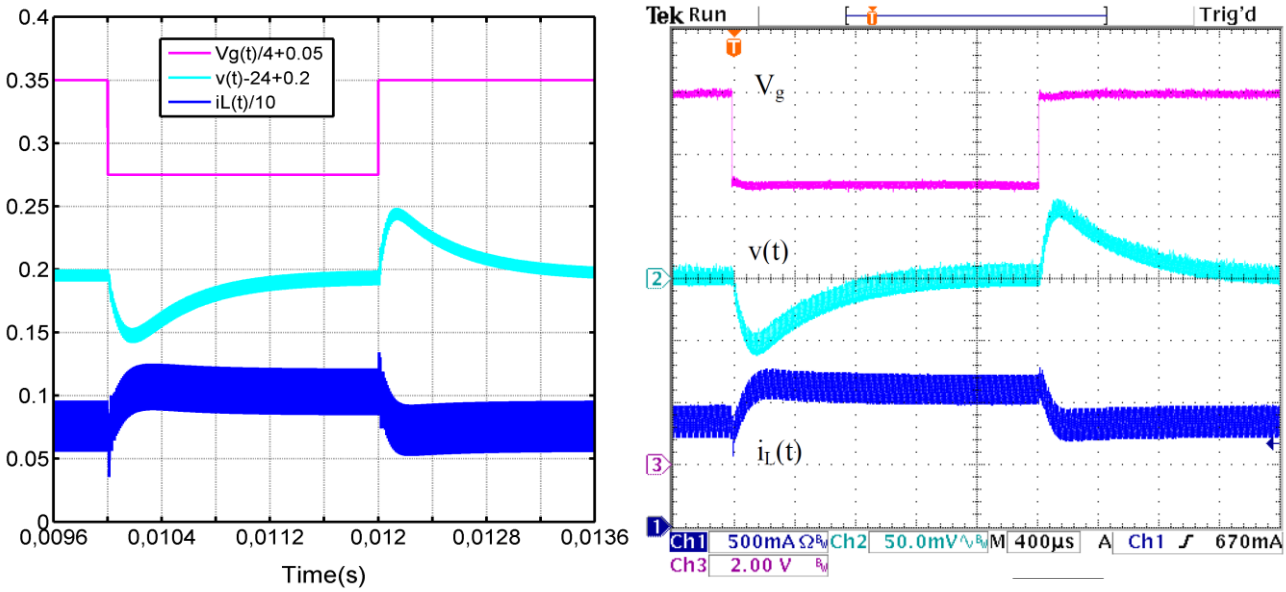
Fig. 6: Output voltage response to a load change from 66 Ω to 33 Ω: (a) simulated, (b) experimental



(a) (b)

Fig. 7: Output voltage response to load change from 33 Ω to 66 Ω: (a) simulated, (b) experimental

Fig. 8 show the simulated (Fig. 8a) and experimental (Fig 8b) transient response for input voltage variations. A variation of -3 V is applied first to V_g and, after 2 ms the nominal value of Vg=12 V is again established. Observe that Fig.8 depicts the input voltage variation and the inductor current transient response beside the output voltage transient response. Both simulated and experimental results of the output voltage are in good concordance showing a fast transient recovery of the desired output voltage value in both negative and positive transitions.



(a) (b)

Fig. 8: Output voltage and inductor current transient response to input voltage variations: (a) simulated, (b) experimental

5. Discussion and Conclusions

This work has presented a new procedure that allows the design of a digital controller to regulate the output voltage of a boost converter. This controller is based on an inner non linear current control loop and an outer discrete PI voltage control loop. The inner loop is designed following a discrete-time sliding mode concept whereas the outer loop is obtained by means of a Direct Digital Design procedure after deriving a discrete small-signal representation of the current loop. A complete stability analysis has been also provided.

The use of a new discrete-time model of the boost converter has allowed obtaining an analytical expression for the current loop control law. Moreover, the derived current to output voltage discrete-time transfer function has facilitated the subsequent design of sliding-mode based PWM controllers for output voltage regulation in boosts converters. This model has been validated by comparing its frequency response with the one corresponding to the switched model using PSIM simulator.

The proposed method is based on a discrete –time analysis leading straightforwardly to a simple digital implementation based on a DSC in a clear-cut contrast with the two main previous antecedents of this work. Thus, it has to be pointed out that Zero Average Dynamics approach [23-24] is based on a complex digital implementation of the controller, which is derived from a continuous-time analysis of the converter and requires a FPGA. Also, sliding mode-based PWM [21-22] implements analogically a control strategy derived from a continuous –time description of the converter and therefore cannot be classified as a digital control.

The proposed control combines the advantages of an analog control in terms of fast response and the benefits of a digital implementation such as programmability and noise immunity, and offers the additional profit of operating at constant switching frequency.

Acknoledgements

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