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Compact drain-current model for undoped cylindrical surrounding-gate metal-oxide-semiconductor field effect transistors including short channel effects

Billel Smaani,[1,a)] Saida Latreche,[1] and Benjamín Iñiguez[2]
[1]*Département d'Electronique, Université Constantine 1, Faculté des sciences de la technologie, Laboratoire Hyperfréquences et Semi-conducteurs (LHS), Constantine, Algeria*
[2]*DEEEA, Universitat Rovira i Virgili (URV), Tarragona, Spain*

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In this paper, we present a compact model for undoped short-channel cylindrical surrounding-gate MOSFETs. The drain-current model is expressed as a function of the mobile charge density, which is calculated using the analytical expressions of the surface potential and the difference between surface and center potentials model. The short-channel effects are well incorporated in the drain-current model, such as the drain-induced barrier lowering, the charge sharing effect (V_T Roll-off), the subthreshold slope degradation, and the channel length modulation. A comparison of the model results with 3D numerical simulations using Silvaco Atlas-TCAD presents a good agreement from subthreshold to strong inversion regime and for different bias voltages. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4844395]

I. INTRODUCTION

The CMOS technology evolution is approaching the limit caused by the increase of the parasitic physical effects, especially the short-channel effects (SCEs) which appear in the nanoscale short-channel devices.[1] As a solution to this physicals problems, a variety of Multiple Gate SOI MOSFETs architecture have been developed, the Cylindrical Surrounding-Gate (SRG) SOI MOSFET is one of the best device in the technology scaling.[1,2] This structure reduces the SCEs and offers an excellent control of the electrostatic potential in silicon channel. The undoped silicon channel of the SRG MOSFET reduces the surface and Coulomb's scattering.[3] On the other hand, compact models for the SRG MOSFETs are important to improve the application of these devices for circuit design and simulation.[4]

Most of the published models are developed for long-channel SRG MOSFET, for both cases: undoped and doped silicon channels,[4–6] and from low to high doped case.[7] However, reducing the channel length below 100 nm increases the short-channel effects, such as the drain-induced barrier lowering (DIBL), the channel length modulation (CLM), and the subthreshold slope. Those effects cannot be ignored.[8] In this context, a few compact models are developed to model the SCEs in short-channel SRG MOSFET. Chiang[9] proposed a compact model for highly doped channel device. El Hamid *et al.*[10] and Ray and Mahapatra[11] developed analytical SRG MOSFET models. However, the calculation of the potential requires numerical iterative methods, which are not suitable for circuit simulation because they consume time. Børli *et al.*[12] proposed a compact modeling framework for short-channel nanoscale Gate All Around MOSFET. However, it is less useful for circuit simulation and circuit design application, because they used a conformal mapping method with a self-consistent procedure.

In this work, we present a compact drain-current model for nanoscale short-channel undoped SRG MOSFET. It is based on the analytical expressions of the surface potentials and the difference of potentials for long-channel SRG MOSFET model.[7] The drain-current model is then derived to model the SCEs: DIBL, V_T Roll-off, subthreshold slope degradation, and channel length modulation. The SCEs effects are modeled through simple analytical expressions, which is suitable for circuits design applications. The surface potentials are calculated using the Lambert W functions, which prove their utility in many engineering and physicals applications.[13] The quantum effects and the mobility degradation are not addressed in this paper. The quantum effects are significant when the radius of the cylindrical body is smaller than 5 nm. To verify the validity of the drain-current model, a comparison is considered with 3D numerical simulations obtained using Silvaco Atlas-TCAD.[14]

II. MODEL DESCRIPTION

A. Device structure

The undoped SRG MOSFETs structure considered in this work is shown in Fig. 1, where L is the channel silicon length, tox is the oxide thickness, and R is the radius of cylindrical silicon channel. Vgs and Vds are the gate and the drain voltage polarization, respectively.

B. Surface potentials

Under the gradual channel approximation (GCA), the Poisson's equation can be presented as[6]

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\Phi}{dr}\right)=\frac{q.N_A}{\varepsilon_{si}}[\exp(\beta).(\Phi-V_{ch}-2\Phi_F)+1], \quad (1)$$

[a)]Author to whom correspondence should be addressed. Electronic mail: billel1248@yahoo.fr

where Φ is the electrostatic potential, q is the electric charge, ε_{si} is the permittivity of silicon, N_A is the uniform acceptor concentration, $\beta(=q/KT)$ is the reciprocal of thermal voltage $(\Phi_t = 1/\beta)$, V_{ch} is the quasi Fermi potential in the channel, and $\Phi_F(=\beta^{-1}\ln(N_A/n_i))$ is the Fermi potential.

The boundary conditions used for Eq. (1) are $C_{ox}(V_{gs} - V_{fb} - \Phi_s) = Q_{si} = -\varepsilon_{si}E_s$ for $r = R$ and $d\Phi/dr = 0$ for $r = 0$, where $Q_{si}(=Q_m + Q_p)$ is the silicon charge density per unit gate area, Q_m is the inversion charge density per unit gate area, $Q_p(=qN_AR/2)$ is the fixed charge density per unit gate area, ε_{ox} is the permittivity of oxide, $E_s = E(r = R)$ is the surface electric field, $\Phi_s = \Phi(r = R)$ is the surface potential, V_{fb} is the flat band voltage, and $C_{ox}(=\varepsilon_{ox}/R\ln(1 + t_{ox}/R))$ is the cylindrical oxide capacitance.[8]

From Eq. (1) and its boundary conditions, an analytical solution of the surface potential in subthreshold regime $\Phi_{s_{bT}}$ is obtained using the Lambert W function as[7]

$$\Phi_{sbT} = V_{gs} - V_{fb} - \frac{Q_p}{C_{ox}} - \Phi_t LambertW \times \left[\frac{Q_p}{C_{ox}\Phi_t}\exp\left(\frac{V_{gs} - V_{fb} - \frac{Q_p}{C_{ox}} - V_{ch} - 2\Phi_F}{\Phi_t}\right)\right]. \quad (2)$$

And in the above threshold voltage regime, the surface potential $\Phi_{s_{aT}}$ is calculated by

$$\Phi_{saT} = V_{gs} - V_{fb} - 2\Phi_t LambertW\left[\frac{1}{2C_{ox}\Phi_t}\sqrt{\frac{4Q_p\varepsilon_{si}\Phi_t}{R}} \times \sqrt{1 - \frac{1}{\alpha} + \frac{1}{\alpha}e^{-\alpha}}\exp\left(\frac{V_{gs} - V_{fb} - \frac{Q_p}{C_{ox}} - V_{ch} - 2\Phi_F}{2\Phi_t}\right)\right], \quad (3)$$

where $\alpha = (\Phi_s - \Phi_0)/\Phi_t$ is the normalized difference between surface and center potentials.

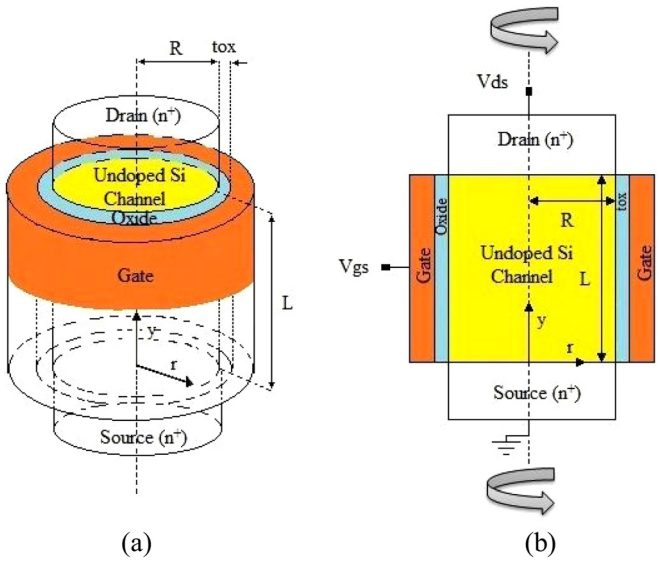

FIG. 1. (a) Structure of the SRG MOSFET. (b) The cross-section of the undoped n-type SRG MOSFET.

The final surface potential Φ_s continues from subthreshold to above threshold voltage regime is then calculated with the following interpolation function:

$$\Phi_s = \frac{1}{2}\{\Phi_{sbT}[1 - \tanh(10(V_{gs} - V_{TH} - V_{ch}))] + \Phi_{saT}[1 + \tanh(10(V_{gs} - V_{TH} - V_{ch}))]\}, \quad (4)$$

where V_{TH} is the threshold voltage of the device.

C. Difference of potentials

The difference between surface and center potentials $\Phi_d(=\Phi_s - \Phi_0)$ is calculated with the following empirical expressions, with the similar way as for Double Gate MOSFET model.[15]

In subthreshold regime:

$$\Phi_{db} = \Phi d_{bT} + \frac{19}{16}\Phi_t\left[\frac{\exp\left(\frac{V_{gs} - V_{TH} - V_{ch}}{\Phi_t}\right)}{1 + \exp\left(\frac{V_{gs} - V_{TH} - V_{ch}}{\Phi_t}\right)}\right]. \quad (5)$$

And in the above threshold voltage regime:

$$\Phi_{da} = \left(\frac{\Phi d_{bT}}{3} + \Phi_{dm} - 0.028V\right) - \left(\frac{\Phi d_{bT}}{3} + \Phi_{dm} - 0.028V - \Phi_{dT}\right) \times \left(\frac{1 - \frac{V_{gs} - V_{TH} - V_{ch}}{V_{gm} - V_{TH} - V_{ch}}}{1 + 1.35(V_{gs} - V_{TH} - V_{ch})}\right), \quad (6)$$

where V_{gm} is the maximum gate voltage polarization.

The difference between surface and center potentials Φ_d continues from subthreshold Φ_{db} to above threshold voltage regime Φ_{da} is calculated with the following interpolation function:

$$\Phi_d = \frac{1}{2}\{\Phi_{db}[1 - \tanh(50(V_{gs} - V_{TH} - V_{ch}))] + \Phi_{da}[1 + \tanh(50(V_{gs} - V_{TH} - V_{ch}))]\}. \quad (7)$$

Using the full-depletion approximation applied to Eq. (1), the analytical solution of the difference of potentials in subthreshold regime Φd_{bT} is obtained as

$$\Phi d_{bT} = \Phi_{s_{bT}} - \Phi_{0_{bT}} = \frac{qN_AR^2}{4\varepsilon_{si}}. \quad (8)$$

In subthreshold regime, the center potential $\Phi_{0_{bT}}$ is then calculated substituting the solutions of Eqs. (2) and (8) at $\Phi_{0_{bT}} = \Phi_{sbT} - \Phi d_{bT}$.

The difference of potential at the threshold voltage $\Phi_{dT}(V_{gs} = V_{TH})$ is calculated by $\Phi_{dT} = \Phi d_{bT} + 0.626\Phi_t$, where Φ_{dm} is the difference of potential at the maximum gate voltage $(V_{gs} = V_{gm})$ calculated with the following empirical expression:[7]

$$\Phi_{dm} = 0.162 - 0.047t_{ox} + 0.0045t_{ox}^2 + 0.00836R - 12.10^{-5}R^2. \quad (9)$$

D. The mobile charge density

The normalized mobile charge density, q_m, as a function of the difference between surface and center potential, α, is calculated with the following expression:[7,16]

$$q_m = \sqrt{\frac{4q_p\varepsilon_{si}}{C_{ox}R}}\sqrt{\alpha} \times \sqrt{\frac{1}{2} + \left[\frac{1 - \frac{1}{\alpha} + \frac{1}{\alpha}\exp(-\alpha)}{\alpha}\right]\exp\left(\frac{\Phi_s - V_{ch} - 2\Phi_F}{\Phi_t}\right)} - q_p, \quad (10)$$

where $q_p = Q_p/C_{ox}\Phi_t$ is the normalized fixed charge density. q_m takes the value of q_s at the source ($V = 0$) and q_d at the drain ($V = V_{ds}$).

III. SHORT CHANNEL EFFECTS

A. Mobility model

The mobility μ dependence with the longitudinal field is calculated with the following approximated relation:[17]

$$\mu = \frac{\mu_0}{\sqrt{1 + \left(\mu_0\frac{V_{deff}}{L\nu_{sat}}\right)^2}}, \quad (11)$$

where μ_0 is the low-field mobility and ν_{sat} is the carrier saturation velocity equals to $\nu_{sat} = 1.45 \times 10^7$cm/s.

The effective drain voltage V_{deff} continuing from subthreshold to above threshold voltage regime is given by[18]

$$V_{deff} = V_{sat} + \frac{1}{2}\left[\left(V_{ds} - V_{sat} + \frac{\Phi_t}{3}\right) - \sqrt{\left(V_{ds} - V_{sat} + \frac{\Phi_t}{3}\right)^2 + 4\frac{\Phi_t}{3}V_{sat}}\right]. \quad (12)$$

The saturation voltage V_{sat} can be expressed as

$$V_{sat} = \frac{\Phi_t}{\tau}\left[q_s - q_{sat} + 2\ln\left(\frac{q_s + \frac{q_p}{2}}{q_{sat} + \frac{q_p}{2}}\right)\right], \quad (13)$$

where τ is used as a fitting parameter.

q_{sat} is the charge at the drain saturation given by

$$q_{sat} = \sqrt{\left(\frac{\nu_{sat}L}{\mu_0\Phi_t} + 2\right)^2 + q_s^2 + 4q_s} - \left(\frac{\nu_{sat}L}{\mu_0\Phi_t} + 2\right). \quad (14)$$

B. The DIBL and V_T Roll-off effects

In short-channel device where the channel length is smaller than 50 nm, the DIBL and V_T Roll-off effects create a lowering of the threshold voltage. These effects have an important degradation on the device characteristics. The charge sharing effect (V_T Roll-off) and the drain induced barrier lowering effects are modeled via a threshold voltage correction as[18]

$$\Delta V_{TH} = \sigma\left(\frac{l_c}{L}\right)^2\Phi_F\left[1 - \exp\left(-\frac{L}{0.3lm}\right)\right] \times \left[1 + \frac{|V_{ch}|}{4.39\Phi_t} - \exp\left(-\frac{|V_{ch}|}{0.22\Phi_t}\right)\right], \quad (15)$$

where l_c is the natural length of the cylindrical surrounding-gate MOSFET equal to $l_c = \sqrt{\frac{2\varepsilon_{si}R^2\ln(1+t_{ox}/R)+\varepsilon_{ox}R^2}{4\varepsilon_{ox}}}2$. $lm(= 10\,\mu m)$ is the reference length and $\sigma(=2.05)$ is used as an adjusting parameter.

The threshold voltage V_{TH} including DIBL and V_T Roll-off effect is given by

$$V_{TH} = V_{TO} - \Delta V_{TH}. \quad (16)$$

V_{TO} is the threshold voltage of long-channel device, calculated with the following expression:[7]

$$V_{TO} = V_{fb} + 2\Phi_F + \Phi_t\ln\left[\frac{C_{ox}}{4C_{si}}\left(1 + \frac{\Phi_t C_{ox}}{Q_p}\right)\right] + \frac{1}{C_{ox}}\sqrt{\frac{4Q_p\varepsilon_{si}\Phi_t}{R}}.\sqrt{\alpha_T} \times \sqrt{\left[\frac{1}{2} + \left[\frac{1 - \frac{1}{\alpha_T} + \frac{1}{\alpha_T}e^{-\alpha_T}}{\alpha_T}\right]\left[\frac{C_{ox}}{4C_{si}}\left(1 + \frac{\Phi_t C_{ox}}{Q_p}\right)\right]\right]}, \quad (17)$$

where α_T is the normalized difference of potentials at the threshold voltage.

C. Subthreshold slope degradation

The subthreshold slope degradation SS expressed as a function of the channel length reduction is modeled by the following expression:[19]

$$SS = \frac{1}{2}\{(1 - 1.2e^{(\frac{L}{2R})})[1 - \tanh(30(V_{gs} - V_{TH}))] + [1 + \tanh(30(V_{gs} - V_{TH}))]\}. \quad (18)$$

This short-channel effect is incorporated into the core model by including the SS expression in the subthreshold drain-current term $(2((q_s - q_d) + q_p\ln(\frac{q_d + 2q_p}{q_s + 2q_p})))$ of Eq. (21).

D. Channel length modulation

Above saturation, the channel length modulation effect makes the channel length shorter $L = L - \Delta L$. This effect is modeled by[18]

$$\Delta L = \lambda.l_c.\left(\ln\left(\frac{L}{l_c}\right) - 1\right)\ln\left(1 + \mu_0\frac{|V_{ds} - V_{deffs}|}{\nu_{sat}l_c}\right), \quad (19)$$

where λ is treated as a fitting parameter.

In subthreshold region, the effective drain voltage drain V_{deffs} voltage is given by the following interpolation function:

$$V_{deffs} = \frac{1}{2}\left\{V_{ds}\left[1-\tanh\left[3\left(1-\frac{V_{gs}}{V_{TH}}\right)\right]\right] + V_{deff}\left[1+\tanh\left[3\left(1-\frac{V_{gs}}{V_{TH}}\right)\right]\right]\right\}. \quad (20)$$

IV. DRAIN CURRENT MODEL WITH SHORT CHANNEL EFFECTS

Considering the drift–diffusion transport[20,21] and using Eqs. (10), (11), (18), and (19), the drain-current I_{ds} of short-channel SRG MOSFET included SCEs is calculated as[7]

$$I_{ds} = \mu W C_{ox} \Phi_t^2 \times \left\{\frac{\frac{1}{2}\left(q_s^2-q_d^2\right)+\left[2\left((q_s-q_d)+q_p \ln\left(\frac{q_d+2q_p}{q_s+2q_p}\right)\right)\right]^{SS}}{(L-\Delta L)}\right\}, \quad (21)$$

where $W = 2\pi R$ is the channel silicon width.

V. RESULTS AND DISCUSSION

In order to verify the validity of the proposed drain-current model, we have made a numerical simulation of the considered device using the commercial simulator Silvaco Atlas-TCAD. We have considered an undoped SRG MOSFET $N_A = 5.10^{15}\,cm^{-3}$ with n-type and mid-gap metal gate with work function of 4.62 eV, doping concentration of the source/drain contact regions $N_D = 10^{20}\,cm^{-3}$. The nanometric short-channel device has an oxide thickness of 1.5 nm, silicon body radius of 6 nm, and a channel length varying from 10 to 30 nm, as shown in Table I. We have simulated the characteristics of the nanoscale undoped SRG MOSFET in the whole operation region, from subthreshold to above threshold voltage regime of operation. The output characteristics were obtained for Vgs equals to 0.5 V, 1 V, and 1.5 V. The transfer characteristics were obtained for Vgs varies from −0.5 V to 2 V, and Vds fixed at 0.05 V and 1 V.

Figs. 2(a) and 2(b) shows the comparison between the modeled drain-current versus gate voltage and the 3D numerical simulation. For Vgs = −0.5 V to 2 V and Vds = 0.05, 1 V, the modeled drain current has a good agreement with 3D simulation for 10 nm channel length of device

TABLE I. Parameters of the proposed drain-current model of undoped SRG MOSFET.

Design parameters				Fitting parameters		
L (nm)	R (nm)	t_{ox} (nm)	N_A (cm^{-3})	λ	τ	μ_0 (cm^2/V s)
10, 20, and 30	6	1.5	5×10^{15}	0.9	0.8	1030

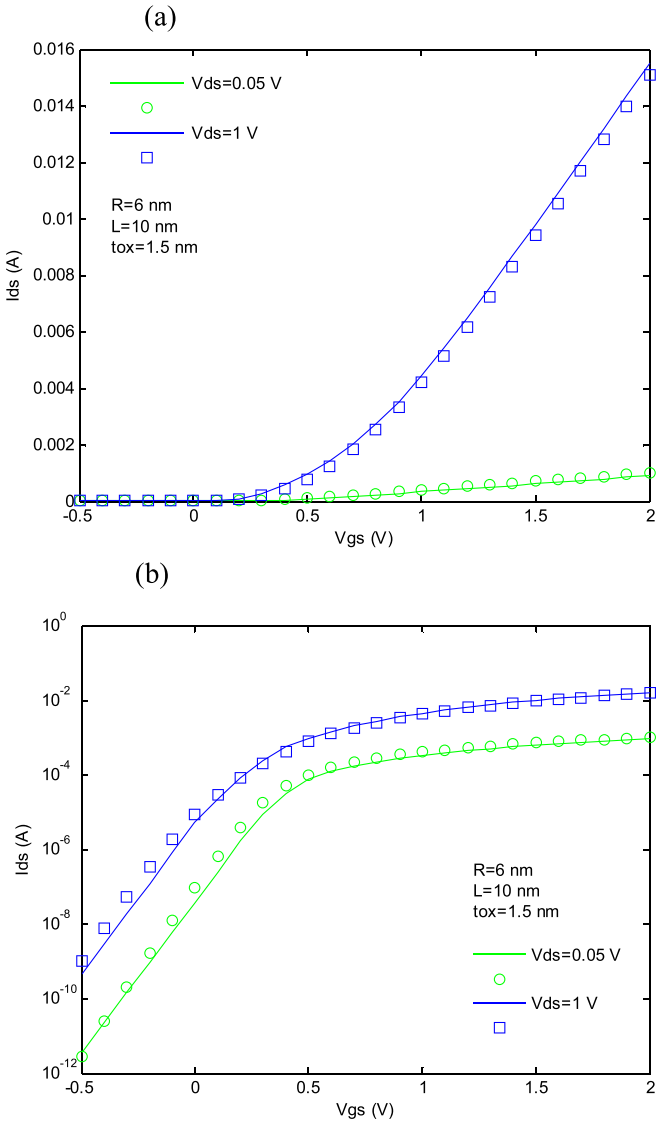

FIG. 2. Drain current versus gate-voltage of short-channel undoped SRG MOSFET model, in (a) Linear scale and (b) logarithmic scale. Compact model: lines; numerical simulations: Symbols.

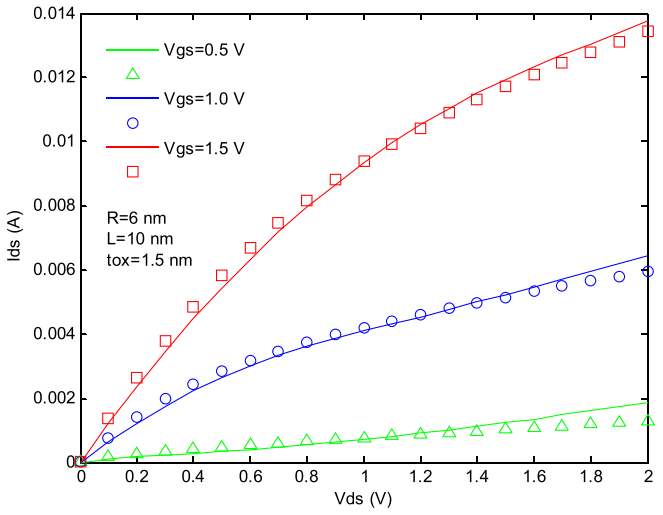

FIG. 3. Drain current versus drain-voltage of short-channel undoped SRG MOSFET model. Compact model: lines; numerical simulations: Symbols.

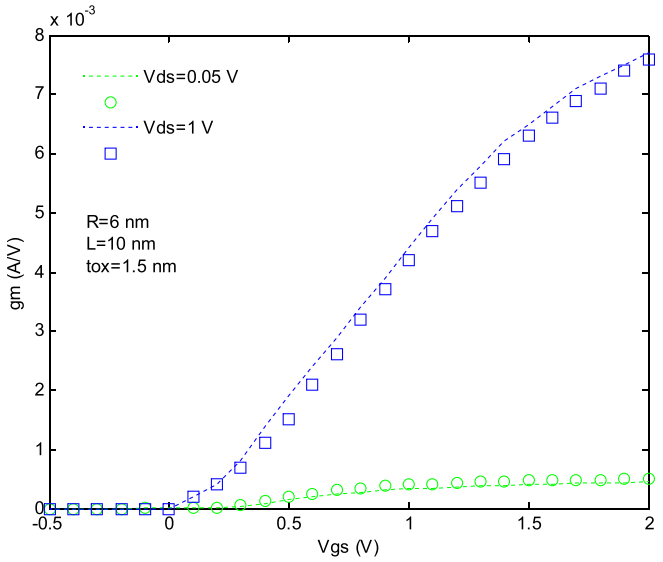

FIG. 4. Transconductance versus gate voltage, for short-channel undoped SRG MOSFET model. Compact model: lines; numerical simulations: Symbols.

at low and high drain voltage. Fig. 2(b) demonstrates the modeled drain current in logarithmic scale versus gate voltage compared with the 3D simulation. We can see that the DIBL, V_T Roll-off, and subthreshold slope are well included in the drain-current model and with the considered fitting parameters. We can also observe that the shift on the threshold voltage due to the DIBL-Roll off is very important in 10 nm channel length of device, and it is well described by the presented drain-voltage characteristic.

Fig. 3 shows the modeled drain current versus drain voltage compared with the 3D numerical simulation. For Vgs = 0.5 V, 1 V, and 1.5 V, good agreement is also found compared with 3D simulation for short-channel device of 10 nm channel length. Fig. 4 illustrates the transconductance versus gate voltage for a device of 10 nm channel length and for Vds = 0.05 and 1 V. Compared with the 3D numerical simulation, good agreement is found for low and for high drain voltage. In Fig. 5, we also illustrate the variation of the conductance versus drain voltage for low and high gate voltage Vgs = 0.05 and 1 V, compared with the 3D simulation, the agreement is satisfactory. As shown in Fig. 6, for a channel length of 20 and 30 nm, the output characteristic agrees well with 3D numerical simulation, especially in the above threshold voltage region through the fitted parameters of CLM effect. In Fig. 7, we can observe the accuracy of the modeled drain current of short-channel device for different channel silicon lengths (L = 10, 20, and 30 nm). As we can see, the I-Vg has a good behavior from subthreshold to above threshold voltage regime and for different channel silicon lengths. The modeled drain-current agree well with the 3D numerical simulation.

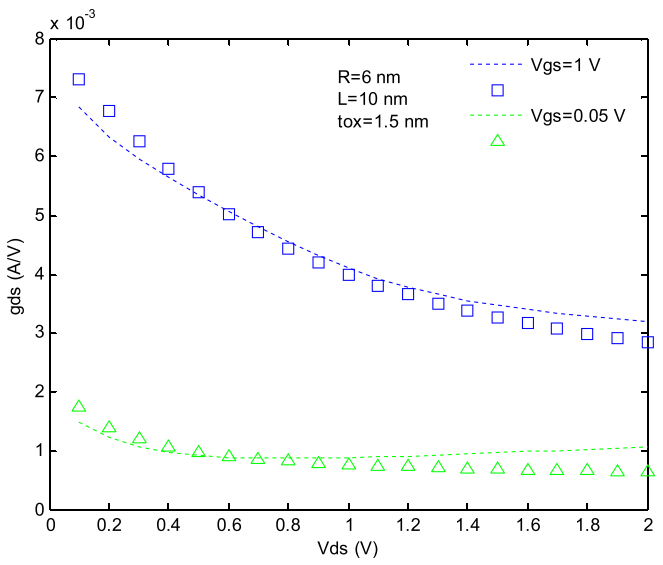

FIG. 5. Conductance versus drain voltage for short-channel undoped SRG MOSFET model. Compact model: lines; numerical simulations: Symbols.

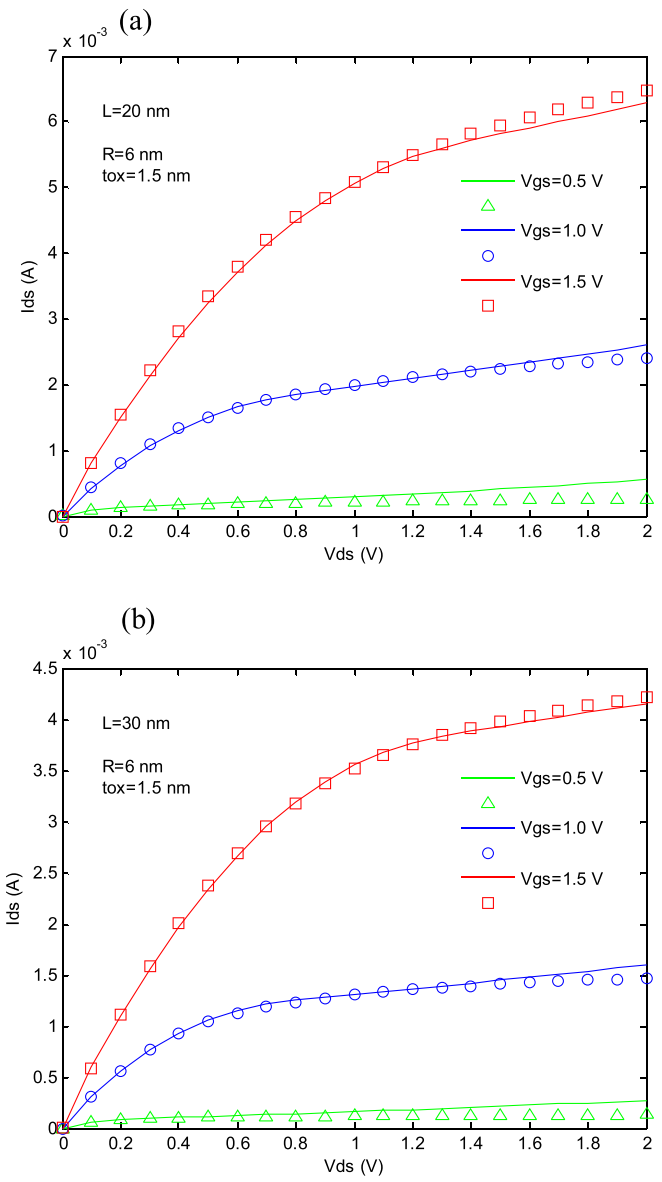

FIG. 6. Drain current versus drain-voltage of short-channel undoped SRG MOSFET model for: (a) Channel length of 20 nm; (b) channel length of 30 nm. Compact model: lines; numerical simulations: Symbols.

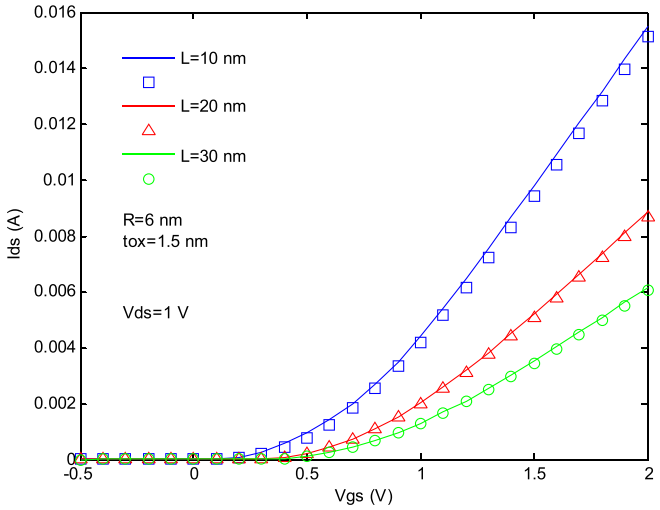

FIG. 7. Drain current versus gate-voltage of short channel undoped SRG MOSFET model for different channel lengths. Compact model: lines; numerical simulations: Symbols.

VI. CONCLUSION

A compact drain-current model for short-channel undoped SRG SOI MOSFETs has been presented. The drain-current model takes into account the short-channel effects, such as the DIBL, V_T Roll-off, the subthreshold slope degradation, and the channel length modulation. The mobile charge density is calculated using analytical expressions of the surface potentials and difference of potentials model. The proposed drain-current model has brought a number of interesting advantages which are summarized as follows: The short-channel effects are modeled using simple analytical expressions, the drain-current model is calculated with a fast computation time and without any iterative methods, and the compact drain-current model has a small number of fitting parameters (λ,τ, and μ_0). These advantages give the opportunity for the model to be used in circuit design application and also for circuit simulation. The transfer and the output characteristics of the model are compared with 3D numerical simulation, and good agreement was found from subthreshold to above threshold voltage regime.

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