Energy Management DC System Based on Current-Controlled Buck-Boost Modules

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***Abstract*—This paper presents the design guidelines of a series hybrid fuel cell system, including control and protection loops. This hybrid system consists of a fuel cell (FC), an auxiliary storage device (ASD), and current-controlled DC–DC converters responsible for managing the energy transfer between the FC, the ASD, and the load. The main advantages of the selected converter are its voltage step-up and step-down properties, high efficiency, and low input and output current ripples, which enable it to be positioned in all system locations, provided the corresponding controllers are suitably designed. Also, using the same module for all system converters simplifies the design and construction tasks. The theoretical analyses have been verified by simulations and validated experimentally on a 48 V 1500 W purpose-built DC bus.**

***Index Terms*—Current control, DC–DC power converters, digital control, energy management, fuel cell, power conditioning, power system control.**

I. Introduction

CENTRALIZED generation coexists today with a new tendency given by environmental considerations and topological flexibility. This new model, known as distributed generation (DG), is characterized by a small generation size. The generating equipment is usually renewable or, at least, presents similar characteristics to those of efficient and environmentally friendly systems [1], [2]. Proton exchange membrane fuel cell (PEMFC) systems are good candidates for supplying electrical power in DG systems [3], residential environments [4], electric vehicles [5], [6], and DC bus applications [7].

However, the relatively short lifespan of PEMFCs represents a significant barrier for their commercialization in both stationary and mobile applications [8], [9]. The literature shows several possible causes of FC power degradation, e.g., the corrosion and contamination of components, poor water management, current ripple, and oxygen starvation [10]. A PEMFC stack is a complex system that requires an auxiliary power-conditioning system to ensure safe, reliable, and efficient operation under different operating conditions. It is important to keep the membrane humidified in order to improve performance and extend the lifetime of a PEMFC. To mitigate PEMFC problems caused by flooding or drying, a boost-cascade-buck converter, which selects its most suitable operating point to avoid these issues, is proposed in [11]. A bidirectional isolated DC–DC converter controlled by phase-shift angle and duty cycle was designed and analyzed in [12] to favorably limit the input current ripple for the FC.

The PEM stack is considered slow because its dynamics are limited by the mechanical devices (mainly a compressor) that supply the air-flow (oxygen) to the cathode. As a consequence of the dynamic response limitations, a load transient could cause a short-duration large-voltage drop, which is characteristic of the oxygen starvation phenomenon that could be harmful for the PEMFC [13]. Prevention of this undesired phenomenon has been addressed experimentally by two approaches. The first of these focuses on airflow rate control by means of a model predictive control [14]–[17]. One disadvantage of this strategy is that the air compressor dynamics may be much slower than the variations in the load current. This makes it impossible to avoid sags in the oxygen excess ratio after large and fast load transients [15], which can lead to the appearance of oxygen starvation phenomena. The second approach uses batteries, capacitors, or other ASDs to ensure a fast dynamic response to any load power transient. These systems prevent the oxygen starvation phenomenon by limiting the slew-rate (SR) of the FC current by means of current-controlled DC–DC converters [18]. This set of elements, known as a FC hybrid system, are needed to support the operation of the FC [19].

In [20] and [21], a single boost converter stage was used to regulate the DC bus voltage and limit the SR of the FC current. This FC hybrid system requires an oversized ASD to supply fast load transients and an additional circuit capable of limiting the SR of the FC current during startup and shutdown. In this paper, we propose a series hybrid topology (shown in Fig. 1) to prevent the problem of oxygen starvation. This topology also reduces the ASD size and increases the bandwidth of the DC bus voltage v_o regulation loop. The key element in this topology is the noninverting buck-boost DC–DC switching converter introduced in [22] along with the current control proposed in [23] and improved in [24]. The use of this converter module in a DC multistage system is presented for the first time in this paper. The main characteristics of the modular converter are: its voltage step-up and step-down properties, high efficiency, and low input and output current ripples. This module can control the input or the

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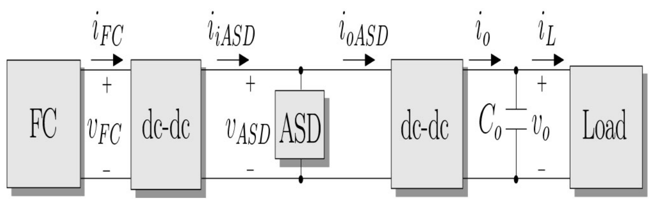


Fig. 1. Fuel cell series hybrid topology simulated and implemented in this paper.

output current with a wide bandwidth, thus making the design of the different protection and regulation loops required from the master controller easier. Thanks to all the above features, this module can be positioned at any of the converter locations in the fuel cell hybrid system illustrated in Fig. 1. Since each converter has its own low-level analog current controller, the main system control loops in the master controller, which regulate v_o, v_{ASD} and i_{FC}, have been designed independently, thus avoiding the complex master algorithms reported in [25]–[27].

The master control stage can be designed and implemented either in an analog [28] or in a digital [29] way. The improvement in processing capability goes together with the increasing importance of digital control techniques and decreasing costs [30]. The main advantages of digital control implementation over analog control implementation are its greater sensibility and better reliability, reduced effects of noise and disturbances, compactness, light weight, and programming flexibility. All these advantages enable the complex design and implementation tasks of the various controls and protections of the system illustrated in Fig. 1 to be simplified.

The design procedure and digital implementation of the master controller, together with the selection of the FC system elements in Fig. 1 are presented in Section II of this paper. Thorough experimental and simulation results are provided and discussed in Section III. Finally, our main conclusions are summarized in Section IV.

II. Fuel Cell Series Hybrid System Design

A. Auxiliary Storage Device

As mentioned above, since the dynamics of PEMFC are slow, a fast load transient could trigger oxygen starvation. We have chosen an electrolytic capacitor C_{ASD} over a battery as the auxiliary storage device because its higher charge and discharge rates are better able to improve the performance of the FC hybrid system. The idealized experimental behavior illustrated in Fig. 2 is used to size the required energy storage. The design is based on a load power P_o variation from zero to the maximum FC power P_{FCmax}, which will be initially given by C_{ASD} because the safe operation of the FC requires its power P_{FC} and current i_{FC} SRs to be limited using a DC–DC current-controlled switching converter. In accordance with the FC current minimum SR (SR_{FCu}) given in Table I, a power-up time T_{FCu} of 2 s is set as shown in Fig. 2. In the same way, a load power variation from P_{FCmax} to zero requires enough energy to be stored in the capacitor to guarantee a FC power-down time T_{FCd} of 0.5 s (see Fig. 2).

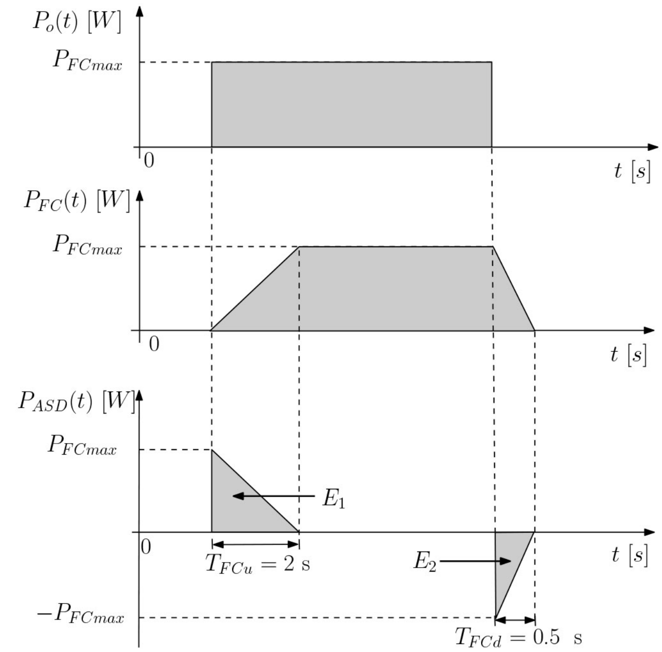


Fig. 2. Power profiles $P_o(t)$, $P_{FC}(t)$, and $P_{ASD}(t)$ used to calculate the ASD capacitor.

TABLE I
FC Series Hybrid System Specifications

Parameter	Value	Units	Description
V_{FCmin}	32.0	V	FC minimum voltage
V_{FCmax}	51.2	V	FC maximum voltage
V_{oref}	48.0	V	Output voltage reference
V_{ASDref}	50.0	V	ASD voltage reference
V_{ASDmin}	25.0	V	ASD minimum voltage
V_{ASDmax}	57.0	V	ASD maximum voltage
$-SR_{FCd}$	-32.0	A/s	FC current minimum SR
SR_{FCu}	8.00	A/s	FC current maximum SR
$P_{o\,\max}$	1.50	kW	Output maximum peak power
$P_{FC\,\max}$	500	W	FC peak power
C_o	2.350	mF	Dc bus capacity
C_{ASD}	600	mF	ASD capacity
$I_{\max}$	16.0	A	Converters maximum current
$\omega_o/2\pi$	2.37	kHz	v_o loop bandwidth
$\omega_{ASD}/2\pi$	1.33	Hz	v_{ASD} loop bandwidth

The electrolytic capacitor value is therefore calculated by considering its discharging and charging intervals, which correspond to energies E_1 and E_2, respectively

$$
\begin{aligned}
|E_1| &= \frac{P_{FCmax}\ T_{FCu}}{2} \leq \frac{C_{ASD}\left(V_{ASDref}^2 - V_{ASDmin}^2\right)}{2} \\
|E_2| &= \frac{P_{FCmax}\ T_{FCd}}{2} \leq -\frac{C_{ASD}\left(V_{ASDref}^2 - V_{ASDmax}^2\right)}{2}.
\end{aligned} \tag{1}
$$

The required auxiliary storage capacitance C_{ASD} should be the greater of the two values obtained from the absolute

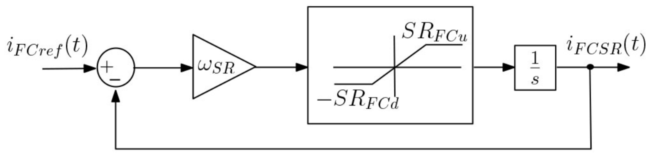


Fig. 3. FC slew-rate (SR) limiter used to avoid the oxygen starvation phenomenon.

charge and discharge energies in (1). In this way, we selected a 600 mF commercial capacitor with an equivalent series resistance (ESR) of 1 mΩ.

B. Fuel Cell Current Slew-Rate Limitation

To avoid the undesired oxygen starvation phenomenon, we implemented the FC current SR limiter whose block diagram is shown in Fig. 3. While the FC SR current is within the range $(-SR_{FCd}, SR_{FCu})$, the limiter works as a low-pass filter and its corresponding transfer function is given by

$$H_{SR}(s) = \frac{i_{FCSR}(s)}{i_{FCref}(s)} = \frac{\omega_{SR}}{s + \omega_{SR}} \tag{2}$$

where the ω_{SR} pole must be selected so that the crossover frequency is greater than the ASD voltage loop control bandwidth and smaller than the quantization noise frequency. This parameter has been set experimentally at 157 rad/s.

C. Output DC Bus Capacitor

The sizing criteria for the output capacitor C_o, which is regulated at 48 V, are presented in this subsection. The C_o value was selected following the recommendations of the European Cooperation for Space Standardization (ECSS) [31] concerning output impedance specifications. These specifications allow a 1% voltage change under a 50% load perturbation, which is defined as

$$Z_{o\,\max} = \frac{\Delta v_o}{\Delta i_o} = \frac{0.01 v_o}{0.5 P_o / v_o} = \frac{0.02 v_o^2}{P_o} = 30\ \text{m}\Omega. \tag{3}$$

Following the same specifications, the value for C_o is obtained from

$$\frac{1}{\omega_o C_o} \leq Z_{o\,\max} \tag{4}$$

where ω_o is the crossover frequency of the bus voltage loop. A minimum C_o value has been calculated according to the FC system specifications in Table I. Finally, by connecting several commercial capacitors in parallel to ensure a low ESR value, a bus capacitance of 2.35 mF with an ESR of 11.8 mΩ has been achieved.

The DC bus small-signal block diagram enables the output voltage to be controlled as shown in Fig. 4. In this figure, the transfer function $G_{CVo}(s)$ is the PI controller that regulates the bus voltage v_o, which is described in the next section. The closed loop converter transfer function $H_i(s)$ obtained from [23] can be modeled as a second-order low-pass filter

$$H_i(s) = \frac{\hat{i}_o(s)}{\hat{i}_{oref}(s)} = \frac{\omega_{ci}^2}{s^2 + 2\zeta\omega_{ci}s + \omega_{ci}^2} \tag{5}$$

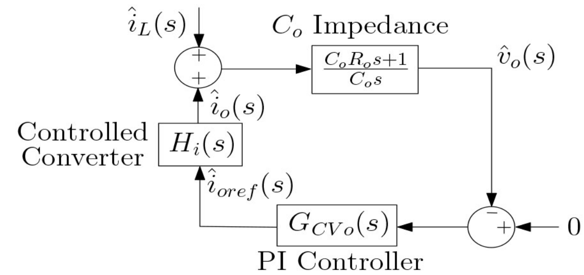
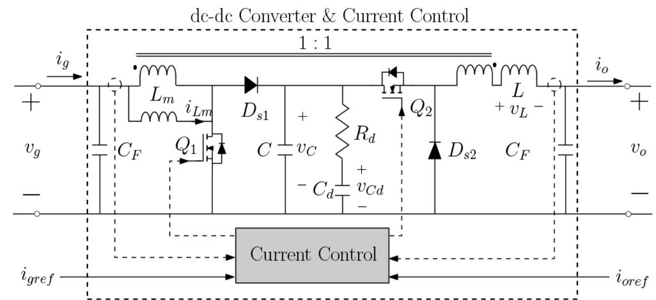
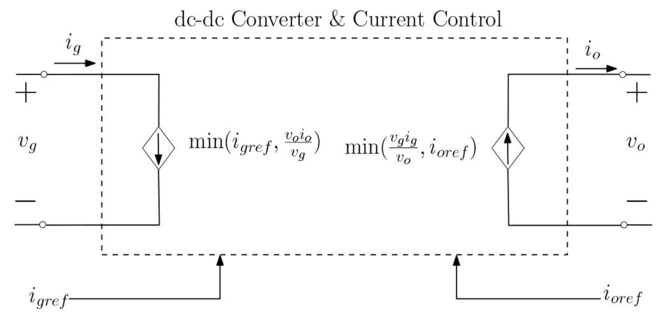


Fig. 4. Small-signal block diagram of the bus voltage v_o regulation loop.



(a)



(b)

Fig. 5. Proposed modular buck-boost converter and its respective current control. (a) Switching model to study short-time simulations. (b) Block diagram to study long-time simulations.

where ω_{ci} is the natural frequency with a value of $2\pi 8$ krad/s and ζ is the damping ratio with a value of 0.44.

D. Switching DC–DC Converters

The key element in this PEMFC hybrid system is a modular buck-boost converter that is capable of adapting the different unregulated voltages of source-like elements such as the FC and the ASD. Depending on the operating point of the PEMFC, the state of charge of C_{ASD}, and the desired DC bus voltage, the converters operate in buck ($v_{FC} > v_{ASD}$), ($v_{ASD} > v_o$) or boost modes ($v_{FC} < v_{ASD}$), ($v_{ASD} < v_o$). The reduced input current ripple of the FC-connected converter is also favorable for the FC operation and lifetime. Its input current regulation enables the FC current SR to be limited very easily. Moreover, the wide bandwidth output current control provides good load regulation with short-circuit protection without increasing the computing load at the master controller. The current control also facilitates the parallel connection of converter stages. All these properties (buck and boost modes, low current ripple, high bandwidth, short-circuit protection,

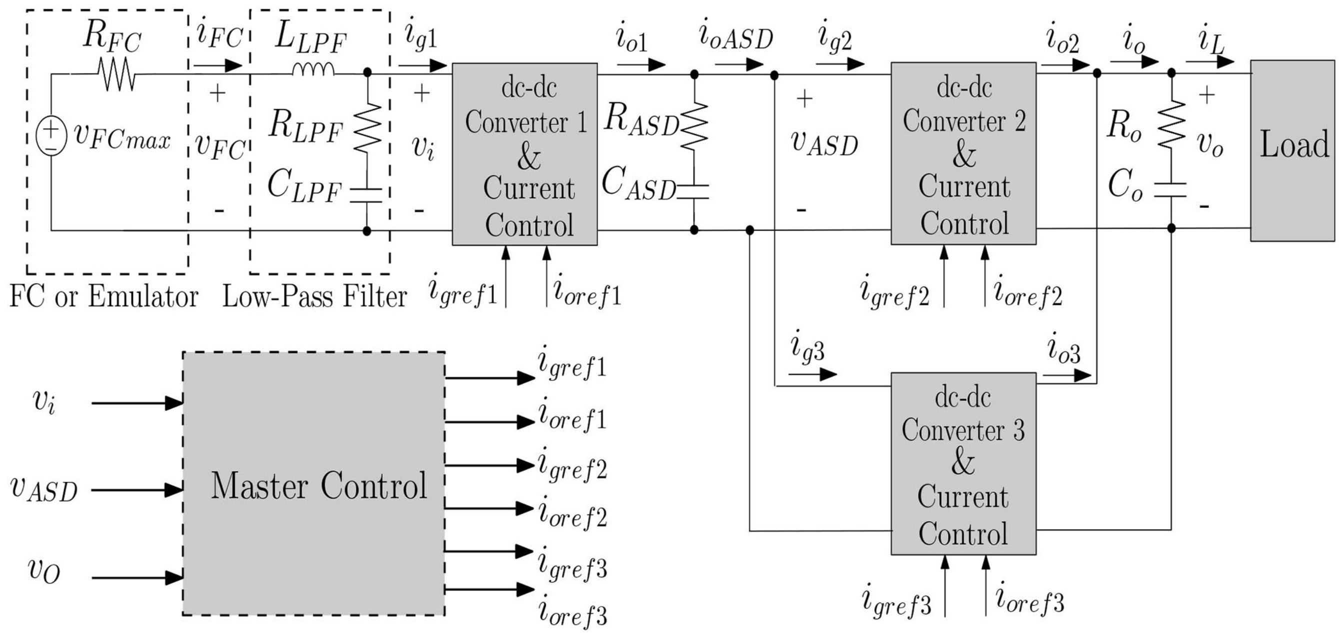


Fig. 6. FC series hybrid topology circuit. The FC system elements are FC or emulator, second order low-pass filter, modular buck-boost converters 1, 2, and 3, ASD capacitor C_{ASD}, DC bus capacitor C_o, and load. The master control regulates the input/output port voltages from each converter using the current reference values.

current regulation, and parallel-easy) make the converter an excellent choice as a building block for all the converters required in the PEMFC hybrid system.

The converter has two different models depending on the required time scale. The first one shown in Fig. 5(a) is a dynamic model that enables the study of the short-time transitions. The second, shown in Fig. 5(b), is a static model for making long-time simulations. The buck-boost converter shown in Fig. 5(a) combines a boost stage in cascade with a buck stage, with magnetic coupling between input and output inductors. A detailed study of the mathematical model, component values, and main characteristics of this converter has been presented in [23]. Additional input and output 22-μF 100 V film capacitors C_F have been added to each converter to avoid propagating high frequency current components through the wiring, thus reducing EMC-related problems.

Fig. 6 presents the circuit diagram implementation of the FC series hybrid topology shown in Fig. 1 using the same current-controlled buck-boost module as converters 1, 2, and 3. The high-side current sensors on these modules, indicated in Fig. 5(a) enable the parallel connection of converters 2 and 3 shown in Fig. 6, thus increasing the system peak power and improving its reliability. If one of the two converters connected in parallel fails, the system will still be operational, though the maximum output peak power will be lower.

E. Digital Master Controller

The digital master control block shown in Fig. 6 sends the current references to the analog current loops of each converter to regulate the different voltages of the system. The aims of the master control include FC SR current limitation, FC, and capacitor range voltage protection, output voltage v_o regulation

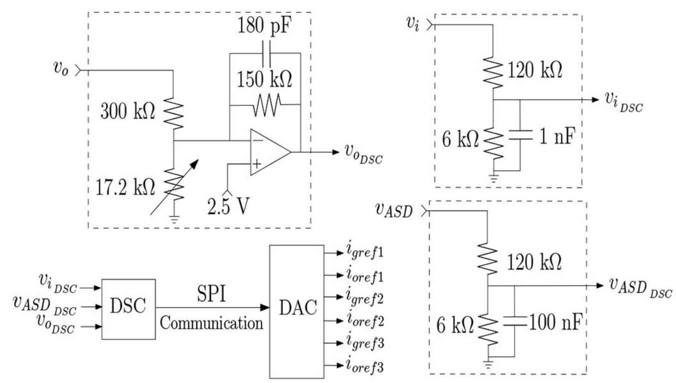


Fig. 7. Master control diagram circuit.

at 48 V, maximum current limitation in each converter, and safe startup and shutdown of the system. The master control has been implemented on a Texas Instruments TMS320F28335 digital signal controller (DSC) which is represented in Fig. 7 as a block together with voltage sensor stages and digital to analog converters (DACs). Detailed block diagrams of the master control loops required to regulate and protect the FC, the ASD, and the bus voltages of the hybrid topology are shown in Fig. 8. The master control specifications and analog parameters are listed in Tables I and II, respectively. The design expressions in Table II are a first approach for determining the parameters of the FC system control loops, from which some of the parameter values have been refined through a frequency analysis conducted with MATLABs SISO tool. The parameters in Table II without a simplified design expression have been determined by simulations and SISO tool stability analyses.

The bilinear transformation enables conversion from the analog PI controllers in Fig. 8 to the digital controllers to

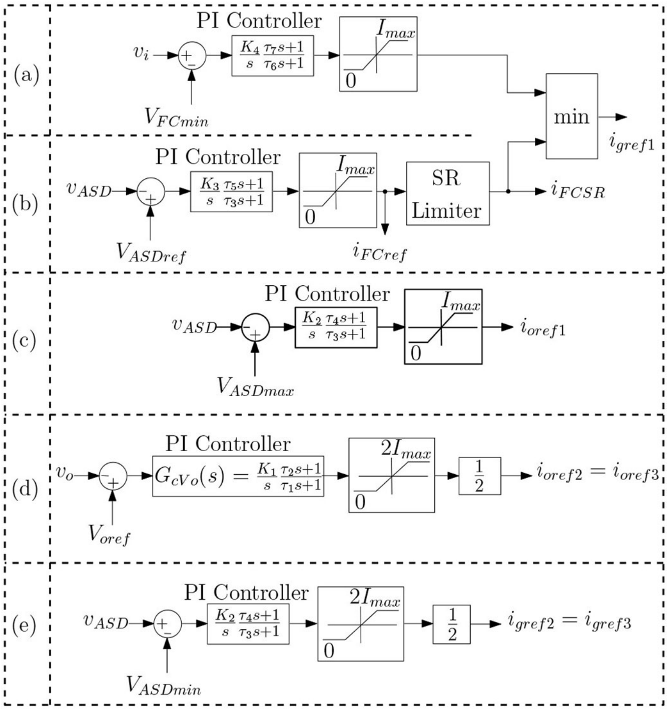


Fig. 8. FC series hybrid system control and protection block diagrams. (a) and (b) The FC minimum voltage V_{FCmin} and the ASD voltage reference V_{ASD} are limited and regulated by means of i_{gref1}. (c) ASD maximum voltage protection loop. (d) Output voltage v_o regulation loop. (e) ASD minimum voltage protection loop.

be implemented by the DSC. The general z-transfer function $G_C(z)$ for all the PI controllers with period T_s is given by

$$G_C(z) = \frac{y(z)}{e(z)} = G_C(s)\Big|_{s=\frac{2(1-z^{-1})}{T_s(1+z^{-1})}} = \frac{b_0 + b_1 z^{-1}}{1 - z^{-1}} \tag{6}$$

where the PI controller recurrence relation in the linear zone can be expressed as

$$y_n = y_{n-1} + b_o e_n + b_1 e_{n-1}. \tag{7}$$

The integral windup of the PI controllers can be addressed if their outputs $y_{n,limited}$ are bounded by $Ymin$ and $Ymax$, that is

$$y_{n,limited} = \begin{cases} y_n & Ymin \leq y_n \leq Ymax \\ Ymin & y_n < Ymin \\ Ymax & y_n > Ymax. \end{cases} \tag{8}$$

All the additional poles were implemented with analog circuits to reduce the computational costs and time-delays of the digital controls. These poles, which work as anti-aliasing low-pass filters, are required because the switching frequencies of the converters are not synchronized.

III. Simulation and Experimental Results

Once the FC system parameters have been designed and the controls have been implemented, specific experiments must be conducted to verify the correct performance of the entire system. These experiments are the FC system's startup and shutdown, its operation under load transients, and the system protection, which are illustrated in Sections III-A–C, respectively. Finally, Section III-D reports experiments of the

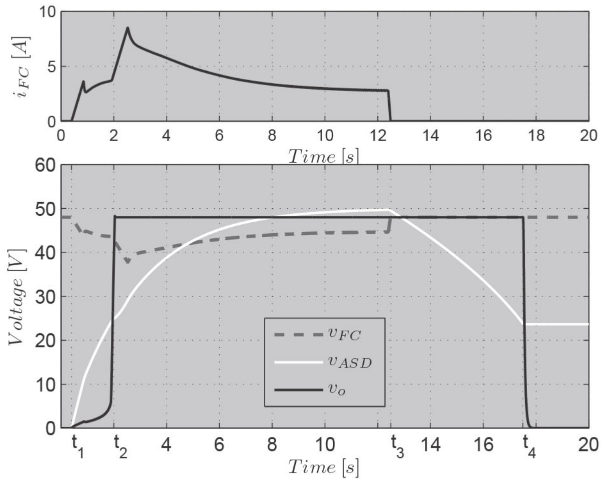
TABLE II
Loops Parameters of FC Series Hybrid System Master Control

Parameter	Design Formula	Value	Units
K_1	$C_o\omega_o$	34.9	A/(V·s)
K_2	-	11.0	A/(V·s)
K_3	$C_{ASD}\omega_{ASD}$	5.00	A/(V·s)
K_4	-	4.00	A/(V·s)
ω_{SR}	-	157	rad/s
τ_1	C_oR_o	27.7	μs
τ_2	$10/\omega_o$	672	μs
τ_3	$C_{ASD}R_{ASD}$	600	μs
τ_4	-	100	ms
τ_5	$10/\omega_{ASD}$	1.20	s
τ_6	-	22	ns
τ_7	-	159	ms

series hybrid topology connected to a Nexa PEMFC from Ballard, rather than using the FC emulator or the FC Thévenin equivalent circuit [32] used in the first three subsections.

A. FC Hybrid System Startup and Shutdown

The first experiment tested the FC system's startup and shutdown in comparison with the simulation presented in Fig. 9(a). The simplified modular buck-boost converter from Fig. 5(b) was used in the simulation. In the experiment, a FC emulator was used instead of the real fuel cell. Fig. 9(a) shows how initially the capacitor was discharged until t_1, where the fuel cell started up and the capacitor began to charge. The figure shows how the FC current had an appropriate slew-rate SR_{FCu} and the output voltage v_o was not yet regulated because the capacitor had not reached its minimum voltage V_{ASDmin} of 25 V. The control loops active during this interval therefore corresponded to those presented in Fig. 8(b) and (e). At instant t_2, the capacitor reached V_{ASDmin}, v_o was then regulated at $V_{oref} = 48$ V by means of the control loop of Fig. 8(d), and the fuel cell current SR continued to be limited. Between t_2 and t_3 the capacitor continued charging until it reached its reference value V_{ASDref} of 50 V because the control loop presented in Fig. 8(b) was active. After the corresponding signal was applied at t_3, the fuel cell shut down with a correct current slew-rate SR_{FCd}, and the output voltage v_o continued to be regulated until the voltage capacitor decreased to V_{ASDmin}, which occurred at t_4. Finally, the master control tried to regulate the minimum voltage capacitor from t_4 onward. The corresponding experimental result shown in Fig. 9(b) is in good agreement with the simulation. Both the experimental and the simulated figures, illustrate that the slew-rates SR_{FCu} and SR_{FCd} of the FC current were limited correctly, the output and capacitor voltages were well regulated, and the integral windup effect was properly managed, as can be seen at instant t_2. In the FC system's startup and shutdown experiment, and in the remaining ones, the V_{FCmin} and V_{ASDmax} protection loops of Fig. 8(a) and (c) did not need to be activated by the



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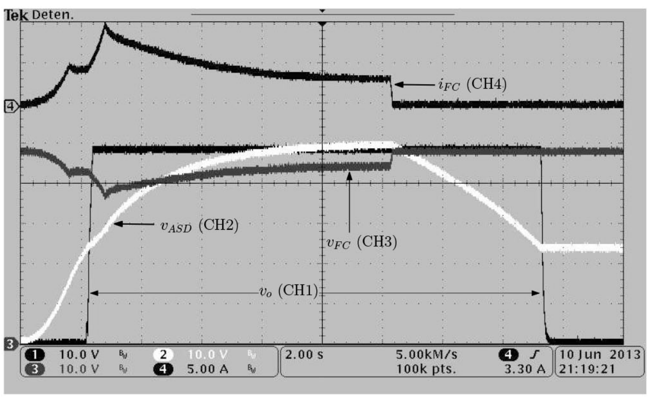
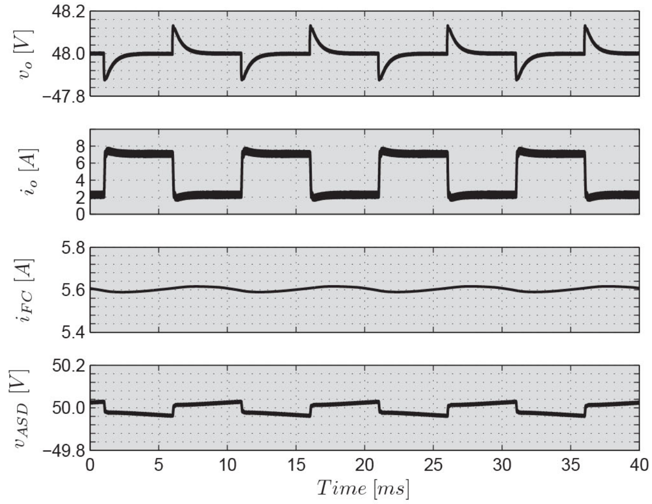


(b)

Fig. 9. FC system startup and shutdown with a constant resistance load of 22.6 Ω. (a) PSIM simulation. (b) Experimental measurement. CH1: DC bus voltage v_o (10 V/div). CH2: ASD voltage v_{ASD} (10 V/div). CH3: FC voltage v_{FC} (10 V/div). CH4: FC current i_{FC} (5 A/div). Time base of 2 s.



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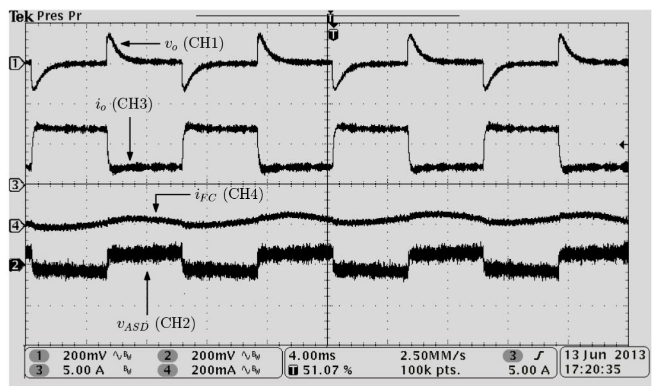

(b)

Fig. 10. FC system below a pulsating load power profile, with $I_{FC} = 5.57$ A, $V_{ASD} = 50$ V and $V_o = 48$ V as mean values. (a) PSIM simulation. (b) Experimental measurement. CH1: bus voltage v_o (200 mV/div, AC coupling). CH2: ASD voltage v_{ASD} (200 mV/div, AC coupling). CH3: Output current i_o (5 A/div). CH4: FC current i_{FC} (200 mA/div, AC coupling). Time base of 4 ms.

master control. Although not included in this paper, the correct activation and performance of these protections were also tested.

B. FC Hybrid System Operation Under Load Transients

The second experiment conducted verified output impedance ECSS specification (3) by applying the load resistance changes from 22.6 Ω to 7.2 Ω with a frequency of 100 Hz and a 50% duty cycle shown in Fig. 10(a). During the experiment, the master control loops of Fig. 8(b) and (d) satisfactory regulated the capacitor voltage V_{ASD} and the output voltage v_o to 50 V and 48 V, respectively. In the simulation, the switching model of the buck-boost converter presented in Fig. 5(a) was used while the experiment was carried out using the PEMFC emulator instead of the real fuel cell. The experimental result presented in Fig. 10(b) is in a good agreement with the simulation. The DC bus impedance has been designed, according to (3), to be less than or equal to 30 mΩ. This was achieved since Fig. 10(b) shows that an output current change Δi_o of 5 A caused an output voltage transient Δv_o of 150 mV. In addition, the capacitor voltage exhibited a peak ripple of less than 40 mV due to the capacitor's ESR. Also, as Fig. 10(b) shows, the fuel cell current ripple was very small.

The next experiment tested the FC hybrid system under large periodic load variations, which produce repetitive capacitor charging and discharging cycles. A step-like load variation from 22.6 Ω to 2.4 Ω with a frequency of 0.5 Hz and a 10% duty cycle was applied to obtain the simulation and experimental results shown in Fig. 11. The simplified buck-boost converter model from Fig. 5(b) was used in the simulation. The maximum fuel cell power was 512 W, which is in agreement with the product of the FC parameters V_{FCmin} and I_{max} in Table I. However, the large variations required a load peak power of 850 W, which produced a charge and discharge of the capacitor. Fig. 11 shows that the bus voltage and the fuel cell current were well regulated and limited during this demanding experiment. The figure also shows good agreement between the experimental data and the simulation results.

C. FC System Protection

The first experiment in this subsection used a low nominal resistance load of 50 mΩ, connected in series with an ON-state

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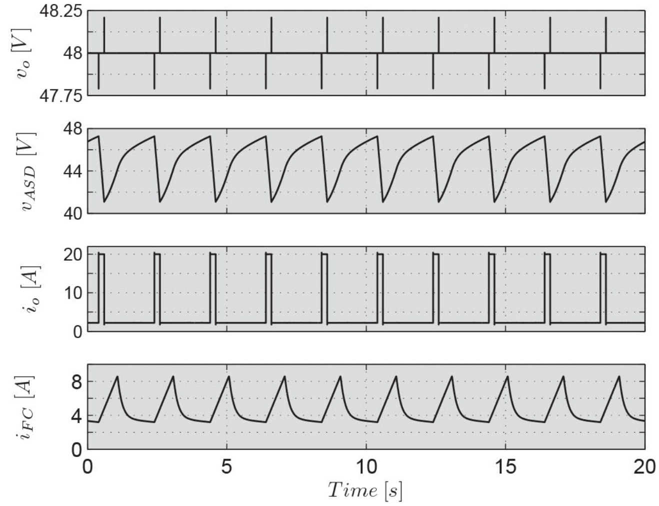

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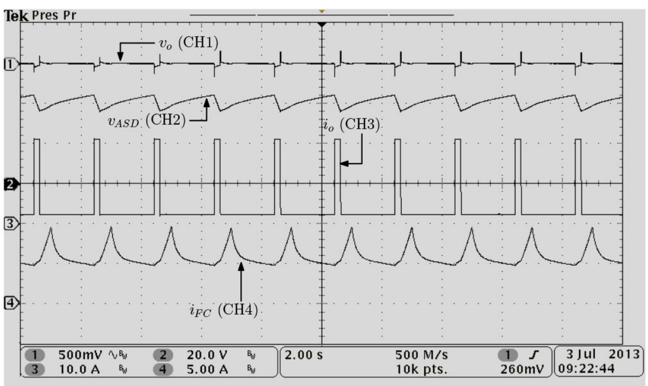
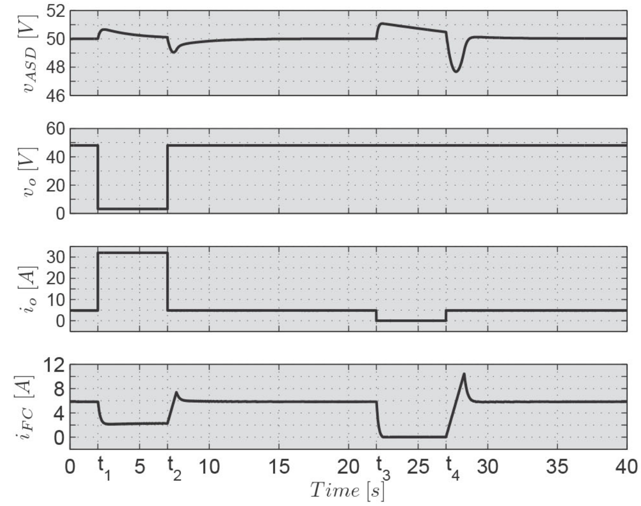


(b)

Fig. 11. Large load variations from 22.6 Ω to 2.4 Ω, with a frequency of 0.5 Hz and a 10% duty cycle that produce the capacitor charge and discharge. (a) PSIM simulation. (b) Experimental measurement. CH1: DC bus voltage v_o (500 mV/div, AC coupling). CH2: ASD voltage v_{ASD} (20 V/div). CH3: Output current i_o (10 A/div). CH4: FC current i_{FC} (5 A/div). Time base of 2 s.



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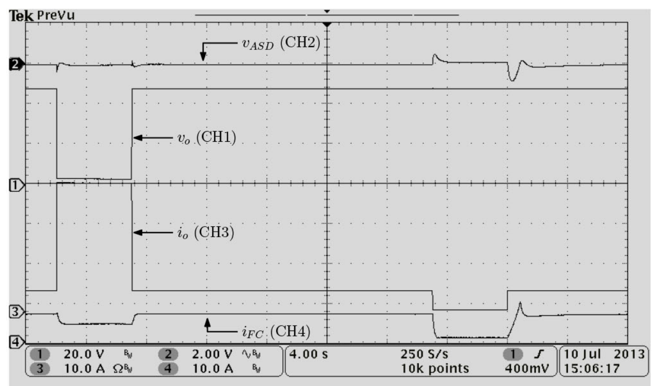

(b)

Fig. 12. Controlled short circuit and open circuit on the load side with a duration of 5 s each. (a) PSIM simulation. (b) Experimental measurement. CH1: DC bus voltage v_o (2 V/div). CH2: ASD voltage v_{ASD} (2 V/div, AC coupling). CH3: Output current i_o (10 A/div). CH4: FC current i_{FC} (10 A/div). Time base of 4 s.

N-channel MOSFET as a practical solution for emulating a real and removable short-circuit. The same circuit was used in the corresponding simulation. Fig. 12(a) shows, together with the results for the emulated short-circuit, the response obtained with an open circuit as the load. The simulation was performed using the simplified modular buck-boost converter model of Fig. 5(b) in order to avoid using a small time-step. Fig. 12(a) shows how initially v_o and v_{ASD} were regulated at V_{oref} and V_{ASDref}, respectively. Between t_1 and t_2 the very low resistance load was connected and the output current i_o limited correctly, with a maximum value of 32 A, given that each of the parallel connected DC–DC converters (2 and 3) contributed with a maximum current I_{max} of 16 A. In the (t_3, t_4) time interval, all the loads were disconnected and the output current i_o was equal to zero. Both the emulated short-circuit and the open circuit situations show that the FC current slew-rates SR_{FCu} and SR_{FCd} were limited correctly.

In the corresponding experimental results shown in Fig. 12(b), once the N-channel MOSFET was turned on, a maximum current of 32.14 A with a minimum voltage of 2.76 V were measured, which corresponds to an applied load of 85.9 mΩ. This load was the result of the aggregation of the MOSFET ON-resistance and the 50 mΩ of the resistor in series. Despite the severity of the experiments, the maximum ASD voltage undershoot was less than 2.9 V. This undershoot was mainly caused by the limitation in the FC current SR, which can be seen in the bottom-right hand side (CH4) of the figure. The FC system recovered its initial operation point smoothly after the ultralow resistance load and the open circuit were removed at t_2 and t_4, respectively.

The main purpose of the simulation depicted in Fig. 13(a) was to illustrate the suitable performance of the V_{ASDmin} loop under an overload variation. At t_1 the load was changed from 22.6 Ω to 4.0 Ω, and the load change was reversed at t_2. The simplified modular buck-boost converter model from Fig. 5(b) was also used in this simulation. The FC system recovered its initial operation point when the overload was removed at t_2. Again, these results are in excellent agreement with the corresponding experimental results shown in Fig. 13(b). The experimental traces were split between two oscillograms due to the limitation in the number of oscilloscope channels. The V_{ASD} signal was included in both

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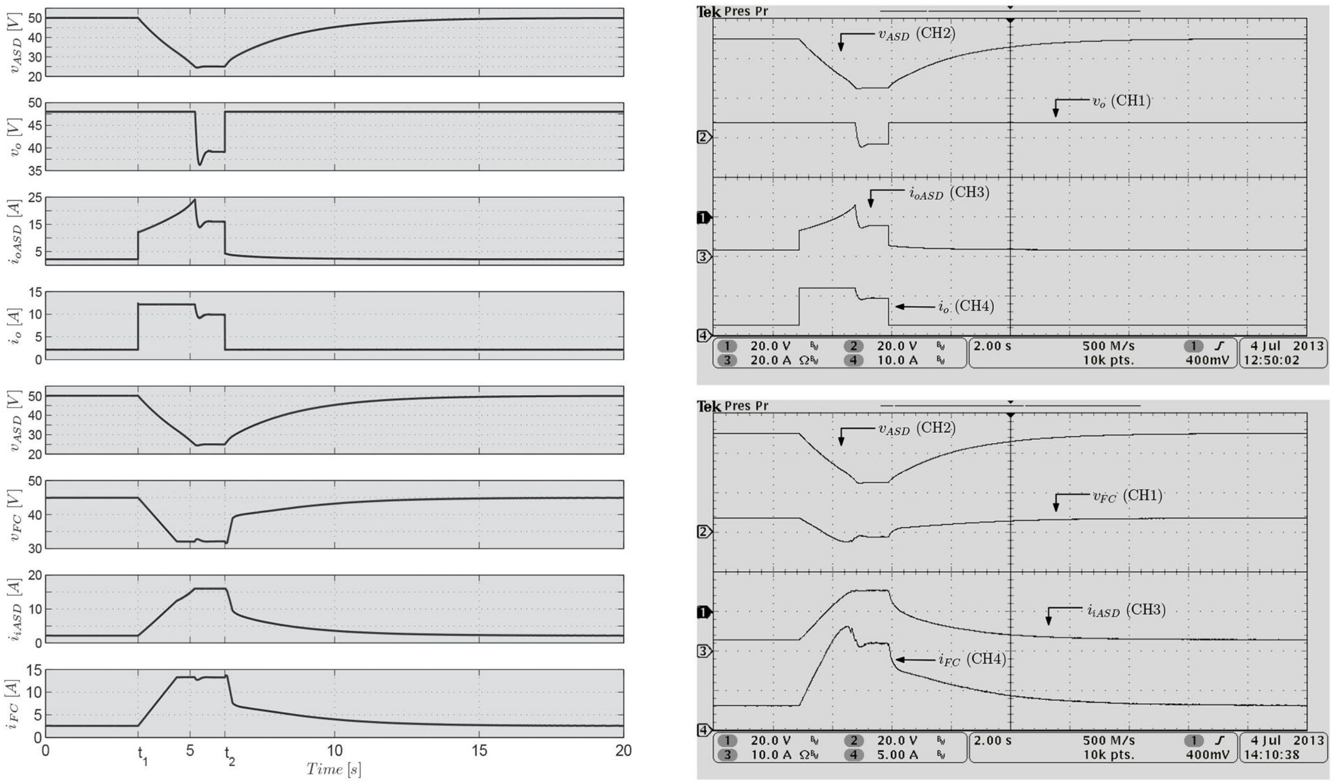
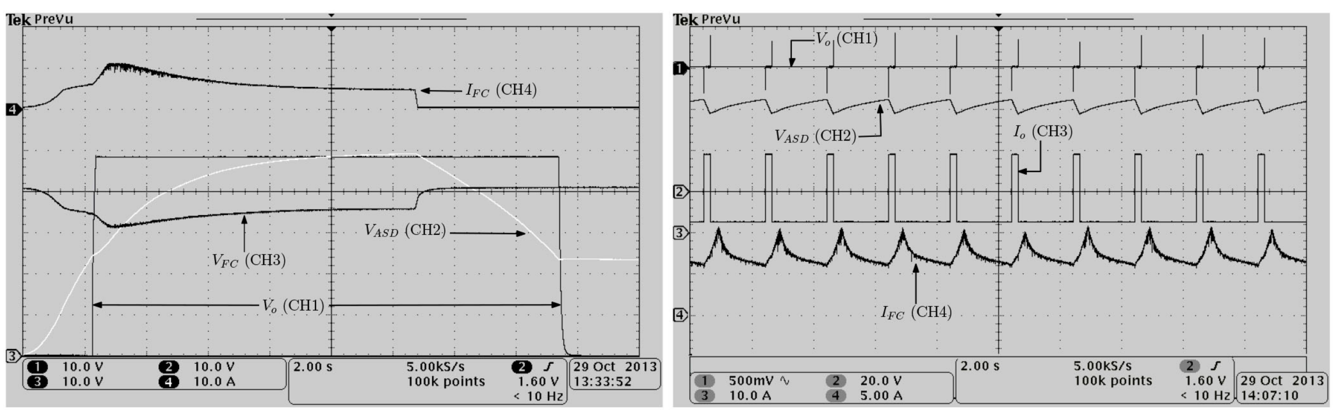


(a) (b)

Fig. 13. Main FC system variables during an overload. (a) PSIM simulation. (b) Experimental measurement. DC bus voltage v_o (20 V/div), FC voltage v_{FC} (20 V/div), ASD voltage v_{ASD} (20 V/div), ASD output current i_{oASD} (20 A/div), ASD input current i_{iASD} (10 A/div), output current i_o (10 A/div), FC current i_{FC} (5 A/div). Time base of 2 s.



(a) (b)

Fig. 14. FC system using the Nexa PEMFC instead of the FC emulator to illustrate good agreement between them. (a) FC system startup and shutdown with a constant resistance load from 22.6 Ω. CH1: DC bus voltage v_o (10 V/div). CH2: ASD voltage v_{ASD} (10 V/div). CH3: FC voltage v_{FC} (10 V/div). CH4: FC current i_{FC} (5 A/div). (b) Large load variations from 22.6 Ω to 2.6 Ω, with a frequency of 0.5 Hz and a 10% duty cycle that produce the capacitor charge and discharge. Experimental measurement. CH1: DC bus voltage v_o (500 mV/div, AC coupling). CH2: ASD voltage v_{ASD} (20 V/div). CH3: Output current i_o (10 A/div). CH4: FC current i_{FC} (5 A/div). The same time base of 2 s.

oscillograms in order to show that all the signals corresponded to the same experiment. Again, in all experiments in this subsection the FC emulator was used.

D. FC System Using the Ballard's Nexa PEMFC

Once the FC series hybrid system and the protection loops from Fig. 8 had been validated, the FC emulator from Fig. 6 was replaced by the real Nexa fuel cell. The Nexa PEMFC is a fully integrated system that produces unregulated DC power, up to 1200 W, from a supply of hydrogen and air. The FC system specifications in Table I are within the voltage and power ranges that can be provided by the Nexa fuel cell. This subsection presents only the cases in which there were clear visible differences between the emulator and the real fuel cell. Despite the differences, the experimental results shown in Fig. 14(a) and (b) are similar to the start-up and shutdown and large load variation results previously shown in Figs. 9(b) and 11(b), respectively. These results validate the previously used FC emulator as a simplified and acceptable FC model. The differences between the FC emulator and the real FC currents were mainly due to the noise introduced by the auxiliary systems of the Nexa FC, especially the air compressor and the cooling motor [33], which were not taken into account in the simulations.

IV. Conclusion

A FC hybrid series topology and its corresponding digital master control have been designed, simulated, and experimentally validated on a 48 V, 1500 W DC bus platform. Three 800 W current-controlled buck-boost converter modules have been used in this topology to regulate the system voltages and currents. The input and output current reference values of the modules were provided by a digital master controller implemented in a DSC. Five different control loops provided the desired system features, the most relevant of which were the SR limitation of the PEMFC current, the regulation of auxiliary storage capacitor and bus voltages, and the protection of the overcurrent/short-circuit. All these features have been tested by simulations and experiments using both an emulator and a commercial PEMFC. Agreement between the simulation and experimental results was good in all the tests: start-up and shutdown, high and low frequency periodic load transients, and open circuit, short-circuit, and overload transient behavior.

Another contribution of this paper is a simplified block diagram of the converter, which enabled low frequency simulations to be made with reasonable step-size and computation times that would not be achievable using a switched model of the non-inverting buck-boost structure. The modular properties of the buck-boost converter make it a good candidate for analyzing and validating other DG systems in future studies.

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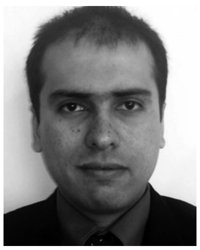

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