



## UMEM-BASED CAPACITANCE MODEL FOR ORGANIC FIELD EFFECT TRANSISTORS: DEVELOPMENT AND IMPLEMENTATION

Alejandra Castro Carranza

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Alejandra Castro-Carranza

**UMEM-BASED CAPACITANCE MODEL FOR  
ORGANIC FIELD EFFECT TRANSISTORS:  
Development and implementation**

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We STATE that the present study, entitled “UMEM-Based Capacitance Model for Organic Field Effect Transistors: development and implementation”, presented by Alejandra Castro Carranza for the award of the degree of doctor, has been carried out under our supervision at the Department of Electronic, Electric and Automatic Engineering of this university, and that it fulfills all requirements to be eligible for the European Doctorate Award.

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- 16.** A. Castro-Carranza, M. Estrada, R. Picos, B. Iñíguez, J. Pallarès, “Charge and capacitance modeling in OTFTs”, Graduated Student Meeting on Electronic Engineering 2009, 18-19 Jun., Tarragona, Spain.
  
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## General Introduction

Organic materials and devices based on small molecules, polymers and composites have received a great deal of attention over the past years. When in the 1970's A. J. Heeger, H. Shirakawa and A. G. MacDiarmid developed a conductive polymer by doping Polyacetylene, their work, which earned them the Nobel Prize in chemistry in 2000, opened to a new era for Electronics where both n-type and p-type semiconductors based on organic molecules were created and employed since then, leading to significant applications in microelectronics [Macdiarmid-1980]. Even more attention was paid to organic semiconductors since their mobility approached that of the amorphous silicon [Y.Lin-1997]and, that different groups of the scientific community, as well as investors, have focused their efforts into the research and improvement of new organic materials and device technology.

Amongst their advantages, organic polymers are cheaper, easier to manufacture, more flexible than their inorganic analogs due to the weak Van der Waals force interacting between organic molecules. In addition the low fabrication costs of organic electronic devices make them appealing for the market place. In spite of their promising advantages and applications where Silicon is not suitable, organic materials present also drawbacks (e.g. the low mobility that causes low performance and the degradation that makes devices reduce their lifetime). This keeps engineers and researchers in a continuous seeking to optimize them somehow before and after applying these materials to devices.

Even so, the possibility for printing circuits completely made of plastics and polymers paves the way for exploiting both innovative and challenging applications for flexible “plastic” devices: organic field effect transistors (OFETs), electrodes, batteries, photovoltaic cells and light emitting diodes (OLEDs). OFETs are of particular interest due to their potential applications in large area and relatively low cost circuits since the circuits based on such devices will be very appropriate for flexible applications such as sensors and displays. In addition, this flexibility will also improve their portability and robustness.

Nevertheless to develop efficient designs of complex integrated circuits based on OFETs, preliminary optimization and modeling is required to provide means for circuit simulation and to study the behavior of devices in order to determine how to improve them. Circuit simulation is an essential tool in designing integrated circuits. The accuracy of circuit simulation depends on the accuracy of the device model. Thus, to this purpose, the availability of accurate analytical models is particularly necessary. Some I-V standard models of OFETs have been already reported to describe the device characteristics, but there is still work to be done in both, charge and capacitance models, which are important to describe their dynamic response.

A dynamic model is necessary to analyze OFETs in order to propose physical parameters able to optimize their real operation efficiency. In order to be of practical usefulness for circuit designers, models should be compact, i.e., they should provide continue, and of course, efficient and accurate algorithms to calculate charges, currents, and their derivatives.

In this thesis we present the development of a compact capacitance model for OTFTs assuming quasi-static operation. For this, we obtained the total charges at the gate, source and drain electrodes, based on the integration of the charge density expressions derived from the solution of the Poisson's equation in Organic Thin Film Transistors (OTFTs). The parameters applied on our capacitance model are the ones extracted from the current-voltage characteristics of the devices by means of the Unified Model and Extraction Method [Estrada-2008a]. For this reason we have called it UMEM-Based Capacitance Model (UBCM).

The dynamic OFET model we present assumes the transistor to be in quasi-static operation, i.e., the charge densities at any position in the channel are assumed to depend on the instantaneous values of the terminal voltages only. If, however, the rate of variation of the terminal voltages is high, the quasi-static approximation is no longer valid. Nonetheless, our capacitance model is one of the few reported in literature, but with several advantages over the others, such as that UBCM is compact, analytical and continuous between the different operation transitions of the OFETs, i.e. from subthreshold to accumulation and from linear to saturation regimes. Also, we validated our capacitance model against experimental data, which had not been done previously in literature due to the complex disordered nature of organic materials. After the development and validation with experimental data, we successfully implemented the UBCM in a circuit simulator by means of its code in Verilog-A.

The thesis is divided into five chapters and four appendixes. For understanding the physical basis of the model we will review in **chapter 1** the operation

principles of OFETs, their electrical characteristics, structures, applied materials and fabrication techniques; as well as the carrier transport characteristics within the organic semiconductors.

Subsequently in **chapter 2** we introduce our model by standing out its advantages and the applied extraction procedure method, comparing it to other capacitance models and extraction procedures reported in literature.

In **chapter 3** the Unified Model and Extraction Method is described in order to identify and understand the parameters used on the UBCM, whose evolution is described subsequently in **chapter 4** by different approximations: from considering only the accumulation operation regime, to be a frequency-dependent model for OFETs valid in accumulation, partial and total depletion regimes. In the same chapter we use the device simulator Atlas from Silvaco to understand the effects of frequency on the capacitance characteristics of the OFETs in order to take them into account in our model.

Finally **chapter 5** presents the successful implementation of UBCM, showing AC, DC and transient simulations. Subsequently general conclusions and future work are described.

More detailed descriptions are included at the beginning of each chapter.

## **Objective**

The aim of this thesis is the development of a new accurate compact charge and capacitance model for organic field effect transistors (OFETs), valid in all device operation regimes, i.e. accumulation, partial and total depletion. Amongst the capacitance model requirements are the continuity between operation regions, i.e. linear and saturation, and the use of the unified model and extraction method (UMEM), in order to obtain a final C-V model consistent with the I-V one described by UMEM.

## **Methodology**

The methodology applied in this thesis involves mainly the use of fabrication techniques such as spin coating, sputtering and photolithographic processes carried out at CINVESTAV (Mexico City), as well as characterization techniques, i.e. current-voltage (I-V) and capacitance- voltage (CV). We also studied OTFTs fabricated in CEA-LITEN (Grenoble) and with collaboration of IMEP-LAHC from Minatec (Grenoble).

We used the device simulators ATLAS and ATHENAS from Silvaco to analyze the variation of different physical and structural parameters in the OTFTs.

The UBCM was developed and validated with Mathcad, to subsequently implement its Verilog-A and Spice codes in the circuit simulator SMASH from Dolphin Integration.



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# CHAPTER 1.

## TFTs and Organic Materials

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In this chapter we introduce the organic field effect transistors (OFETs), their structures, operation principles and electrical characteristics, as well as fabrication techniques, applied materials and finally applications. We compare the crystal inorganic semiconductor physics with that of organic semiconductors, focusing on the main properties of these amorphous organic materials that determine to the carrier transport within them.

## 1. TFTs and Organic Materials

### 1.1 Organic Thin Film Transistors (OTFT)

The origin of OTFTs dates back from the mid 1920's, when Julius Edgar Lilienfeld patented for the first time the basic principle of the later known "field effect transistor"(FET) in his work "Method and apparatus for controlling electric current" [Lilienfeld-1930]. Subsequently Oscar Heil described the possibility of controlling the resistance in a semiconducting material with an electric field in his British patent in 1935 [Heil-1935]. But it was not until 1947 when the first junction FET was fabricated and studied by William Shockley and co-workers at Bell Laboratories in USA.

At the same Labs, the discovery that the Si surface could be oxidized to form a highly stable insulating film with excellent interface qualities, and the continuous technology research, gave place to the metal-oxide-semiconductor field-effect-transistor (MOSFET) in 1960 [Orton-2004].

Within a very few years RCA pioneered the introduction of the up-to-now successful MOS devices into integrated circuits. There in 1961, Paul K. Weimer invented the thin film transistor (TFT), demonstrating that "a high-gain transistor can be built using a semiconductor as imperfect as a polycrystalline evaporated layer" [Weimer-1962], showing their considerable promise as amplifiers or switches suitable for use in large area circuits. The TFT was also used as a tool to measure the mobility of a-Si:H TFTs, since at that time it was difficult with other techniques [Spear-1972]. Thanks to that, applications on Liquid-Crystal Displays (LCDs) and on integrated-logic circuits were possible to achieve, in applications where crystalline silicon can be no longer applied [LeComber-1981]. Afterwards in 1986 the next significant event took place when Tsumura, Koezuka, and Ando of Mitsubishi

Chemical developed the first organic field effect transistor (OFET) based on polythiophene with recognizable current gain [Tsumura-1986]. Since then, even though not immediately, different device geometries, materials and technological processes have been applied on OFETs, as well as deeper studies have been performed, and models developed where the understanding of the physics of the device is essential. OFETs are also called organic TFTs (OTFTs) because their geometries are similar to those of thin-film silicon transistor (TFT) [Dosev-2003].

### 1.1.1 Principles

An OTFT is basically a three terminal device (Gate, Drain and Source) in which the current flow going between source and drain is modulated by a gate potential. A major difference with commonly used inorganic transistors is that no inversion layer is formed. Here the conduction occurs by means of the majority carriers, which accumulate at the semiconductor/insulator interface; inversion in organic materials is not formed because the transistors do not reach the thermodynamic equilibrium, and so the steady state, this all due to the high rate of trapped charge within the material [Brondijk-2012].

The metal-insulator-semiconductor (MIS) structure formed respectively by the gate electrode, the dielectric and the organic semiconductor as active layer constitutes the core structure for the whole device. Induced charge is localized at the interface between the semiconductor and the dielectric, by applying a voltage to the gate electrode (field effect). As the density of thermally induced free carriers in organic semiconductors is very low, much lower than the one in commonly used inorganic semiconductors, when the semiconductor is not accumulated at a given bias at gate electrode ( $V_G$ ), it is possible to achieve that

practically no current flows between drain and source electrodes when a voltage on drain ( $V_D$ ) is applied.

The sign of the charge in the channel is opposite to the sign of the applied voltage at gate. For example, Fig. 1a shows an OTFT with a p-type organic semiconductor. By applying negative bias at gate electrode, positive charges will accumulate at the interface insulator-semiconductor, to form a p-channel. As negative bias is applied to the drain electrode, when the channel is formed, electrons are transported through the channel from drain to source. Oppositely occurs in an n-channel device, Fig. 1b.

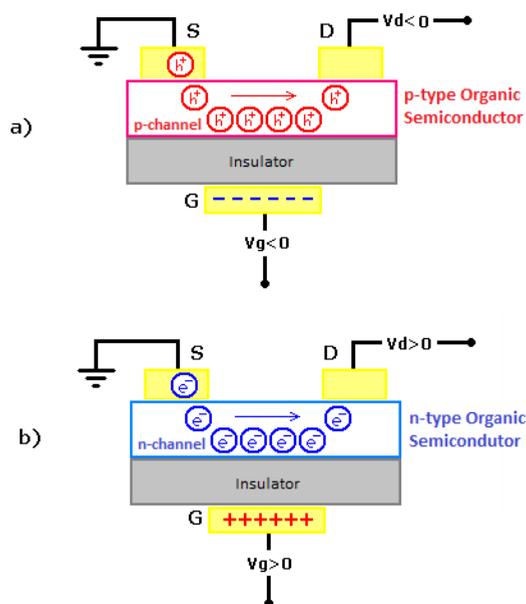


Fig.1.1. Schematic view of two biased OTFTs: a) p-channel and b) n-channel

The drain-to source current ( $I_{DS}$ ) expressions resemble to those of MOSFETs [Sze].  $I_{DS}$  current expressions for TFTs can similarly be obtained considering ideal conditions, i.e. there are no interface traps, the concentration of charge is

uniform along the channel, carrier mobility in the accumulation layer is constant, and assuming the so-called gradual approximation [Shockley-1952], proved also to be valid for OFETs [Weiss-2012]. This approximation assumes that the transverse field (in the  $y$  direction) in the channel is much larger than the longitudinal field ( $x$  direction). In other words, it considers that the potential variation along the channel is smaller compared to the variation of the transversal potential, so when the channel is already formed, the accumulated charge density at a point  $x$ , ( $Q_s(x)$ ) along the channel is given by the potential at such point  $V(x)$ ,

$$Q_s(x) = C_i V(x) \quad (1.1)$$

where  $C_i$  is the insulator capacitance per unit area.

With these conditions, if we apply a voltage  $V_G$  to the gate to form the channel of the OTFT shown in fig. 2, and we divide it into several uniform elemental strips, we can calculate the induced charge  $Q_x$  in one strip localized at a distance  $x$  from the source of width  $dx$ .

$$dQ_x = -C_i [V_G - V_T - V(x)] W dx \quad (1.2)$$

where  $V_T$  is the threshold voltage,  $W$  is the channel width and  $V(x)$  is the potential at the point  $x$  along the channel induced by biasing the drain, i.e. at the source  $V(0)=0$  and  $V(x)=V_D$ . The minus sign refers to the charge at the channel which we are analyzing. A positive sign would refer to the charge at gate electrode since the voltage is applied on such electrode.

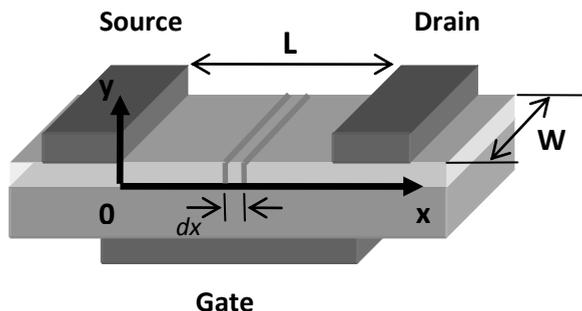


Fig.1.2. Schematic view of an OTFT with the required parameters to obtain the induced charge in the channel and thus the  $I_{DS}$ .

From physics we know that the electric current is given by the rate at which the electric charge is transferred through a surface over a time  $t$ . So  $I_{DS}$  can be calculated by means of the charge  $Q_x$  in the strip  $dx$ . Applying the chain rule, we get:

$$I_{DS} = \frac{dQ_x}{dt} = \frac{dQ_x}{dx} \frac{dx}{dt} \quad (1.3)$$

The average velocity  $v$  of the charge carriers in the current flow is described by the mobility  $\mu$  of the carriers and the applied electric field  $E$

$$v = \mu E \rightarrow \frac{dx}{dt} = \mu \left( -\frac{dV}{dx} \right) \quad (1.4)$$

keeping in mind that one of the ideal conditions assumed at the beginning was that the mobility is constant.

So, replacing (1.2) and  $dx/dt$  from (1.4) in (1.3) we obtain:

$$I_{DS} dx = W \mu C_i [V_G - V_T - V(x)] dV \quad (1.5)$$

Finally  $I_{DS}$  is calculated by integrating Eq. (1.5) from source ( $x=0$ ,  $V(x)=0$ ) to drain ( $x=L$ ,  $V(x)=V_D$ ).

$$I_{DS} = \frac{W}{L} \mu C_i \left[ V_G - V_T - \frac{V_D}{2} \right] V_D \quad (1.6)$$

If a small drain voltage  $V_D$  is applied, a current will flow from the source to the drain through the conducting channel which acts as a resistance, and  $I_{DS}$  is proportional to  $V_D$ . This is the *linear regime*, where  $V_D < (V_G - V_T)$ , Fig.1.3.

If  $V_D$  keeps increasing up to the value  $V_D \approx (V_G - V_T)$  then, similarly to MOSFETS, the “pinch-off” will be reached and with it, the device will get into the *saturation regime*. Replacing  $V_D$  under this condition,  $I_{DS}$  becomes:

$$I_{DS} = \frac{W}{2L} \mu C_i (V_G - V_T)^2 \quad (1.7)$$

As  $V_D$  increases, it eventually reaches a point at which the channel depth at the point  $x=L$  is reduced to 0 referring to a narrow depletion zone formed in the channel next to the drain because the local potential there drops below threshold. Further increase of  $V_D$  leads to an extension of the depletion zone and thus to a shift of the pinch off point towards the source which becomes subsequently independent of the drain voltage. The pinch off potential remains  $\approx (V_G - V_T)$ .

$I_{DS}$  can be plotted in domain of  $V_G$  at different values of  $V_D$  or in domain of  $V_D$  at different values of  $V_G$ . They are called *transfer* and *output* characteristics respectively. Figure 1.3 shows such characteristics of a p-channel OTFT.

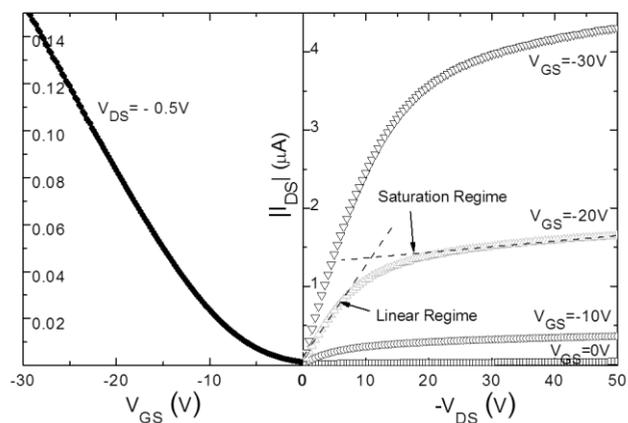


Fig.1.3. Transfer characteristic in linear regime (left) and Output (right) characteristics of a p-channel OTFT where the operation regimes are indicated.

Notice that the device does not saturate completely in figure 1.3. The lack of a complete saturation in OTFTs, depending on the materials used, has been attributed to short channel effects [Austin-2002] and to bulk, interface, and grain boundary traps [Schön-2001], [Armstrong-1998], [Stallinga-2006a], which experimentally, it is difficult to determine the exact location of them. The density of traps affecting the mobility in the device will be studied subsequently.

Attention must be paid to the similarity of the basic equation (1.6), and the shapes of the curves of figure 1.3, with those obtained for inversion-channel MOSFETs [Sze]. This is the reason why it is frequent in literature to find the use of the MOSFET model to describe TFTs. Empirically, the curves are the same, but the complications start when the measured data are analyzed and parameter extraction is attempted. As a good example may serve the determination of the donor density from the threshold voltage, something that

is common for a p-type inversion-channel MOSFET, but does not make sense in the TFT framework, since the doping concentration is not a parameter in accumulation TFTs. Also, the drift currents in a TFT, which depend on the density and not on the gradient, always dominate and the diffusion current is practically zero [Stallinga-2006b]. Mistakes are often made when trying to extract the threshold voltage and mobility with MOSFETS equations, but this will be discussed later in chapters 2 and 3.

### 1.1.2 Architectures and Technological Processes

An OFET can be assembled in several configurations (Fig. 1.4). Remember that an OTFT is made by a thin semiconducting layer, an insulator and the gate, source and drain contacts which are deposited as a *staggered* or *planar* configuration. In the staggered structure the semiconductor layer separates the drain and source electrodes from the gate electrode, whereas in the planar configuration, the three electrodes are located at the same side with respect to the semiconductor layer. Regarding to the gate, it can be deposited either over the substrate with the dielectric layer on top (bottom-gate configuration) or with the gate dielectric at the top of the whole structure (top-gate configuration). Thus we can have staggered top-gate (Fig. 1.4a) and staggered bottom-gate configurations (Fig. 1.4b), as well as planar top-gate (Fig.1.4c) and planar bottom-gate configuration (Fig.1.4d).

Organic semiconductors are usually obtained as thin films; accordingly, OTFTs often present an inverted architecture (bottom-gate configuration), in which the gate electrode is laid down first, the deposition of the semiconducting film usually being the last step. Compared to thin films obtained by thermal

evaporation in a high-vacuum environment, a spin-coated polymer semiconducting layer exhibits very low surface roughness [Ling-2004].

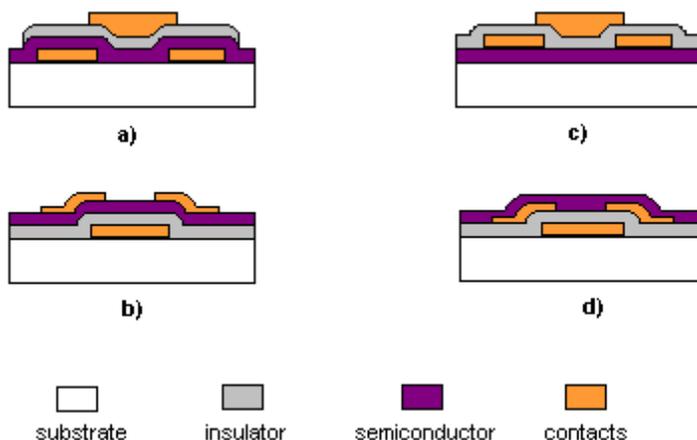


Fig.1.4. Different OFET configurations: (a) staggered top-gate/bottom-contacts configuration, (b) staggered bottom-gate/top-contacts configuration, (c) planar top-gate configuration and (d) planar bottom-gate configuration.

Bottom-gate OTFTs are a conventional device structure for material-testing purpose. Unfortunately, the oxygen and moisture can easily penetrate into the active layer and degrade the device performances for bottom-gate OTFTs because the organic semiconducting materials are exposed to air. It has been demonstrated by different groups that top-gate OTFTs exhibit higher stability than bottom-gate devices [Rost-2004]. Also experimental results and device simulation have shown that staggered structure is better than the planar structure regarding the contact resistance [Martin-2001], [Shim-2010]. Although the current characteristics are similar, the limitation of the current level appears in the planar structure as the gate bias increases.

At the beginning of the organic electronics era, the gate in OTFTs was constituted by a highly doped silicon wafer, on which a silicon oxide layer was thermally grown, but over the past years, the gradual substitution of silicon oxide by polymeric dielectrics is spreading out, since the latter are flexible and solution-processable. The source and drain can be deposited by either conventional microlithographic techniques when gold is applied; or by micro-contact printing technique, when conductive polymers substitute gold.

Sputter deposition, photolithography and spin-coating techniques have been employed to fabricate respectively, gold electrodes and organic semiconductor and dielectric films with a controlled thickness [Cabrini-2012]. (More information about advanced fabrication techniques can be found in the suggested bibliography from the APPENDIX section).

The dielectric/organic semiconductor interface, the most important one in OTFTs, plays a key role in the device performance, because the conductive channel is located on the few molecular layers near the gate dielectric layer [Dinelli-2004], [Smits-2008], [Chua-2005]. To establish good contact between the organic semiconducting layer and the dielectric layer, it is necessary to ensure that the surface roughness of these layers is extremely low [Sundar-2004] [Boer-2003].

### **1.1.3 Applications**

The limitation of wafer size in conventional silicon-based technologies is no longer a problem for organic electronics, because organic integrated circuits (ICs) can be fabricated on a substrate of very large surface, e.g. roll-to-roll printing on a flexible plastic substrate. This special feature enables many applications, e.g. large-surface sensors, flat-panel displays, surface lighting,

photovoltaics, where the silicon ICs is not appropriate due to either high cost or processing difficulties. The excellent mechanical flexibility of organic electronic devices is expected to open up a range of new application opportunities in electronics, such as flexible displays, robotic sensors, and biological and medical electronic applications.



Fig. 1.5. a) SONY's organic thin film transistor driven, full color, flexible OLED display (80  $\mu\text{m}$ -thick and 4 inches wide), able to reproduce moving images while being rolled around a cylinder with a radius of 4 mm., b) SAMSUNG's transparent smart window.

At the present, the switching devices of many commercial active matrix flat-panel displays are based on amorphous or polycrystalline silicon. The size of glass substrate limits the cost reduction, however, the nearly non size-limited substrate for the OFETs' fabrication could enable very large displays, based on either liquid crystal pixels or organic light-emitting diode (OLED). For instance, the SONY OLED television has been released into the commercial market, and additionally very light weight, flexible and transparent applications of organic displays with very high image quality have been recently proposed [Sony], e.g. Fig. 1.5a. OTFT-display development has marked a path to a variety of applications, e.g. *wearable smart-phones*, *intelligent paper*, *roll-over displays* and *smart windows*, which offer the opportunity to smart glass and

window manufacturers for enhancing functionality and energy conservation benefits through integration OLED displays and photovoltaics into the windows, Fig.1.5b.

Another application of OFETs is the organic radio frequency identification tag ORFID, which has shown much greater advantages compared to the currently used code bar for the domains of retail and logistics because of their very low cost, flexibility, good robustness. For example, in application to the red wine, the organic RFID tags offer much more information, such as the brand history, planting environments, fermenting methods, recommendations of conservation and drinking, or even more, offers the possibility to read bio-information from outside the skin, or from implantable electronics that directly extract health information from the body [Kuribara-2012].

## **1.2 From Silicon Crystals to Organic Semiconductor**

In the silicon crystal, every atom (valence IV) is strongly linked to the four neighboring atoms by the covalent bonds. The binding energies are as high as 76kcal/mol which is much higher than the lattice vibration energy; the lattice arrangement is thus not significantly affected by the phonons. Hence the lattice periodicity is kept nearly perfect and the crystal is called rigid. In this kind of medium, the charge carriers can move as highly delocalized plan waves (Bloch waves) with very high velocity. However, due to the presence of diffusion centers (e.g., phonons or defects), the charge carriers cannot always accelerate under an electrical field but rather, have a mean free path, in which they move without interaction. Note that the kinetic energy of carriers is obtained from two collisions, exhibiting a mean drift velocity which decreases with the temperature since the number of phonons increases at higher temperatures.

Therefore, the mean velocity obtained by unit electrical field is defined as mobility,  $\mu$  ( $\text{cm}^2/\text{Vs}$ ). In silicon, the values of  $\mu$  at room temperature can reach  $1400 \text{ cm}^2/\text{Vs}$  and  $500 \text{ cm}^2/\text{Vs}$ , for the electrons and the holes, respectively.

The conducting type of silicon semiconductor depends on the majority impurities that are often called dopant. The dopant changes the thermal equilibrium of intrinsic semiconductors to conduct principally by one type of carriers: either electrons or holes. Hence there are two types of doping: if the dopant introduces excess electrons into the silicon, it is referred as to donor (valence V), on the other hand if the dopant introduces excess holes, it is referred as to acceptor (valence III). So, we have two kinds of classical semiconductors: p-type and n-type.

The energetic position of the Fermi level in a semiconductor represents the balance between the concentration of holes and electrons that occupy allowed energy levels under equilibrium condition (dark, no applied voltage). If the Fermi level is closer to  $E_c$  the material is called n-type since more electrons are available for conduction than holes, otherwise it is called p-type.

In The energetic position of the Fermi-level ( $E_F$ ) in semiconductors is important for two reasons:

- a) Together with the work-function of the metal the Fermi level determines whether a blocking or ohmic contact is formed at the semiconductor/metal interface.
- b) The relative position of the Fermi levels is a measure for the type of conductivity whether the semiconductor conducts preferably holes in the Valence band ( $E_V$ ) or electrons in the Conduction band ( $E_C$ ).

Thus, the position of the Fermi level can be written as a function of both the effective density of states in the conduction band ( $N_C$ ) and valence band ( $N_V$ ) as well as the concentration of donors ( $N_D$ ) and acceptors ( $N_A$ ) [Sze]

For n-type semiconductors this gives :

$$E_F = E_C - kT \cdot \ln\left(\frac{N_C}{N_D}\right) \quad (1.8)$$

whereas for p-type semiconductors the relation is:

$$E_F = E_V - kT \cdot \ln\left(\frac{N_V}{N_A}\right) \quad (1.9)$$

$E_V$  and  $E_C$  stand for the top edge of the valence band and the bottom edge of the conduction band respectively. These expressions have also been used with organic materials as an approximation.

### 1.2.1 Band diagram: HOMO and LUMO levels

As previously mentioned band theory is well established for inorganic semiconductors, in such theory electronic transitions mainly occurs at valence and conduction band [Sze]. Similarly, for organic materials, it has been suggested the formation bands where the transport occurs. The nature of these bands has been attributed to the dimerization, which is the alternation between

simple ( $\pi$ ) - and a double-bond ( $\sigma$ ). Fig. 1.6 shows the double bond in ethane [Castro-Carranza-2011a],

This huge electron lattice coupling in this kind of materials causes most of the charges to be localized under thermal equilibrium conditions. To generate mobile charge additional energy is required, the electrons of the  $\pi$  atomic orbitals formed by a  $sp^2$ -hybridization of atoms are far from the carbon core, so they are easily polarized and can become mobile charge.

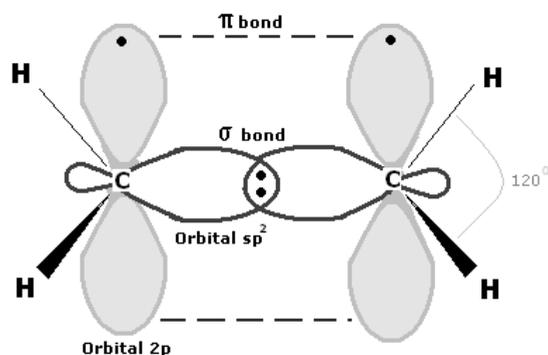


Fig. 1.6: Type  $\pi$  and  $\sigma$  bonds in ethane molecules ( $CH_2=CH_2$ ).

The occupied orbital of less energy derived from the double bond is called HOMO (highest occupied molecular orbital) and the next non-occupied orbital with a higher energy is called LUMO (lowest unoccupied molecular orbital). The difference between HOMO and LUMO is the band gap ( $E_g$ ). In particular,  $E_V$  may be seen as the HOMO (Highest Occupied Molecular Orbital) level and  $E_C$  as the LUMO (Lowest Unoccupied Molecular Orbital) level in a quasi molecular model.

It has been proposed that in organic semiconductors, the band gap can be influenced by [Roncali-1997]:

$$E_g = E_{ld} + E_d + E_{Res} + E_{Sub} + E_{int} \quad (1.10)$$

where  $E_{ld}$  is the energy related to bond length dimerization,  $E_d$  is the energy related to the mean deviation from planarity,  $E_{Res}$  is the energy related to the aromatic resonance energy of the cycle,  $E_{Sub}$  is the energy related to the inductive or mesomeric electronic effects of eventual substitution, and  $E_{int}$  is the energy related to the intermolecular or interchain coupling in the solid state. The main synthetic strategies adopted for the design of organic semiconductors will be focused on the reduction of the energetic contribution of one or more of the parameters of equation 12, to get a better control of  $E_g$ .

### 1.3 Organic Materials for OTFTs

Organic materials are chemical compounds whose molecules contain carbon. These molecules have covalent bonds of carbon-carbon and/or carbon-hydrogen, which can also contain nitrogen, oxygen, phosphorus, sulphur, boron or any other halogen such as fluorine, chlorine or iodine.

The basic structure of organic materials is based on single molecular compounds with a very defined, stable and specific architecture. This basic structure is called *monomer* which has small molecular mass, and many of them together give place to different compounds based on their molecular weight:

- (i) **Oligomers** (small molecules). Low molecular weight materials formed by a finite number of monomers (generally less than 10), e.g. Hexithiophene (6T), Pentacene, TIPS-Pentacene, Perylene, Rubrene, Oligothiophene and TPD C60. These materials generally show the highest mobility values.
  
- (ii) **Polymers**. High molecular weight materials (big molecules called macromolecules), which joint form chains of an unlimited number of monomers. The brackets indicate the infinite periodicity of the monomer in the polymer, i.e. P3HT, PCBM, Fig. 1.7.

The “mechanical” properties depend mainly on the position and number of side chains. Side chains are usually attached molecules which introduce or improve solubility. They are more successfully applied in solubilising the molecule; additionally they can better prevent aggregation between molecules.

Pentacenes are attractive building blocks for molecular devices due to their inherent electronic properties, excellent film-forming characteristics, and the ability to adjust the electronic behavior required for a particular device [Gruhm-2002]. PTAA polymers have been widely studied and commonly used in OTFTs since they have shown high charge carrier mobility values (up to  $\sim 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  [Barad-2009]), especially when the molecular weight is low, and besides they are operationally and environmentally very stable due to a high ionization potential.

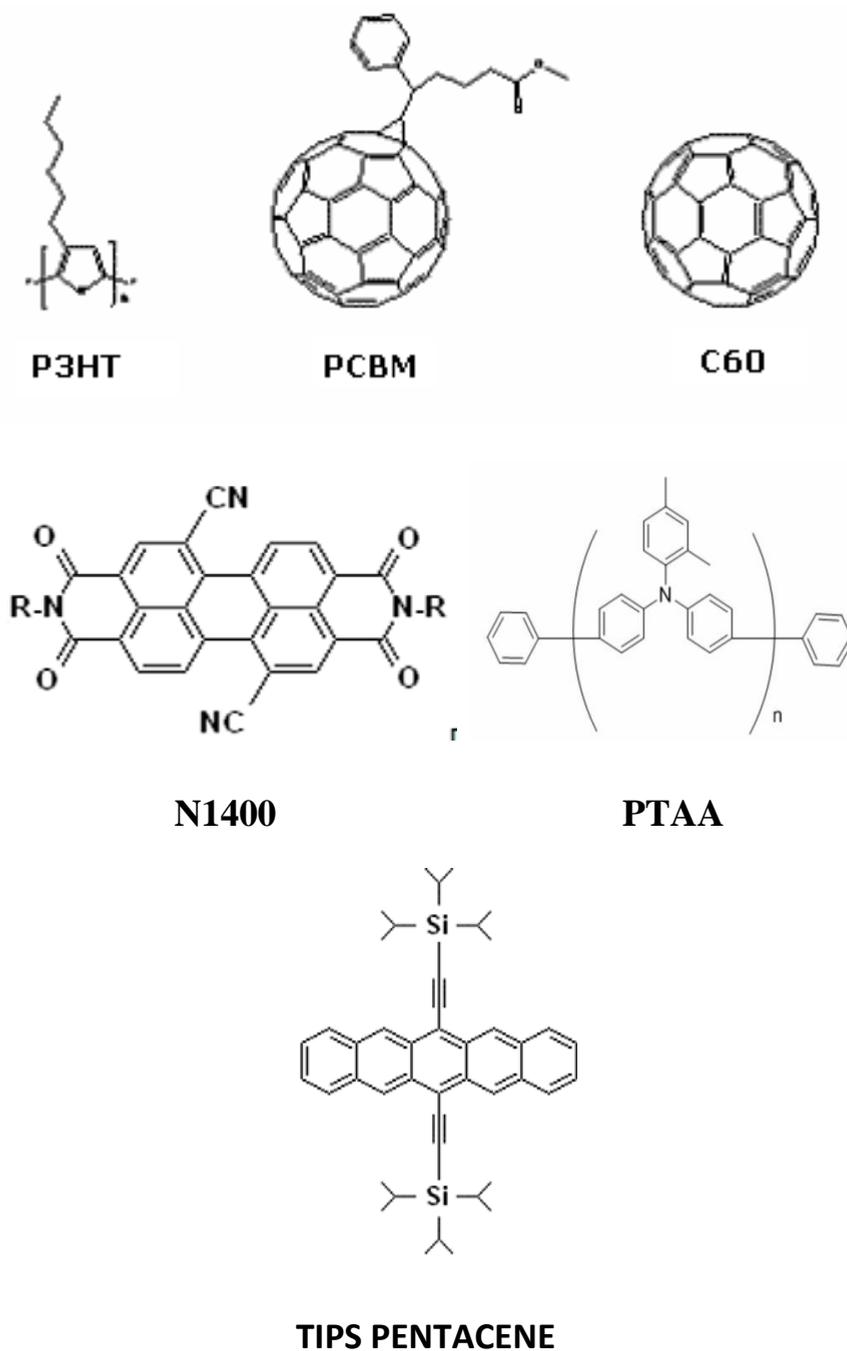


Fig.1.7. Examples of oligomers and polymers.

To fabricate the basic logical electrical circuits both kind of organic materials, P and N type semiconductors, are required. Because more of the organic materials with higher mobility are P-type, these have been more extensively studied. Detailed studies of new N-type materials are less than for P-type materials. Different organic materials such as Siloles, Fullerenes, Acenes and Rylene Diimides have been applied to N-channel devices. Fullerene-based acceptors have exhibited the highest efficiencies in organic photovoltaics, but Rylene Diimides with their relative high electron mobilities, high electron affinities and good chemical, photochemical and thermal stabilities, have shown the best mobility values on N-channel OTFTs [Anthony-2010]. The rylene diimides include naphthalene diimides (NDI) and perylene diimides (PDI), which have been relevant in the improvement of field effect transistor mobility  $\mu_{FET}$  [Facchetti-2011]. However the DOS characterization for this kind of materials is still rare.

Whereas results have demonstrated that rather than PDIs, NDIs comonomers are the choice to achieve higher-performance OTFTs due to their larger electron affinity and better air stability [Chen-2009]. In fact, H. Yan et al. reported a polymer based on a NDI core (Polyera Activink<sup>TM</sup> N2200) OTFT which exhibited a  $\mu_{FET}$  up to  $0.85 \text{ cm}^2/\text{Vs}$  in ambient conditions [Yan-2009]. Later on, measurements of the bulk electron transport by means of time-of-flight technique in N2200 devices were performed, revealing a potential usage of this new NDI polymer for applications that rely on efficient bulk electron transport [Steyrleuthner-2010].

However, the PDI small molecule N,N-dialkylsubstituted - (1,7 & 1,6) - dicyanoperylene - 3,4:9,10 - bis(dicarbiximide) derivative (Polyera Activink<sup>TM</sup>

N1400) shows an interesting mobility feature by comparing to other materials. In chapter 3 devices fabricated with this material are analyzed.

## **1.4 Models and Theories of Carrier Transport Mechanisms in Organic Materials**

At present, the exact charge transport physics in organic semiconductors is not completely understood yet. Several theories have been proposed to describe charge transport in disordered organic semiconductors, but it is probable that neither of these mechanisms will describe completely the physics of these materials, and that several mechanisms occur at the same time. In the following, the principle mechanisms are listed. (For a more complete overview, it is suggested [Verlaak-T],

### **1.4.1 The Polaron Model**

A Polaron is a quasi-particle composed of a charge and its accompanying polarization field which affects the particle properties such as the energy and the effective mass. Polaronic effects in charge carrier transport are strong in organic semiconductors whether they are molecular crystals or the based on polymers because when a deformation in the molecular chain is formed due to a charged particles, they are self trapped in an initial site and transfer to another neutral site, due to the lattice vibration [Holstein-1959]. The mobility of the small Polaron is calculated by solving the time-dependent Schrödinger equation, and depends on is the polaron binding energy  $E_b$ , which is defined as the energy gain of an infinitely slow carrier due to the polarization and deformation of the lattice [Horowitz-1998].

### 1.4.2 Variable Range Hopping (VRH)

In very disordered system, a large number of localized states distribute in the band tails where the charge carriers cannot move freely and only transfer by hopping, either in nearest neighboring localized states(nearest neighbor hopping) or to the smallest barrier sites (variable range/energy hopping) [Mott-1979]. As the hopping rate can be enhanced by phonon vibrations, sometimes it is called phonon-assisted hopping, and the observed mobility shows a thermal activation behavior, i.e.,  $d\mu/dT > 0$  or  $\mu \sim \exp(-Ea/kT)$ , where  $Ea$  is the average activation energy (usually in the range of dozens to hundreds of meV) [Xu-T]  $kT$  is the thermal energy. At ultra low temperatures, thermal activation is negligible and the carrier mobility will fall down to zero. Due to the existence of hopping barrier, carrier mobility is strongly dependent on the position of Fermi level in the band. As the Fermi level moves over the energy level of localized states, the hopping barrier decreases because of deep traps filling and finally, the mobility increases while the Fermi level is rising. This explains the field dependent mobility in amorphous and polycrystalline organic transistors

### 1.4.3 Multiple trapping and release (MTR)

The MTR model has been used for describing charge carrier transport in inorganic disordered materials, e.g. to model the gate-voltage dependent mobility in hydrogenated amorphous silicon [Shur-1984] as well as in sexithiophene (6T) to explain its temperature dependent mobility.

The model assumes that charge transport occurs through delocalized, extended states (in the band), being limited by a distribution of traps located near the transport band. Traps are low energy states that are present due to impurities, defects, grain boundaries, tail states due to disorder, etc. Charge carriers are trapped while being transported in extended states; the carrier can be released

after a certain time, usually by thermal activation. The time the carrier spends trapped depends on the depth of the trap and the temperature. Carrier transport in the MTR model is thus described as a series of transport, trapping and release.

This kind of carrier transport is very similar to the thermally activated hopping and the carrier mobility also exhibits a thermal activation behavior [Vissenberg-1998]. By MTR transport, the mobility in organic transistor often shows a power law dependence on the gate voltage.

#### 1.4.4 Distribution of density of states *DOS*

Understanding charge transport is fundamental to improve the performance of any electronic device. Nowadays it is widely accepted that trap states have an important role in charge transport for organic materials [Nicolai-2012]. While defects in conventional semiconductors are well known, the formation of defects in organic materials is still not well understood [Gregg-2009]. It has been proposed for OTFT's that interfacial defects create trap states [Sirringhaus-2005]. Even, it has been proposed that when the materials are doped the DOS increases [Arkhipov-2005], [Gregg-2009]. DOS can be represented by exponential or addition distributions.

Figure 1.6 shows valence band, conduction band and DOS distributions, Localized DOS are those whose energy is inside  $E_g$  and delocalized DOS refer to the states outside of  $E_g$ . In Fig. 5, DOS is represented by exponential distributions. The equations of DOS distributions will be described later. Fig. 5 also shows band-tail states. These states are commonly represented by an exponential DOS distribution and its nature have been typically assigned to the disorder within the material for non-crystalline inorganic materials [Shur-

1984], for organic amorphous materials like in case of polymers, the existence of such tail states are very probable [Stallinga-2011].

Depending on the DOS, in non-equilibrium conditions the occupancy in the material can change and therefore so can the quasi-Fermi levels. These trap states can also act as recombination centers of free charge carriers. Their characterization and reduction are important for increasing the performance of any organic electronic device.

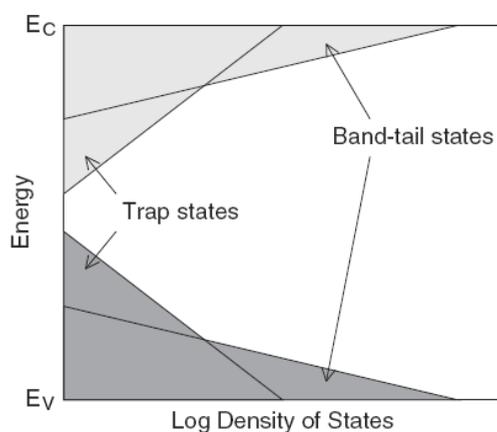


Fig. 1.6 Band diagram of inorganic amorphous semiconductors (after Shur and Hack; [Shur-1984])

The mathematical expression for a Gaussian DOS is given by [Nicolai-2011]:

$$g(E) = \frac{N}{\sigma \cdot 2\sqrt{2\pi}} \cdot \exp\left(-\frac{E^2}{2\sigma^2}\right) \quad (1.11)$$

where  $\sigma$  is the variance of the distribution,  $N$  is the maximum of the DOS, and  $E$  is measured relative to the center of the DOS.

For simplicity, exponential DOS have sometimes been used to approximate these Gaussian distributions [Nicolai-2011]. Exponential DOS is given by:

$$g(E) = gd_o \cdot \exp\left(-\frac{E_r}{kT_o}\right) \quad (1.12)$$

where  $gd_o$  is the maximum of the DOS,  $E_r$  is the relative energy to one of the bands, and  $T_o$  is the characteristic temperature of DOS distribution.

To characterized trap states different spectroscopic techniques have been used such as impedance spectroscopy [Ecker-2011] or deep level transient spectroscopy [Campbell-2000].

## 1.5 Summary

In this chapter we have introduced basic concepts of the OFETs operation, from their fabrication techniques and materials, to the physics and theories involving such devices. We also remarked the advantages of OFETs according to the organic-material properties applied on its fabrication. This general and introductory chapter can help the interested reader to go in depth in organic semiconductors physics, and for this a list of suggested readings are included in the appendix section.



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## **CHAPTER 2.**

### **State of the Art and Current Trends of Compact Models for OFETs**

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In this chapter we stand out the advantages of the Unified Model and Extraction Method over other I-V models, and thus, we also stand out our capacitance model, which is consistent with the I-V characteristics of the OTFT, from which extracted parameters are obtained.

## 2. State of the Art and Current Trends of Compact Models for OTFTs

Compact models of circuit elements are simple models that are developed to be incorporated in circuit simulators. A sustainable compact model must represent consistently the behavior of the device in an analytical, simple and easy derivable form, in order to make the results of the simulators useful to circuit designers. It has to be upgradable and reducible and, of course, physically justified. The conflicting objectives of model simplicity and accuracy make the compact modeling field an exciting and challenging research area for device physicists, modeling engineers and circuit designers working on describing the behavior of a certain device using explicit and high-ordered continuity expressions for a lower consumption of computational time, and to prevent lack of convergence in circuit simulators [Gildenblat-2010]. For this, smoothening and interpolation functions are often used to assure continuity between operating regimes.

To develop a model, it is necessary to understand the physics of the device, propose approximations to simplify the theoretical aspects and make possible the calculation of basic device parameters; mathematical tools and methods to implement calculations that guaranty continuity between different operation regimes of the device; parameter extraction procedures and verification of the model: against experiment or device simulation.

Different models for OFETs have been proposed up to now, nevertheless some of them are numerical and others are analytical but without being compact. In the following a brief state of the art regarding models for OFETs will be mentioned. Additionally to the charge transport models applied on models for

OTFTs, crucial parameters such as threshold voltage and contact resistance are also necessary to take into account when developing a compact model as will be seen in the following.

## 2.1 Current-Voltage Models

Most of the developed current-voltage (I-V) models for OFETs reported up to now in literature reproduce with more or less precision the behavior of the drain current with bias, at least in one of the device operation regions. Amongst these models main differences are found in:

- *The expressions to model charge mobility.* E.g. the charge carrier transport theories described in general terms in section 1.4 or even the classic Silicon MOSFET mobility model.
- *The number and characteristics of model parameters.*
- *The extraction procedures.*

When Tsumura's et al. first OTFT based on polythiophene with a recognizable gain was obtained, it was seen that the shape of the current-voltage characteristics resembled to those of the MOS transistor [Tsumura-1986], fact that subsequently gave rise to use widely the MOSFET model for analyzing the charge transport in OFETS. Even though it can be an approximation, it has been demonstrated that it is not a completely correct technique, since charge transport and mobility in amorphous materials are not the same as in crystalline ones.

OTFTs can present deformation at the origin of the output characteristics, due to non-ohmic contacts at drain and source. They can also have leakage current across the gate dielectric and/or polarization effects, which can be significant

and have to be taken into account. Also, the highly-disordered nature of the organic materials, mainly polymers, gave place to question about the validity of the extraction of parameters from the I-V characteristics mainly when obtaining the bias dependent mobility, contact resistance and threshold voltage. For these reasons, models and extraction procedures designed for amorphous transistors, specifically for organic ones had to be necessary proposed.

Regarding charge mobility models, variable-range hopping, is the one mostly accepted, while the distribution of acceptor-type and donor-type localized states, is represented as Gaussian distributions or as an exponential distribution with one characteristic temperature,  $T_0$ , (as already seen in the previous chapter) for the acceptor type and other for the donor-type states.

### 2.1.1 Extraction of threshold voltage

The threshold voltage  $V_T$ , for any field effect transistor, is a key parameter for other parameter evaluation such as mobility and contact resistance. In Si MOSFETs, threshold voltage separates the weak and strong inversion, whereas in OFETs it separates the above threshold and subthreshold regions. In an ideal situation (zero difference of the gate work function and the Fermi level of organic semiconductor, i.e. flat band voltage equal to 0) the threshold voltage would be zero, so a greater gate voltage will immediately accumulate charge carriers and the organic semiconductor conductivity will also increase.

Due to the large number of traps distributed in OFETs and the presence of charge injection barrier, the  $V_T$  is significantly shifted, thus when extracting such parameter it is important to have an accurate extraction procedure that do not insert additional errors in the obtained  $V_T$  value.

In conventional silicon MOSFETs, several methods have been developed for threshold voltage extraction in both, linear and saturation regimes [Ortíz-Conde-2002]. Subsequently, these techniques for extracting the Si-MOSFETs  $V_T$  were also applied on OFETs [Boudinet-2009]. Although these methods can provide an approximation, a question would be arised: Are such extraction techniques completely correct for OFETs?

In OFETs the turn-on in the subthreshold region of operation is not as abrupt as in high quality crystalline semiconductor device. Significant current can flow before the device enters the extrapolated higher transconductance region in the transfer curve. The part of the linear and saturation which one may expect to be linear (according to the model) may not be, leading to some ambiguity in the  $V_T$  determination. Also the extrapolation of the expression for  $\sqrt{I_D}$  into a region in which the model does not apply to get the  $V_T$  when extrapolating to zero point has no universally agreed upon physical significance, since the drain current does not depend on  $(V_G-V_T)^2$ , but on  $(V_G-V_T)^n$  [Ryu-2005].

### 2.1.2 Contact resistance

To obtain an efficient OFET, the presence of a low contact resistance is essential. A number of works reported that the contact resistance in staggered bottom-contact (BC) OFETs is much higher than that in top-contact and botton-gate (TC) devices. Due to the presence of contacts the self organization process of molecules is disrupted and hence, very small grains even voids are formed at the contact edges, resulting in a large number of traps which capture the passing carriers and significantly reduce the carrier mobility in the contact region, manifesting as higher contact resistance.

As charge carriers are injected from contacts, the injection barrier is a key factor to determine contact resistance. The different charge injection barrier

can explain the non-linear behavior also accounted for higher contact resistance. Another factor is the metal penetration into the organic film. The metal, in particular noble metals, diffuses into the organic bulk, forming clusters of metallic and nonmetallic metal atoms. As the diffusion is expanded, the effective contact area is significantly increased. More importantly, if the metal penetrates the entire organic film (very thin generally) and reaches the dielectric surface where a channel will be created, the access resistance falls down to nearly zero. This feature is also important to explain the gate-voltage dependent contact resistance.

On the other hand, in the coplanar configuration, the effective contact area is determined by the contact thickness and the width. It is widely believed that, in staggered OFETs the overall contact resistance is dominated by the bulk resistance, however in coplanar OFETs the overall contact resistance is dominated by the contribution of a low conductive access region in the immediate vicinity of contacts where a large number of defects and thus charge traps reside in. This could explain the stronger gate-voltage dependence of contact resistance in staggered devices, the bulk dominant resistance strongly relies on the carrier density controlled by the gate voltage. The dominant defect-rich access component in coplanar devices sometimes is characterized by a depletion region at negative gate biases and its width is modulated by the gate voltage, resulting in a gate voltage dependent contact resistance.

To model the contact resistance in OFETs, there are two general approaches taken into account: constant resistance and voltage-dependent resistance. Different I-V models considering contact effects have been proposed [Natali-2007], [Altazin-2011]. Nevertheless they do not have a method to extract

device parameters and their models are not compact, nor are developed for being directly implemented in circuit simulators. Other I-V compact models have been developed considering the contact resistance as done by Deen et al. in their different works [Deen-2008], [Deen-2009b], [Bullejos-2009], [Jiménez-2011] whose basis is the Unified Model and Extraction Method (UMEM), which will be described subsequently, but the drawback in these models is the rising number of parameters that may affect the accuracy of the modeling.

### 2.1.3 UMEM

Regardless how sophisticated a semiconductor device model is, the model is useless and inaccurate if a viable parameter extraction method is not in place. The most widely used methods for extracting the semiconductor device parameters from the I-V measurements, using a junction diode as an example, can be classified into the following groups[Ortiz-Conde-1999]:

1. Extrapolation for the linear part of the plot of  $\ln(I)$  versus  $V$  where the presence of a large resistance can significantly affect the linear characteristic of the  $\ln(I)$  vs.  $V$  plot to such an extent that the parameters extracted from this method become unreliable.
2. Sophisticated algebraic manipulations and of the I-V data to generate plots which allow the separation of the effects of  $R$ .
3. Use of the small-signal conductance, or derivative of the current with respect to voltage. This method is highly sensitive to measurement errors because the derivative is equivalent to a high-pass filter.
4. Use of integration of the current with respect to voltage. This method is immune to measurement errors because the integration is equivalent to a low-pass filter.

5. Addition of an external resistance in series with the device in I–V measurements. This method requires further experimental work.
6. Direct vertical optimization of the parameters from the I–V data by minimizing the vertical quadratic error.

According to the classification above, an effective parameter extraction procedure is proposed for thin film transistors based on point number 4, which explains its effectiveness. This method is the so called UMEM [Cerdeira-2001]. UMEM has been adapted to extract and then model organic and inorganic TFTs based on a-Si:H [Cerdeira-2001], nanocrystal materials [Cerdeira-2004], amorphous Si carbide [Estrada-2006], 34dditiona and small molecule organic materials [Estrada-2008a] and lately on amorphous oxide semiconductors [Cerdeira-2012] and hybrid pentacene-CdS devices [Mejía-2012]. The modeling covers the above-threshold and subthreshold regimes with a continuous transition between linear and saturation regimes. In the following chapter UMEM is described in detail.

The I-V model for OTFTs used with UMEM is based on the solution of Poisson's equation assuming that the concentration of localized charge can be considered much larger than the concentration of free charge in all the operation regions, and that the DOS is exponential [Estrada-2008a]. Only under such considerations analytical expression for the electric field are obtained, as well as for the induced sheet charge in the channel, after which the drain current is calculated integrating the mobile charge along the channel, in a similar way as was done for a-Si:H TFTs in the subthreshold region [Shur-1984].

$$I_{DS} = P(T, T_0) \frac{W}{L} C_i \frac{T}{2T_0} \left[ (V_{GS} - V_T)^{\frac{2T_0}{T}} - (V_{GS} - V_T - V_{DS})^{\frac{2T_0}{T}} \right] \quad (2.1)$$

where:

$$P(T, T_0) = P'(T, T_0) \frac{C_i^\gamma}{\epsilon_s^\gamma} (V_{GS} - V_T)^\gamma \quad (2.2)$$

$$P'(T, T_0) = \frac{qk_b T N_V \cdot \exp\left[-\frac{E_T}{K_b T}\right]}{\left[\pi q k_b T g_{d0} \cdot \exp\left[-\frac{E_T}{K_b T}\right]\right]^{\frac{T_0}{T}}} \left[ \frac{\sin(\pi T / T_0)}{2K_b T_0} \right]^{\frac{T_0}{T}} \quad (2.3)$$

and

$$\gamma = \frac{2T_0}{T} - 2 \quad (2.4)$$

$W$  and  $L$  are the channel width and channel length respectively,  $C_i$  is the insulator capacitance per unit area,  $T$  and  $T_0$  are the absolute temperature and the characteristic temperature of the  $DOS$ ,  $V_T$  is the threshold voltage,  $V_{GS}$  is the gate-to-source voltage, and  $V_{DS}$  is the drain-to-source voltage.  $\epsilon_s$  is the semiconductor permittivity,  $k_b$  the boltzman constant, and  $g_{d0}$  is the density of localized states.  $\Gamma$  is a parameter that describes the disorder within the organic semiconductor.

Although OTFTs' carrier transport mechanism is different to that of a-Si:H TFT, (2.1) resulted to have the same form as the current in a-Si:H TFT [Shur-1984] where the field-effect mobility expression is [Fjeldly-1998]:

$$\mu_{FET} = \frac{\mu_0}{V_{aa}^\gamma} (V_{GS} - V_T)^\gamma \quad (2.5)$$

where  $V_{aa}$  is an adimensional parameter and  $\mu_0$  can be taken as  $1 \text{ cm}^2/\text{Vs}$ . Note that the mobility depends on the gate bias and on  $\gamma$ . As higher the value of  $\gamma$  is, higher the disordered nature of the material is; depending on  $V_{aa}$ , the mobility will decrease.

Thus, to obtain the field effect mobility expression from the drain current in (2.1), (2.5) is applied:

$$\mu_{FET} = \frac{\mu_0}{V_{aa}^\gamma} (V_{GS} - V_T)^\gamma = \mu_0 P(T, T_0) \quad (2.6)$$

The final expression to describe the field effect mobility resulted as:

$$\mu_{FET}(V_{GS}, T, T_0, g_{d0}) = \frac{\mu_0 q k_b T N_V \cdot \exp\left[-\frac{E_T}{K_b T}\right]}{\left[\pi q k_b T g_{d0} \cdot \exp\left[-\frac{E_T}{K_b T}\right]\right]^{\frac{T_0}{T}}} \left[\frac{\sin(\pi T/T_0)}{2 K_b T_0}\right]^{\frac{T_0}{T}} \frac{C_i^\gamma}{\varepsilon_s^\gamma} (V_{GS} - V_T)^\gamma \quad (2.7)$$

Notice that the field effect mobility obtained by variable range hopping in [Vissenberg-1998] resembles to (2.6) once  $P(T, T_0)$  is replaced. See equation (15) of [Vissenberg-1998]. The advantages of the I-V model of UMEM for OTFTs are that it is an analytical expression, no fitting parameters are needed, all model parameters represent physical magnitudes, the dependence of the mobility on the density of localized states ( $g_{d0}$ ) is explicitly considered.

The complete expression to model the I-V characteristic above threshold is shown in (3.16) and (3.20) of the following chapter

## 2.2 Capacitance Models

I-V model is not enough for circuit simulation because in real circuits, the devices operate under time-varying terminal voltages, i.e. dynamic operation [Tsividis]. In order to calculate the dynamic behavior of the device and so, to enable AC and transient simulation, terminal charge and capacitance modeling of OFETs are needed.

Many approaches for C-V models have been published, but comparison with experiment is very limited or has not been presented due to the difficulties for validating with measurement because of the complex properties of organic materials that affect charge transport, such as density of bulk states or interface states. Not all of the expressions reported for capacitance models for OTFTs are analytical [Calvetti-2005]. Neither do they guarantee continuity when passing from the linear to the saturation regime [Fadlallah-2006], [Li-2010], neglect the threshold voltage [Torricelli-2009], consider the overlap capacitance or are validated with C-V experimental data [Torricelli-2009], [Calvetti-2005], [Li-2010]. Frequency response of C-V models have also been proposed as alternatives, but they use numerical fitting parameters that affect the accuracy of the modeling [Miyadera-2007], [Hamadani-2008], [Ullah-2009], [Jung-2007], and some of them apply C-V models for MIS capacitors on OTFTs as an approximation [Ullah-2009], [Jung-2007], and are not directly linked to the I-V characteristics of the OTFT.

Taking as a starting point the capacitance model for OTFTs valid only in the accumulation regime previously developed in [Castro-Carranza-2012a], in this letter we present a complete compact quasi-static capacitance model valid in all OTFT operation regimes: accumulation, partial depletion and full depletion at low and medium frequencies. The model is continuous in the entire regimes, as

well as when passing from the linear to the saturation condition. The overlap capacitance is also considered. The parameters of the model are extracted analytically from the I-V characteristics of the devices using the unified model and parameter extraction method (UMEM).

### 2.3 Summary

The Unified Compact Model and Parameter Extraction Method (UMEM) provides precise modeling of OTFTs *I-V* characteristics and mobility as function of bias and temperature, including a simple and well defined extraction procedure.

It also allows determining DOS parameters ( $T_0$  and  $g_{do}$ ) and if necessary can take into account involuntary channel conductivity and non-ohmic resistance frequently observed in OTFTs.

Difference in mobility behavior for different materials, can be related to DOS parameters.

It was seen that the expression to model gate bias and temperature dependent charge mobility can be reached through different approaches, e.g., using the concept of the transport energy level [MTR], using percolation [Visseberg-1998] or using a charge model [Shur-1998], [Estrada-2008a].

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## CHAPTER 3.

### **UMEM: Extraction of parameters from the I-V characteristics**

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As seen in the previous chapter, the unified model and extraction method (UMEM) shows advantages over other current-voltage models for OTFTs, mainly because most of its parameters have a clear physical meaning and because they are related to the properties of the material. In this chapter such parameters are introduced and their contribution for modeling the I-V characteristics is described by steps, including additional comments with the aim of identifying the parameters applied on the charge and capacitance model developed in this thesis.

### 3. UMEM: Extraction of parameters from the I-V characteristics

The model parameters are obtained from the current-voltage (I-V) characteristics of each OTFT under study. However, to successfully extract such parameters, it is important to have in mind that I-V characteristics of OTFTs are known to change with the application of prolonged voltages, i.e. bias-stress effect, which leads to operational instability [Zilker-2001].

For the extraction, output characteristics at different values of  $V_{GS}$  as well as transfer characteristics in linear and saturation regimes are needed; nevertheless it is suggested to generate the transfer characteristics from the output ones, so data can effectively match.

Additionally it is important to define from this point the voltage values for each operation condition: we will identify  $V_{DSl}$  as the drain voltage at which transfer characteristic in linear regime is measured and  $V_{DSs}$  as the transfer one measured in saturation regime, whereas  $V_{GSmax}$  will be the maximum gate voltage up to which linear transfer curves are measured and  $V_{DSmax}$  the maximum drain voltage up to which output curves are measured.

Once we have the set of the output and transfer characteristics of the device as well as the bias conditions defined, the data is processed by UMEM with the following steps for extracting the model parameters in different operation regimes.

#### 3.1 Above threshold regime ( $V_{GS} > V_T$ )

As seen in the previous chapter, the mobility in OTFTs is described by the power law equation dependent of the parameter  $\gamma$ , which describes the disorder

within the organic material (Eq. 2.). The drain current in linear region, i.e. for small  $V_{DS}$  values, and for  $V_{GS} > V_T$  is:

$$I_{DS} = \frac{W}{L} C_i \mu_0 \frac{(V_{GS} - V_T)^{1+\gamma} V_{DS}}{V_{aa}^\gamma} \quad (3.1)$$

In section 2.1.2, the  $V_T$  extraction in OTFTs was discussed, and since it cannot be calculated from the  $I_{DS}$  expression like in crystalline devices because  $I_{DS} \propto (V_{GS} - V_T)^{1+\gamma}$ , UMEM initiates its parameter extraction calculating the  $V_T$  value applying the integral function  $HI(V_{GS})$  using (3.1) [Ortiz-Conde-2001]. From this point, the steps for the above threshold regime are numbered:

**Step 1.** *Correction of the channel conductivity due to involuntary doping.* To obtain sufficient electrical conductivity for a useful current density, organic materials are doped under control [Ho-1999], [Kobayashi-2004], nevertheless substrate residual chemical species and ambient air can induce an involuntary doping in these materials.

In OTFTs, mainly in those using polythiophenes based polymers, atmospheric water and oxygen have a greater effect on the susceptibility of the device operation to air, causing an increase in the conductivity of the active layer and a slight decrease in field-effect mobility with exposure at ambient pressure [Hoshino-2004], [Liu-2009].

Thus, from the output characteristics we calculate the slope of  $I_{DS}$  vs.  $V_{DS}$  at  $V_{GS} < V_T$  (e.g.  $V_{GS} = 0$  V) between  $V_{DSmax}$  and  $V_{DSmax} - 2$ . The correction factor  $CC$  will be calculated as  $CC = 1/\text{slope}$ .

We subtract the current due to involuntary doping, expressed by  $CC/V_{DS}$ , from the measured curves in order to obtain corrected curves which are the ones used to extract the model parameters.

**Step 2.** Find  $V_{GSH1}$ , the maximum  $V_{GS}$  value for the  $HI(V_{GS})$ . Depending on the materials and technology applied on the OTFT, at high electric fields, effects of contact resistance, insulator-semiconductor interface or grain size of the bulk (in the case of small molecule materials) affect the I-V characteristics of the device [Xu-2010], [Mottaghi-2006]. We can observe such affectation e.g. when the transconductance of the channel stops increasing in the same rate as done at low values of  $V_{GS}$ . For this reason, to avoid errors in the parameter extraction, we find  $V_{GSH1}$  which is the value where the maximum point of the second differentiation of the transfer characteristic in linear regime is reached.

Since some measurement data present noise when differentiating, it is suggested to interpolate such data and apply the adaptive smoothing method for computer derivation.

**Step 3.** Calculation of  $V_T$  and  $\gamma$ . The integral function  $HI(V_{GS})$  is calculated with the experimental data of the transfer characteristic in linear regime  $I_{DSt}(V_{GS}, V_{DS1})$ , where the upper limit of integration is  $V_{GSH1}$ .

$$HI(V_{GS}) = \frac{\int_0^{V_{GS}=V_{GSH1}} I_{DSt}(V_{GS}) dV_{GS}}{I_{DSt}(V_{GS})} = \frac{1}{2+\gamma} (V_{GS} - V_T) \quad (3.2)$$

$HI(V_{GS})$  is linear in the strong accumulation region. Therefore, a plot of function  $HI(V_{GS})$  has a slope that defines the value of  $\gamma$  calculated as:

$$\gamma = \frac{1}{\text{slope}} - 2 \quad (3.3)$$

and the  $V_{GS}$  axis intercept allows us to obtain the value of  $V_T$  as follows:

$$V_T = \frac{\text{intercept}}{\text{slope}} \quad (3.4)$$

With (3.3) and (3.4) a straight-line fit of  $HI(V_{GS})$  plot is done in strong accumulation region to verify that the extracted values model correctly the  $HI(V_{GS})$  function, and according to (3.1), the remaining parameters may be obtained with:

$$\frac{W}{L} C_i \frac{\mu_0}{V_{aa}^\gamma} V_{DSt} = \frac{I_{DSt}}{(V_{GS} - V_T)^{1+\gamma}} \quad (3.5)$$

**Step 4.** Calculate the slope  $P_A$ . From (3.5) we obtain:

$$I_{DSt}^{\frac{1}{1+\gamma}} = P_A (V_{GS} - V_T) = \left[ \frac{W}{L} C_i \frac{\mu_0}{V_{aa}^\gamma} V_{DSt} \right]^{\frac{1}{1+\gamma}} (V_{GS} - V_T) \quad (3.6)$$

**Step 5.** Field effect mobility at low fields ( $\mu_{FET0}$ ). It is obtained by means of  $P_A$  as follows.

$$\mu_{FET0} = \frac{\mu_0}{V_{aa}^\gamma} = \frac{LP_A^{1+\gamma}}{WC_i V_{DSt}} \quad (3.7)$$

**Step 6.** Field effect mobility ( $\mu_{FET}$ ).

$$\mu_{FET} = \mu_{FET0} (V_{GS} - V_T)^\gamma \quad (3.8)$$

**Step 7. Series resistance  $I$ .** It is calculated for the maximum measured  $V_{GS}$ , i.e.  $V_{GSmax}$ .

$$R = \frac{V_{DS1}}{I_{DSlin}(V_{GSmax})} - \frac{1}{\frac{W}{L}C_i\mu_{FET}(V_{GSmax}-V_T)} \quad (3.9)$$

$R$  is a linear parameter that approximates the value of the real series resistance of the device. In some cases it is taken as  $0 \Omega$  when the calculation gives a negative value which is physically inconsistent. This is valid as long as the contact resistance does not affect the output characteristics at low  $V_{DS}$  values, in other words, as long as the difference between the work function of the semiconductor and the one of the drain and source contact is small.

However, if the contact resistance in the OTFTs is non-linear, we will calculate it by means of the voltage drop present in the diode formed by the semiconductor and the metal.

This procedure is based on the facts that the non-ohmic contact reduces  $I_{DS}$  at small bias. As the applied  $V_{DS}$  increases beyond the knee of the diode I-V curve, (near or after the maximum slope in the region of deformation), the applied voltage starts to fall mostly across the transistor.

The total  $V_{DS}$  applied directly on the contact is given by [Sze]:

$$V_{DStotal} = V_{DS} + V_{DSdiode} = \frac{I_{DS}}{G(V_{GS}, V_{DStotal})\xi} + \eta \frac{kT}{q} \log\left(\frac{I_{DS}}{I_{OD}}\right) \quad (3.10)$$

where  $G(V_{GS}, V_{DStotal})$  is the channel conductance of the OTFT (see Ref. [Estrada-2005]),  $\xi$  is a fitting parameter accounting for the real voltage across

the transistor when the diode resistance is significant,  $\eta$  is the ideality factor of the diode, and  $I_{OD}$  represents a constant value, called the saturation current of the diode, under reverse bias conditions, where  $V_{diode} \ll 0$ .

As an approximation, the contact resistance  $R_C$  in the OTFT can be estimated by fitting the measured output characteristics of the device with the following:

$$R_C = R_O + R_{CO} e^{-(\eta_d V_{DS} + \eta_g V_{GS})} \quad (3.11)$$

where  $R_O$  is the metal contact resistance,  $R_{CO}$  is the diode resistance, and  $\eta_d$  and  $\eta_g$  are fitting parameters describing drain and gate bias dependent ideality factors respectively.

Finally, the total resistance is the addition of the series resistance  $R$  calculated in (3.9) and  $R_C$ .

$$R_T = R + R_C \quad (3.12)$$

**Step 8.** *Calculation of the slope  $P_S$* , which is obtained similarly as  $P_A$ , but with the measured transfer characteristic in saturation regime ( $I_{DStsat}$ ).

$$I_{DStsat}^{\frac{1}{1+\gamma}} = P_S (V_{GS} - V_T) = \left[ \frac{W}{L} C_i \frac{\mu_0}{V_{aa}^\gamma} V_{DSS} \right]^{\frac{1}{1+\gamma}} (V_{GS} - V_T) \quad (3.13)$$

**Step 9.** *Saturation voltage  $V_{DSAT}$  (pinch-off)*. Once calculated  $P_S$  we can obtain the saturation parameter described in (3.14), whose value can be between 0.5 and 1 depending on the device technology.

$$\alpha_S = \frac{V_{DS1} P_S^{2+\gamma} \sqrt{2}}{P_A^{1+\gamma}} \quad (3.14)$$

Thus  $V_{DSAT}$  is given by:

$$V_{DSAT} = \alpha_S (V_{GS} - V_T) \quad (3.15)$$

**Step 10.** *Calculation of  $m$ .* This parameter adjusts analytically the curvature of the knee region of the output characteristics, i. e. the transition joining the linear and saturation regimes of the curves.

As already indicated previously, for modeling the I-V characteristics above threshold, we use [Fjeldly-1998], [Estrada-2008a]:

$$I_{DSa}(V_{GS}, V_{DS}) = \frac{W}{L} C_i \mu_{FET0} \frac{(V_{GS} - V_T)^{1+\gamma} V_{DS} (1 + \lambda |V_{DS}|)}{\left[ 1 + R_T \frac{W}{L} C_i \mu_{FET} (V_{GS} - V_T) \right] \left[ 1 + \left( \frac{V_{DS}}{V_{DSAT}} \right)^m \right]^{\frac{1}{m}}} \quad (3.16)$$

From (3.16),  $m$  is calculated with the  $V_{GS}$  maximum measured output characteristics in the pinch-off condition, i.e.  $I_{Dsexp}(V_{GS2}, V_{DSAT})$ , where  $V_{GS1}$  is the gate-to-source voltage equal or near  $V_{GSmax}$ . Considering  $V_{DSAT2} = \alpha_S (V_{GS2} - V_T)$  and  $\lambda = 0$

$$m = \frac{\log(2)}{\log \left( \frac{\frac{W}{L} C_i \mu_{FET0} \left[ \frac{(V_{DSAT2})^{1+\gamma}}{\alpha_S} \frac{V_{DSAT2}}{I_{Dsexp}(V_{GS2}, V_{DSAT})} \right]}{1 + \left[ R_T \frac{W}{L} C_i \mu_{FET0} \left( \frac{V_{DSAT2}}{\alpha_S} \right)^{1+\gamma} \right]}{\right)} \right)} \quad (3.17)$$

**Step 11.** *Calculation of the channel length modulation parameter  $\lambda$ .* When we refer to a channel length modulation, we point out the dependence of the OTFT channel length reduction  $\Delta L$  on  $V_{DS}$  when the pinch-off condition is reached.

For this reason,  $\lambda$  adjusts the saturation region of the model curves and is obtained from (3.13) evaluated under the saturation condition ( $V_{DSs}$ ) and the highest voltage from the output experimental data ( $V_{GS2}$ ).

$$\lambda = \frac{\left(\frac{I_{DSexp}(V_{GS2}, V_{DSmax})}{V_{DSmax}}\right)^2 \left[1 + \left[R \frac{W}{L} C_i \mu_{FET0} \left(\frac{V_{DSAT2}}{\alpha_S}\right)^{1+\gamma}\right]\right] \left[1 + \left(\frac{V_{DSmax}}{V_{DSAT2}}\right)^m\right]^{\frac{1}{m}}}{\frac{W}{L} C_i \mu_{FET0} \left(\frac{V_{DSAT2}}{\alpha_S}\right)^{1+\gamma}} - \frac{1}{V_{DSmax}} \quad (3.18)$$

**Step 13.** Finally we model the I-V characteristics with (3.16), but adding the current due to involuntary doping, expressed by  $CC/V_{DS}$ .

### 3.2 Subthreshold regime $V_{GS} > V_T$

In most cases, the subthreshold drain-to-source current  $I_{sub}$  approximates an exponential function of  $V_{GS}$ ; to model it, the following exponential expression was applied [Cerdeira-2011], [Kim-2012].

$$I_{sub} = I_{DSa} (V_{sub}, V_{DS}) \exp^{\frac{2.3}{S} V_{GT}} + I_0 \quad (3.19)$$

where  $I_{DSa}$  is the above threshold regime drain-to-source current described in (3.16),  $V_{sub}$  is a gate voltage value near to which the exponential dependence of  $I_{Dsa}$  starts;  $V_{GT} = V_{GS} - V_T$ , and  $I_0$  is the measured off current at a gate voltage sufficiently below  $V_T$ .  $S$  is the subthreshold slope for the linear and transfer

curves respectively.

To obtain the value of  $S$  we plot  $I_{DS}$  vs.  $V_{DS}$  in semilogarithmic scale and we calculate the slope of the experimental curve in the region where the plot is linear.

Finally, the total drain-to-source current in the OTFT is calculated as the sum of the two components: in the Subthreshold ( $I_{sub}$ ) and above threshold regimes ( $I_{Dsa}$ ). The  $\tanh$  function is used to join both regions

$$I_{DS} = I_{sub} \frac{1 - \tanh \delta}{2} + I_{Dsa} \frac{1 + \tanh \delta}{2} \quad (3.20)$$

where  $\delta = (V_{GT} - K)QI$  and  $K$  and  $QI$  are fitting parameters of the tanh function.

### 3.3 Calculation of the Density of states (DOS)

Even though it has been proved, experimentally and theoretically, that organic materials present a Gaussian distribution of DOS as seen previously in chapter 1, for modeling purposes, the exponential distribution is a good approximation for calculating the average DOS in the organic active layer.

As previously mentioned, the exponential distribution is defined by (3.21)

$$g(E) = g_0 \exp\left(-\frac{E}{Ea}\right) \quad (3.21)$$

where  $E$  is the relative energy respect the energy band in eV,  $g_0$  is the concentration of the localized states (acceptor states in n-type semiconductors,

and donor ones in p-type materials) in  $\text{cm}^{-3}$  and  $Ea$  is the characteristic energy, describing the exponential variation of the  $DOS$  function broadness, given by  $Ea = k_b T_0$ .  $K_b$  is the Boltzmann constant and  $T_0$  is the characteristic temperature of the  $DOS$  distribution which is associated with the disorder within the material since it depends on  $\gamma$  [Shur-1984].

$$T_0 = \frac{T}{2}(\gamma + 2) \quad (3.22)$$

where  $T$  is the absolute temperature.

$G_0$  is also extracted using the device geometry, temperature, and gate voltage overdrive dependent mobility expression obtained in [Estrada-2008a]. It is calculated from (2.7) in chapter 2, obtaining that:

$$g_{do} = \frac{\sin\left(\frac{\pi T}{T_0}\right)}{2\pi q k_b^2 T_0 T} \left[ \frac{V_{aa}^\gamma q N_V k_b T C_i^\gamma}{\epsilon_s^{(T_0/T)^{-1}}} \right]^{\frac{T}{T_0}} \quad (3.23)$$

### 3.4 Analysis of extracted parameters: Effect of $DOS$ on mobility in OTFTs.

Factors such as the properties of organic materials, gate dielectrics and electrodes [Park-2006], [J.Kim-2009], [Singh-2012], thickness of the active layer [Lee-2003], [Gburek-2010], the nature of the contact interfaces between the functional components [Boudinet-2010a], [Zhang-2011], [Dong-2012], and even fabrication conditions [Hoshino-2004] determine the performance of OTFTs. Nevertheless the main parameter affecting such performance is the low

mobility of carriers in organic materials due to their disordered nature determined by distributions of trap states localized between the HOMO and LUMO levels. Because of the relation of these states and the electrical performance of OTFTs, the understanding of their density of states (*DOS*) distribution is very useful to optimize the performance of devices fabricated with a specific material and for the synthesis of new organic materials.

As UMEM results to be a simple and precise tool to perform the *DOS* characterization of organic materials applied on OTFTs, in the following, we analyze the effect of the *DOS* on the field-dependent mobility of different materials by means of the model extracted parameters.

For this purpose devices fabricated with the n-type small molecule PDI N,N-dialkylsubstituted – (1,7 & 1,6) – dicyanoperylene – 3,4 : 9,10 – bis(dicarbiximide) derivative (Polyera Activink™ N1400), whose *DOS* had not been studied previously, were modeled [Castro-Carranza-2012b]. The extracted parameters were compared with those of devices fabricated with the more known p-type small-molecule 6,13-bis (triisopropylsilylethynyl) pentacene (TIPS-Pentacene), and the p-type polymer poly(triarylamine) (PTAA). The OTFTs were fabricated with a staggered bottom contact configuration as shown in figure 3.1. Drain and source electrodes were obtained by depositing 30-nm-thick layers of Au by plasma vapor deposition and patterned by photolithography on polyethylene naphthalene flexible substrates. Solutions of the three semiconductors were separately deposited by spin coating and cured at 388 K to eliminate their solvents. Afterward, a 1.2- $\mu\text{m}$  thick film of Cytop dielectric was spin coated on top of the semiconductor layers, respectively. Finally, Ag ink gate electrodes were printed by inkjet.

Details of the technological process of these devices can be found in [Verilhac-2010], [Boudinet-2010b].

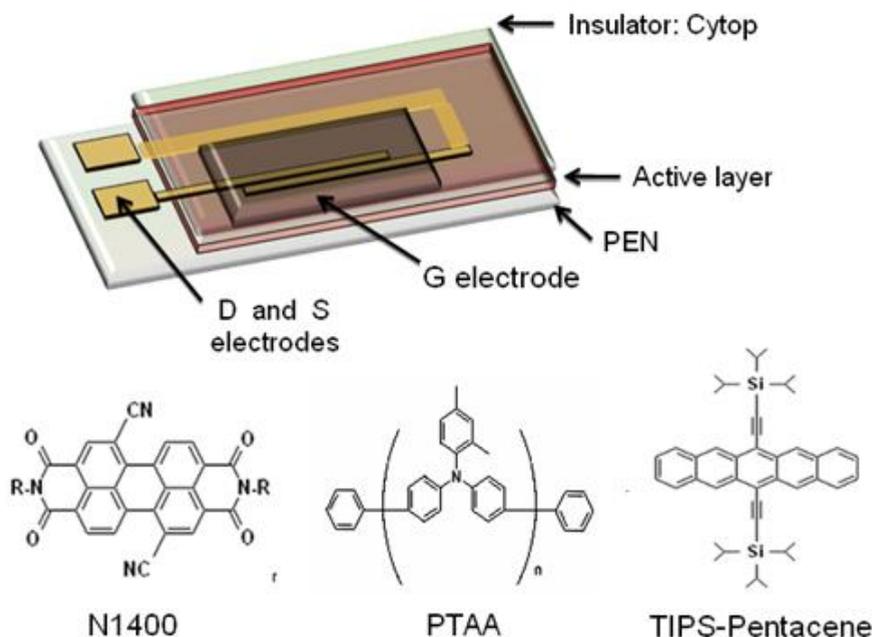


Fig.3.1. Chemical structures of the organic semiconductors used as active layers and the cross section of the fabricated staggered bottom contact OTFTs.

Transistors with different channel lengths  $L$  and widths  $W$  were fabricated. The values are shown in Table I. The current–voltage ( $I$ – $V$ ) characteristics of the devices were measured using an HP 4155A semiconductor parameter analyzer at room conditions.

Figure 3.2 shows the experimental and modeled output characteristics of OTFTs with active layers made of the perylene diimide Polyera Activink<sup>TM</sup> N1400, PTAA and TIPS-Pentacene respectively. All devices showed an ohmic contact checked by the slope of the lin-lin representation of their output characteristics respectively. The values of the extracted parameters in Table 3.1

show quite good repeatability, for all devices in the sample, independently of the channel length and width.

As shown in Table 3.1, TIPS-Pentacene transistors presented the highest mobility values followed by the PTAA and finally by the Polyera Activink<sup>TM</sup> N1400 ones. As TIPS-Pentacene and PTAA present similar  $E_a$  around 30meV, we attributed the difference in mobility to  $g_{d0}$ . Meanwhile that for the perylene diimide, the low mobility is due to a highest  $E_a$  which is around 50meV. These DOS parameters can be graphically visualized by plotting (3.21) with the extracted parameters as shown in figure 3.3.

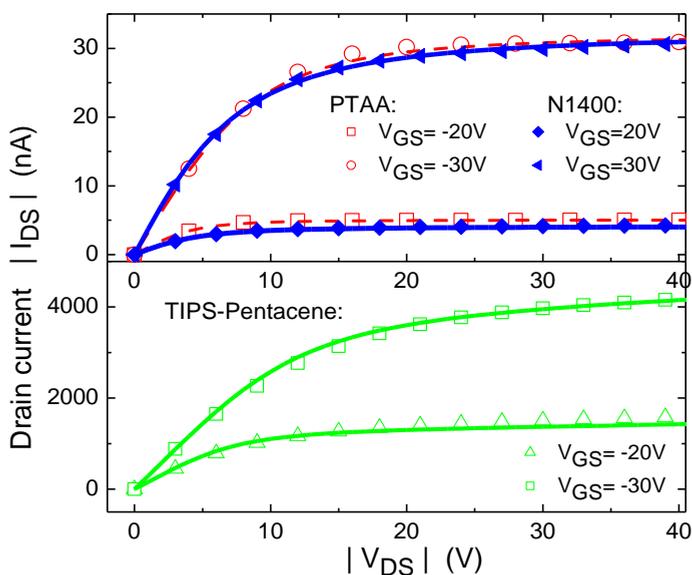


Fig. 3.2. (Symbols) Experimental and (lines) modeled output characteristics of TFTs based on the PDI Polyera Activink N1400, PTAA, and TIPS-Pentacene at  $|V_{GS}| = 20$  and  $30$  V, for OTFTs with  $W = 200 \mu\text{m}$  and  $L = 50 \mu\text{m}$ .

Model parameters	Material							
	Polyera Activink N1400				PTAA		TIPS-Pentacene	
$W$ ( $\mu\text{m}$ )	200	200	500	10000	200	200	200	200
$L$ ( $\mu\text{m}$ )	20	50	20	200	50	100	50	100
$\gamma$	1.71	2.21	1.76	2.00	0.55	0.61	0.36	0.40
$\mu_{FETLV}$ ( $\text{cm}^2/\text{Vs}$ )	$3.6 \times 10^{-5}$	$1.5 \times 10^{-5}$	$2.7 \times 10^{-5}$	$1.2 \times 10^{-5}$	$5.0 \times 10^{-3}$	$4.4 \times 10^{-3}$	0.49	0.58
$\mu_{FETHV}$ ( $\text{cm}^2/\text{Vs}$ )	0.037	0.108	0.035	0.042	0.041	0.048	2.051	2.868
$T_0$ (K)	557	631	564	600	382	392	353	361
$g_0$ ( $\text{cm}^{-3}/\text{eV}$ )	$2.4 \times 10^{21}$	$6.9 \times 10^{20}$	$2.3 \times 10^{21}$	$1.5 \times 10^{21}$	$1.9 \times 10^{22}$	$1.5 \times 10^{22}$	$1 \times 10^{21}$	$7.6 \times 10^{20}$
$E_g$ (eV)	0.048	0.054	0.049	0.052	0.033	0.034	0.030	0.031

$\mu_{FETLV}$  is the value of mobility at  $|V_{GS}-V_{FB}|=1\text{V}$ .  $\mu_{FETHV}$  is the mobility value at  $|V_{GS}|=60\text{V}$

Table 3.1. Extracted values for different transistors based on Polyera Activink N1400, PTAA and TIPS-Pentacene.

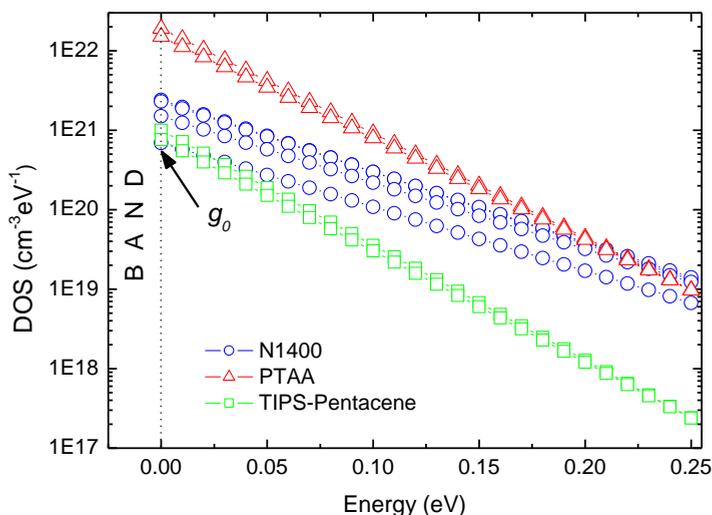


Fig. 3.3. Exponential DOS of the OTFTs under study.

Fig. 3.4 shows the dependence of the field-effect mobility  $\mu_{FET}$  on the gate voltage, as well as the dependence of the induced sheet charge of free carriers in the channel ( $ps$ ,  $ns$ ) on the gate voltage obtained in [Estrada-2008] and described in (3.24), for the three materials.  $Ps$  refers to holes in a p-type semiconductor, and  $ns$  refers to electrons in an n-type one, i.e.,

$$ps, ns(V_{GS}, T, T_0) = P^*(T, T_0) \cdot [C_i(V_{GS} - V_{FB})] \frac{2T_0}{T}^{-1} \quad (3.24)$$

where  $C_i$  is the dielectric capacitance per unit area, and

$$P^*(T, T_0) = N_{v,c} kT \left[ \frac{\sin(\pi T/T_0)}{g_{d0} (2\pi q)^k T_0 T} \right] \frac{T_0}{T} (\epsilon_s \epsilon_0)^{-\frac{T_0}{T} + 1} \quad (3.25)$$

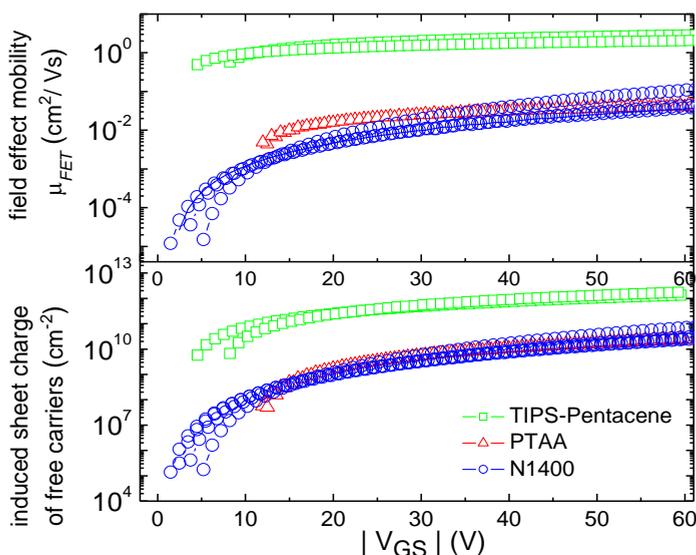


Fig. 3.4.  $|V_{GS}|$ -dependent mobility  $\mu_{FET}$  and induced charge of free carriers ( $ps$ ,  $ns$ ) referring to holes in a p-type semiconductor and electrons in an n-type one, respectively, for the studied OTFTs.

$N_V$  is the effective DOS in the valence band used in (3.25) for a p-type semiconductor, and  $N_C$  the effective DOS in the conduction band for an n-type semiconductor.  $E_0$  is the vacuum permittivity, and  $\epsilon_s$  is the relative dielectric constant of the semiconductor layer assumed as 3.5 for the three materials. Although the mobility of TIPS-Pentacene is higher than that of PTAA, the dependence on  $V_{GS}$  for both kinds of transistors is similar. However, there is a higher dependence of mobility on  $V_{GS}$  for the PDI N1400 transistors. Such mobility increment is around four orders of magnitude in the range of  $|V_{GS}|$  between 0 and 60 V, and it is attributed to the increase in the free-charge release from deep states, as shown in Figure 3.4. For this reason, at high  $|V_{GS}|$  values, the Polyera Activink N1400 mobility is similar to the PTAA one. The highest value of mobility presented in TIPS-Pentacene is attributed to a higher induced sheet charge of free charge since its DOS broadness is the smallest among the materials.

### 3.5 Summary

In this chapter we showed the feasibility of UMEM as a tool to extract parameters on OTFTs. With it we performed an analysis of the extracted parameters of the OTFTs based on N1400, Tips-Pentace and PTAA, where we show that the mobility is affected by the distribution of density of states in the material and by the induced sheet charge of free carriers. For the same characteristic energy  $E_a$ , the higher concentration of states  $g_{d0}$  is, the lower is the mobility value; while for a same  $g_{d0}$ , the higher  $E_a$  is, the lower is the mobility value. In the case of a high mobility material such the case of TIPS-Pentacene presenting small values of both  $g_{d0}$  and  $E_a$ , the higher values of mobility can be attributed to a higher ratio of free to localized carriers. The perylene diimide Polyera Activink<sup>TM</sup> N1400 showed high field dependence of

mobility and an interesting enhancement of it at high electric fields. It was suggested that its lower  $g_{d0}$  and higher  $Ea$  produces an increase of free charge from deep states at high  $V_{GS}$ .

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## CHAPTER 4.

### **UBCM: UMEM-based capacitance model for OFETs**

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In this chapter we present the development of the UMEM-based charge and capacitance model for OTFTs, which we have called UBCM. It is a compact and analytical quasi-static model that uses UMEM's extracted parameters from the I-V characteristics of the OTFTs.

In the following we show the evolution of UBCM described by three approximations: the capacitance model valid only in accumulation condition; the capacitance model valid in accumulation and total depletion; and finally the frequency dependent capacitance model in accumulation, partial and total depletion conditions.

## 4. UBCM: UMEM-based capacitance model for OTFTs

### 4.1 Charge Model

To develop the charge model we consider that the mobile charge as function of gate bias may be expressed as done by M. Shur et al. [Shur-1984], [Fjeldly-1998]

$$Q_{mob} = \frac{C_i (V_{GT} - V)^{1+\gamma}}{V_{aa}^\gamma} \quad (4.1)$$

where  $V$  is the potential applied along the channel of the OTFT, and  $V_{GT} = V_{GS} - V_T$ .  $V_{GS}$  is the gate-source voltage,  $V_T$  the threshold voltage; and  $C_i$  is the insulator capacitance per unit area. As already seen in previous chapters,  $\gamma$ , which is related to the disorder within the material, and  $V_{aa}$  are parameters extracted by UMEM from the measured electrical characteristics of the device. The energy distribution of states in the material is represented by an exponential function, where the characteristic temperature  $T_0$  is related to the model parameter  $\gamma$  as shown in chapter 3 by (3.22).

The drain current is calculated as indicated,

$$I_{DS} = W\mu_0 Q_{mob} \frac{dV}{dx} \quad (4.2)$$

where  $W$  is the channel width, and  $dV/dx$  is the differential term of the potential dependent on the position along the channel length ( $L$ ).

From (4.2) an expression for  $dx$  is obtained

$$dx = \frac{W\mu_0 Q_{mob}}{I_{DS}} dV \quad (4.3)$$

By integrating (4.3), we obtain an equation for the drain current

$$\int_0^L dx = \frac{WC_i}{I_D} \left( \frac{\mu_0}{V_{aa}^\gamma} \right) \int_0^{V_{DS}} (V_{GT} - V)^{1+\gamma} dV \quad (4.4)$$

$$I_D = \frac{-WC_i}{L} \left( \frac{\mu_0}{V_{aa}^\gamma} \right) \left[ \frac{(V_{GT} - V_{DS})^{2+\gamma} - (V_{GT})^{2+\gamma}}{2 + \gamma} \right] \quad (4.5)$$

$V_{DS}$  is replaced with the effective drain-source voltage  $V_{Dse}$  to describe the transition of the output characteristic from the linear to saturation regions.

$$V_{Dse} = \frac{V_{DS}}{\left[ 1 + \left( \frac{V_{DS}}{\beta V_{GT}} \right)^{m^*} \right]^{\frac{1}{m^*}}} \quad (4.6)$$

where  $m^*$  and  $\beta$  are fitting parameters.  $M^*$  adjusts the knee of the output I-V characteristics and the saturation voltage is  $\beta V_{GT}$ .

Finally after replacing  $V_{DS}$  with  $V_{Dse}$ , and adding a factor  $[1 + \lambda V_{DS}]$  to reproduce the behavior of the drain current in saturation region, a generalized  $I_D$  expression is obtained

$$I_D = \pm \frac{-WC_i}{L} \left( \frac{\mu_0}{V_{aa}^\gamma} \right) \frac{[(V_{GT} - V_{DSe})^{2+\gamma} - V_{GT}^{2+\gamma}]}{(2+\gamma)} \cdot [1 + \lambda V_{DS}] \quad (4.7)$$

where the positive sign is given for an N-channel OTFT, and the negative one for a P-channel device. Parameter  $\lambda$  is extracted by UMEM as already explained in step 11 of the previous chapter and obtained by (3.18).

This drain current expression has a similar form as the ones reported in [Fadlallah-2006], [Marinov-2009]. If we linearize it with respect to  $V_{DS}$  around  $V_{DS} = 0$  V and we use an interpolation function to obtain the desired behavior in saturation, we obtain the drain current in [Estrada-2008a] that corresponds to UMEM for OTFTs (3.16)

By definition, the total charge at the channel  $Q_{CH}$  is calculated as

$$Q_{CH} = W \int_0^L C_i (V_{GT} - V) dx \quad (4.8)$$

Replacing (4.3) in (4.8), the total charge in the channel, as function of  $V_{GS}$  and  $V_{DS}$  can be rewritten as (4.9)

$$Q_{CH} = W \int_0^{V_{DS}} C_i (V_{GT} - V) \frac{W\mu_0 Q_{mob}}{I_D^*} dV \quad (4.9)$$

where  $I_D^* = I_D / [1 + \lambda V_{DS}]$ .

After solving (4.9), a generalized expression for the total charge in the channel is obtained, which is also equal in magnitude to the total charge at the gate electrode. The detailed procedure is described in Appendix A for a P-type OTFT.

$$Q_G = -Q_{CH} = \mp \left[ -WLC_i \frac{(2 + \gamma)}{(3 + \gamma)} \left[ \frac{(V_{GT} - V_{DSe})^{3+\gamma} - V_{GT}^{3+\gamma}}{(V_{GT} - V_{DSe})^{2+\gamma} - V_{GT}^{2+\gamma}} \right] \right] \quad (4.10)$$

The total charge at the drain is obtained following the Ward–Dutton’s channel charge partitioning scheme [Ward-1978] (see Appendix A).

$$Q_D = \mp \frac{LWC_i(2 + \gamma)}{\left[ (V_{GT} - V_{DSe})^{2+\gamma} - V_{GT}^{2+\gamma} \right]^2} \cdot \left[ \frac{B}{(5 + 2\gamma)} - \frac{A_3 \cdot (V_{GT})^{2+\gamma}}{(3 + \gamma)} \right] \quad (4.11)$$

Where  $B = (V_{GT} - V_{DSe})^{5+2\gamma} - V_{GT}^{5+2\gamma}$  and  $A_3 = (V_{GT} - V_{DSe})^{3+\gamma} - V_{GT}^{3+\gamma}$ .

Finally the total charge at the source is calculated as

$$Q_S = \mp(Q_{CH} - Q_D) \quad (4.12)$$

Equations (4.10), (4.11) and (4.12) with negative sign describe the total charge at the corresponding electrodes of an N-channel OTFT. In contrast, for a P-channel device, (4.10)–(4.12) are taken with the positive sign [Castro-Carranza2012a].

The modeled total charge at gate, drain and source electrodes of a typical upper contact OTFT fabricated with PMMA on P3HT [Mejía-2008] is shown in figure 4.1. As gate bias increases, the total charge increases in a rate described by  $\gamma$ , i.e. the variation of charge depends on the disorder within the material of the active layer of the device.

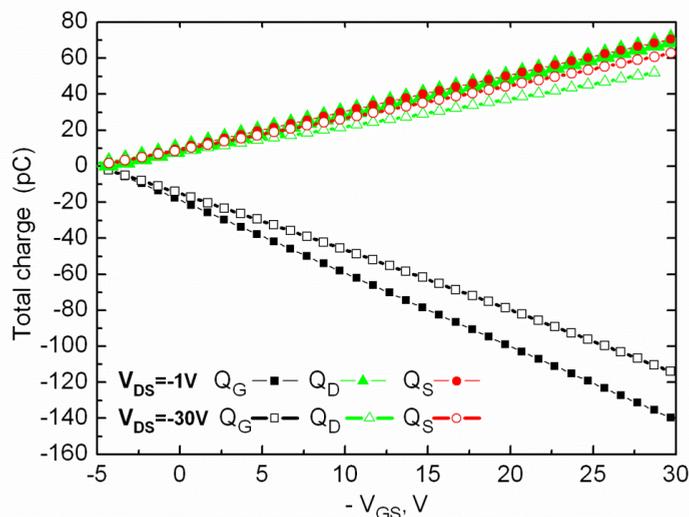


Fig. 4.1. Modeled total charge at gate, drain and source electrodes of a typical upper contact PMMA on P3HT TFT as function of gate-source voltage  $V_{GS}$  and threshold voltage  $V_T = -5$  V, in linear ( $V_{DS} = -1$  V) and saturation ( $V_{DS} = -30$  V) regimes.

## 4.2 Capacitance Model

As previously shown in chapter 2, a three terminal device requires nine nonreciprocal capacitances for small-signal simulation [Lu-2006], [Tsvidis-1999]. The nonreciprocal intrinsic capacitances are defined as:

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j} \quad i \neq j \quad (4.13)$$

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \quad i = j \quad (4.14)$$

where  $i$  and  $j$  refer to any of the three electrodes of the OFET: gate G, drain D and source S.

Capacitance, defined in (4.13) and (4.14), describes the relation between a variation of charge  $Q_i$  at the  $i$  electrode due to change of potential  $V_j$  of the  $j$  electrode [Tsidis-1999]. As  $C_{ij}$  represents the variation of charge  $Q_i$  at the  $i$  electrode due to change of potential  $V_j$  of the  $j$  electrode and  $C_{ji}$  represents the variation of charge  $Q_j$  at the  $j$  electrode due to change of potential  $V_i$  of the  $i$  electrode,  $C_{ij} \neq C_{ji}$ .

To obtain the nine intrinsic capacitances, it is not necessary to calculate all of them, as there is the following relation between them by applying the charge conservation law

$$C_{GG} = C_{GS} + C_{GD} = C_{SG} + C_{DG} \quad (4.15)$$

$$C_{DD} = C_{DS} + C_{DG} = C_{SD} + C_{GD} \quad (4.16)$$

$$C_{SS} = C_{SG} + C_{SD} = C_{GS} + C_{DS} \quad (4.17)$$

Four capacitances are independent from the others: the gate to gate capacitance  $C_{GG}$ , the gate to drain capacitance  $C_{GD}$ , the drain to drain capacitance  $C_{DD}$  and the drain to gate capacitance  $C_{DG}$ . Once these four intrinsic capacitances are

obtained, the remaining five ones can be calculated by means of (4.15) – (4.17)

as

$$C_{GS} = C_{GG} - C_{GD} \quad (4.18)$$

$$C_{SG} = C_{GG} - C_{DG} \quad (4.19)$$

$$C_{DS} = C_{DD} - C_{DG} \quad (4.20)$$

$$C_{SD} = C_{DD} - C_{GD} \quad (4.21)$$

Finally,  $C_{SS}$  can be obtained as (4.17).

$C_{GG}$  is one of the four independent capacitances and experimentally it is measured by applying a potential to the gate while grounding the drain and source electrodes. Its magnitude is equal to the magnitude of the channel-to-gate capacitance  $C_{CH-G}$ , which covers the intrinsic and extrinsic capacitance effects in the active area of the OTFT. Thus, in the following, we use  $C_{GG}$  to validate the UBCM.

We also considered the effect of the extrinsic capacitance due to the overlap of the gate with the source and drain contact areas, i.e. the parasitic coupling capacitance caused by the physical proximity of the gate and the source or drain electrodes, which must be added to the intrinsic capacitances in order to get the total capacitance  $C_{ij}$  in the device [Tsividis-1999]. The overlap capacitance is calculated as:

$$C_{OVR} = W \cdot L_{OVR} \cdot C_i \quad (4.22)$$

where  $L_{OVR}$  is the overlap length between gate and drain contacts and between gate and source contacts as can be seen in figure 4.2, where a symmetric overlapping is assumed in the devices we analyzed.

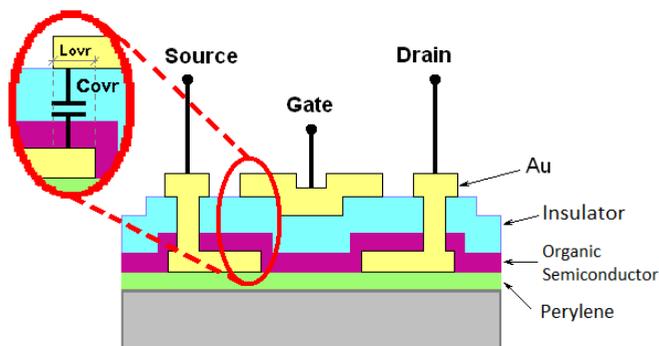


Fig. 4.2. Cross-section of the upper contact OTFT analyzed with this model, and the zoomed gate-to-source overlap capacitance  $C_{OVR}$  of the structure

### First Approximation: Valid in accumulation Regime ( $V_{GS} > V_T$ )

The total charge at the gate, drain and source electrodes described by (4.10), (4.11) and (4.12) respectively are obtained applying the generalized drain current expression (4.7) which is valid only for the above threshold condition  $V_{GS} > V_T$ , i.e. accumulation regime.

Thus, after the differentiation procedure of (4.13) and (4.14), analytical expressions for the four independent intrinsic capacitances for the above threshold condition are obtained considering the  $C_{OVR}$  effect.

$$C_{GG} = WLC_i(2 + \gamma) \left[ 1 - \frac{(2 + \gamma)A_1A_3}{(3 + \gamma)A_2^2} \right] + 2C_{OVR} \quad (4.23)$$

where

$$A_1 = (V_{GT} - V_{DSe})^{1+\gamma} - V_{GT}^{1+\gamma} \quad (4.24)$$

$$A_2 = (V_{GT} - V_{DSe})^{2+\gamma} - V_{GT}^{2+\gamma} \quad (4.25)$$

$$A_3 = (V_{GT} - V_{DSe})^{3+\gamma} - V_{GT}^{3+\gamma} \quad (4.26)$$

$$C_{GD} = \frac{WLC_i(2 + \gamma)}{A_2} \left[ V_{GT}^{2+\gamma} - \frac{(2 + \gamma)V_{GT}^{1+\gamma}A_3}{(3 + \gamma)A_2} \right] + C_{OVR} \quad (4.27)$$

$$C_{DD} = \frac{WLC_i(2 + \gamma)}{A_2^2} \left[ (V_{GT} - V_{DSe})^{4+2\gamma} + (4 + 2\gamma)(V_{GT} - V_{DSe})^{1+\gamma}N_{D1} - N_{D2} \right] + C_{OVR} \quad (4.28)$$

where

$$N_{D1} = \left[ \frac{V_{GT}^{2+\gamma}A_3}{(3 + \gamma)A_2} - \frac{B}{(5 + 2\gamma)A_2} \right] \quad (4.29)$$

$$B = (V_{GT} - V_{DSe})^{5+2\gamma} - V_{GT}^{5+2\gamma} \quad (4.30)$$

$$N_{D2} = V_{GT}^{2+\gamma}(V_{GT} - V_{DSe})^{2+\gamma} \quad (4.31)$$

$$C_{DG} = \frac{WLC_i(2 + \gamma)}{A_2^2} \cdot \left[ D - \frac{(4 + 2\gamma)N_{DG}A_1}{A_2} - \frac{(2 + \gamma)V_{GT}^{1+\gamma}A_3}{(3 + \gamma)} - V_{GT}^{2+\gamma}A_2 \right] + C_{OVR} \quad (4.32)$$

where

$$D = (V_{GT} - V_{DSe})^{4+2\gamma} - V_{GT}^{4+2\gamma} \quad (4.33)$$

$$N_{DG} = \left[ \frac{B}{(5 + 2\gamma)} - \frac{V_{GT}^{2+\gamma} A_3}{(3 + \gamma)} \right] \quad (4.34)$$

The capacitance equations directly obtained by the differentiation of the charge equations present a singularity under the  $V_{DS}=0$  condition (a 0/0 division) which can be solved by means of the asymptotic limit applying l'Hôpital rule, as proposed in [Iñíguez-2010].

Upper contact Poly(3-Hexylthiophene) (P3HT) on Poly(Methyl Methacrylate) (PMMA) TFTs were used to validate our capacitance model in accumulation regime. As shown schematically in figure 4.2, they were fabricated on a gold-perylene-glass substrate where drain and source contacts were defined by photolithographic process. A 0.66wt% dilution of Sigma-Aldrich regioregular P3HT in chloroform was spun to obtain a 90nm layer. Afterwards a 380–420 nm thick dielectric layer of PMMA 950K diluted in anisole at 6wt% from Microchem was also obtained by spin-coating technique. A detailed fabrication process of these devices is reported in [Mejía-2008].

Output and transfer characteristics of an upper contact P3HT/PMMA OTFT with dimensions  $W=210\mu\text{m}$ ,  $L=30\mu\text{m}$  and  $L_{OVR}=15\mu\text{m}$  were measured and model parameters extracted by UMEM are shown in Table 4.1 where the field effect mobility  $\mu_{FET}$  was obtained as indicated in (3.8) of the previous chapter. Figures 4.3a and 4.3b show the output and transfer characteristics of the device under study, respectively. Experimental and modeled curves are compared, where UMEM  $I_{DS}$  refers to (3.16) and the non-linearised  $I_{DS}$  refers to (4.7) which provides an approximation of the drain current allowing a simpler

analytical differentiation of the total charge at each electrode, in order to obtain the transcapacitances.

Parameter	value	units
$V_{FB}$	5.306	V
$\gamma$	0.815	
$V_{aa}$	$1.89 \times 10^3$	V
$m$	1.176	
$\lambda$	$-3.879 \times 10^{-4}$	1/V
$\mu_{FETO} (V_{GT}=-1V)$	$2.144 \times 10^{-3}$	$\text{cm}^2/\text{Vs}$
$\mu_{FET} (V_{GT}=-30V)$	0.039	$\text{cm}^2/\text{Vs}$
$T_0$	442.184	K
$gd_0$	$1.859 \times 10^{22}$	$\text{cm}^{-3}$
$\alpha$	0.508	

Table 4.1. Model parameters extracted for the PMMA on P3HT  
 OTFT with  $W=210 \mu\text{m}$  and  $L=30 \mu\text{m}$

For the same modeled OTFT, in figures 4.4a and 4.4b we show the curves of  $C_{GG}$ ,  $C_{GD}$  and  $C_{GS}$  as function of  $V_{DS}$ , for two values of  $V_{GS}$  and normalized to  $C_i+2C_{OVR}$ , obtained by simulation in Silvaco ATLAS [Atlas], by models reported in [Fadlallah-2006], [Li-2010] and by our model. As can be seen in Figure 4a, in the linear regime ( $V_{GT} > V_{DS}$ ), all models follow a similar behavior as the ATLAS simulation. However, when the operation of the device passes from the linear to the saturation regime ( $V_{GT} > V_{DS}$ ), see Figure 4b, our model shows to be continuous in the transition between the linear and saturation regimes, and converges to the expected values of capacitance [K.Kim-2010], while the other two models fail to describe the variation of the capacitance with the applied bias.

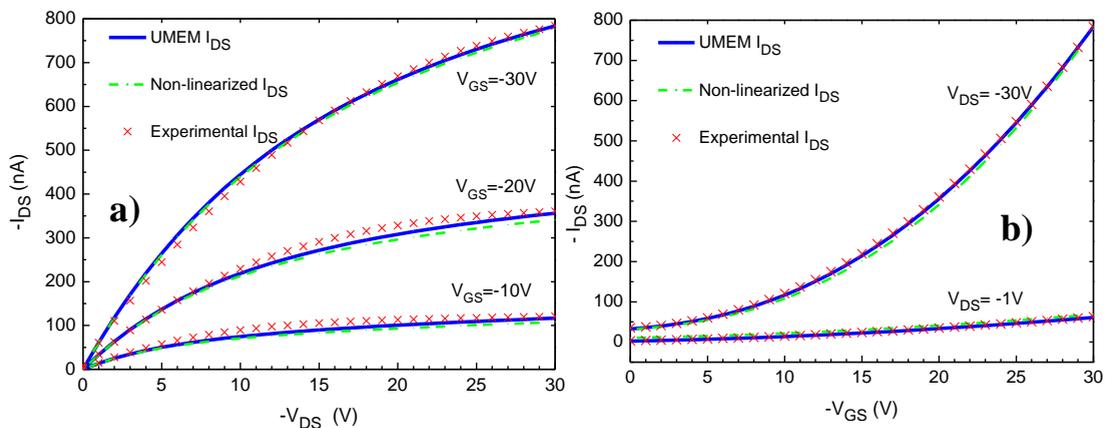


Fig. 4.3 Output and transfer characteristics of the device under study

T. Output and b) Transfer characteristics in linear ( $V_{DS} = -1$  V) and saturation ( $V_{DS} = -30$  V) regimes

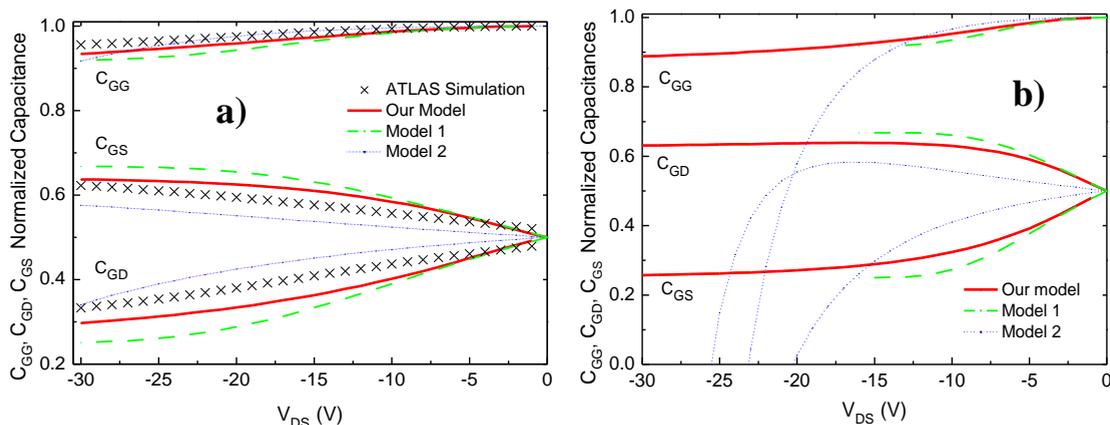


Fig. 4.4. Comparison of  $C_{GG}$ ,  $C_{GD}$  and  $C_{GS}$  against  $V_{DS}$  using different models for a)  $V_{GS} = -30$  V and b)  $V_{GS} = -10$  V. Capacitance is normalized to  $(WLC_i + 2C_{OVR})$  where  $WLC_i = 4.04 \times 10^{-13}$  F and  $C_{OVR} = 2.02 \times 10^{-13}$  F considering a dielectric thickness  $d_i = 360$  nm. Model 1 refers to [Fadlallah-2006] whereas Model 2 to [Li-2010].

It is worth to remark that when the saturation condition is reached, a variation of the voltage at the drain will not affect the rest of the device because of the pinch-off. However, even though the gate charge will not change due to  $V_D$ ,  $C_{GD}$  will approach a constant value established by the  $C_{OVR}$  magnitude.

Simulation in ATLAS was performed at 10 kHz since experimental measurements of capacitance of OTFTs in accumulation are expected to be similar for lower frequencies [Xu-2010], [Girolamo-2010].

Figure 4.5 shows the experimental capacitance  $C_{GG}$  vs  $V_G$  curve, normalized to  $C_i + 2C_{OVR}$ , for a PMMA on P3HT OTFT with  $W=210 \mu\text{m}$ ,  $L=30 \mu\text{m}$  and  $L_{OVR}=15 \mu\text{m}$ , with  $V_{DS}=0$ . Since the observed variation is very small, we present a zoom around the region where the variation is observed.

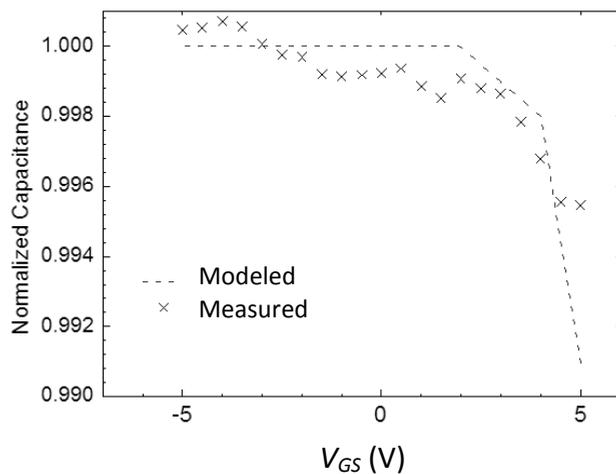


Fig. 4.5. Measured normalized  $C_{GG}$  in upper contact PMMA on P3HT OTFT with dimensions  $W = 210 \mu\text{m}$ ,  $L = 30 \mu\text{m}$  and  $L_{OVR} = 15 \mu\text{m}$  when drain and source are connected to ground. Modeled normalized  $C_{GG}$  calculated for  $V_{DS} = 0.1 \text{ V}$  is also shown. Both capacitances are normalized to  $(WLC_i + 2C_{OVR})$ .

Deviation of the experimental points is due to the values of the measured capacitance, which lie in the order of  $5 \times 10^{-13}$  F. The modeled curve was calculated for  $V_{DS}=0.1$  V to avoid convergence problems around  $V_{DS}=0$ .

#### 4.2.2 Second Approximation: Addition of Depletion Regime

The charge control and capacitance model previously developed was valid only in the above threshold regime [Castro-Carranza-2012a]. It depended on the drain-to-source current, which was described by means of a non-linearized expression. To add the depletion-regime operation of the device, in this approximation, the subthreshold drain-to source current  $I_{Dsub}$  is considered by means of an exponential expression, dependent on drain-to-source current above threshold regime  $I_{DSa}$  (3.19).

The total drain-to-source current in the OTFT is calculated as the sum of the two components, in above threshold and subthreshold regimes as shown in (3.20). Thus to obtain the total charge at the electrodes under these joint regions, we replace the total drain-to-source current  $I_{DS}$  in (A1) from Appendix A to obtain in the total charge in the channel obtained according to [Castro-Carranza-2012a], as follows:

$$Q_{CH2} = \mp \frac{-W^2 C_i^2}{\left( I_{sub} \frac{1 - \tanh \delta}{2} + I_{DSa} \frac{1 + \tanh \delta}{2} \right)} \mu_{FET0} \left[ \frac{(V_{GT} - V_{DSe})^{3+\gamma} - V_{GT}^{3+\gamma}}{3 + \gamma} \right] \quad (4.35)$$

And by replacing (3.20) in (A6) we obtain the total charge at the drain as:

$$Q_{D2} = \mp \frac{-(WC_i)^3}{L \cdot \left( I_{sub} \frac{1 - \tanh \delta}{2} + I_{Dsa} \frac{1 + \tanh \delta}{2} \right)^2} \mu_{FET0}^2 \left( \frac{1}{2 + \gamma} \right) \cdot \left[ \frac{B}{(-1)(5 + 2\gamma)} - \frac{A_3 \cdot (V_{GT})^{2 + \gamma}}{(-1)(3 + \gamma)} \right] \quad (4.36)$$

Where  $B = (V_{GT} - V_{DSe})^{5 + 2\gamma} - V_{GT}^{5 + 2\gamma}$  and  $A_3 = (V_{GT} - V_{DSe})^{3 + \gamma} - V_{GT}^{3 + \gamma}$ .

Finally the total charge at the source is given by (4.12). The negative sign describes the total charge at the corresponding electrodes of an N-channel OTFT. In contrast, for a P-channel device the positive sign is taken.

The capacitance model is obtained by differentiating the total charges at the electrodes described in (4.35) and (4.36) according to (4.13) and (4.14). To validate the drain-current and capacitance models, again, upper-contact P3HT/PMMA TFTs were fabricated and characterized. The UMEM parameters in Table 4.2 were extracted to model the drain-current above threshold and in the subthreshold region, showing a quite well modeling as seen in Figure 4.6a.

Parameter	P3HT OTFT	PCDTBT OTFT	Units
$V_T$	1.02	-4.72	V
$\gamma$	0.31	0.36	
$m$	3.11	1.98	
$\lambda$	$-6.38 \times 10^{-4}$	$-1.67 \times 10^{-4}$	1/V
$\mu_0$ ( $V_{GT} = -1V$ )	$8.20 \times 10^{-4}$	$1.57 \times 10^{-4}$	$\text{cm}^2/\text{Vs}$
$\mu_{FET}$ ( $V_{GT} = -30V$ )	$1.22 \times 10^{-3}$	$3.10 \times 10^{-4}$	$\text{cm}^2/\text{Vs}$
$T_0$	318	329	K
$gd_0$	$9 \times 10^{23}$	$3.46 \times 10^{24}$	$\text{cm}^{-3}$
$\alpha$	0.85	0.71	

TABLE 4.2. UMEM model parameters extracted from the I-V characteristics of the OTFTs under study.

The capacitance is also well reproduced above threshold as shown in Figure 4.6b. The experimental capacitances between 500 KHz and 1 kHz in accumulation behave similarly and are well described by the model, showing that a good agreement is obtained and that the model has been notably improved by comparing with the first approximation of Fig. 4.5. Nevertheless, the capacitance model is valid up to the subthreshold region where the exponential of the current is able to describe the I-V characteristic, in other words, the exponential function applied in Subthreshold (3.19) is not enough to describe the physics of the device when the condition of total depletion of the channel is reached [Castro-Carranza-2012c].

We also modeled OTFTs with poly[N-9''-hepta-decanyl-2,7-carbazole-alt-5,5-(4',7'-di-2-thienyl-2',1',3'-benzothiadiazole)] (PCDTBT) in the active layer and PMMA as insulator. The measurements and the modeled I-V and C-V characteristics are compared in Figures 4.7a and 4.7b respectively, showing a good agreement except in the total depletion condition, as similarly seen for the P3HT/PMMA devices. Notice that C-V characteristics show that the semiconductor layer depletes but inversion does not occur. This is attributed to trapping of minority carriers or to its negligible injection [Brondijk-2012].

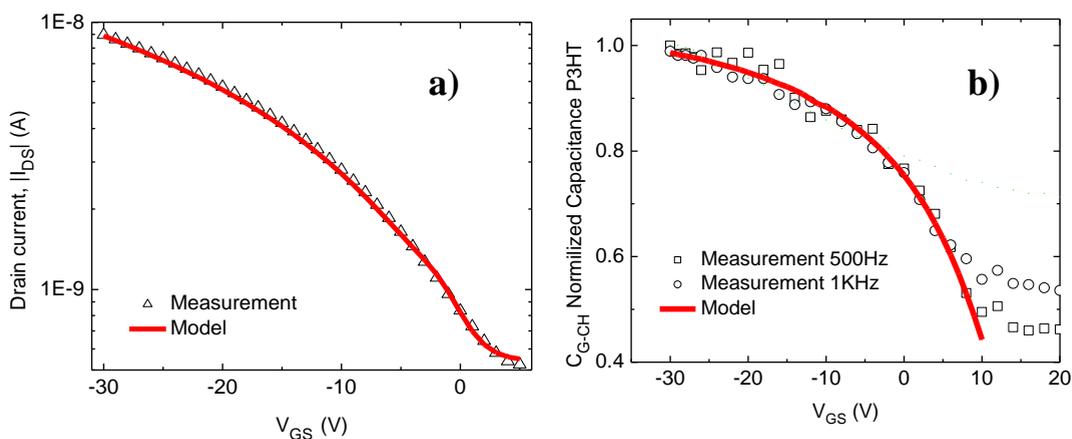


Fig.4.6. Modeled and experimental electrical characteristics of an OTFT fabricated with **P3HT** in the active layer, a channel length  $L=30 \mu\text{m}$ , a channel width  $W=110 \mu\text{m}$  and  $V_T = 2.1 \text{ V}$ : a) Transfer characteristic in linear regime,  $V_{DS} = -5 \text{ V}$  and b) Gate-to-channel capacitance  $C_{C-CH}$  at 500 Hz and 1 kHz.

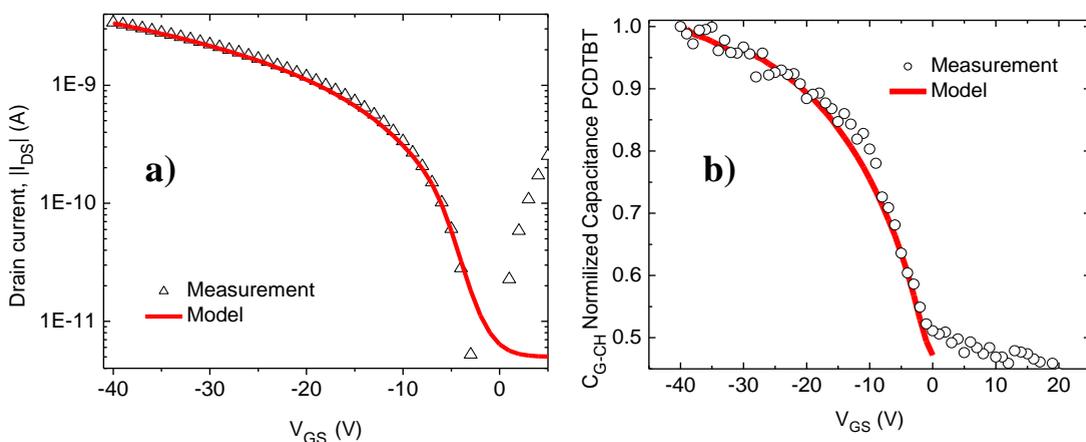


Fig.4.7. Modeled and experimental electrical characteristics of an OTFT fabricated with **PCDTBT** in the active layer,  $L=30 \mu\text{m}$ ,  $W=110$  and  $V_T = -3.6 \text{ V}$ : a) Transfer characteristic in linear regime,  $V_{DS} = -4 \text{ V}$  and b) Gate-to-channel capacitance  $C_{C-CH}$  at 100 Hz.

To account for the depletion region formed in the semiconductor we include the capacitance  $C_D$  assuming that generation/leakage currents in the depletion region are negligible, as similarly done in organic MIS capacitors [Torres-2005]. When the total depletion condition is reached, it is assumed that the depletion width is equal to the semiconductor thickness  $ds$ , giving rise to the minimum capacitance value in the semiconductor layer. The depletion capacitance  $C_D$  per unit area is described by (4.37).

$$C_D = \frac{\epsilon_{sr}\epsilon_0}{ds} \quad (4.37)$$

where  $\epsilon_{sr}$  is the relative permittivity of the semiconductor and  $\epsilon_0$  is the vacuum permittivity.

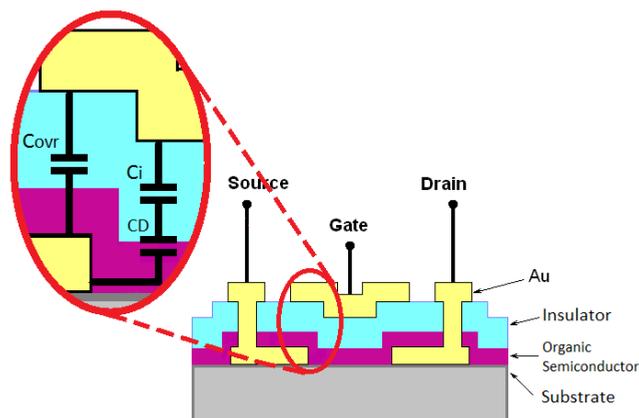


Fig. 4.8. Cross-section of the upper contact OTFT analyzed with this model, and the zoomed gate-to-source overlap capacitance  $C_{OVR}$  of the structure

An equivalent capacitance is obtained by the sum of the series arrangement of the insulator capacitance and the depleted semiconductor,  $C_i$  and  $C_D$ , Figure 4.8,

which will give an approximation of the minimum capacitance in the depletion region of the OTFT.

$$C_{Deq} = \frac{(C_D)(C_i)}{C_D + C_i} \quad (4.38)$$

The total capacitance model is given by the sum of the capacitances in accumulation and depletion regimes, sewed by a *tanh* function as follows:

$$C_{GG} = C_{Deq3} \left( \frac{1 - \tanh[(V_{GS} - V_T + Q1) \cdot Q2]}{2} \right) + \frac{\partial(-Q_{CH2})}{\partial V_{GS}} \left( \frac{1 + \tanh[(V_{GS} - V_T + Q1) \cdot Q2]}{2} \right) \quad (4.39)$$

Where *Q1* and *Q2* are fitting parameters of the tanh function.

Capacitance characteristics of P3HT/PMMA and PCDTBT/PMMA OTFTs with  $W=110 \mu\text{m}$  and  $L=30 \mu\text{m}$  were modeled and are shown in Figures 4.9 and 4.10 respectively. In this devices the contact resistance is negligible since an ohmic contact is present in the semiconductor-contact junction, for both, P3HT and PCDTBT with Au. It was seen from the lin-lin plot of the output characteristics at low  $V_{DS}$ .

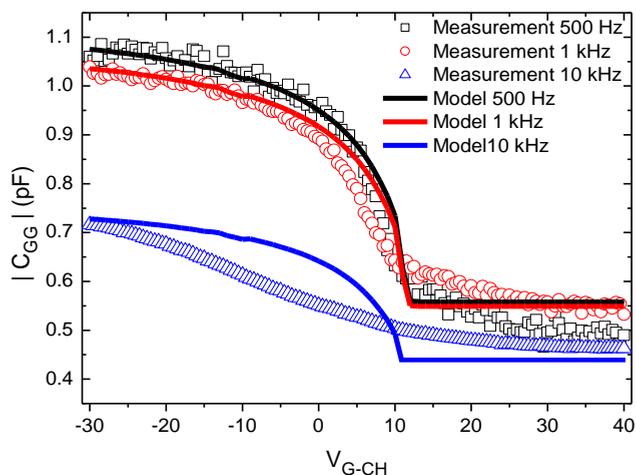


Fig.4.9. Experimental gate-to-gate capacitance  $C_{GG}$  at different frequencies of an OTFT fabricated with **P3HT** in the active layer and compared to the second approximation of the capacitance model .

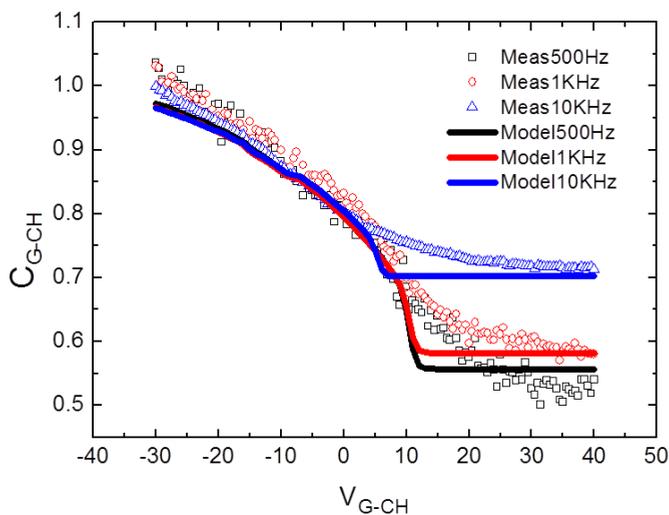


Fig.4.10. Experimental gate-to-gate capacitance  $C_{GG}$  at different frequencies of an OTFT fabricated with **PCDTBT** in the active layer and compared to the second approximation of the capacitance model .

### **4.2.3 Preliminary Study of frequency dispersion effects to consider in a capacitance model for OTFTs**

The capacitance in a metal-dielectric semiconductor structure conforms of the capacitance due to the dielectric in series with the capacitance due to the depleted region in the semiconductor. Each capacitance will show frequency dependence due to the frequency dependence of the dielectric constant of each material. The variation of the capacitance in accumulation of the TFT is mainly due to frequency dependence of the capacitance due to the dielectric. As the semiconductor depletes, the decrease in capacitance will also depend on trapped carriers that cannot follow the small signal variation at such high frequencies. Other complementary effects have been studied as the one of contact interface molecular doping [Miyadera-2007a] and the presence of grain boundary [Miyadera-2007b] in small molecule organic materials. In general, the impact of the frequency dispersion can be noticed at each operation regime of the CV characteristic.

Device simulation is a powerful tool to study the effect of different parameters on the behavior of a certain magnitude, which is difficult and sometimes impossible to achieve in an experimental way. In this paper we use device simulations to study the influence of some material parameters in the behavior of the device capacitance with frequency. The study includes the analysis of variation of the minority carrier lifetime  $\tau$  variations, the density of localized states (DOS), capture section  $\sigma$  and the impurity concentration of the semiconductor ( $NB$ ) on the capacitance behavior with frequency.

In this section we present the analysis for a Polymer TFT (PTFT) fabricated with Poly(Methyl Methacrylate) (PMMA) on Poly(3-Hexyl-thiophene) (P3HT)[Castro-Carranza-2011b].

For validation purposes, the simulation of C-V curves at 1 MHz, with input data extracted from experiment for these TFTs, were compared with measured CV curves. Experimental devices with a channel length  $L=30\mu\text{m}$ , a channel width  $W=210\mu\text{m}$  and a total overlap length  $L_{ovr}=30\mu\text{m}$ , were prepared starting with the deposition of 70nm-thick drain and source gold electrodes on glass substrate. Afterwards, an 80nm – thick P3HT film was deposited by spin-coating, followed by the deposition, also by spin coating of a 320nm-thick PMMA one were deposited as well. After etching the contact areas, a gold layer is deposited in order to get the upper contact structure [Mejía-2008]. A final 200 nm-thick gold layer is deposited. Etching technique is applied in order to define the three electrodes: Source, Gate and Drain.

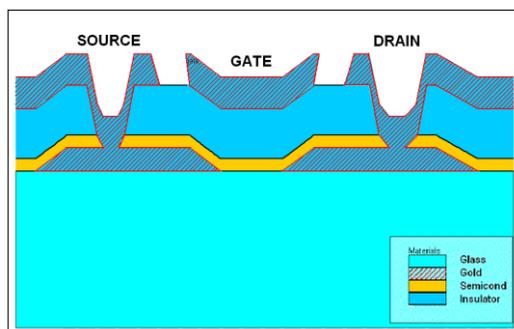


Fig 4.11. Silvaco ATHENAS 2-D Structure of the simulated PTFTs.

The structure of these devices was also prepared in the device simulator Silvaco ATHENAS, to correspond to the experimental devices, see Figure 4.1,1 with the same channel length, channel width and overlap. 2-D

Simulations in Atlas of CV curves at 1 MHz, 1 kHz and 100 Hz, for different material parameters were done.

As reference point, the structure of Figure 4.11 was simulated considering Si as the semiconductor layer using Atlas default parameters for this material. The minority carrier lifetime was considered to be  $\tau_0=1 \times 10^{-7}$  s, the minority carrier capture section  $\sigma=1 \times 10^{-15}$  cm<sup>2</sup> and the charge carrier mobility was  $\mu=1000$  cm<sup>2</sup>/Vs. As expected, up to 1 MHz, no frequency dependence of the C-V characteristics is observed, as shown in Figure 4.12.

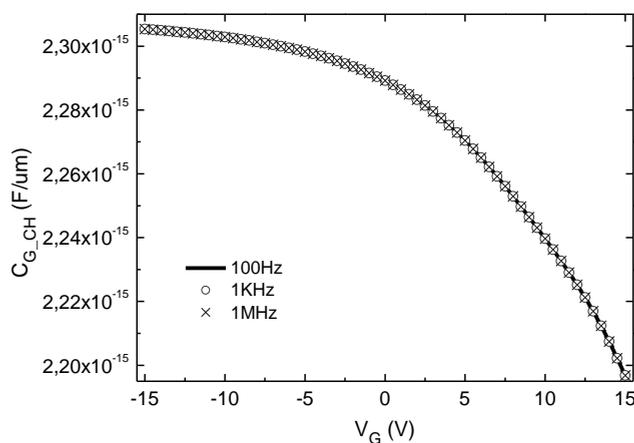


Fig 4.12. Simulated gate-to-channel capacitance  $C_{G\_CH}$  vs.  $V_G$  of a TFT considering Si as the semiconductor layer.

In order to describe the P3HT layer, simulations were obtained changing the semiconductor band gap  $E_g$  to that of the P3HT:  $E_{gP3HT}=1.8$  eV, the Highest Occupied Molecular Orbital  $HOMO_{P3HT}= 5$  eV, and the Lowest Unoccupied Molecular Orbital  $LUMO_{P3HT}= 3.2$  eV [Nolasco-2010]. The effective density of states in the conduction band  $N_c$  and in the valence band  $N_v$  are given as  $1 \times 10^{21}$  cm<sup>-3</sup> to represent those of the P3HT. Minority carrier capture section

and lifetime were kept the same as for Si. Simulations are validated with experimental data of the PMMA on P3HT TFT, measured with the capacitance meter Boonton 72 at 1MHz, Figure 4.13.

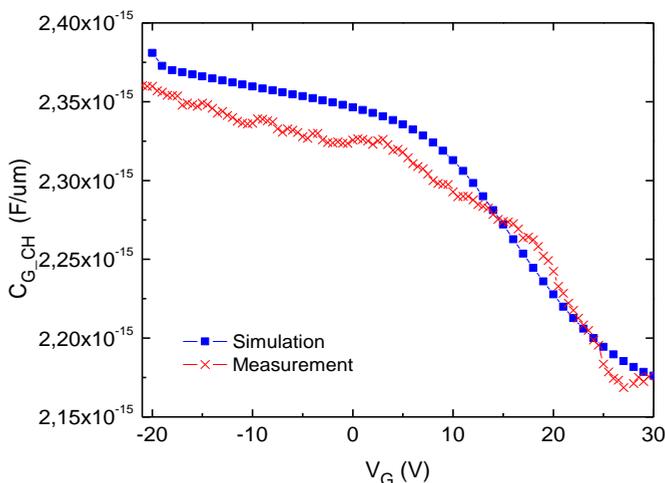


Fig.4.13. Experimental and simulated  $C_{G,CH}$  vs.  $V_G$  characteristic of a PMMA on P3HT TFT at 1MHz.

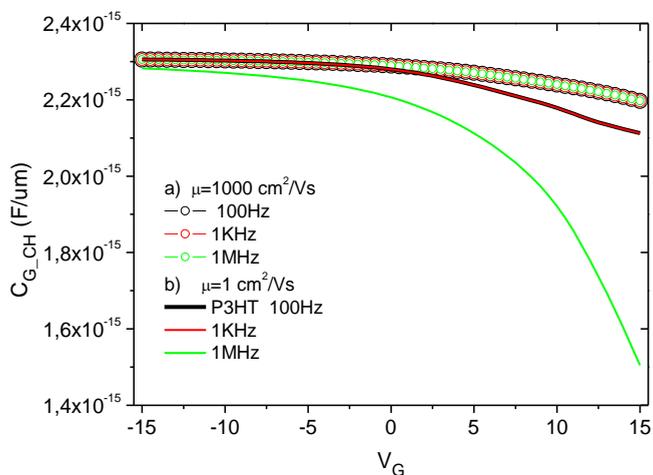


Fig.4.14. Comparison of  $C_{G,CH}$  vs.  $V_G$  characteristic for a TFT with P3HT layer, considering  $\sigma=1 \times 10^{-15} \text{ cm}^{-2}$  and  $\tau_0=1 \times 10^{-7} \text{ s}$  with a)  $\mu=1000 \text{ cm}^2/\text{Vs}$ , and b)  $\mu=1 \text{ cm}^2/\text{Vs}$  at different frequencies.

When mobility was decreased down to  $\mu=1 \text{ cm}^2/\text{Vs}$ , the gate-to-channel capacitance  $C_{G\_CH}$  under accumulation condition is slightly reduced at 1 MHz. In addition, when the gate bias  $V_G$  increases in order to enter the depletion condition,  $C_{G\_CH}$  drops much faster than for  $\mu=1000 \text{ cm}^2/\text{Vs}$ , Figure 4.14.

Figure 4.15 shows again that for P3HT, if the mobility is reduced,  $C_{G\_CH}(V_G)$  decreases more significantly as frequency increases. For a constant mobility in the order or below  $1 \text{ cm}^2/\text{Vs}$ , if  $\tau_0$  decreases from  $1 \times 10^{-7} \text{ s}$  to  $1 \times 10^{-9} \text{ s}$ , the  $C_{G\_CH}$  drop towards depletion regime is more pronounced at higher frequency. Under accumulation regime, however, the capacitance remains the same. This behavior can be explained since  $\tau_0$  is related to the minority carrier behavior; the variation of the capacitance in accumulation due to this parameter is expected to be insignificant since the channel in this PTFT is formed by accumulation of charge. Although not shown, variation of the capture section  $\sigma$  from  $1 \times 10^{-15} \text{ cm}^2$  to  $1 \times 10^{-10} \text{ cm}^2$ , caused  $C_{G\_CH}$  to decrease more in the depletion regime; but the capacitance in accumulation is not affected either.

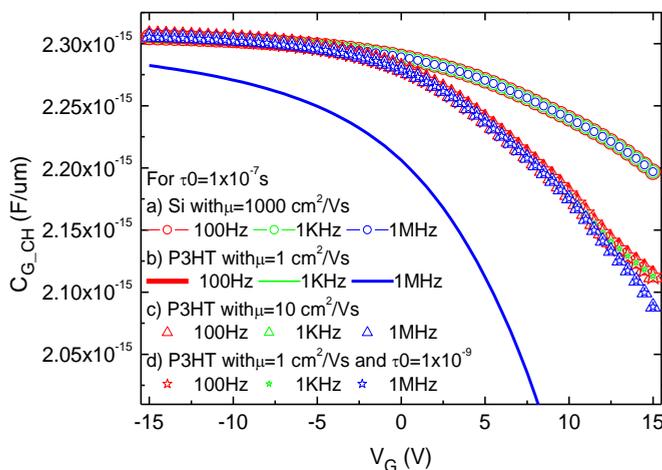


Fig. 4.15.  $C_{G\_CH}$  vs.  $V_G$  characteristics for  $\tau_0=1 \times 10^{-7}$ , considering the semiconductor to be:

- T. Si with  $\mu=1000 \text{ cm}^2/\text{Vs}$ ; b) P3HT with  $\mu=1 \text{ cm}^2/\text{Vs}$ ; c) P3HT with  $\mu=10 \text{ cm}^2/\text{Vs}$ ; and
- d) P3HT with  $\mu=1 \text{ cm}^2/\text{Vs}$  and  $\tau_0=1 \times 10^{-9}$ .

The effect of the semiconductor doping and the introduction of a distribution of localized states  $DOS$  into the semiconductor are shown in Figure 4.16 by comparing the  $C_{G\_CH}$  for three cases of semiconductor layer: a) Si with a semiconductor doping  $NB= 1 \times 10^{17} \text{ cm}^{-3}$ ; b) P3HT with  $NB_{P3HT}= 1 \times 10^{17} \text{ cm}^{-3}$  and a  $DOS$  extracted from measurements; and c) P3HT with  $DOS$  and  $NB_{P3HT}=1 \times 10^{13} \text{ cm}^{-3}$ . At low frequency and throughout the depletion regime, a significant variation is noticed. As higher the frequency, higher the capacitance drop under all regimes. The effect of a  $DOS$  causes a capacitance variation due to the reduction of the free carrier concentration; in other words, free carriers are trapped due to a  $DOS$  and while they are trapped, at higher frequencies, such carriers will remain trapped due to the inability of following the high frequency small signal.

It is important to remark that the semiconductor doping  $NB$  is an important parameter to take into account because its effect determines how many free carriers will be present in the material. If  $NB$  is lower, the capacitance will get into depletion regime easily due to a higher rate of trapped charge, and more potential will be necessary to get into accumulation regime as seen in Figure 4.16.

Simulations showed that the variation of the characteristics of the active material such as the energy gap  $E_g$  and HOMO, and LUMO levels do not affect the behavior of  $C_{G\_CH}$  vs. frequency. On the contrary, the dependence of  $C_{G\_CH}$  on frequency is significant as carrier mobility reduces. The mobility is affected by the distribution of localized states  $DOS$  and the semiconductor doping  $NA$ . The presence of  $DOS$ , characterized by the characteristic temperature  $T_0$  and the concentration of localized states  $gd_0$ , reduces the carrier

mobility, which in these devices is due to the hopping mechanism and showed considerable effect on the frequency dispersion of the TFTs capacitance.

The minority carrier lifetime  $\tau_0$  and the minority carrier capture section  $\sigma$  do not affect significantly the capacitance characteristic at different frequencies.

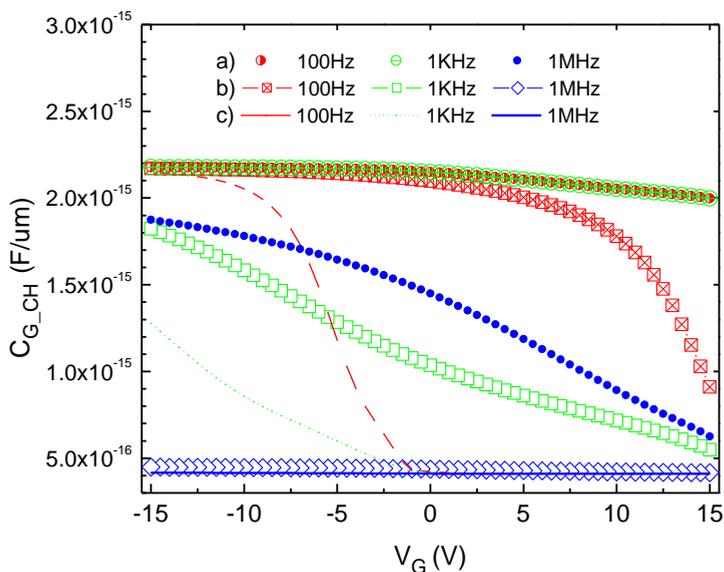


Fig.4.16.  $C_{G,CH}$  vs.  $V_G$  considering  $\tau_0=1 \times 10^{-7} s$  and  $\mu=1 \text{ cm}^2/Vs$  for three semiconductor layer conditions: a) Si with  $NA= 1 \times 10^{13} \text{ cm}^{-3}$ ; b) P3HT with  $NA_{P3HT}= 1 \times 10^{17} \text{ cm}^{-3}$ ; and c) P3HT with  $NA_{P3HT}=1 \times 10^{13} \text{ cm}^{-3}$ .

The present preliminary study provides important details for the optimization of the active layer properties and device characteristics at different frequency operating range. The identification of the parameters affecting the frequency dispersion through the operation regimes will be subsequently taken into account to improve our compact capacitance model.

#### 4.2.4 Third Approximation: Frequency dependent UBCM in accumulation, partial and total depletion conditions

The capacitance in accumulation of the OTFT is mainly is affected by the frequency dependence of the insulator capacitance. As the semiconductor depletes, the decrease in capacitance will also depend on trapped carriers that cannot follow the small signal variation at such high frequencies. For this reason, to model the effects of frequency dispersion in OTFTs, we first analyzed simpler structures, i.e. metal-insulator-semiconductor capacitors [Estrada-s]. It was seen that up to  $f=100$  kHz, the capacitance in accumulation,  $C_{accum}$  in MIS structures reduces in a similar way as frequency increases, independently of the polymer used as semiconductor layer and also of its thickness.

The variation of  $C_{accum}$  vs.  $f$  for the different MIS structures (with different semiconductors) is shown in Figure 4.17. In this figure it is also plotted the variation of capacitance with frequency observed for a capacitor containing only PMMA, confirming that the reduction of  $C_{accum}$  with frequency up to around 100 kHz in Structures 1 and 2, is mainly due to the reduction of the dielectric constant of the PMMA, which follows the empirical formula proposed by [Cole-1941] to represent the variation of the dielectric constant for a considerable number of liquids and solids:

$$k_i = k_{i\infty} + \frac{(k_{i0} - k_{i\infty})}{[1 + j\omega\tau]^p} \quad (4.40)$$

$k_{i0}$  and  $k_{i\infty}$  are the permittivity at very low and very high frequencies, respectively,  $\tau$  is the relaxation time and  $1 > p > 0$ . In Fig. 4.17, adjustment is

obtained for  $k_{i0}=3.56$ ,  $k_{i\infty}=2.56$ ,  $\tau=1\times 10^{-2}$  s and  $p=0.22$ . A value of  $k_i=2.6$  at 1 MHz was reported before in [Puigdollers-2004], [Estrada-2008b] for PMMA.

The variation of  $C_{accum}$  with frequency in the range below 1 MHz has also been observed by other authors. For example, in some figures presented in [Torres-2005], it is seen that  $C_{accum}$  is also frequency dependent in the frequency range between 5 kHz and 1 MHz in PTFTS using polysilsesquioxane (PSQ) as insulating layer and P3HT as semiconductor.

In Fig. 4.17 it is also seen that for devices in Structure 1, at frequencies above 100 kHz,  $C_{accum}$  decreases more rapidly than expected if only the variation of  $k_i$  vs.  $f$  is considered. For devices in Structure 3,  $C_{accum}$  started to deviate from the reduction due to the  $k_i$  of the PMMA at frequencies around 80 kHz.

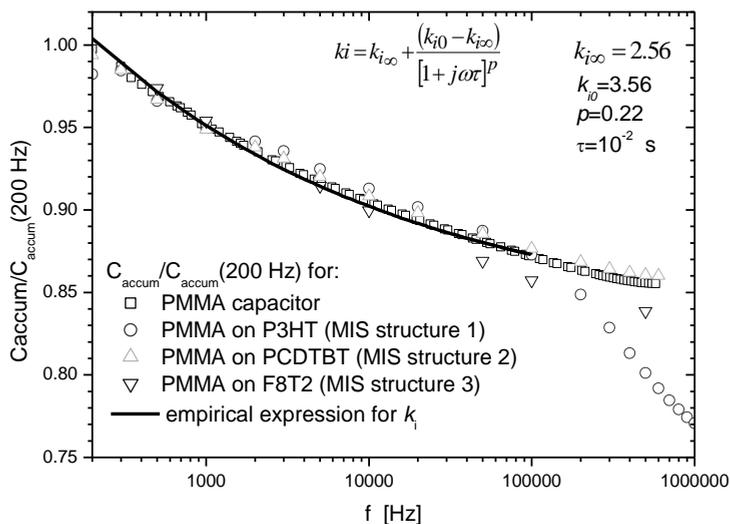


Fig.4.17. Variation of the capacitance in accumulation at different frequencies normalized to its value at 200 Hz for Structures 1, 2 and 3 and for a capacitor with only PMMA. The empirical law of the variation of the dielectric constant  $k_i$  is also shown.

In the second approximation it was possible to describe the capacitance in accumulation and total depletion, but as seen in Figures 4.9 and 4.10, an abrupt change of capacitance occurs when the total depletion condition is reached, indicating that the depletion width in the semiconductor is equal to the layer thickness  $ds$ . Nevertheless in real devices partial depletion occurs before reaching the total depletion condition, forming a gate-voltage-dependent capacitance in subthreshold. In other words, in below threshold condition, a depleted layer is formed in the semiconductor which gives place to the depletion capacitance, which differing from (4.37), it depends on the depletion width in the semiconductor  $W_D$ :

$$C_D = \frac{\epsilon_s LW}{W_D} \quad (4.41)$$

where  $\epsilon_s$  is the permittivity of the semiconductor layer,  $L$  and  $W$  are the channel length and width of the device respectively. The depletion gate-bias-dependent width  $W_D$  is given by:

$$W_D = -\frac{\epsilon_s}{C_i} + \sqrt{\frac{\epsilon_s^2}{C_i^2} + \frac{2\epsilon_s|V_{GS} - V_T|}{qN_B}} \quad (4.42)$$

$q$  is the electron charge and  $N_B$  is the semiconductor concentration which is in the order of  $\sim 10^{14} \text{ cm}^{-3}$  in non-intentionally doped molecular semiconductors whereas up to  $\sim 10^{17} \text{ cm}^{-3}$  in polymeric materials [Kim-2013].

When  $W_D$  extends to the total width of the semiconductor layer  $ds$ , the condition of full depletion is reached. Thus,  $W_D$  will be replaced by  $ds$  (4.37). In organic materials inversion is not observed as already mentioned in chapter

1 [Brondijk-2012]. The equivalent capacitance in the depletion regime is then obtained from the sum of the series combination of  $C_i$  and  $C_D$ , i.e.  $C_{eq}=(C_D \cdot C_i)/(C_D+C_i)$  as (4.38).

Finally the complete capacitance model is given by the sum of the capacitances from the accumulation to depletion regimes, joint by a *tanh* function as follows [Castro-Carranza-s]:

$$C_{GGtotal} = C_{Deq} \times \frac{1 - \tanh\left[\frac{(V_{GT} + \Delta V_T)Q2}{2}\right]}{2} + C_{Gga} \times \frac{1 + \tanh\left[\frac{(V_{GT} + \Delta V_T)Q2}{2}\right]}{2} \quad (4.42)$$

where  $\Delta_T$  is the shift in the threshold voltage of the C-V characteristic at different frequencies, and  $Q2$  is a transition parameter of the *tanh* function.

To validate this approximation of our model, staggered OTFTs with upper contacts and active layers based on (*PCDTBT*) and poly(3-hexylthiophene) (*P3HT*) were fabricated. Au contacts were deposited, and the poly(methyl methacrylate) (*PMMA*) was applied as insulator. The channel lengths of the OTFTs are  $L=30\mu\text{m}$ , the channel widths  $W=210\mu\text{m}$  and  $L_{OVR}=15\mu\text{m}$ .

The output and transfer characteristics of the devices under study were measured and modeled by UMEM [Estrada-2008a]. The extracted parameters are shown in Table 4.4, where  $m$ ,  $\lambda$  and  $\alpha$  are fitting parameters, and  $\mu_{FET}$  is the field effect mobility obtained as indicated in [Castro-Carranza-2012b]. These extracted parameters were applied on the capacitance model.

The relative permittivity constants of *PCBTBT* and *P3HT* were assumed to be  $\epsilon_r = 3.2$  [Raja-2011], and for *PMMA*, the dielectric constant is described by

(4.40).  $N_B$  was assumed as  $1 \times 10^{17} \text{ cm}^{-3}$  [Reséndiz-2010],  $K = 2$  and  $QI = 0.45$  for both devices. Experimental and modeled curves are compared as shown in Figure 4.18 and Figure 4.19, where it can be seen that the capacitance model gives a good description of the behavior of  $C_{GG}$  in all the operating regimes at low and medium frequencies. As frequency increases a non static model is necessary.

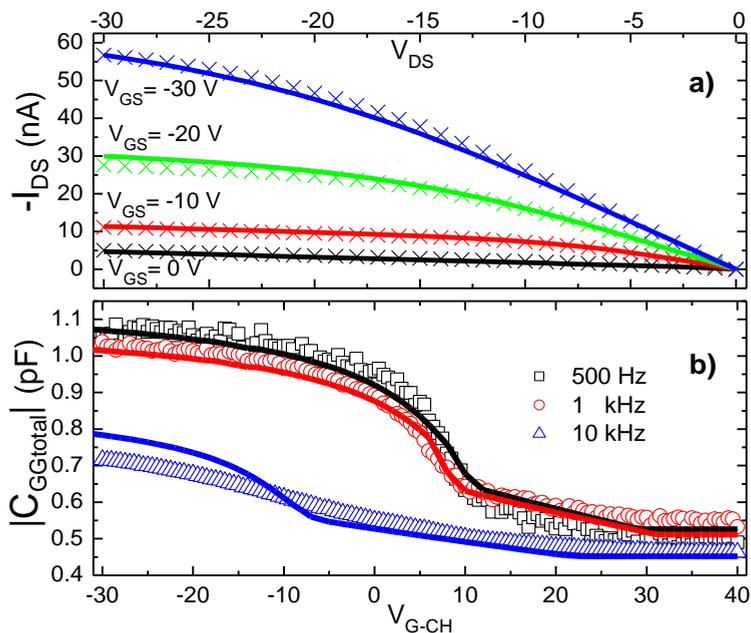


Fig. 4.18. Experimental (symbols) and modeled (solid lines) electrical characteristics of the PMMA/P3HT OTFT with insulator thickness  $d_{PMMA}=330$  nm and  $d_{P3HT}=80$  nm: a) Output characteristics, and b) Capacitance-Voltage model compared with experimental data.

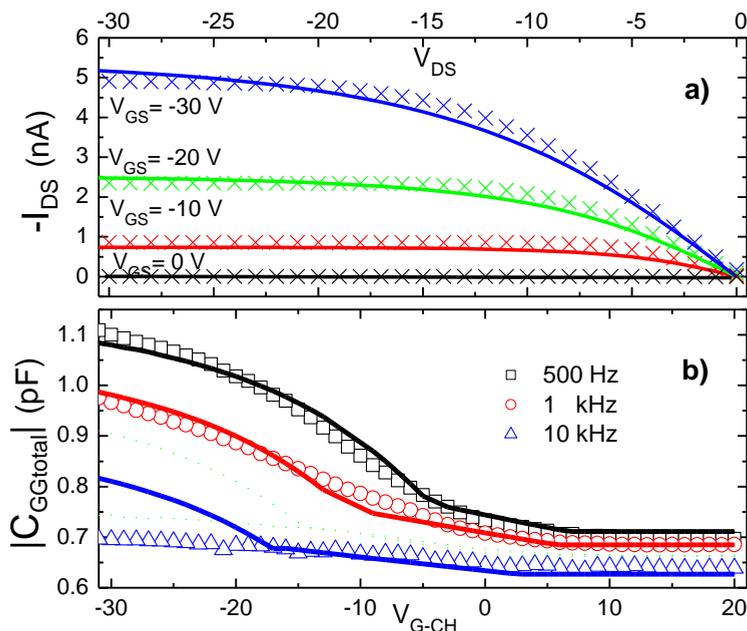


Fig. 4.19. Experimental (symbols) and modeled (solid lines) electrical characteristics of the PMMA/PCDTBT OTFT with insulator thickness  $d_{PMMA}=390$  nm and  $d_{PCDTBT}=50$  nm: a) Output characteristics, and b) Capacitance-Voltage model compared with experimental data.

### 4.3 Summary

We have presented a C-V compact model for OTFT valid in accumulation and depletion regimes for different frequencies where overlap capacitance is considered. . It assumes quasi-static operation and it is valid at medium frequencies. The model is physically-based and consistent with the channel current model previously developed for OTFTs valid for above and below threshold voltage conditions. The capacitance is well reproduced by the model. In P3HT OTFTs, experimental capacitances between 500 KHz and 10 KHz in accumulation behave similarly and are well described by the model, showing that a good agreement is obtained and that the model has been notably improved.

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## CHAPTER 5.

# Implementation of UBCM in Verilog-A for circuit simulation

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Once the models are proposed, developed and validated, their implementation in circuit simulators is the last step to make current use of them, whether for academic or commercial circuit design of both, digital and analog applications. In this chapter we present the implementation of the unified current-voltage and the UMEM-based charge and capacitance models for OTFTs. For this purpose, we used the circuit simulator SMASH to implement our unified models for OTFTs in Verilog-A.

## 5.1 Circuit Simulation

In previous chapters we stood out the importance of a device simulator such as ATLAS. Manufacturing challenges of new device structures force research groups to analyze the studied structure by means of device simulators, e.g. Silvaco ATLAS [Atlas] or Technology Computer-Aided Design tools (TCAD). These device simulators use a mesh on 2D surfaces and 3D volumes, solving each defined grid point iteratively with the help of a partial differential equation solver. Depending on the mesh refinement and the resulting number of points of simulation of a device, the solving time can take from few minutes, to several hours, and even weeks. These device simulators offer a wide variety of parameters to change, related to the materials and the parameters of the device structure. Furthermore, device simulations can predict and offer insight into the device physics of novel devices.

Without device simulations, the development costs for new devices would increase considerably. However, besides all the advantages which are given to the device designers, these kind of numerical device simulations are not applicable in circuit simulators.

In contrast to device simulations and device designers, the physics of the devices conforming a circuit arrange is of minor interest for circuit designers. From a circuit designer's point of view, the function, verification and testing of simple and complex analogue and digital circuits is more important. A condition for obtaining a correct behavior of the circuit is that the real device elements are modeled sufficiently similar to the implementation of the simulation software. In result, this saves time and costs for the development of

electronic circuits, as well as their misbehaviors. Circuit simulators are used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

Simulations based on mathematical models play a major role in computer aided design of integrated circuits (ICs). Decreasing structure sizes, increasing packing densities and driving frequencies require the use of refined mathematical models and to take into account secondary, parasitic effects. This leads to very high dimensional problems which nowadays require simulation times too large for the short time-to-market demands in industry. Modern Model Order Reduction (MOR) techniques present a way out of this dilemma in providing surrogate models which keep the main characteristics of the device while requiring a significantly lower simulation time than the full model.

It is important to remark that a simulation is only as accurate as its model. *Physical-based models*, as indicated by the name, try to use physics-based equations to describe the behavior of the transistor with the advantage that they are able to predict the behavior of scale devices. Normally, these types of models do not introduce empirical fitting parameters. However, a disadvantage is that equations are often not continuous for all transistor operation regimes. These models are commonly applied to describe the behavior of long-channel devices. Numerical-fit models have no relation to the principle basics of the device. The equations of these models consist of a countless number of fitting parameters where every change of physical device parameters requires a complete new set of fitting parameters. Finally empirical models are in between the two mentioned above. These models use physic-based equations

and introduce several fitting parameters to simplify and improve the models. However, these fitting parameters reduce the ability to predict the correct behavior of transistors by changing certain physical characteristics of the device under study.

All these models have to fulfill the same requirements. The behavior of the device has to be described as accurately as possible, i.e. as its application necessities. The models in circuit simulators should consist of analytical closed-formed equations, i.e. compact models, which were already described in previous chapters. Compact models save execution time, because electrical connections in a circuit simulator are solved with iterative methods. Furthermore, due to convergence reasons, a continuous first derivative of the model is required.

In our specific case, UMEM-based I-V and C-V models are compact, thus once our models are proposed, developed and validated, their implementation in circuit simulators is the last step to make current use of them, whether for academic or commercial circuit design of both, digital and analog applications.

Up to now, the most famous circuit simulators are SPICE (Simulation program with Integrated Circuit Emphasis) [Nagel-1973] which is a powerful and general-purpose, open source analog electronic circuit simulator. We used SMASH [Smash] to implement our unified I-V [Estrada-2008a] and C-V models for OTFTs [Castro-Carranza-2012a], [Castro-Carranza-s] in Verilog-A. SMASH, from Dolphin Integration, is a mixed-signal simulator that enables the development and verification of analog and mixed-signal Silicon Ips and Integrated Circuits, providing simplicity to beginners. The schematic diagram

showing the development steps of the implementation of UBCM in circuit simulators is illustrated in Figure 5.1. First the model was validated with experimental data in Mathcad from Mathworks, and then the Verilog-A code of the model was created, so it could be executed in SMASH and subsequently create the SPICE code to guaranty a fast execution of the simulation (See appendix C).

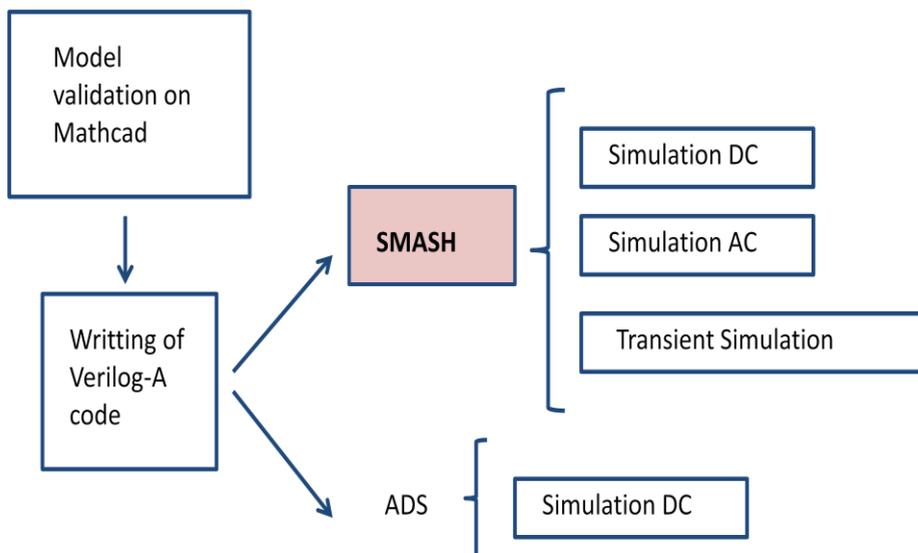


Fig.5.1. Schematic diagram of the UBCM development: from validation in Mathcad, to its implementation in SMASH and ADS circuit simulator.

The Verilog-A language is a high-level language that uses modules to describe the structure and behavior of analog systems and their components. With the analog statements of Verilog-A, you can describe a wide range of conservative systems and signal-flow systems, such as electrical, mechanical, fluid dynamic, and thermodynamic systems Verilog-AMS HDL lets designers of analog and mixed-signal systems and integrated circuits create and use modules which

encapsulate high-level behavioral descriptions as well as structural descriptions of systems and components. The behavior of each module can be described mathematically in terms of its ports and external parameters applied to the module. The structure of each component can be described in terms of interconnected sub-components. These descriptions can be used in many disciplines such as electrical, mechanical, fluid dynamics, and thermodynamics.

The complete model was integrated into SMASH using Verilog-A. To validate the implementation of our model, staggered OTFTs based on P3HT and PMMA were characterized. The extracted parameters of one device are shown in Table 5.1. As seen in Figure 5.2 and Figure 5.3, the DC simulation and the small signal one, respectively, are well modeled by means of SMASH and validated with experimental data.

Parameters		Units
$V_T$	1.02	V
$\gamma$	0.31	
$m$	3.11	
$\lambda$	$-6.38 \times 10^{-4}$	1/V
$\mu_0$ ( $V_{GT}=-1V$ )	$8.20 \times 10^{-4}$	$\text{cm}^2/\text{Vs}$
$\mu_{FET}$ ( $V_{GT}=-30V$ )	$1.22 \times 10^{-3}$	$\text{cm}^2/\text{Vs}$
$T_0$	318	K
$gd_0$	$9 \times 10^{23}$	$\text{cm}^{-3}$
$\alpha$	0.85	

Table 5.1. UMEM extracted parameters

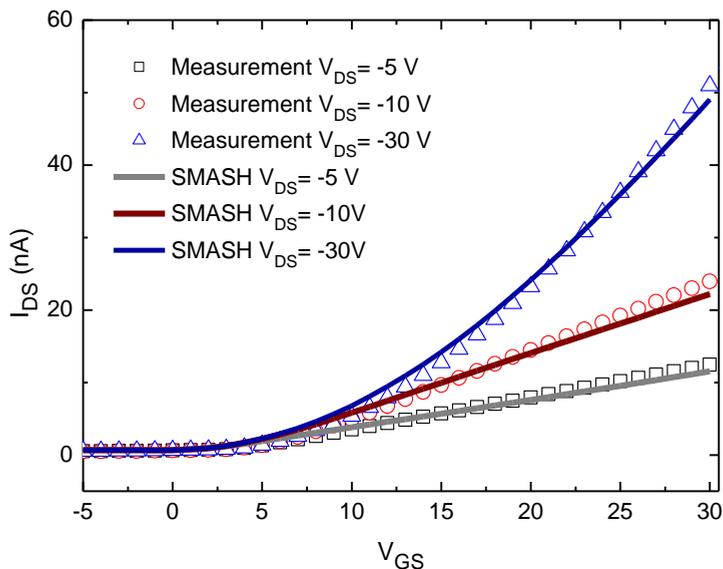


Fig.5.2. Comparison of OTFT transfer characteristics: experimental data (symbols) and DC SMASH simulation (lines).

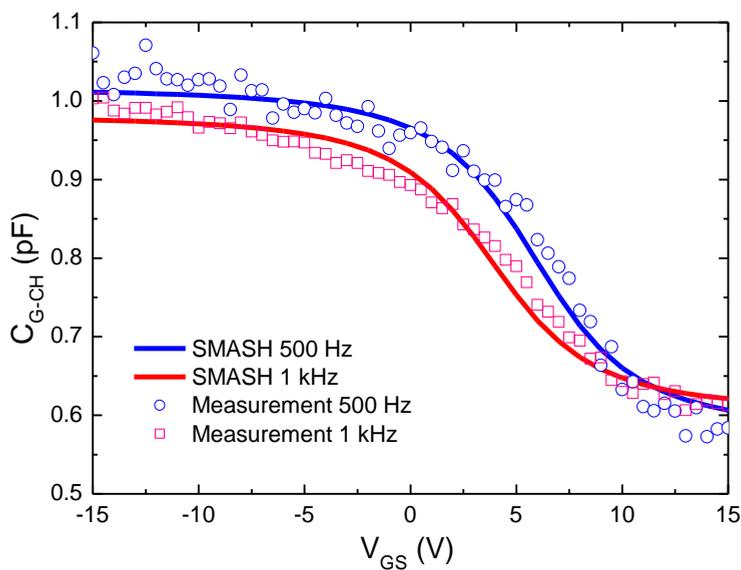


Fig. 5.3. Comparison of small signal response of the gate-to-channel capacitance: experimental data (symbols) and SMASH simulation (lines).

## 5.2 Organic Inverter

Inverters (logic doors) are elementary components for electrical circuits and are heavily used in those traditional techniques. The CMOS (complementary metal oxide semiconductor) inverter is a basic building block for digital circuit design. The inverter performs the logic operation of  $B$  to  $\bar{B}$ , i.e. when positive voltage is applied, the n-type transistor is pulled on, and the output is pulled to the source voltage. When the gate is off at 0V, the p-type transistor is on, and the output is grounded to 0V.

CMOS devices have two important characteristics: high noise immunity and low static power consumption. CMOS devices will draw significant power only when the transistors are switching between on and off states. As a result, CMOS devices do not produce as much heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip.

Historically, CMOS had not been possible in the area of printed and flexible electronics, because only p-type organic semiconductors had shown the requisite level of performance. With n-type organic semiconductors, CMOS circuits are now possible for the first time, leading to simpler circuit design and lower device power consumption.

Recently, organic inverters have been considered as one of the key elements in organic flexible circuits and have drawn more attention because they are flexible and economic to produce. Complementary circuits composed of both

p-type and n-type transistors are typically used in silicon technology, but at the present organic inverters with high gain are already fabricated.

To show the transient response of the model, the extracted parameters of the inverter fabricated with Pentacene and PTCDI-C13 as active semiconductors reported in [Papadopoulos-2012] were applied, with a load capacitance of 3 fF. The simulation is shown in Fig. 5.4. With these preliminary results, we show the performance of UMEM and UBCCM in SMASH. This model can be extended successfully to study the ring oscillator.

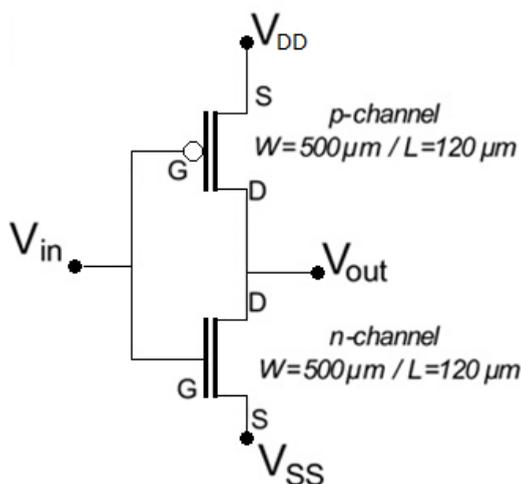


Fig. 5.4 Circuit diagram of an organic complementary inverter from [Papadopoulos-2012]

The values of the parameters of the organic model used.

Parameter	p-type	n-type
$L$	$120 \times 10^{-6}$	$120 \times 10^{-6}$
$W$	$500 \times 10^{-6}$	$500 \times 10^{-6}$
$A$	0.00095852	0
$R_o$	$10^{10}$	$10^{10}$
$m$	1.5422	3.4656
$T_{ox}$	$165 \times 10^{-9}$	$165 \times 10^{-9}$
$V_t$	0.70869	5.4272
$\Gamma$	0.133237	0.1
$\text{Alfa}$	0.88734	0.61682
$R$	837.6009	0
$V_{aa}$	0.014047	20100
$\text{Mu}0$	$42 \times 10^{-6}$	$6.9 \times 10^{-6}$

Table 5.1 UMEM extracted parameters of devices forming the inverter in [Papadopoulos-2012]

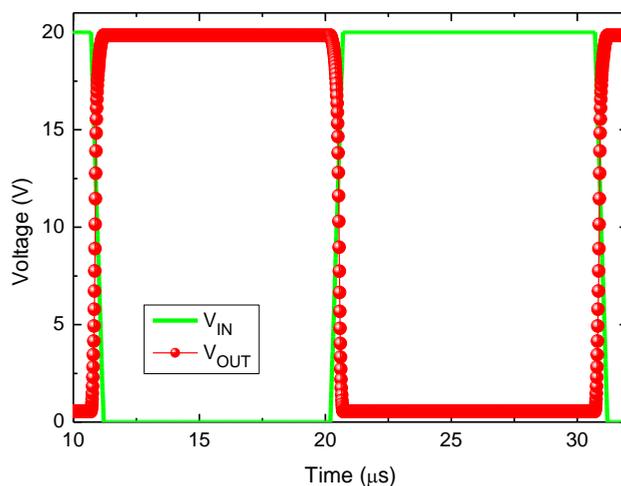


Fig.5.4. Simulated transient response of the inverter reported in [Papadopoulos-2012] using our charge control model in SMASH.

### 5.3 Summary

The unified I-V and C-V model for OFETs was integrated into the circuit simulator SMASH from Dolphin Integration using Verilog-A. To validate the implementation of our model, staggered OTFTs based on P3HT and PMMA were characterized, showing

a good agreement. To show the transient response of the model, the extracted parameters of the inverter fabricated with pentacene and PTCDI-C13 as active semiconductors reported in [5] were applied, with a load capacitance of 3 fF. The simulation is shown in Fig. 3. With these preliminary results, we show the performance of UMEM and UBCCM in SMASH. This model can be extended to study the ring oscillator.



## General Conclusions and Future Work

In this thesis we have developed an accurate quasi-static compact charge and capacitance model for organic field-effect transistors conformed by the Unified Model and Extraction Method (UMEM) parameters and which we have called UMEM-Based Capacitance Model for OFETs (UBCM). For this purpose we performed device fabrication, characterization, modeling and device and circuit simulation.

UBCM is physically based and consistent with the I-V model previously developed for OTFTs [Estrada-2008a], where the model parameters are extracted from the I-V experimental characteristics of the device using a simple and precise parameter extraction method (UMEM). Comparing with the few capacitance models for OFETS reported in literature up to date, UBCM shows advantages over them: It is compact, analytical and continuous in the transitions between different operation conditions of the OFETs, covering both, subthreshold and above threshold operation conditions and from linear to saturation regimes. Additionally to intrinsic capacitances, it considers the overlap capacitance which is commonly present in real devices. Also it has proved to be valid for different materials at low and medium frequencies ever since the quasi-static approximation has been used. An important aspect of UBCM is that we validated it against experimental data, i.e. I-V related C-V characteristics, fact that had not been done previously in literature due to the complex disordered nature of organic materials.

The main advantage of this work is the analytical and explicit character of the charge and capacitance model that makes an easy implementation in circuit simulators. And according to this, the complete model was integrated into the circuit simulator SMASH using Verilog-A. To validate the implementation of our model, staggered OTFTs based on P3HT and PMMA were characterized. The DC simulation and the small signal one, respectively, are well modeled by means of SMASH. We validated the simulated transcapacitances with measurements, obtaining a good agreement when comparing both data, which have not been reported before elsewhere.

We also showed the simulated transient response of our compact model by means of an organic inverter, which had not been reported before elsewhere. With these preliminary results, we show the performance of UMEM and UBCM in SMASH, indicating that our models are stable and can be extended to more complex circuits.

Even though UBCM offers to circuit designers an accurate model for describing the dynamic response of OFETs, it is important to take into account additional operation conditions of the devices in order to provide an extended model. For this reason the future work will take into consideration the improvement of UBCM by adding the non-quasi static operation for modeling the capacitance at higher frequencies, as well as the frequency dependent capacitance at different temperatures.

## APPENDIX A

### Calculation of total charge at the electrodes for a P-type OTFT.

#### • Total Charge in the Channel

Replacing (4.1) in (4.9)

$$\begin{aligned} Q_{CH} &= W \int_0^{V_{DS}} C_i(V_{GT} - V) \frac{W\mu_0}{I_D^*} \left[ \frac{C_i(V_{GT} - V)^{1+\gamma}}{Vaa^\gamma} \right] dV \\ &= \frac{W^2 C_i^2}{I_D^*} \left( \frac{\mu_0}{Vaa^\gamma} \right) \int_0^{V_{DS}} (V_{GT} - V)^{2+\gamma} dV \\ &= \frac{-W^2 C_i^2}{I_D^*} \left( \frac{\mu_0}{Vaa^\gamma} \right) \left[ \frac{(V_{GT} - V_{DS})^{3+\gamma}}{3+\gamma} - \frac{V_{GT}^{3+\gamma}}{3+\gamma} \right] \end{aligned}$$

(A1)

And then replacing  $I_D^*$  and substituting  $V_{DS}$  by  $V_{Dse}$  we obtain:

$$Q_{CH} = LWC_i \left( \frac{2+\gamma}{3+\gamma} \right) \left[ \frac{(V_{GT} - V_{Dse})^{3+\gamma}}{3+\gamma} - \frac{V_{GT}^{3+\gamma}}{3+\gamma} \right]$$

(A2)

#### • Total Charge at the Drain

From the Ward and Dutton's channel charge partitioning scheme [Ward-1978],

$$Q_D = \frac{W}{L} \int_0^L x [C_i(V_{GT} - V)] dx$$

(A3)

$x$  is obtained by means of (4.3) as follows

$$\int_0^x dx = \int_0^V \frac{W\mu_0}{I_D^*} \left[ \frac{C_i(V_{GT} - V)^{1+\gamma}}{Vaa^\gamma} \right] dV$$

(A4)

$$x = \frac{-WC_i}{I_D^*} \left( \frac{\mu_0}{Vaa^\gamma} \right) \left[ \frac{(V_{GT} - V)^{2+\gamma}}{2+\gamma} - \frac{(V_{GT})^{2+\gamma}}{2+\gamma} \right]$$

(A5)

replacing (4.3) and (A5) in (A3)

$$\begin{aligned}
 Q_D &= \frac{W}{L} \int_0^{V_{DS}} \left[ \frac{-WC_i}{I_D^*} \left( \frac{\mu_0}{V_{aa}^\gamma} \right) \left[ \frac{(V_{GT} - V)^{2+\gamma} - (V_{GT})^{2+\gamma}}{2 + \gamma} \right] \right] C_i (V_{GT} - V) \left[ \frac{W \cdot \mu_0 \cdot Q_{mob}}{I_D^*} dV \right] \\
 &= \frac{-(WC_i)^3}{L \cdot (I_D^*)^2} \left( \frac{\mu_0}{V_{aa}^\gamma} \right)^2 \left( \frac{1}{2 + \gamma} \right) \cdot \int_0^{V_{DS}} \left[ (V_{GT} - V)^{4+2\gamma} - (V_{GT})^{2+\gamma} (V_{GT} - V)^{2+\gamma} \right] dV \\
 &= \frac{-(WC_i)^3}{L \cdot (I_D^*)^2} \left( \frac{\mu_0}{V_{aa}^\gamma} \right)^2 \left( \frac{1}{2 + \gamma} \right) \cdot \left[ \frac{B}{(-1)(5 + 2\gamma)} - \frac{A_3 \cdot (V_{GT})^{2+\gamma}}{(-1)(3 + \gamma)} \right] \\
 &\quad (A6)
 \end{aligned}$$

where

$$\begin{aligned}
 B &= (V_{GT} - V_{DSe})^{5+2\gamma} - V_{GT}^{5+2\gamma} \\
 &\quad (A7)
 \end{aligned}$$

$$\begin{aligned}
 A_3 &= (V_{GT} - V_{DSe})^{3+\gamma} - V_{GT}^{3+\gamma} \\
 &\quad (A8)
 \end{aligned}$$

$$\begin{aligned}
 Q_D &= \frac{LWC_i(2 + \gamma)}{\left[ (V_{GT} - V_{DSe})^{2+\gamma} - V_{GT}^{2+\gamma} \right]^2} \cdot \left[ \frac{B}{(5 + 2\gamma)} - \frac{A_3 \cdot (V_{GT})^{2+\gamma}}{(3 + \gamma)} \right] \\
 &\quad (A9)
 \end{aligned}$$

### • Total Charge at the Source

$$\begin{aligned}
 Q_S &= Q_{CH} - Q_D \\
 &= LWC_i \left( \frac{2 + \gamma}{A_2} \right) \cdot \left[ \left( \frac{A_3}{3 + \gamma} \right) - \left( \frac{1}{A_2} \right) \left( \frac{B}{(5 + 2\gamma)} - \frac{A_3 \cdot (V_{GT})^{2+\gamma}}{(3 + \gamma)} \right) \right] \\
 &\quad (A10)
 \end{aligned}$$

where

$$\begin{aligned}
 A_2 &= (V_{GT} - V_{DSe})^{2+\gamma} - V_{GT}^{2+\gamma} \\
 &\quad (A11)
 \end{aligned}$$

## APPENDIX B

### UBCM: Verilog-A code

```
`include "disciplines.h"
`include "constants.h"

// For Berkeley Spice compatibility
//`define P_K (1.3806226e-23) //Boltzmann's constant eV/K
//`define P_Q (1.6021918e-19) //Charge - Coulomb
// `define M_PI (3.14159265358979323846)
`define P_E0 (8.854214871e-12) //Permittivity in vacuum F/m

//Definition of module, with its 3 terminals
module otft_1(d, g, s);

//The following three nodes are declared as input/output ("inout")
inout d, g, s;

//these nodes will be accessed under "electrical" discipline
electrical d, g, s;

//internal nodes
branch (d, s) canal;

//TFT model

/** Model Parameters Definitions

//Geometry
(*info="1.0 N-TYPE, -1.0 P-TYPE") parameter real TYPE=1 from[-1:1] exclude 0;
(*info="Channel length UNITS=>m") parameter real L = 30e-6 from[0.0:inf];
(*info="Channel Width UNITS=>m") parameter real W = 210e-6 from[0.0:inf];

// MODEL PARAMETERS
(*info="Saturation modulation parameter UNITS=>eV") parameter real
ALPHASAT=0.847;
(*info="Relative dielectric constant of substrate") parameter real
EPS=3.2;
(*info="Relative dielectric constant of gate insulator") parameter real
EPSI=3;
(*info="Power law mobility parameter") parameter real
GAMMA=0.117;
(*info="Output conductance parameter UNITS=>1/V") parameter real
LAMBDA=-6.388e-4;
(*info="Knee shape parameter ") parameter real
M=3.105;
(*info="Drain Resistance UNITS=>ohm") parameter real RD =
3.144e6;
(*info="Source Resistance UNITS=>ohm ") parameter real RS =
3.144e6;
(*info="Parameter measurement temperature UNITS=>°C") parameter real
TNOM=27;
(*info="Thin oxide thickness UNITS=>m") parameter real
TOX=310e-9;
```

## UMEM-Based Capacitance Model for OFETs

---

```
(*info="Characteristic voltage for field effect mobility UNITS=>V"*)parameter
real VAA=3.073e26;
(*info="Zero bias threshold voltage UNITS=>V"*)           parameter real
VT0=1.002;
(*info="Slope of the linear transfer curve in subthreshold"*)parameter real
SL=6;
(*info="A value above VT to sew the curves below/above threshold"*)parameter
real DVL=2;
(*info="A value to avoid imaginary numbers when sewing the 2
regions"*)parameter real QL=0.45;
(*info="IOFF for the linear transfer curve UNITS=>A"*)   parameter real
IOL=4.924e-10;
(*info="Slope of the saturation transfer curve in subthreshold"*)parameter real
SS=6;
(*info="Value similar to DVL but obtained in saturation"*)parameter real DVS=2;
(*info="A value to avoid imaginary numbers when sewing the 2
regions"*)parameter real QS=0.5;
(*info="IOFF for the saturation transfer curve"*)       parameter real
IOS=5.1e-9;

// ##### UBCM parameters #####

(*info="Semiconductor thickness (m)"*) parameter real TS=80e-9;
(*info="Offset capacitance from measurements (F)"*)   parameter real OFFSET=3e-
14;
//(*info="")parameter real Q1C=4.0;
(*info="Overlap length between gate and drain (m)"*) parameter real LOVD=15e-
6;
(*info="Overlap length between gate and source (m)"*) parameter real LOVS=15e-
6;
(*info="Band gap of the semiconductor (eV)"*)         parameter real EG=1.83;
// taken from P3HT
(*info="Carrier concentration in valence band m^-3"*) parameter real NCS=2e27;
// = 2e21 cm^-3
(*info="Carrier concentration in valence band m^-3 "*)parameter real NVS=2e27;
// = 2e21 cm^-3
(*info="Semiconductor non intentional doping m^-3"*) parameter real NB=2e23;
// = 2e17cm^-3
parameter real M1=4;
parameter real SHIFTQ=7;
parameter real DELTAQ=50;
parameter real VMINQ=0.1;
parameter real VDMIN=0.7;

// For calculation of basic variables
real VTH, NIEG, EPSIF;//, EPSI;

//Extrapolated addition of tanh fitting parameters
real ACF, VTDF, FACTF;

// Capacitance equations
parameter real f=10000 from[10:1000000];
real cif; // Frequency dependent insulator capacitance
real covfd; // Frequency dependent gate-drain overlap capacitance
real covfs; // Frequency dependent source-drain overlap capacitance
real covf; // Total frequency dependent overlap capacitance
real fisf; // Frequency and Vg dependent surface potential
// real wof, wtdl, wtdf, cdf, cgf;
real qa,qb,qd;
real vgc,k, k1, k2, k2D, k3, k4, expo, vdseD,vdsq, vdseq, vgtQ,vdQ;
```

```

real dencaa, caa, ca, cb, cc, cd, ce, cf, cg, ch, ck, cd1,cd2;//WMAXF,
(* desc="qtotItot" *)real qtotitot;
(* desc="qtot" *)real qtot;
(* desc="qgate" *)real qgate;
(* desc="qdrain" *)real qdrain;
(* desc="qsource" *)real qsource;
(* desc="cgga" *)real cgga;
(* desc="cgd" *)real cgd;
(* desc="cgs" *)real cgs;
(* desc="CggNum" *)real CggNum;

#####

//Internal Variables
real EPSI0, EPS0;

//Variables 109ddditional
real MOS25cg, MUFET;

//Temperature Variables
real TNOMO;
real VT;

//Variables for bias voltages
real Vds, Vgs, Vgd;
real vgs, vgd, vds, mode;
real vgt, vgte, vdse, vsate;

//Variables for subthreshold
real vgtDL, vgtedL, vsatedL, vdsedL;
real nsadL, gchidL, gchdL, idcdL;
real idscL;

real vgtDS, vgtedS, vsatedS, vdsedS;
real nsadS, gchidS, gchdS, idcdS;
real idscS;

//Variables for final results
real idc, ids, ifinal;

// Variables for description
real nsa, gchi, gch, VMIN, DELTA;

//real debug1;
analog begin
    // Initial Values

    EPSIF = 2.6 + ((3.54 - 2.6) / (1+pow(f/207,0.39)));
    //EPSI=EPSIF*0.67;

    VMIN = 0.1;
    DELTA = 1;
    TNOMO =TNOM+`P_CELSIUS0;
    EPSI0 = `P_E0 * EPSI;
    EPS0 = `P_E0 * EPS;
    VT= -VT0;
    MOS25cg = EPSI0 / TOX;
    MUFET = (1/pow(VAA,GAMMA))*1e-4; // UNITS=> (m^2)/Vs

Vds = TYPE * V(d, s);
Vgs = TYPE * V(g, s);
    
```

## UMEM-Based Capacitance Model for OFETs

```

Vgd      = TYPE * V(g, d);

//Initialize node voltages
if (Vds >= 0.0)
  begin
    mode = 1;
    vds = Vds;
    vgs = Vgs;
    vgd = Vgd;
  end
else
  begin //reverse mode
    mode = -1;
    vds = -Vds;
    vgs = Vgd;
    vgd = Vgs;
  end

//Description
vgt = (VMIN/2) * (1+((vgs-VT)/VMIN) + sqrt((DELTA*DELTA)+pow((((vgs-
VT)/VMIN)-1),2)));

// Above Threshold Characteristic
vsate = ALPHASAT * vgt;
vdse = vds / (pow((1 + (pow((vds/vsate),M))), (1 / M)));
nsa = (pow(vgt ,GAMMA)) * vgt * (MOS25cg / `P_Q);
gchi = `P_Q * nsa * MUFET * (W / L);
gch = gchi / (1 + (gchi * (RS + RD)));
idc = gch * vdse * (1 + (LAMBDA * (abs(vds)-ALPHASAT*(vgt))));

//Current
//Subthreshold Lineal Characteristic
if (vgs < VT0)
  begin
    vgtDL = VT + DVL;
    vgtedL = vgtDL - VT;
    vsatedL = ALPHASAT * vgtedL;
    vdsedL = vds / (pow((1 + (pow((vds/vsatedL),M))), (1 / M)));
    nsadL = (pow(vgtedL ,GAMMA)) * vgtedL * (MOS25cg / `P_Q);
    gchidL = `P_Q * nsadL * MUFET * (W / L);
    gchdL = gchidL / (1 + (gchidL * (RS + RD)));
    idcdL = gchdL * vdsedL * (1 + (LAMBDA * vds));
    idscL = idcdL * exp((vgt / SL) * 2.3);
    ids = abs(idscL) * (1 - tanh((vgs - vgtDL) * QL)) / 2 + abs(idc) * (1 +
tanh((vgs - vgtDL) * QL)) / 2 + IOL;
  end

//Subthreshold Saturation Characteristics
else
  begin
    vgtDS = VT + DVS;
    vgtedS = vgtDS - VT;
    vsatedS = ALPHASAT * vgtedS;
    vdsedS = vds / (pow((1 + (pow((vds/vsatedS),M))), (1 / M)));
    nsadS = (pow(vgtedS ,GAMMA)) * vgtedS * (MOS25cg / `P_Q);
    gchidS = `P_Q * nsadS * MUFET * (W / L);
    gchdS = gchidS / (1 + (gchidS * (RS + RD)));
    idcdS = gchdS * vdsedS * (1 + (LAMBDA * vds));
    idscS = idcdS * exp((vgt / SS) * 2.3);
    ids = (abs(idscS) * (1 - tanh((vgs - vgtDS) * QS)) / 2 + abs(idc) * (1
+ tanh((vgs - vgtDS) * QS)) / 2 + IOL);
  end

```

```

end

ifinal = ids;

if (mode > 0)
    I(canal) <+ TYPE * ifinal;
else
    I(canal) <+ -TYPE * ifinal;

covfd = cif * W * (LOVD);
covfs = cif * W * (LOVS);
covf = covfd + covfs;

qa=( pow((vgt - vdse), (3+GAMMA))- pow((vgt), (3+GAMMA)));
qb=((3 + GAMMA)*(-1)* ids ) / (1 + (LAMBDA * vds));
qtotitot = (W*cif) * (W*cif) * MUFET * qa/qb ;

vgtQ = (VMINQ/2) * (1+((vgs-VT-SHIFTQ)/VMINQ) +
sqrt((DELTAQ*DELTAQ)+pow(((vgs-VT-SHIFTQ)/VMINQ)-1),2));
vdQ= vds / (pow((1 + (pow((vds/(ALPHASAT * vgtQ)),M1)), (1 / M1)));
qtot = -(W*L*cif*(GAMMA+2) / (GAMMA+3)) * (pow((vgtQ-vdQ), (GAMMA+3)) -
pow(vgtQ, (GAMMA+3))) / (pow((vgtQ-vdQ), (GAMMA+2))-pow(vgtQ, (GAMMA+2)));

qgate= -qtot;

qd=(W*L*cif*(GAMMA+2)) / ((pow((vgtQ-vdQ), (GAMMA+2))-
pow(vgtQ, (GAMMA+2)))) * (pow((vgtQ-vdQ), (GAMMA+2))-pow(vgtQ, (GAMMA+2)));
qdrain= qd*((pow((vgtQ-vdQ), (2*GAMMA+5))-pow(vgtQ, (2*GAMMA+5))) / (2*GAMMA+5)) -
((pow((vgtQ-vdQ), (GAMMA+3))-
pow(vgtQ, (GAMMA+3)))) * pow(vgtQ, (GAMMA+2)) / (GAMMA+3));

qsource= -qgate - qdrain;

CggNum=ddx(qgate,V(g)) + (covf);

vgc=vgt;
vdseD=vds / (pow((1 + (pow((vds/(ALPHASAT * (vgc+DVL))),M)), (1 / M)));
k=W*cif*MUFET/L;
k1=pow((W*cif),2.0)*MUFET*1e-4;
k2=pow((vds/vsate),M);
k2D=pow((vds/(ALPHASAT * (vgc+DVL))),M);
k3=(1-tanh((vgc-DVL)*QL))/2.0;
k4=(1+tanh((vgc-DVL)*QL))/2.0;
expo=exp((2.3*vgc)/SL);

dencaa=(k*pow((vgc+DVL), (GAMMA+1)) * (1+(LAMBDA*vds)) *vdseD*expo*k3/(1+RD*k*pow((
vgc+DVL), (GAMMA+1))))+(k*pow(vgc, (GAMMA+1)) * (1+(LAMBDA*vds)) *vdseD*k4/(1+RD*k*pow(
w(vgc, (GAMMA+1))))+IOL;
caa=(-1e4*k1/(GAMMA+3)) * ((pow((vgc-vdse), (GAMMA+2)) * (GAMMA+3)) * (1-
vdseD*k2/(vgc*(1+k2)))) - (pow(vgc, (GAMMA+2)) * (GAMMA+3));
ca=k*pow((vgc+DVL), GAMMA) * (GAMMA+1) * (1+(LAMBDA*vds)) *vdseD*expo*k3/(1+RD*k*pow(
(vgc+DVL), (GAMMA+1)));
cb=k*pow((vgc+DVL), GAMMA) * (1+(LAMBDA*vds)) *vdseD*expo*k3*k2D/((1+RD*k*pow((vgc+
DVL), (GAMMA+1))) * (1+k2D));
cc=k*k*pow((vgc+DVL), ((2*GAMMA)+1)) * (1+(LAMBDA*vds)) *vdseD*expo*k3*RD*(GAMMA+1)
/((1+RD*k*pow((vgc+DVL), (GAMMA+1))) * (1+RD*k*pow((vgc+DVL), (GAMMA+1))));
cd=2.3*k*pow((vgc+DVL), (GAMMA+1)) * (1+(LAMBDA*vds)) *vdseD*expo*k3/(SL*(1+RD*k*po
w((vgc+DVL), (GAMMA+1))));
ce=k*pow((vgc+DVL), (GAMMA+1)) * (1+(LAMBDA*vds)) *vdseD*expo*QL*(1-tanh(pow(((vgc-
DVL)*QL),2)))/(2*(1+RD*k*pow((vgc+DVL), (GAMMA+1))));

```

## UMEM-Based Capacitance Model for OFETs

---

```

cf=k*pow(vgc,GAMMA)*(GAMMA+1)*(1+(LAMBDA*vds))*vdse*k4/(1+RD*k*pow(vgc,(GAMMA+1)));
cg=k*pow(vgc,GAMMA)*(1+(LAMBDA*vds))*vdse*k2*k4/((1+k2)*(1+RD*k*pow(vgc,(GAMMA+1))));
ch=k*k*pow(vgc,((2*GAMMA)+1))*(1+(LAMBDA*vds))*vdse*k4*RD*(GAMMA+1)/((1+RD*k*pow(vgc,(GAMMA+1)))*(1+RD*k*pow(vgc,(GAMMA+1))));
ck=k*pow(vgc,(GAMMA+1))*(1+(LAMBDA*vds))*vdse*QL*(1-tanh(pow(((vgc-DVL)*QL),2)))/(2*(1+RD*k*pow(vgc,(GAMMA+1))));
cd1=k*pow((vgc+DVL),(GAMMA+1))*(1+(LAMBDA*vds))*vdseD*expo*k3/(1+RD*k*pow((vgc+DVL),(GAMMA+1)));
cd2=k*pow(vgc,(GAMMA+1))*(1+(LAMBDA*vds))*vdse*k4/(1+RD*k*pow(vgc,(GAMMA+1)));

cgga=((caa/dencaa)+(1e4*k1/(GAMMA+3))*pow((vgc-vdse),(GAMMA+3))-pow(vgc,(GAMMA+3)))*(ca+cb-cc+cd-ce+cf+cg-ch+ck)/pow((cd1+cd2+IOL),2.0)+covf+OFFSET;

cgd=(2.0*(cgga-covf)*(1-pow((vgc/((2*vgc)-vdse)),2))/3.0)+covfd;

cgs=(2.0*(cgga-covf)*(1-pow(((vgc-vdse)/(2*vgc-vdse)),2))/3.0)+covfs;

    I(s) <+ TYPE * ddt(qsource);
    I(g) <+ TYPE * ddt(qgate);
    I(d) <+ TYPE * ddt(qdrain);

    end
endmodule

```

## APPENDIX C

### SMASH simulation plots

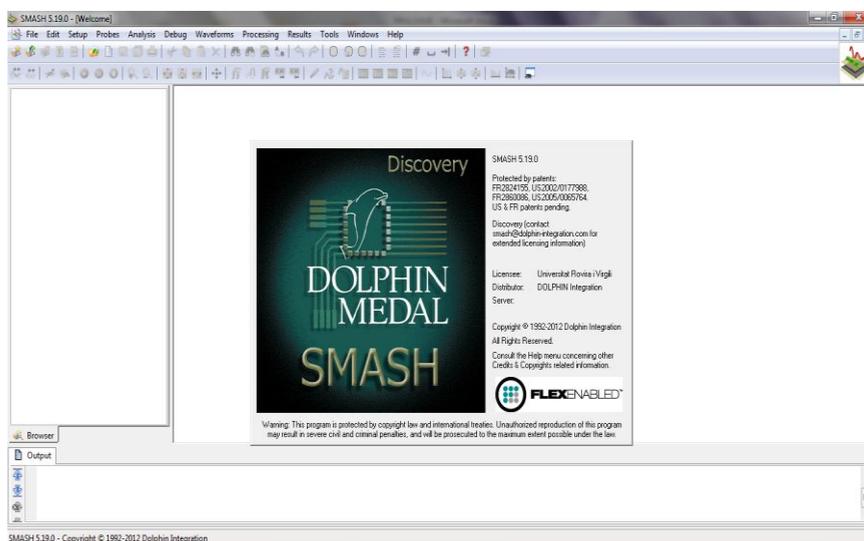


Fig. C1. SMASH from Dolphin Integration.

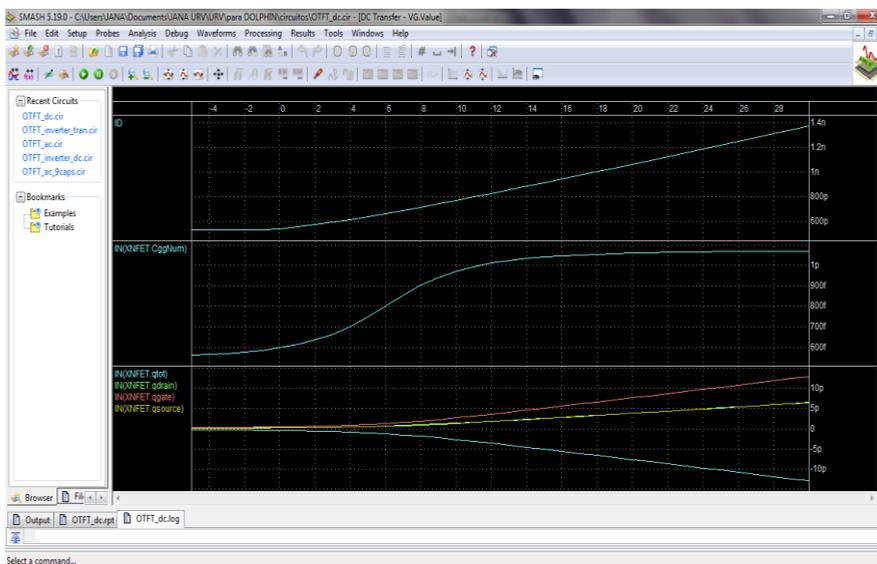


Fig. C2. DC simulation of the OTFT described by the UMEM extracted parameters of table 5.1.

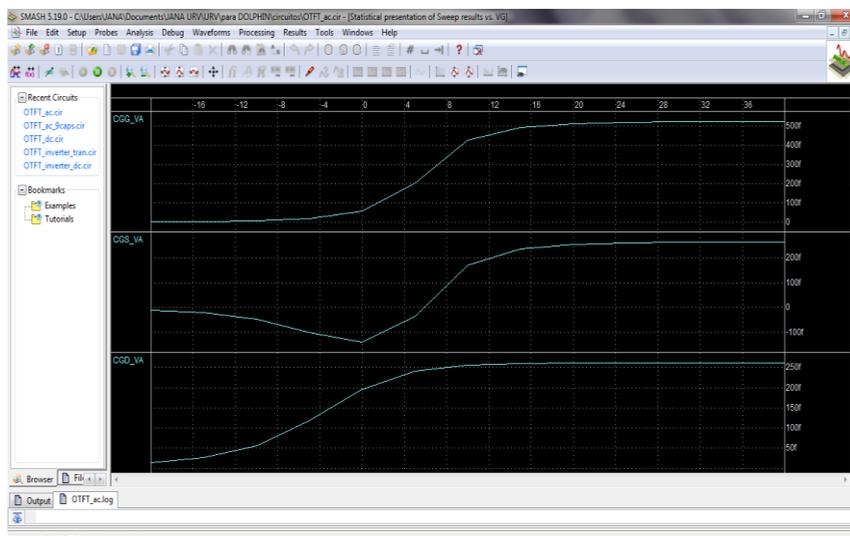


Fig. C3. AC simulation of the OTFT described by the UMEM extracted parameters of table 5.1.

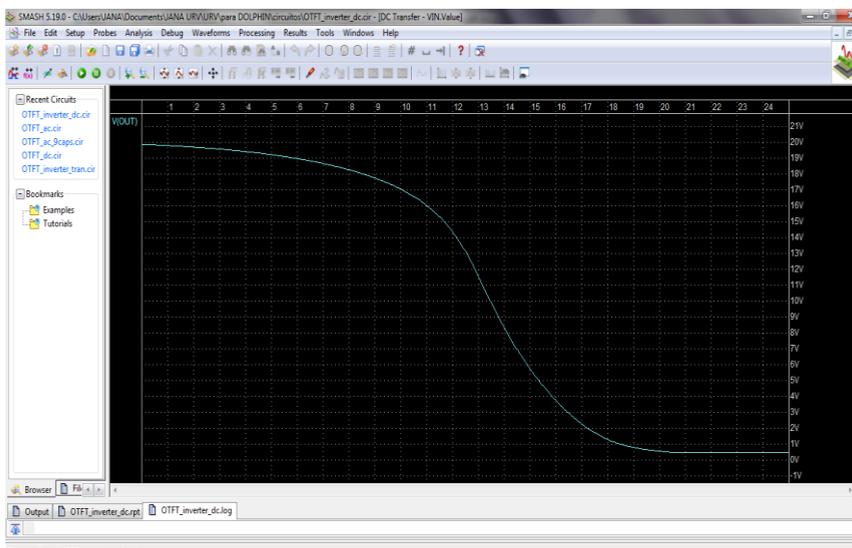


Fig. C4. DC simulation of the inverter reported in [Papadopolous-2012]

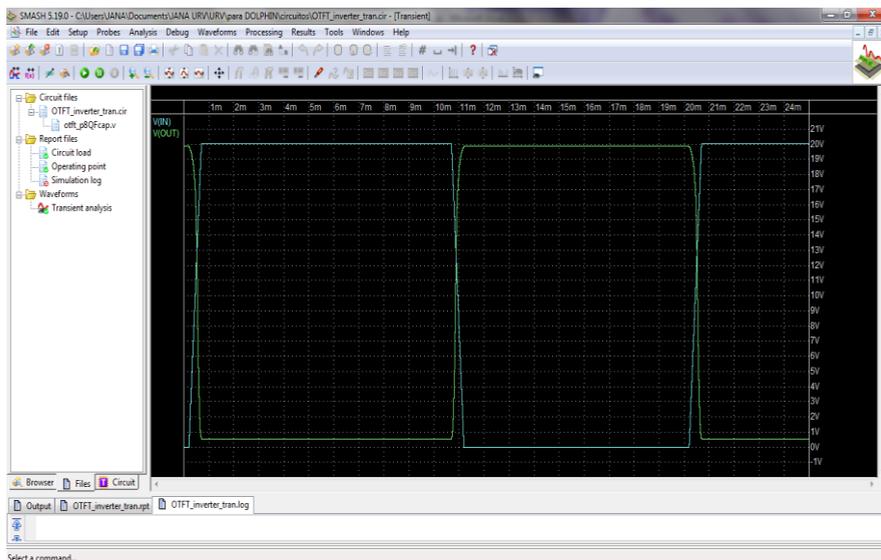


Fig. C5. Transient simulation of the inverter reported in [Papadopoulos-2012]

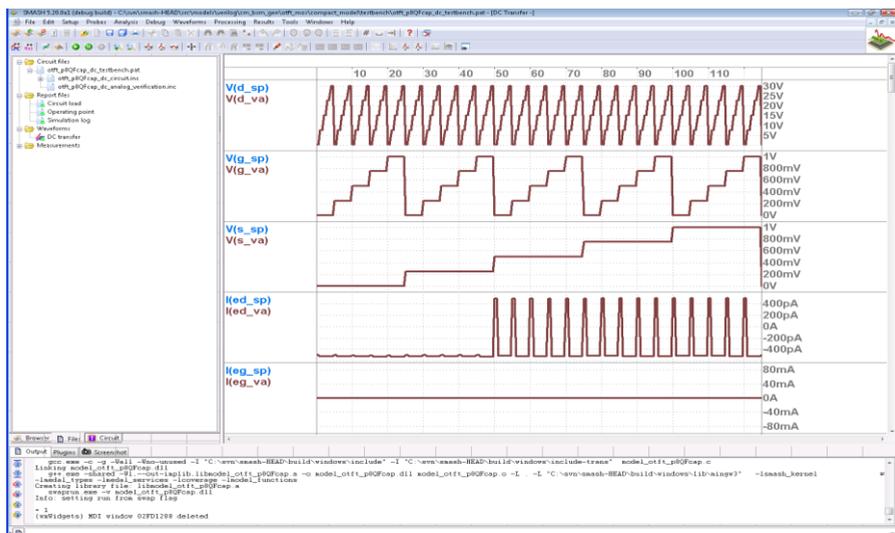


Fig. C6. Comparison between Verilog-A and the Spice codes of the model, showing an identical behaviour.



## APPENDIX D

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