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Design of AC-DC PFC High-Order Converters with Regulated Output Current for Low Power Applications

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Abstract - AC-DC PFC circuits used in low power applications have to overcome important power quality problems related to crest and power factors as well as total harmonic distortion, and in many cases they have to exhibit a high degree of output regulation. The design of efficient drivers for low power applications using high-order converters is considered in this paper. Power factor correction is achieved by imposing a loss-free resistor behaviour to SEPIC and Ćuk converters by means of an internal loop based on sliding-mode control, which requires a hysteretic comparator for its implementation. However, with a constant hysteresis width, the system exhibits harmful harmonic distortion in the input line current waveform, so that a variable hysteresis window is used instead to avoid this distortion near the zero crossings of the input current. The subsequent analysis of the ideal sliding dynamics around the equilibrium point allows the design of an outer control loop to regulate the output current. Mathematical analysis, numerical simulations and experimental results are presented to demonstrate the functionality of the proposed technique obtaining a significant improvement in terms of decreasing the total harmonic distortion. A dimmable LEDs driver supplying an HBLEDs string with a wide range of output current regulation illustrates the design.

Index Terms **—HBLEDs, power factor corrector (PFC), loss-free resistor (LFR), sliding-mode control (SMC), Hysteresis modulation (HM).**

I. INTRODUCTION

Power factor corrector (PFC) design is focused in obtaining high power factor (PF), and low total harmonic distortion (THD). This aim is extended to industrial, commercial and residential scenarios where a large number of electronic devices with this PF issues are used. In this sense, high power quality is increasingly required for power supply systems in order to fulfill the international standards such as IEEE Std. 519, IEC 61000-3-2 or EN 61000-3-2 [1, 2]. For this purpose, and specially in low power applications, switched-mode AC–DC PFC circuits are designed in order to ensure a high PF [3-5]. In this case, some harmonics pollution in current/voltage are still observed due to the switching effects and/or the zero crossing distortion.

The aim of an active PFC circuit is to obtain a resistive behaviour to the circuit input port. This stage can be easily implemented with a diode bridge and with DC-DC converter stages (Fig. 1a). On the other hand, in most low power applications the DC voltage required is lower than the sinusoidal peak, and exceeds tens of volts. Hence, this DC-DC stage should have the ability to step-up and step-down the input voltage in order to raise or reduce the rectified voltage to obtain the appropriate DC voltage value (Fig. 1b).

Input power quality and output voltage regulation can be improved employing indistinctly two or more stages , which eventually result in a fast dynamic response [6]. On the contrary, single stage PFC circuits are less popular due to its difficult output regulation. Although, one converter for PFC and another stage for controlling the output variables it is generally preferred, it is expected that the use of one conversion stage combining both features will improve the efficiency at the expense of making the design more complex.

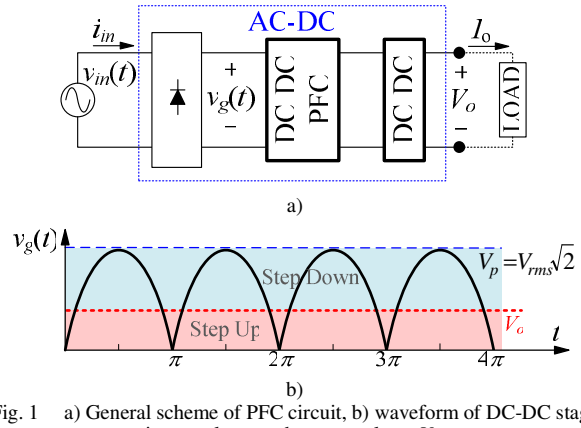

Fig. 1 a) General scheme of PFC circuit, b) waveform of DC-DC stage input voltage and output voltage V_o.

High order topologies refer to voltage step-up and step-down combinations, in which the most suitable for PFC are the Ćuk and SEPIC converters [7]. These converters, under pulse width modulation operation (PWM) and working in discontinuous conduction mode (DCM), exhibit resistive input impedance [4, 8, 9] and therefore can be used as PFC circuits. However, the existence of both pulsating input currents and DCM mode impose the insertion of an EMI input filter to fulfil harmonic standards. This is also the case of the topologies described in [10, 11] employing different control methods. In [12], the SEPIC converter without EMI filter has been proposed to work as a high efficiency adaptation single power stage with active PFC. The PFC has been carried out by means of a Sliding-Mode Control (SMC) forcing the converter to behave as a

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Loss Free Resistor (LFR) [13], so that the converter input port behaves as a pure resistor and all the absorbed power by this resistor is transferred to the output port.

The synthesis of an LFR [14-16] can by carried out by imposing in steady-state the following relationship between the input variables

$$I_1 = g \cdot V_g \tag{1}$$

where I_1, and V_g are the steady-state averaged values of the instantaneous input variables shown in Fig. 2, g represents the conductance characteristic of the PFC input port and is given by $g(t) = k_s \cdot G_{REF}(t)$; where k_s is the voltage sensor gain, and G_{REF} (t) is a reference given by an external control loop regulating the converter output current.

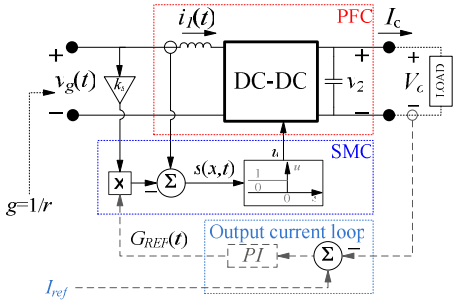

Fig. 2 Block diagram of a SMC-based LFR using a step-up/step-down DC-DC converter.

It has to be pointed out that imposing a sliding-mode regime to the input current requires $i_1(t)$ to be a continuous (non pulsating) function of time, this implying that $i_1(t)$ must an inductor current what justifies the direct application of the method to both SEPIC and Ćuk converters. Also, note that SMC theory implies an infinite switching frequency that should be implemented by means of an ideal comparator as the one depicted in Fig. 2, whose output is given by u=1 when $s(x,t)$ <0 , and u=0 when s(x,t) >0.

However, the practical implementation of a SMC in switching converters requires a hysteresis comparator to limit the switching frequency to an acceptable range. The use of a constant hysteresis width results in a variable switching frequency that depends on the input voltage value. This dependence provokes a loss of the sliding–mode regime and yields a very low value of the switching frequency near the zero crossings instants of the input voltage as illustrated in Fig. 3 in the case of SMC-based Ćuk converter [17].

To mitigate this problem two different techniques were proposed. The first one consists in a PI controller applied to the switching function $s(x,t)$ in order to increase the value of this signal either when the system fails to perform the switching action due to the loss of the sliding-mode regime or when it fails to reach the limits imposed by the hysteresis window [18]. Although an increase in the switching frequency near the zero crossing is obtained, another kind of distortion in the input current $i_1(t)$ waveform arises and therefore the PF and input current THD (I-THD) are negatively affected as it can be deduced observing Fig. 4.

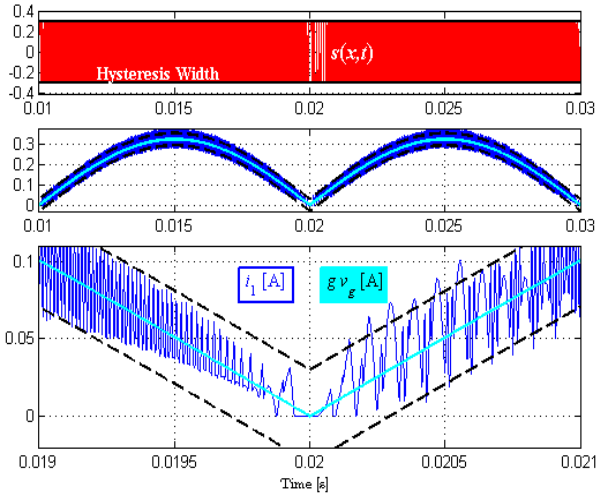

Fig. 4 Input current distortion in SMC when adding a PI controller to the switching surface.

The second technique consists in a time-varying hysteresis width which is made enough small when the input voltage approaches zero. Hence, narrowing the hysteresis width cancels the negative effect of the small value of the input voltage and results in an increase of the switching frequency rather than in

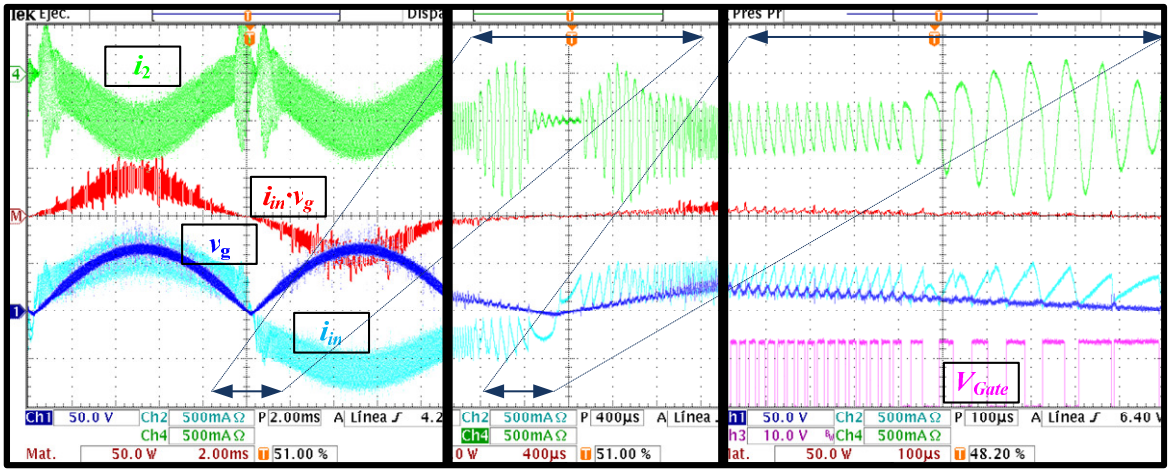

Fig. 3 Loss of sliding-mode regime of an LFR based on the Ćuk converter near the zero crossing of the inductor current.

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its decrease. Satisfactory preliminary results recently published in [19] are provided by this technique, which is now exhaustingly covered in this paper in the design of a voltage step-up/step-down converter with non-pulsating input current.

Hence, the aim of the study here reported is to present an holistic design of a single stage voltage step-up/ step-down low power AC-DC PFC converter having both a low input current THD and a wide range output current regulation. The dynamic analysis of Ćuk and SEPIC converters includes the synthesis of the SM-based LFR, the study of the ideal sliding dynamics (ISD) around the equilibrium point and the design of an external control loop to regulate the output current. This paper provides a theoretical basis for the dynamic analysis together with clear guidelines for the control implementation. As an example, the proposed approach will be applied to the design of an HBLED power supply in which the nominal operating output voltage is lower than the input line voltage. Since the luminous flux and the HBLEDs current are proportional, the output current error with respect to a reference is processed by means of a PI controller in order to regulate the HBLEDs luminous flux.

The remains of the paper is organized as follows. The synthesis of an ideal LFR for AC-DC PFC using Ćuk and SEPIC converters and the corresponding mathematical modelling are described in Section II, this revealing the unconditionally stable nature of the Ćuk converter. In section III, the variable hysteresis width design is presented and its experimental results in a Ćuk converter are compared with those of the constant width approach. The decrease of the total harmonic distortion is also illustrated in section III. The design of the outer control loop for output voltage regulation is covered in section IV. Finally, the conclusions are summarized in Section V.

II. Synthesis of Ideal LFR for AC-DC PFC Applications

In this section the mathematical description of the system acting as a LFR with an input voltage $v_g(t) = Vm\,|\sin(\omega t)|$ is reviewed [14] and adapted to the case of SEPIC and Ćuk converters supplying a serial string of n HBLEDs. The goal of this section is to provide a first assessment on the stability of both converters.

A. Mathematical Description

The LFR behaviour can be obtained using a DC-DC switching converter with a sliding-mode regulation loop whose switching surface is given by

$$s(x,t) = i_1 - g \cdot v_g(t) \tag{2}$$

where i_1 is the input current, $v_g(t)$ is the input voltage and $g = 1/r$ is the LFR emulated conductance, r being its emulated resistance. Under sliding-mode regime and in steady-state operation, $s(x,t) = 0$, and therefore $I_1 = g \cdot V_g$, so that (1) is satisfied. To simplify the design process, $g(t)$ is assumed first constant ,i.e., $g(t) = k_s \cdot G_{REF}$,i.e. , only the inner current loop will be considered as shown in Fig. 5a and Fig. 5b.

It can be observed in both figures that the output voltage can be expressed as $V_{LED} = V_F + I_o\, rd$, where $rd = n \cdot rd'$ and $V_F = n \cdot V_F'$, n being the number of HBLEDs in series, rd' the dynamic resistance and V_F' the forward voltage drop of a single LED respectively.

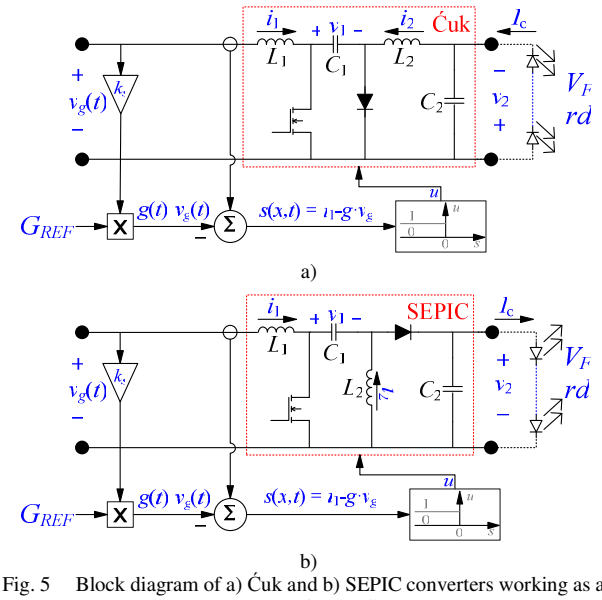

Fig. 5 Block diagram of a) Ćuk and b) SEPIC converters working as an LFR under SMC.

Assuming continuous conduction mode (CCM) operation implies that the system switches between two different topologies corresponding to the two states of the MOSFET, namely, ON ($u(t)$=1) or OFF ($u(t)$=0). The system state equations are therefore expressed as follows

$$\begin{aligned} \dot{x}(t) &= A_1 \cdot x(t) + B_1 \quad \text{for} \quad u = 1 \\ \dot{x}(t) &= A_2 \cdot x(t) + B_2 \quad \text{for} \quad u = 0 \end{aligned} \tag{3}$$

where $x(t) = [i_1(t) \quad i_2(t) \quad v_1(t) \quad v_2(t)]^T$ is the vector of the state variables for both DC-DC converters and the over dot stands for derivation with respect to time. The matrices A_i, and vectors B_i (with i = 1, 2) are state matrices and input vectors in each topology of the converter. These matrices are depicted in TABLE I for each converter.

Equations (3) can be combined into a single bilinear expression given by

$$\dot{x}(t) = [A_1 \cdot x(t) + B_1]u + [A_2 \cdot x(t) + B_2)](1-u) \tag{4}$$

which can be expressed as follows:

$$\dot{x}(t) = A_2 \cdot x(t) + B_2 + [(A_1 - A_2) \cdot x(t) + (B_1 - B_2)]u \tag{5}$$

Defining $A = A_2$, $\delta = B_2$, $B = A_1 - A_2$, $\gamma = B_1 - B_2$, the following bilinear model is obtained

$$\dot{x}(t) = f(x,t) + g(x,t) \cdot u \ \text{ where } \ f(x,t) = A \cdot x(t) + \delta \text{, and}$$
$$g(x,t) = B \cdot x(t) + \gamma \tag{6}$$

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TABLE I STATE MATRICES AND INPUT VECTORS IN EACH TOPOLOGY, TC, EQUIVALENT CONTROL, AND EXISTENCE CONDITIONS OF SMC FOR BOTH CONVERTERS.

	A_1	$A_2 = A$	$B_1=B_2=\delta$, ($\gamma = 0$)	$B = A_1 - A_2$	TC	$u_{eq}(t)$ $\alpha = 1-\frac{g\cdot L_1\cdot\omega}{\tan(\omega t)}$	Existence conditions of SMC
Ćuk	$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{r_d C_2} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{r_d C_2} \end{bmatrix}$	$\begin{bmatrix} \frac{v_g(t)}{L_1} \\ 0 \\ 0 \\ \frac{V_F}{r_d C_2} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{-1}{C_1} & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	$\frac{v_1}{L_1} \neq 0$	$1-\frac{v_g}{v_1}\alpha$	$0 < v_g < v_1/\alpha$
SEPIC	$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{r_d C_2} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & \frac{-1}{r_d C_2} \end{bmatrix}$		$\begin{bmatrix} 0 & 0 & \frac{1}{L_1} & \frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} \\ \frac{-1}{C_1} & \frac{-1}{C_1} & 0 & 0 \\ \frac{-1}{C_2} & \frac{-1}{C_2} & 0 & 0 \end{bmatrix}$	$\frac{v_1+v_2}{L_1} \neq 0$	$1-\frac{v_g}{v_1+v_2}\alpha$	$0 < v_g < (v_1+v_2)/\alpha$

B. Equivalent Control

Taking into account (6), the time derivative of the switching surface can be expressed as follows:

$$\begin{aligned}\dot{s}(x,t) &= \frac{\partial s}{\partial x}\dot{x} - \left(g\cdot\dot{v}_g(t) + \dot{g}\cdot v_g(t)\right) \\ &= \left\langle \nabla s, \left[f(x,t) + g(x,t)u\right]\right\rangle - \left(g\cdot\dot{v}_g(t) + \dot{g}\cdot v_g(t)\right)\end{aligned} \tag{7}$$

where the notation $\langle a,b\rangle$ denotes the scalar product of a and b, and ∇ stands for the gradient operator. According to the equivalent control method [20-22], a necessary condition for the existence of a sliding motion on the switching surface is given by the transversality condition (TC).

$$\left\langle \nabla s, g(x,t)\right\rangle \neq 0 \tag{8}$$

Considering the gradient of the switching surface under study (2), and given that $\gamma = 0$ for both converters, the TC (8) is clearly fulfilled (TABLE I), and a sliding-mode can exist. Imposing the condition $\dot{s}(x,t)\big|_{u=u_{eq}} = 0$ leads to the following expression of the equivalent control:

$$u_{eq}(t) = \frac{\left(g\cdot\dot{v}_g(t) + \dot{g}\cdot v_g(t)\right) - \left\langle \nabla s,\, f(x,t)\right\rangle}{\left\langle \nabla s,\, g(x,t)\right\rangle} \tag{9}$$

In the equivalent control method, the discontinuous variable u is substituted by a continuous variable $u_{eq}(t)$ in (5), this representing the control law that constrains the state trajectories on the switching surface defined by $s(x,t) = 0$. This equivalent control is limited by the maximum and minimum values of the discontinuous variable u, *i.e,*

$$0 < u_{eq}(t) < 1 \tag{10}$$

Also, substituting the expression of u_{eq} in (10) leads to the sliding-mode existence conditions, which are listed in TABLE I, where it can be also observed that an auxiliary parameter α has been defined as

$$\alpha = 1 - \frac{gL_1\omega}{\tan(\omega t)} \tag{11}$$

After some algebra, it can be seen that this parameter is practically equal to one except for a small discontinuity in a zero crossing point. Although a loss of sliding regime is temporarily caused by this discontinuity, the system recovers the sliding regime after this instant, so that this effect is neglected in the rest of the analysis. Moreover, the simplification mentioned before, *i.e.*, $g(t)$ is constant implies $\dot{g} = 0$.

C. Quasi-Static Approach

To simplify the analysis, a quasi-static approach is used [10, 23-25]. The line frequency (50 or 60 Hz) is significantly below the switching frequency, hence, the input voltage of the DC–DC converters can be considered constant during few consecutive switching periods. Thus, this input voltage and consequently the corresponding equilibrium point will be parameterized as a function of $\theta = \omega\cdot t$. Therefore, the full range values of $v_g(\theta)$ will be obtained for $\theta = (0, \pi/2)$.

D. Ideal Sliding Dynamics

The ISD model is represented by a set of nonlinear differential equations by substituting in (6) the discontinuous control u by the continuous variable u_{eq} given in (9) and taking into account the constraint (2) imposed by the switching condition (i.e. $i_1 = g\cdot v_g$). The model for both converters is shown in TABLE II where it can be observed an order reduction in the system dynamics due to the SMC action.

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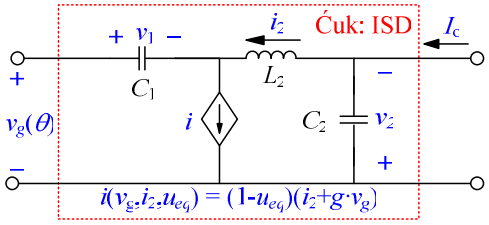
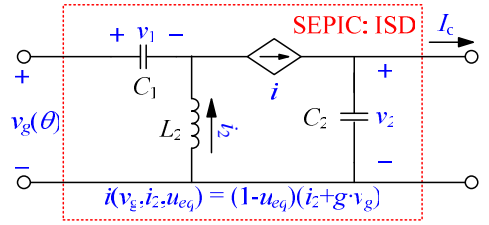
TABLE II IDEAL SLIDING DYNAMICS.

	Ćuk	SEPIC
$\dot{x}=\begin{bmatrix} f_1(x) \\ f_2(x) \\ f_3(x) \end{bmatrix} := \begin{bmatrix} \dot{i}_1 \\ \dot{v}_1 \\ \dot{v}_2 \end{bmatrix}$	$\begin{bmatrix} \dfrac{-v_2+v_1-v_g(\theta)}{L_2} \\ \dfrac{\left(v_g(\theta)-v_1\right)\cdot i_2+g\cdot v_g^2(\theta)}{v_1\cdot C_1} \\ \dfrac{i_2\cdot r_d-v_2+V_F}{r_d\cdot C_2} \end{bmatrix}$	$\begin{bmatrix} \dfrac{v_1-v_g(\theta)}{L_2} \\ \dfrac{\left(v_g(\theta)-v_1-v_2\right)\cdot i_2+g\cdot v_g^2(\theta)}{(v_1+v_2)\cdot C_1} \\ \dfrac{-v_2^2+(V_F-v_1)\cdot v_2+v_g(\theta)\left(g\cdot v_g(\theta)+i_2\right)r_d+v_1\cdot V_F}{(v_1+v_2)\cdot r_d\cdot C_2} \end{bmatrix}$

Based on the ISD equations the equivalent circuits of both Ćuk and SEPIC switching converters are shown in Fig. 6.



a)



b)

Fig. 6 ISD model of a) Ćuk converter and b) SEPIC converter.

The coordinates of the equilibrium point of the ISD is given by:

$$Xss(\theta)=\left.\begin{bmatrix} g\cdot v_g(\theta) \\ g\cdot v_g^2(\theta)/V_2(\theta) \\ v_g(\theta)+V_2(\theta) \\ V_2(\theta) \end{bmatrix}\right|_{Cuk} = \left.\begin{bmatrix} g\cdot v_g(\theta) \\ g\cdot v_g^2(\theta)/V_2(\theta) \\ v_g(\theta) \\ V_2(\theta) \end{bmatrix}\right|_{SEPIC} \quad (12)$$

where $V_2(\theta)=\frac{1}{2}\left(V_F+\sqrt{V_F^2+4g\cdot v_g^2(\theta)r_d}\right)$

According to the expressions of u_{eq} listed in TABLE I, the corresponding equivalent control for both equilibrium points given by (12) can be expressed as follows

$$u_{eq}(\theta)=1-\frac{v_g(\theta)}{v_g(\theta)+V_2(\theta)}\alpha \quad (13)$$

Fig. 7 shows the plot of the expression in (13). Its corresponding numerical simulation using the switched model is also given in the same figure where a remarkable agreement between the ISD and the original switching system can be observed.

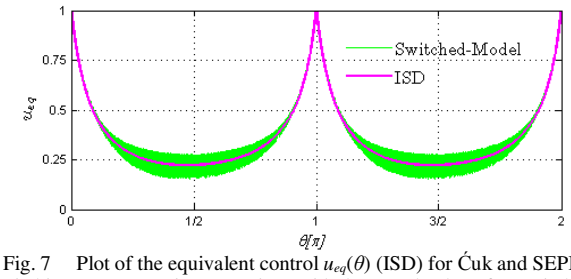


Fig. 7 Plot of the equivalent control $u_{eq}(\theta)$ (ISD) for Ćuk and SEPIC switching converters, in comparison with the actual value of u (switched-model).

E. Stability Analysis

Taking into account the ISD equations given in TABLE II , a linearization around the equilibrium point $Xss(\theta)$ is now carried out in order to study the converter stability. The corresponding Jacobian matrix $J(\theta)$ can be expressed as follows

$$J(\theta)=\left.\begin{bmatrix} \dfrac{\partial f_1(x)}{\partial i_2} & \dfrac{\partial f_1(x)}{\partial v_1} & \dfrac{\partial f_1(x)}{\partial v_2} \\ \dfrac{\partial f_2(x)}{\partial i_2} & \dfrac{\partial f_2(x)}{\partial v_1} & \dfrac{\partial f_2(x)}{\partial v_2} \\ \dfrac{\partial f_3(x)}{\partial i_2} & \dfrac{\partial f_3(x)}{\partial v_1} & \dfrac{\partial f_3(x)}{\partial v_2} \end{bmatrix}\right|_{Xss(\theta)} \quad (14)$$

Therefore, the corresponding 3rd order characteristic polynomial is given by

$$\det(J-sI)=a_3(\theta)s^3+a_2(\theta)s^2+a_1(\theta)s+a_0(\theta) \quad (15)$$

where I is the identity matrix, and parameters $a_i(\theta)$ of each converter are listed in TABLE III.

By applying the Routh-Hurwitz (RH) criteria to the characteristic polynomial of each converter, the corresponding stability conditions are obtained and shown in TABLE III, where it can be observed that the stability is ensured for the whole range of $v_g(\theta)$ in the Ćuk converter . However, the stability is guaranteed in a SEPIC converter provided that the condition presented in TABLE III is fulfilled [14]. For that reason, a Ćuk converter prototype will be used in the sequel to verify the theoretical predictions.

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TABLE III COEFFICIENTS OF THE CHARACTERISTIC EQUATION AND STABILITY CONDITIONS.

	Ćuk	SEPIC
	$a_3(\theta)=1$ $a_2(\theta)=\frac{C_1(v_g(\theta)+V_2(\theta))\cdot V_2(\theta)+g\cdot v_g^2(\theta)\cdot r_d\cdot C_2}{C_1\cdot C_2(v_g(\theta)+V_2(\theta))r_d\cdot V_2(\theta)}$ $a_1(\theta)=\frac{r_d\cdot[(C_1+C_2)\cdot V_2^2(\theta)+C_1\cdot V_2(\theta)\cdot v_g(\theta)]/L_2+g\cdot v_g^2(\theta)}{C_1\cdot C_2(V_2(\theta)+v_g(\theta))r_d\cdot V_2(\theta)}$ $a_0(\theta)=\frac{(r_d\cdot g\cdot v_g^2(\theta)+V_2^2(\theta))/L_2}{C_1\cdot C_2(v_g(\theta)+V_2(\theta))r_d\cdot V_2(\theta)}$	$a_3(\theta)=1$ $a_2(\theta)=\frac{C_1(v_g(\theta)+V_2(\theta))\cdot V_2(\theta)+g\cdot v_g^2(\theta)\cdot r_d(C_1+C_2)}{C_1\cdot C_2(v_g(\theta)+V_2(\theta))r_d\cdot V_2(\theta)}$ $a_1(\theta)=\frac{r_d\cdot C_2\cdot V_2^2(\theta)/L_2+g\cdot v_g^2(\theta)}{C_1\cdot C_2(V_2(\theta)+v_g(\theta))r_d\cdot V_2(\theta)}$ $a_0(\theta)=\frac{(r_d\cdot g\cdot v_g^2(\theta)+V_2^2(\theta))/L_2}{C_1\cdot C_2(v_g(\theta)+V_2(\theta))r_d\cdot V_2}$
R-H criteria: necessary condition	$a_i(\theta) > 0 \quad i=0...3$	
R-H criteria: sufficient conditions	$(a_2(\theta)\cdot a_1(\theta)-a_0(\theta)) > 0$	
Stability conditions	Unconditionally stable	$V_1(\theta)/V_2(\theta) < C_2/C_1$

III. VARIABLE HYSTERESIS WIDTH

A. *Operating Switching Frequency*

Assuming quasi-static steady- state operation in SMC allows describing the waveforms of the control signal $s(x,t)$ as triangular signals as depicted in Fig. 8 where the switching frequency f_o is given by [26]

$$f_o=\frac{1}{T}=\frac{1}{t_{on}+t_{off}}=\frac{1}{2\Delta}\frac{m_{on}\cdot m_{off}}{m_{on}+m_{off}} \tag{16}$$

where t_{on} and t_{off} are the interval duration for $u = 1$ and $u = 0$ respectively, $T = t_{on} + t_{off}$, m_{on} and m_{off} are the slopes of the control signal $s(x,t)$, and Δ is the constant hysteresis width.
The respective expressions of m_{on} and m_{off} slopes are given by

$$m_{on}=\nabla s(x)\cdot\dot{x}\big|_{u=1}$$
$$m_{off}=-\nabla s(x)\cdot\dot{x}\big|_{u=0} \tag{17}$$

and are listed in TABLE IV for both converters.

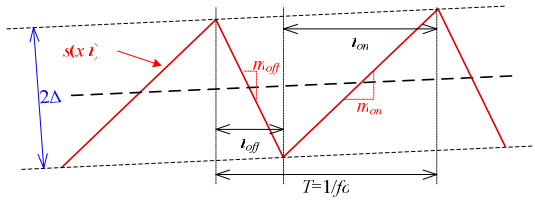

Fig. 8 Sliding surface in CCM steady-state operation determining the switching frequency (f_o).

TABLE IV SLOPES OF THE CONTROL SIGNAL AND SWITCHING FREQUENCY.

	Ćuk	SEPIC
$m_{on}(\theta)$	$v_g(\theta)/L_1$	
$m_{off}(\theta)$	$(V_1(\theta)-v_g(\theta))/L_1$	$(V_1(\theta)+V_2(\theta)-v_g(\theta))/L_1$
$f_o(\theta)$	$\frac{1}{2\Delta L_1}\frac{v_g(\theta)(V_1(\theta)-v_g(\theta))}{V_1(\theta)}$	$\frac{1}{2\Delta L_1}\frac{v_g(\theta)(V_1(\theta)+V_2(\theta)-v_g(\theta))}{V_1(\theta)+V_2(\theta)}$

Besides, from the expression of the equilibrium point (12) and the insertion of (17) in (16), the switching frequency becomes

$$f_o(\theta)=\frac{1}{2\Delta\cdot L_1}\frac{V_2(\theta)\cdot v_g(\theta)}{(V_2(\theta)+v_g(\theta))} \tag{18}$$

Considering that the voltage $V_2(\theta)$ will be constant due to the regulation by an external control loop, it can be seen in (18) that the switching frequency has a maximum value at $v_g(\theta=\pi/2) = Vm$ in the interval $0< \theta <\pi/2$, and tends to zero if V_g tends to zero. Hence, for the parameters shown in TABLE V, the maximum switching frequency is: $f_o \approx 150$ kHz. Finally, the plot of $f_o(\theta)$ in a sliding-mode control implemented with constant hysteresis width is depicted in Fig. 9 for the full range of $v_g(\theta)$.

TABLE V DESIGN SPECIFICATIONS AND PARAMETER VALUES

Component	Value
Input Voltage	v_g = 230 V RMS / 230 V DC
9 x HBLED, Cree, Inc. "Xlamp MC-E" (Cool White)	$V_F \approx$ 100 V, $rd \approx 30\ \Omega$ Po =45 W , $Inom$ =350 mA
L_1	9 mH
L_2	2 mH
C_1	40 nF
C_2	500 µF
$g = ks\ G$ ks: Voltage sensor gain.	Po=45 W, $g = Po/Vi_{rms}^2 \approx 1/1000$ ks = 1/5000, $G_{REF} \approx$ 5 S
Δ: Hysteresis width	Δi_1= 0.03 A
S_1	IPP60R250CP
D	IDD04SG60C
Hysteresis modulation	AD633 (Analogue multiplier)
	TLE 2047 (AOx4)
SMC	AD633 (Analogue multiplier)
	LM319 (Comparator)
	CD4027 (FF RS)
	TC4427 (Driver)

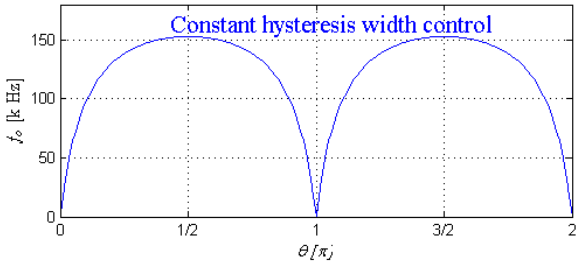

Fig. 9 Steady-state switching frequency (f_o) during one line cycle constant hysteresis width control (Δ).

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B. *Hysteresis Width Modulation*

As it is shown in (18), the switching frequency increases when the hysteresis window (Δ) tends to zero. Therefore, to avoid a decrease of the switching frequency near the zero crossing, Δ is modulated so that it tends to zero when the input voltage does. The modulation applied to Δ is depicted in Fig. 10 and corresponds to the shape

$$\Delta(\theta)=\begin{cases}\delta\cdot v_g(\theta) & \text{if} \quad \delta\cdot v_g(\theta)<\Delta i_1\\ \Delta i_1 & \text{if} \quad \delta\cdot v_g(\theta)>\Delta i_1\end{cases} \tag{19}$$

where $\delta = \Delta i_1 \cdot k/Vm$; k is an amplifier gain, Vm is the input peak of the sinusoidal voltage. This amplifier is used only to vary the slope of width $\Delta(\theta)$ near the zero crossings. The evolution of the hysteresis width from zero to a maximum value Δ_{Max} can be observed in Fig. 11.

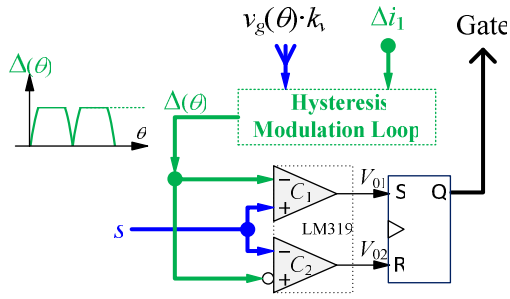

Fig. 10 Block diagram of hysteresis width modulation.

It can be seen from (18) that $\Delta(\theta)$ and the input voltage are proportional so they tend to zero in a similar way, this allowing an increase in the switching frequency near the zero-crossings and therefore a longer time in sliding-mode regime in this critical area.

The block diagram in Fig. 10 corresponds to (19). To ensure that $\Delta(\theta)$ is not greater than a pre-set value Δi_1 (Fig. 12a), a saturation block is used. Thus, when saturation takes place, the switching frequency is determined by (18) and when no saturation occurs (i.e.: in the zero crossings), the switching frequency near the zero crossing can be determined by substituting the modulated hysteresis width by $\Delta(\theta) = \delta v_g(\theta)\cdot$in (18) . Hence,

$$f_o(\theta)=\begin{cases}\dfrac{1}{2\delta\cdot L_1}\cdot\dfrac{V_2(\theta)}{\left(V_2(\theta)+v_g(\theta)\right)} & \text{if} \quad \alpha\cdot v_g(\theta)<\Delta i_1\\ \dfrac{1}{2\Delta i_1\cdot L_1}\cdot\dfrac{V_2(\theta)\cdot v_g(\theta)}{\left(V_2(\theta)+v_g(\theta)\right)} & \text{if} \quad \alpha\cdot v_g(\theta)>\Delta i_1\end{cases} \tag{20}$$

A plot of $f_o(\theta)$ for the conventional control based on constant hysteresis width and the control employing modulated hysteresis width is depicted in Fig. 12b. Compared to the constant hysteresis width situation, a significant increase in the switching frequency near the zero-crossings can be observed. Thus, for the set of parameters of TABLE V , the maximum switching frequency occurs at $\theta = \pi$ yielding $f_o = Vm/(2\cdot\Delta i_1\cdot L_1) \approx 600$ kHz, whereas the minimum switching frequency is the maximum switching frequency of the conventional control ($f_o \approx 150$ kHz). It should be noted that this frequency increase occurs at zero crossings of the input variables and therefore the switching losses are negligible and the overall switching frequency of the system will not be affected.

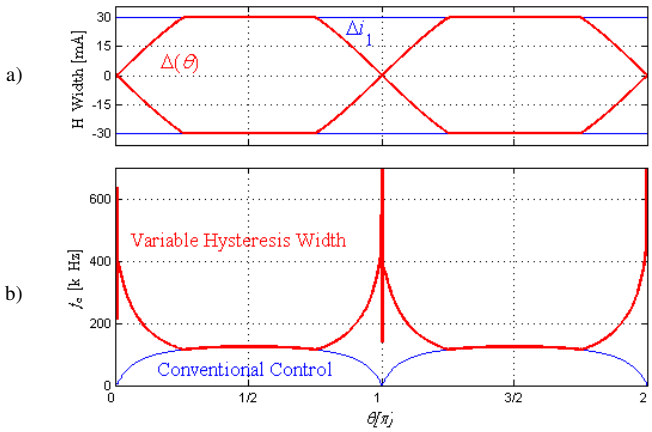

Fig. 12 a) Hysteresis width during one cycle with: conventional control (constant Δ), and with Δ tending to zero as v_g approaches zero. b) Steady-state switching frequency (f_o) during one line cycle with: conventional control (Δ), and with Δ tending to zero as v_g approaches zero.

C. *Simulation and Experimental Design*

With the aim of verifying the theoretical results concerning the stability of the system under SMC, time-domain numerical simulations have been carried out using PSIM simulation program [27]. The prototype has been designed to supply an

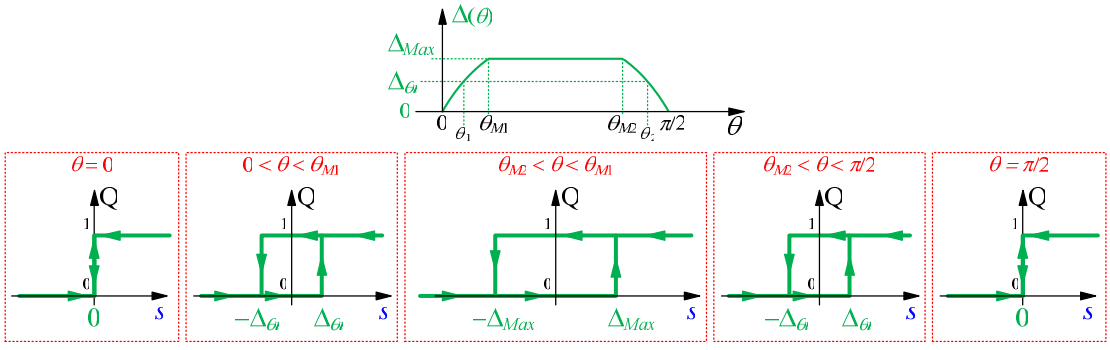

Fig. 11 Hysteresis width modulation as a function of signal $\Delta(\theta)$.

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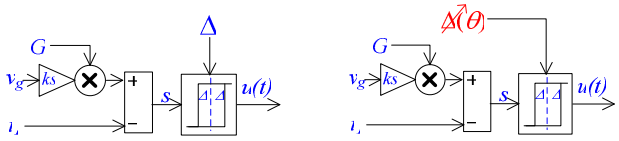
string of 9 HBLEDs "Xlamp MC-E" (Cool White) of Cree, Inc. The requirements regarding voltage and current for these diodes are typically from 200 to 700 mA and from 2.5 Vdc to 4 Vdc respectively (with a typical voltage forward of 3,2 V at 350 mA) [28]. The nominal values for both numerical simulations and prototyping are a DC input voltage V_g = 230 V and rated output power Po = 45 W, corresponding to a serial string of 9 HBLEDs, or equivalently V_{LED} = 100 V. The switching frequency employed is 150 kHz, which ensures that the sliding regime is not lost for the previous values of input and output voltages. Reactive components have been selected assuming a certain degree of ripple in the state variables (between 10% and 20% of the mean value for each variable). All the converter parameters are shown in TABLE V.

In order to generate the switching signal $u(t)$, a hysteretic comparator with an analogue multiplier and a variable hysteresis window is used as depicted in Fig. 13b in a clear-cut contrast with the conventional approach of constant hysteresis width illustrated in Fig. 13a.

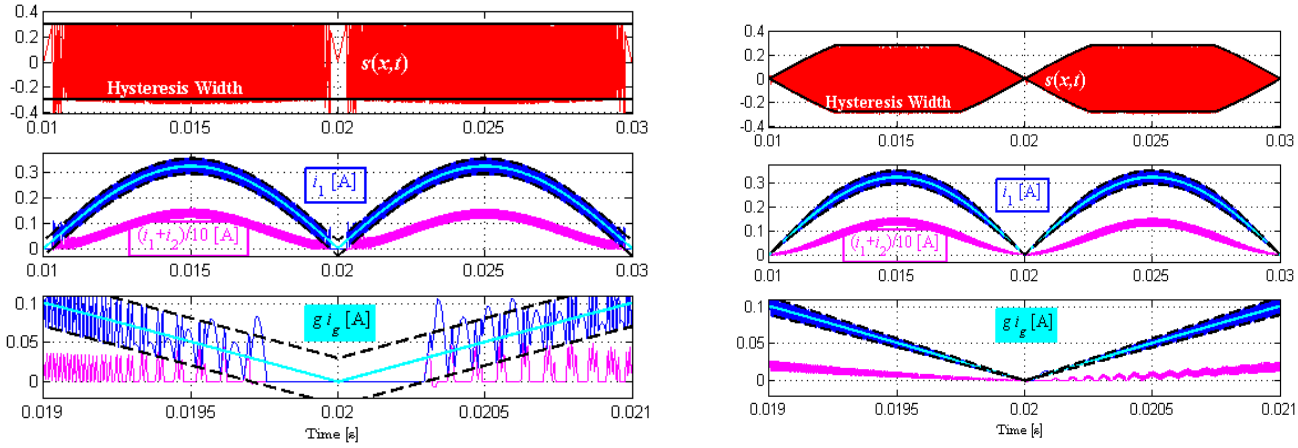
The system behaviour using a conventional control or variable hysteresis window is simulated in Fig. 14a and Fig. 14b respectively in the case of the Ćuk converter. It can be seen that the variable hysteresis width tends to zero as v_g approaches zero, thereby narrowing the width $\Delta(t)$ which implies an increase in the switching frequency. Thus, the duty cycle is controlled down to very low values and a "clean" zero crossing is obtained. Also, when the system is controlled by a variable hysteresis window, the input current ripple is decreased near the zero crossings due to the decrease of the hysteresis width in this region. As a result, the converter behaves as an almost ideal LFR.



a) b)

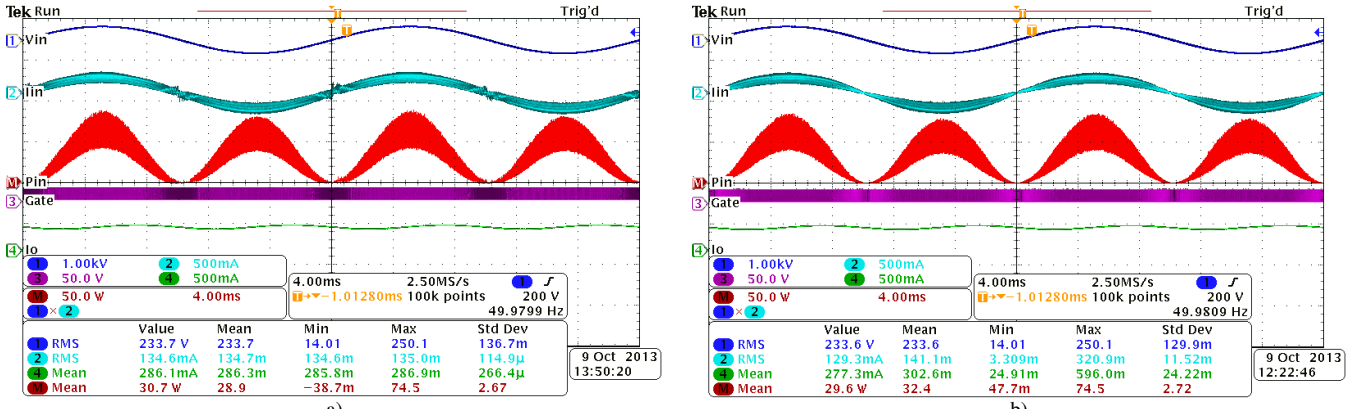
Fig. 13 Control block diagram of the hysteresis control with a) constant, b) variable hysteresis width.

Fig. 14 also shows the sum of both inductor currents (i_1+i_2), which is zero near the zero crossings because the system enters temporarily into DCM. Moreover, in spite of the variable hysteresis width, Fig. 14b shows an oscillation of this sum near the zero crossings region that induces a temporary loss of the sliding regime until the system reaches again a quasi-static steady-state operation. It can be also shown by simulation that although the improvement in the PF is negligible (an increase



a) b)

Fig. 14 Input waveforms of the Ćuk-based LFR with SMC: a) conventional, b) variable hysteresis width control. The bottom waveforms for both controls are a zoom of the intermediate plots.



a) b)

Fig. 15 Comparative waveforms of a Ćuk converter operating in SMC as LFR: a) convectional control, b) variable hysteresis width.

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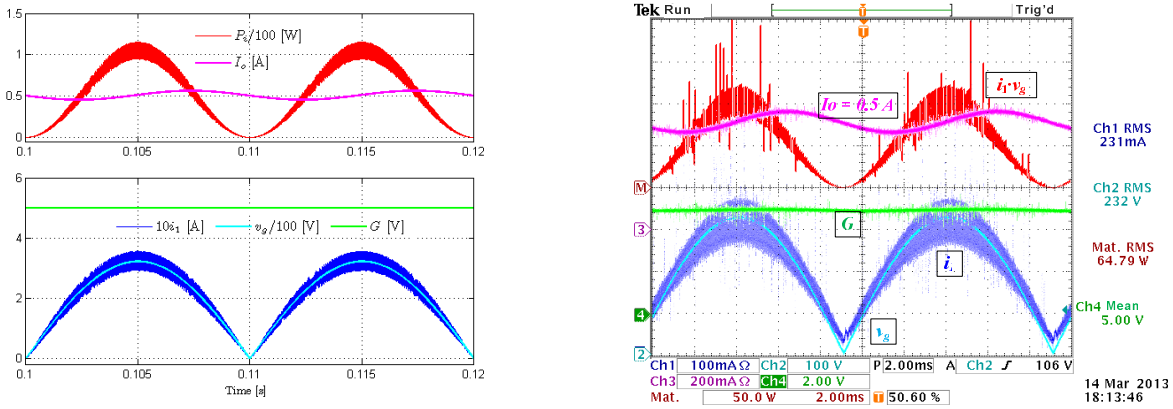

a) b)

Fig. 16 Ćuk-based LFR converter controlled by SMC with a variable hysteresis width (g=G/5000 S): a) simulation, and b) experimental results.

of 0.19% over 99%), an important decrease of 2.5% of the I-THD is achieved, i.e., from 8.8% in the conventional control to 6.3% in the variable hysteresis width.

Fig. 15 corroborates the expected improvement of the variable hysteresis width control by showing the experimental results in a Ćuk-based LFR with SMC using conventional approach (Fig. 15a) and the proposed control (Fig. 15b)

Fig. 16a and Fig. 16b show respectively the simulated and experimental waveforms of the input voltage (v_g), input current (i_1), input power (p_i) and output current (I_o) for the Ćuk converter acting as LFR by means of an internal sliding-mode control loop. In both figures a perfect proportionality between input current and input voltage can be observed, thus validating the active PFC behaviour. The input conductance g relating the input signals is represented by the constant signal G which is provided by the outer control loop. Variables in the simulation are presented with a scaling factor to be depicted in a single graph.

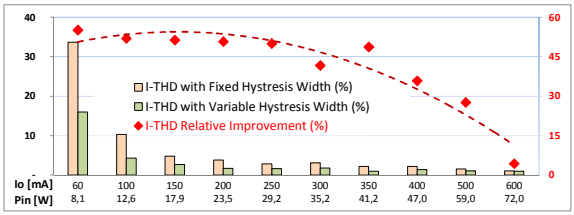

Fig. 17 I-THD for conventional control and variable hysteresis width respectively; and I-THD relative improvement vs. input power or Load current (Ćuk-based LFR converter).

D. THD Improvement

An extension of the analysis of the I-THD performed in the waveforms of Fig. 15a and Fig. 15b has been performed for different levels of load current (or input power). The corresponding results are depicted in Fig. 17, which illustrates the absolute values of I-THD for conventional control and for variable hysteresis width. Furthermore, the relative improvement for the last case is also shown. As an example, note that for the nominal load current of 350 mA the resulting I-THD is 40 % of that obtained with constant hysteresis width. This reduction in the harmonic contents is also obtained at lower power values as illustrated in Fig. 17.

Finally, power quality experimental results for each hysteresis type are plotted in Fig. 18 in the case of a load current of 60 mA (9 W input power). It can be observed (in red) that harmonics 3 and 9 for constant hysteresis width exceed the limit fixed by the harmonic standards IEC61000-3-2, class C (lighting equipment).

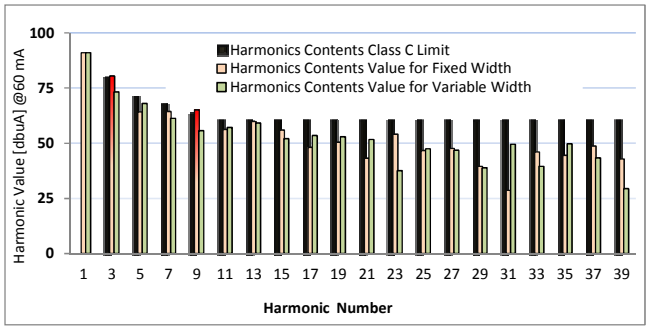

Fig. 18 Power quality experimental results: current harmonics contents for each hysteresis type, and standards IEC61000-3-2, class C (Ćuk-based LFR converter).

IV. Output Current Regulation Design

A. Small-Signal Model

In order to design the outer control loop of the AC-DC PFC, a small-signal model (SSM) for both converters will be derived. From the non- linear ISD of TABLE II, it can be deduced that vector $\dot{x}$ can be expressed as follows

$$\dot{x} = f(x, p) \tag{21}$$

where x is the state vector and $p = [g \quad v_g \quad rd \quad V_F]^T$ is the input and output disturbances vector.

In order to study the stability of the system, expression (20) will be linearized around the equilibrium point Xss(12). This linearization will be performed by extending the Jacobian matrix (14) corresponding to the state vector x to the disturbances vector p as follows

$$\dot{\hat{x}} = \left.\frac{\partial f(x,p)}{\partial x}\right|_{X_{SS}} \hat{x} + \left.\frac{\partial f(x,p)}{\partial p}\right|_{X_{SS}} \hat{p} \tag{22}$$

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After some algebra, the output voltage $\hat{v}_2$ can be expressed in the complex domain s as a linear combination of the perturbations in the input voltage , LFR conductance, HBLED dynamic resistance and HBLED drop voltage, which results in the four transfer functions given in (22) whose parameters g_i, vg_i, rd_i, d_i for both converters are detailed in Annex I.

$$H_1(s)=\left.\frac{\hat{v}_2(s)}{\hat{g}(s)}\right|_{\hat{v}_g=\hat{r}d=\hat{V}_F=0}=\frac{g_2\cdot s^2+g_1\cdot s+g_0}{d_3s^3+d_2s^2+d_1s+d_0}$$
$$H_2(s)=\left.\frac{\hat{v}_2(s)}{\hat{v}_g(s)}\right|_{\hat{g}=\hat{r}d=\hat{V}_F=0}=\frac{vg_2\cdot s^2+vg_1\cdot s+vg_0}{d_3s^3+d_2s^2+d_1s+d_0}$$
$$H_3(s)=\left.\frac{\hat{v}_2(s)}{\hat{r}d(s)}\right|_{\hat{g}=\hat{v}_g=\hat{V}_F=0}=\frac{rd_2\cdot s^2+rd_1\cdot s+rd_0}{d_3s^3+d_2s^2+d_1s+d_0} \quad (23)$$
$$H_4(s)=\left.\frac{\hat{v}_2(s)}{\hat{V}_F(s)}\right|_{\hat{g}=\hat{v}_g=\hat{r}d=0}=\frac{vf_2\cdot s^2+vf_1\cdot s+vf_0}{d_3s^3+d_2s^2+d_1s+d_0}$$

In order to regulate the load current, transfer function $H_1(s)$ should be considered since it represents the relation between output voltage v_2 (hence Io) and control parameter G. The closed-loop dynamic model for both switching converters is shown in Fig. 19 where the effect of the inner loop is represented by H_1 and the output current regulation is carried out by the outer loop including a PI compensator.

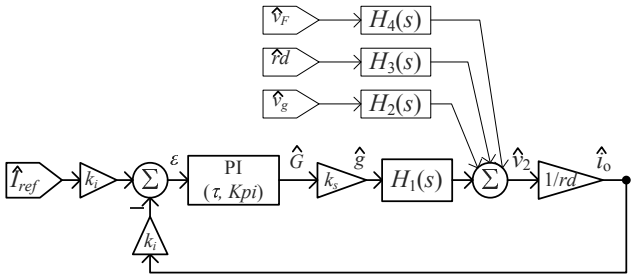

Fig. 19 Small-signal block diagram of Ćuk/SEPIC –based LFR with an outer loop for output current regulation.

It must be taken into account that when the output feedback bandwidth is increased, a ripple appears at twice the line frequency in the sensed variable (i_o) distorting the input parameter (G) and consequently the input current.

This distorted reference must be eliminated in order to obtain an undistorted input current. Thus, the bandwidth of the PI compensator must be relatively low to achieve a suitable response [29-31]. Hence, a compromise between bandwidth (speed response) and input current distortion has to be achieved. For light dimmer applications a slow response (100 ms) is appropriate. Using the Bode diagram depicted in Fig. 20 allows the selection of the PI compensator parameters as τ= 1/500 s, Kpi = 1/10 for 66 degrees phase margin at a crossover frequency of 36 rad/s. The loop gain $T(s)$ has a cero at s_z= –500 rad/s and poles at s_1= –68.13 rad/s, $s_{2,3}$= (–1.67 ± j 6.22)·10^4 rad/s, besides a pole at the origin of the s-plane. This results in closed-loop poles located at, $s_{1,2\text{-CL}}$= (–1.68 ± j 6.28)·10^4 rad/s, and $s_{3,4\text{-CL}}$= (–36.8 ± j 37.7) rad/s. It can be observed that the latter are dominant and determine the dynamic response of the controlled converter with a damping coefficient of 0.7.

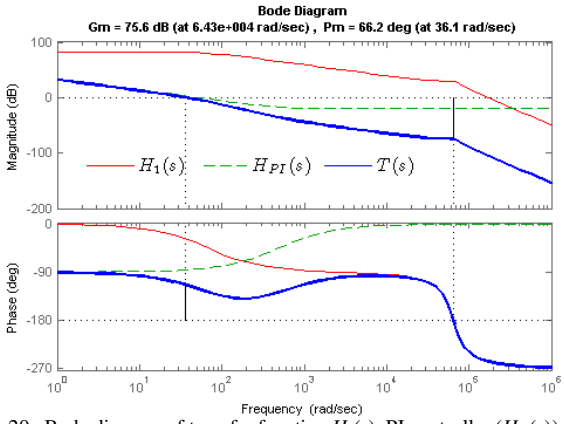

Fig. 20 Bode diagram of transfer function $H_1(s)$, PI controller ($H_{PI}(s)$), and loop gain $T(s)$ in the Ćuk converter-based LFR.

B. *Practical Implementation*

An experimental prototype has been developed to validate the theoretical analysis and PSIM simulations corresponding to the block diagram of the two-loop control circuit illustrated in Fig. 21, where the inner loop implements the PFC with variable hysteresis width and the external loop carries out the output current regulation of an string of 9 HBLEDs “Xlamp MC-E”. A detailed scheme of the control circuit is depicted in Fig. 22. Note that the proposed controller would be equivalent to the classical SMC if the output of the tracker (i) were directly connected to the inverter input (iv). Therefore, the added complexity with respect to SMC implementation is limited to the insertion of two operational amplifiers and an analogue multiplier.

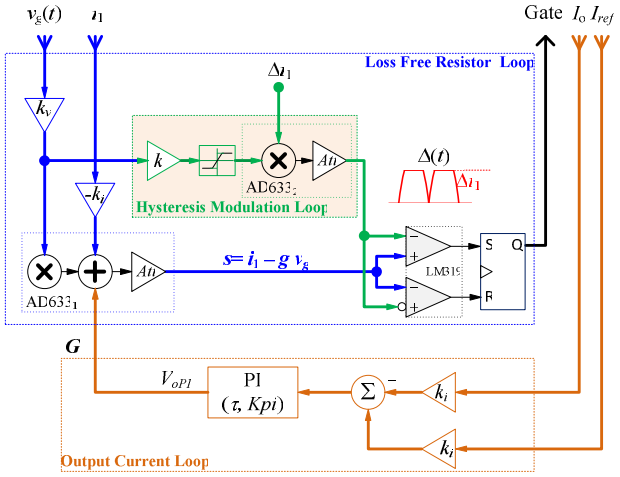

Fig. 21 Block diagram of the control stage Ćuk converter with two-loop control.

Since the use of hysteresis in the control circuit implies a variable switching frequency, this fact has been considered in the design of the magnetic components. Note that the practical operation range of the converter goes from 150 kHz to 400 kHz, and the ferrite cores of both inductors can operate

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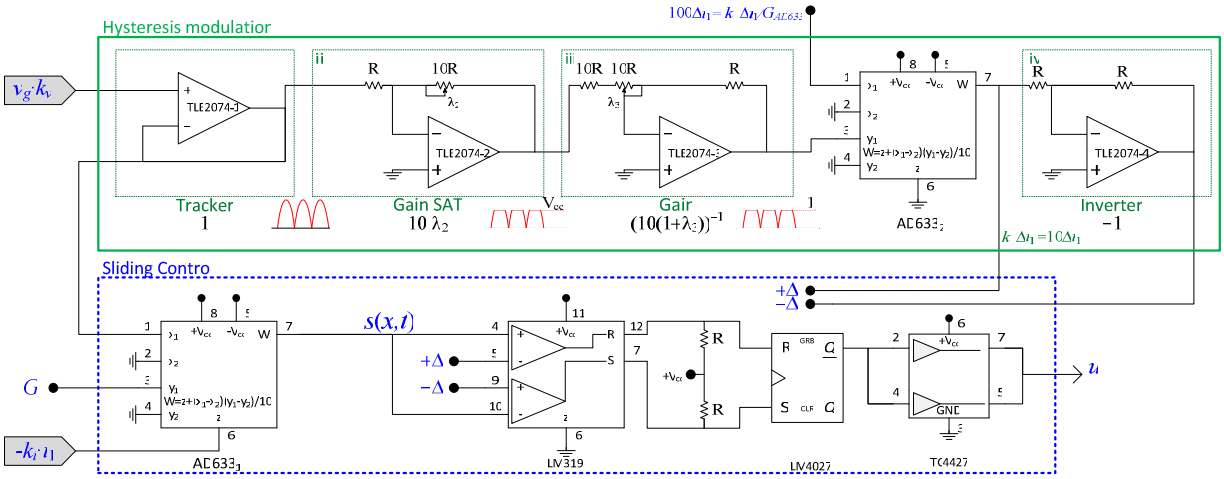

Fig. 22 Control circuit for SMC with variable hysteresis width ($0<\lambda_i<1$, i=2,3).

between 25 kHz to 500 kHz, which guarantees a correct performance in the working zone of the variable hysteresis width proposed in the paper.

The experimental prototype board supplying an string of 9 HBLEDs "Xlamp MC-E" (Cool White) of Cree, Inc is presented in Fig. 23. The set of parameters was given in TABLE V. In this case parameter g is given by $g = G{\cdot}k_s$, where $k_s = k_v/(Att_{AD633}k_i)$, k_v being the voltage sensor gain (k_v = 1/50), k_i the current sensor gain (k_i = 10), and Att_{AD633} the attenuation (Att_{AD633} = 10) of to the analogue multiplier AD633.

Thus, the value of k_s is 1/5000, which has been chosen with the aim of obtaining a wider range of control in the power transfer, and consequently greater control margin over the load current. The hysteresis width modulation circuit consists of 4 blocks (Fig. 22): i) voltage follower, ii) saturation block to control the slope of the hysteresis width at zero crossings, iii) attenuation block plus multiplier to adapt the maximum of the signal (V_{cc}) to the unit value, and insert the maximum admitted ripple in i_1. Finally, iv) an inverter block to obtain the other hysteresis limit.

C. Simulation and Experimental Results

Measurements of efficiency of the Ćuk converter with the two control loops have been carried out considering the power delivered by the full wave rectifier as the input power. They reach up to 94% as shown in TABLE VI and corroborated in Fig. 24.

TABLE VI EFFICIENCY AND FLICKERING VS OUTPUT CURRENT I_o.

I_o (mA) (C_2 500uF)	Efficiency %	ΔI_o (mA)	Flickering $\Delta I_o/(2I_o)$ (%)
100	93	15	8.0
150	93	26	8.7
350	94	84	12.0
500	92	128	12.8

It can be observed in TABLE VI that the flickering increases when the average value of the output current increases. On the contrary, an increase of the output capacitance C_2 implies a decrease of the flickering as illustrated in TABLE VII.

Concerning the harmonic distortion provoked by the insertion of the external control loop, it has to be pointed out that the smallest value of I-THD is 1.26%, when operating with only the internal current control loop and SMC-HM. Adding the external output current regulation loop results in 1.73%, which is a relatively small increase of I-THD.

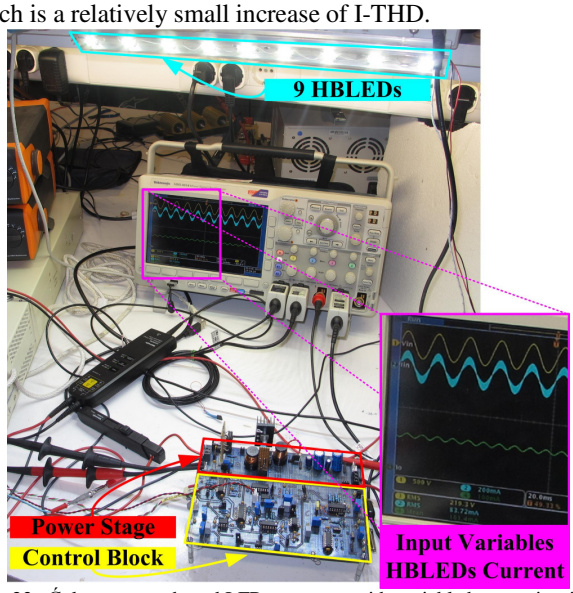

Fig. 23 Ćuk converter-based LFR prototype with variable hysteresis width supplying an string of 9 HBLEDs.

TABLE VII FLICKERING VS OUTPUT CAPACITOR C_2

	I_o = 350 mA	
C_2 (uF)	ΔI_o (mA)	$\Delta I_o/(2I_o)$ (%)
500	84	12
750	64	9
1.000	44	6
1.500	28	4

Moreover, in order to validate the output current control, the SSM prediction has been compared with that of the switched circuit. The block diagram of SSM in Fig. 19 and the switching converter have been modelled in PSIM neglecting load disturbances, i.e., $\hat{rd} = \hat{V}_F = 0$. A plot of the output current is depicted in Fig. 25, where it can be seen the effect of a step change of 300 to 500 mA in the reference (I_{ref}), on the output current (I_o) when the converter is supplied by a fully rectified sinusoidal waveform corresponding to a standard line voltage.

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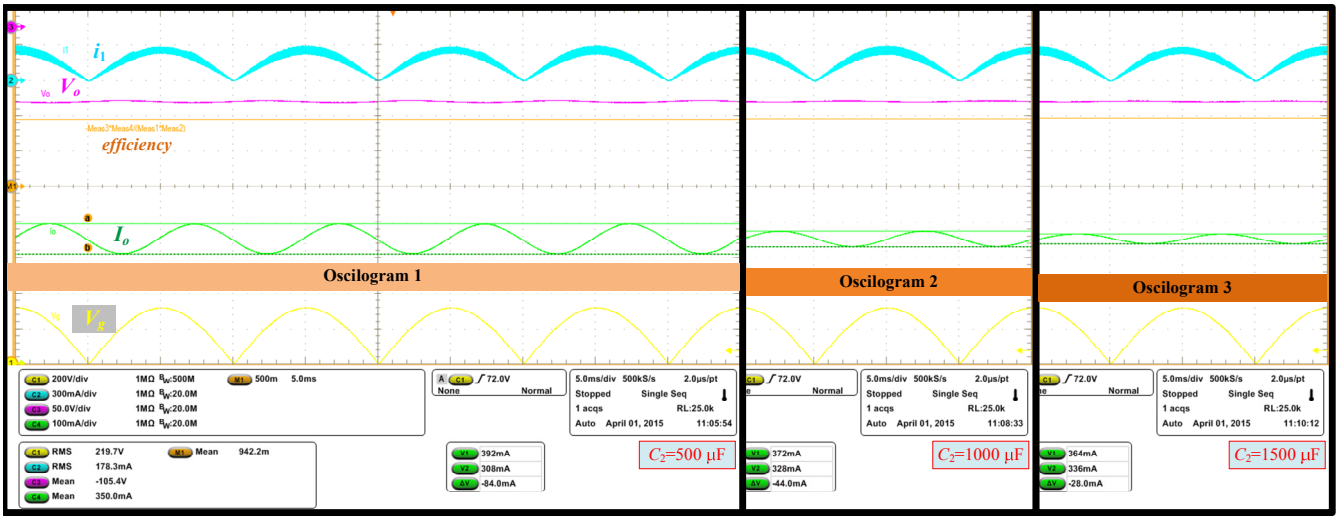

a) b) c)

Fig. 24 Efficiency and output current ripple for different values of output capacitance a) C_2 = 500 uF, b) C_2 = 1000 uF, c) C_2 = 1500 uF.

For the purpose of comparison, the output current predicted by the SSM with or without the perturbation produced by the sinusoidal input voltage is plotted respectively as $I_{oSSM|vg=0}$, and $I_{oSSM|vg=|Vm|\sin(\omega t)}$ in the same figure, and corroborates the theoretical predictions.

The corresponding experimental results are in perfect agreement with the simulation as illustrated in Fig. 26 where it can be seen how the load current tracks the reference current I_{ref} while the input variables maintain the proportionality imposed by the LFR behaviour.

V. CONCLUSIONS

This paper has shown that the Ćuk converter is a better alternative than the SEPIC converter when designing a sliding-mode control-based loss-free resistor due to its unconditionally stable nature. It has been also illustrated that the use of a variable hysteresis width in the design of the sliding-mode internal current loop eliminates the distortion in the zero-crossings of the input current by reducing significantly the I-THD while keeping a unity PF. The analysis of the ISD has led to the design of an external control loop to regulate the output current supplying an HBLEDs string, which results in a wide dimmer range (from 180% to 20% of the HBLED nominal current) with a low I-THD (15%). The experimental measurements in a Ćuk converter are in good agreement with the simulations and the theoretical predictions. In comparison with the main antecedents on the use of Ćuk and SEPIC converters for HBLEDs [32-36], the work here reported presents an extensive dynamical analysis of the two controlling loops in both converters in a clear-cut contrast with the mentioned papers, which are focused on the static analysis to select the appropriate values of the passive components. A compromise among a fast output response, a small flickering and a slow value of I-THD has been solved empirically because an optimal solution for both SMC, and SMC-HM is still an open problem that could be the subject of posterior research in robust control techniques following the procedure reported in [37].

The proposed techniques in this paper can be used in the design of low power single-stage AC-DC PFC converters with a series inductor in the input port requiring a regulated variable (voltage or current) in the output port.

Prospective work contemplates an optimized design of the

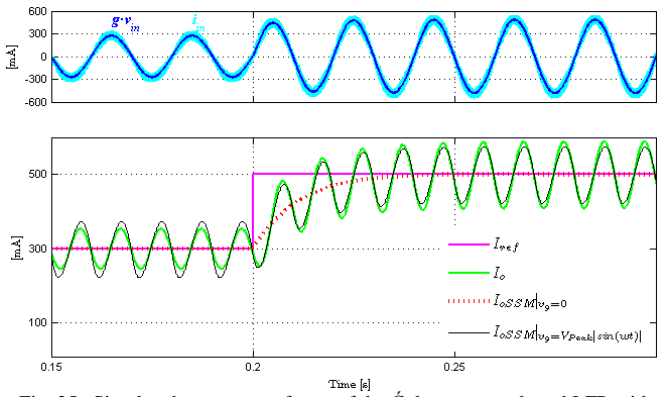

Fig. 25 Simulated output waveforms of the Ćuk converter–based LFR with output current regulation: reference current (I_{ref}), circuit output current (I_o), SSM output current ($I_{oSSM|vg=0}$), and SSM output current considering the AC input voltage disturbances ($I_{oSSM|vg=|Vm|\sin(\omega t)}$).

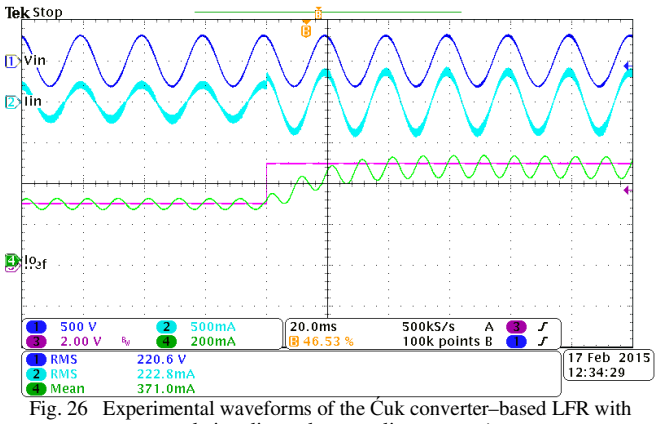

Fig. 26 Experimental waveforms of the Ćuk converter–based LFR with output current regulation: line voltage v_{in}, line current i_{in}, output current reference I_{ref}, output current Io.

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controller in view of a microelectronic implementation of ASIC type.

ANNEX I

TABLE VIII SSM TRANSFER FUNCTION PARAMETERS

Ćuk converter	SEPIC converter
$g_2 = 0$ $g_1 = 0$ $g_0 = r_d \cdot v_g^2 \cdot V_2$	$g_2 = r_d \cdot v_g^2 \cdot V_2 \cdot C_1 \cdot L_2$ $g_1 = 0$ $g_0 = r_d \cdot v_g^2 \cdot V_2$
$vg_1 = -r_d \cdot V_2 \cdot C_1 \cdot (V_2 + v_g)$ $vg_1 = 0$ $vg_0 = 2r_d \cdot V_2 \cdot v_g \cdot g$	$vg_2 = r_d \cdot v_g \cdot g(2V_2 + v_g) C_1 \cdot L_2$ $vg_1 = -r_d \cdot v_g \cdot C_1 \cdot V_2$ $vg_0 = 2r_d \cdot V_2 \cdot v_g \cdot g$
$rd_2 = (V_2 - V_F) V_2 \cdot C_1 \cdot L_2 (V_2 + v_g) / r_d$ $rd_1 = (V_2 - V_F) v_g^2 \cdot g \cdot L_2 / r_d$ $rd_0 = (V_2 - V_F) V_2^2 / r_d$	$rd_2 = (V_2 - V_F) V_2 \cdot C_1 \cdot L_2 (V_2 + v_g) / r_d$ $rd_1 = (V_2 - V_F) v_g^2 \cdot g \cdot L_2 / r_d$ $rd_0 = (V_2 - V_F) V_2^2 / r_d$
$vf_2 = C_1 \cdot L_2 \cdot V_2 (V_2 + v_g)$ $vf_1 = L_2 \cdot v_g^2 \cdot g$ $vf_0 = V_2^2$	$vf_2 = C_1 \cdot L_2 \cdot V_2 (V_2 + v_g)$ $vf_1 = L_2 \cdot V_g^2 \cdot g$ $vf_0 = V_2^2$
$d_3 = C_1 \cdot C_2 \cdot L_2 \cdot V_2 \cdot r_d \cdot (v_g + V_2)$ $d_2 = \left(C_1 \cdot V_2 (v_g + V_2) + r_d v_g^2 g C_2 \right) L_2$ $d_1 = V_2 r_d \left((C_1 + C_2 V_2) + C_1 v_g \right) + L_2 \cdot V_g^2 g$ $d_0 = r_d \cdot v_g^2 \cdot g + V_2^2$	$d_3 = C_1 \cdot C_2 \cdot L_2 \cdot V_2 \cdot r_d \cdot (v_g + V_2)$ $d_2 = \left(C_1 V_2 (v_g + V_2) + r_d v_g^2 g (C_1 + C_2) \right) L_2$ $d_1 = V_2^2 \cdot r_d \cdot C_2 + L_2 \cdot V_g^2 \cdot g$ $d_0 = r_d \cdot v_g^2 \cdot g + V_2^2$

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