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Analytical Multi-Parametric Stability Boundaries of DC-DC Buck Converters Under V^1 Control Concept

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SUMMARY

Two main methods for controlling switching converters exist in the literature. The direct one is the Voltage Mode Control (VMC) which suffers from some disadvantages such as slow response to load variations and an input-voltage-dependent total loop gain. The Current Mode Control (CMC) can overcome these problems but at the expense of extra cost and more complex control design. V^1 concept is a new promising control technique for designing VMC of buck-type converters with an optimal response similar to CMC. In this paper, the dynamics and the stability of buck converters under V^1 control is studied. In particular, subharmonic oscillation limits in the parameter space are addressed. First, a closed-loop state-space model is derived and then used to formulate an analytical matrix-form expression for predicting the stability limit of the system. Using this expression, multi-parametric stability boundaries are obtained. It is shown that the equivalent series inductance of the output capacitor can narrow the stability region. It is also demonstrated that the integral action in the feedback loop of a V^1 controlled buck converter has a negligible effect on the subharmonic oscillation boundary. The theoretical analysis is validated through numerical simulation of the circuit-level switched model of the system.

KEY WORDS: Circuit stability, DC-DC power conversion, Power electronics, Switched mode power supplies, Subharmonic oscillation.

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1. Introduction

One of the key factors affecting the dynamic behavior and the performances of switched mode power converters is the control mode used. Conventional Voltage Mode Control (VMC) is a simple single feedback loop with only the output voltage as a control variable. However, its first generation version features poor response in front of load changes [1]. Also, the total loop gain in conventional VMC schemes is input-voltage-dependent making the controller design conditioned by this parameter. Current Mode Control (CMC) utilizes the inductor current as an additional control variable, which improves the transient response [1] at the expense of extra cost and more complex controller design. Therefore, VMC is still preferred by many designers because its disadvantages can be dealt with by using different techniques. For instance, voltage feed-forward [2] in which the slope of the ramp modulator signal is modified proportionally to the input voltage provides an input-voltage-independent total loop gain. Different ripple-based VMC control schemes have been also proposed to improve the load transient response of switching converters. For instance, V^2 control was proposed in [3–5] by using the parasitic output voltage ripple instead of the inductor current as an additional feedback signal. The V^2 control technique is composed of two voltage loops. One slow outer voltage loop responsible for regulating the output voltage and another fast inner voltage loop to improve load transient response. Therefore, the V^2control only uses the output voltage but it works properly only with a non-ideal output capacitor characterized by a high Equivalent Series Resistance (ESR). The V^2I_C was proposed in [6] by adding the capacitor current information using only the output voltage and by taking into account the Equivalent Series Inductance (ESL) of the output capacitor whose value becomes significant at high switching frequencies. Recently, it has been proved in [7] that the V^2I_C control can be implemented as a type-III VMC [8] with a single feedback path and measuring only the output voltage hence introducing the V^1 control concept. It has also been shown that such a VMC can exhibit a kind of feed-forward of the output current under some design conditions hence having similar time response to the one corresponding to the previous controllers. Accordingly, low-cost, very fast controllers that only sense the output voltage can be used. This is possible because the output voltage contains the information of almost all the signals of the buck converter power stage. By exploiting this feature, a conventional VMC can be designed to behave as a CMC in terms of system response speed in front of load changes. A detailed discussion on deriving the V^1 control can be found in [7]. In that work it has been shown that by only using the output voltage in the feedback loop and with an appropriate choice of the poles

and the zeros of the compensator, an extremely fast response under load steps can be achieved similar to the results obtained when ripple-based control and CMC strategies are used.

The development of new controllers for switching converters must be accompanied with accurate tools to predict their dynamical behavior to enhance their performances. The design of such converters would require a comprehensive knowledge about suitable ways of their modeling and stability analysis, particularly, with novel and advanced control techniques. The desired behavior of any power electronic system is a periodic orbit with the same period as the external clock and the modulating ramp signals used to generate the duty cycle of the driving PWM signal. However, due to the presence of switching nonlinearities, it is possible that undesired instabilities in the form of subharmonic oscillations take place. This important issue was not addressed in [7] and the stability limit under the new V^1 controller was not determined. We will show that the system can exhibit subharmonic oscillation if the system parameters are inappropriately selected based on conventional design guidelines based on averaged models or simplified discrete-time models. The effect of the main parameters such as the duty cycle, the slope or amplitude of the ramp modulator, the poles and the zeros of the controller as well as that of the parasitic parameters such as the ESL of the capacitor are revealed. The integral action will be shown to have a negligible effect on the subharmonic oscillation boundary in this control strategy.

Multi-parametric stability boundaries of switching converters are usually tackled by using numerical techniques such as in [9, 10], semi-analytical approaches like in [11–14] or analytical methods as recently reported in [15–17]. In this paper, we carry out study of of the stability limits of the buck converter under the novel and advanced V^1 control strategy. Multi-parametric stability boundaries of the system are determined by using an analytical approach.

The rest of the paper is organized as follows. Section 2 presents the system description along with its state-space modeling and steady-state response. Subsequently, in Section 3 a closed-form expression corresponding to subharmonic oscillation occurrence in switching regulators is derived for the buck converter under V^1 control demonstrating that the integral action has a negligible effect on the subharmonic oscillation boundary. Multi-parametric stability boundaries of the system are presented in Section 4 which are also validated in Section 5 by numerical simulations performed using a switched model implemented in PSIM© software. A comparison with conventional type-III compensation design is also provided showing that the stability limits of the buck converter with the two compensator designs are different. Finally, conclusions are presented in the last section.

2. System description and open-loop s-domain modeling

2.1. System description

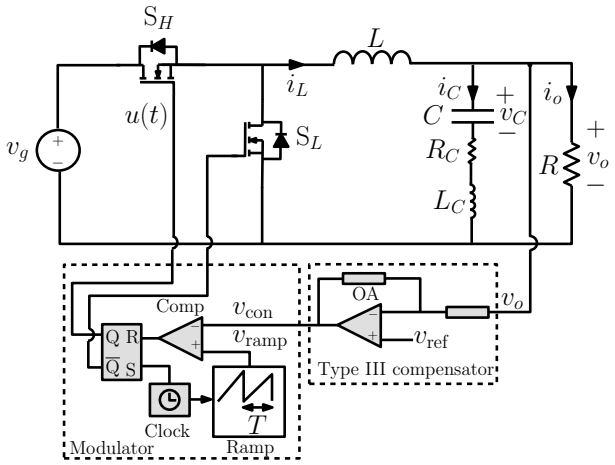


Figure 1. Schematic circuit diagram of a buck converter with the output capacitor modeled as an RLC network and under type-III compensation scheme.

Fig. 1 shows the circuit diagram of a DC-DC buck converter under VMC. Like in [7], a type-III compensation scheme [8, 18] is used to implement V^1 control. The VMC network comprises an error amplifier with the reference voltage $v_{\rm ref}$ on one pin input and the output v_o from the buck converter on the other pin. The activation of the high side and the low side switches S_H and S_L is carried out as follows: the error voltage $e_v = v_{\rm ref} - v_{\rm o}$ is processed by means of the compensator, and the output $v_{\rm con}$ of this compensator is connected to the inverting pin of the comparator whereas a $T-$periodic ramp signal $v_{\rm ramp}$ is applied to the non-inverting pin. The output of the comparator is connected to the reset entry of an SR flip-flop while a $T-$periodic clock synchronized with the ramp signal is connected to its set entry in such a way that the switch S_H is turned ON (therefore $u = 1$) at the starting of each period and it is turned OFF ($u = 0$) whenever $v_{\rm con} = v_{\rm ramp}$. S_L is driven complimentarily to S_H.

2.2. The s-domain open-loop model of the power stage

Parasitic parameters of the output capacitor are included because of their effects on subharmonic oscillation boundaries. In addition to the Equivalent Series Resistance (ESR) of the capacitor, its ESL is also taken into account in the modeling. Note that the ESL is rarely specified by manufacturers or taken into account by researchers. However, its value becomes significant at high switching frequencies.

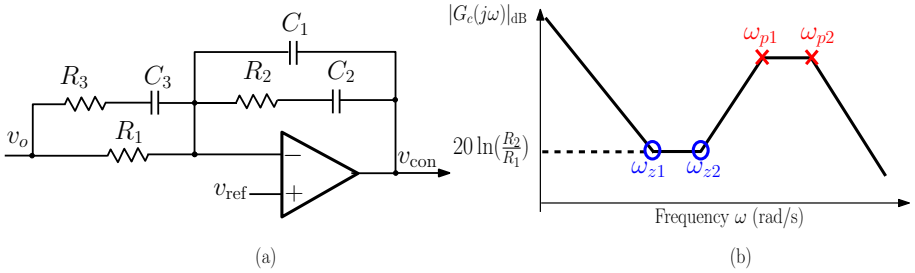


Figure 2. Schematic circuit diagram of a type-III compensator (a) and the modulus of its frequency response (b).

Details on accurate modeling of capacitors can be found in [19]. While, traditionally this parameter is neglected for stability analysis, it has been shown in [11] that its effect cannot be ignored. Note that with this parasitic effect, a new state variable i_C, the capacitor current, is added to the system dynamics. The transfer function from the binary control signal u to the output voltage v_o of the power stage can be expressed as follows:

$$H_p(s) = \frac{\frac{Rv_g}{L_C LC}(L_C C s^2 + R_C C s + 1)}{s^3 + (\frac{L}{R} + \frac{L_C}{R}(1 + \frac{R_C}{R}))s^2 + \frac{L}{L_C C}s + \frac{R}{L_C LC}} \tag{1}$$

Note that if the ESL L_C is neglected, the previous transfer function mode becomes the conventional transfer function of a buck converter without ESL [1].

2.3. The s-domain model of the controller

As stated previously in the introduction, the V^1 control is inspired from the ripple-based V^{2}I$_C$ control [11] and, as demonstrated in [7], its corresponding e_v-to-$v_{\rm con}$ transfer function can be expressed in a similar way to a type-III controller as follows:

$$G_c(s) = \frac{W_i}{s}\frac{(s/\omega_{z1}+1)(s/\omega_{z2}+1)}{(s/\omega_{p1}+1)(s/\omega_{p2}+1)}. \tag{2}$$

where W_i is the integrator gain, ω_{z1} and ω_{z2} are two zeros and ω_{p1} and ω_{p2} are two poles to be placed appropriately. Fig. 2 shows the schematic circuit diagram of a type-III compensation network and its asymptotic Bode modulus plot. It can be noted that the network utilizes two zeros to improve phase margin and to counteract the effects of the poles of the power stage. According to Fig. 2-a, the zeros, the poles and the integrator gain are given by the following expressions in terms of the passive

components [8]:

$$\begin{aligned} \omega_{z1} &= \frac{1}{R_2C_2},\ \omega_{z2} = \frac{1}{(R_1+R_3)C_3} \\ \omega_{p1} &= \frac{C_1+C_2}{R_2C_1C_2},\quad \omega_{p2} = \frac{1}{R_3C_3},\ W_i = \frac{1}{R_1(C_1+C_2)} \end{aligned} \tag{3}$$

3. State-space mathematical system modeling

3.1. State-space modeling of the power stage

Let us define $\mathbf{x}_p = (v_C,\, i_L,\, i_C)^\intercal$ to be the vector of the state variables of the power stage whose output is the voltage v_o which can be expressed as a weighted difference between the two state variables i_L (the inductor current) and i_C (the capacitor current), namely, $v_o = R(i_L - i_C)$. Accordingly, let $\mathbf{C}_p^\intercal = (0,\ R,\ -R)$. Therefore the state-space model of the power stage is as follows:

$$\dot{\mathbf{x}}_p = \mathbf{A}_p\mathbf{x}_p + \mathbf{B}_p v_g u, \tag{4a}$$

$$v_o = \mathbf{C}_p^\intercal \mathbf{x}_p, \tag{4b}$$

where the overdot stands for taking the derivative with respect to time and the matrices $\mathbf{A}_p$ and $\mathbf{B}_p$ are given by:

$$\mathbf{A}_p = \begin{pmatrix} 0 & 0 & \frac{1}{C} \\ 0 & -\frac{R}{L} & \frac{R}{L} \\ -\frac{1}{L_C} & \frac{R}{L_C} & -\frac{R+R_C}{L_C} \end{pmatrix},\ \mathbf{B}_p = \begin{pmatrix} 0 \\ \frac{1}{L} \\ 0 \end{pmatrix}. \tag{5}$$

All the variables and parameters appearing in (5) can be identified in the schematic circuit diagram of Fig. 1. Note that because the ESL of the output capacitor was taken into account, the model of the power stage is of third order contrarily to the conventional second order model of the power stage of a buck converter without an ESL.

3.2. State-space modeling of the V^1 compensator

Performing a partial fraction decomposition, (2) can be rewritten in the following form:

$$G_c(s) = \frac{W_i}{s} + \frac{W_{p1}}{s+\omega_{p1}} + \frac{W_{p2}}{s+\omega_{p2}}, \tag{6}$$

where W_{p1} and W_{p2} are feedback coefficients corresponding to the state variables v_{p1} and v_{p2} of the controller. These coefficients can be expressed as follows:

$$W_{p1} = \frac{W_i\omega_{p2}(\omega_{z1}\omega_{z2} - \omega_{p1}(\omega_{z1}+\omega_{z2}) + \omega_{p1}^2)}{\omega_{z1}\omega_{z2}(\omega_{p1}-\omega_{p2})}, \tag{7a}$$

$$W_{p2} = -\frac{W_i\omega_{p1}(\omega_{z1}\omega_{z2} - \omega_{p2}(\omega_{z1}+\omega_{z2}) + \omega_{p2}^2)}{\omega_{z1}\omega_{z2}(\omega_{p1}-\omega_{p2})}. \tag{7b}$$

In a conventional design, the zeros are placed close to the LC resonant frequency of the buck converter power stage, and one of the poles is placed at one half of the switching frequency [8]. Several design procedures are proposed in [7] for the new V^1 control design depending on the quality factor Q of the impedance of the output capacitor. For a quality factor $Q < 1/2$, the zeros and poles for the V^1 control scheme are selected as follows [7]:

$$\omega_{z1} = \frac{W_i}{k_v},\ \omega_{z2} = \frac{k_v}{k_iC},\ \omega_{p1} = \frac{1}{R_CC},\ \omega_{p2} = \frac{R_C}{L_C}, \tag{8}$$

where k_v corresponds to the voltage feedback gain, and k_i can be viewed as a virtual current feedback gain. Let $\mathbf{x}_c = (v_{p1},\ \ v_{p2})^\intercal$ be the vector of the two state variables of the controller by excluding the state variable v_i of the integrator which is included separately in the model to have a well-posed problem when solving for the system steady-state solution [16]. The equations describing the motion of the controller can be written as follows:

$$\dot{\mathbf{x}}_c = \mathbf{A}_c\mathbf{x}_c + \mathbf{B}_ce_v, \tag{9a}$$

$$\dot{v}_i = v_{\rm ref} - \mathbf{C}_p^\intercal\mathbf{x}_p. \tag{9b}$$

$$v_{\rm con} = \mathbf{C}_c^\intercal\mathbf{x}_c + W_iv_i \tag{9c}$$

where $e_v = v_{\rm ref} - \mathbf{C}_p^\intercal\mathbf{x}_p$ is the error voltage which is also the input of the controller, v_i is the integral of the error and $v_{\rm con}$ is the output of the controller. The matrices $\mathbf{A}_c$, $\mathbf{B}_c$ and and $\mathbf{C}_c$ are given by:

$$\mathbf{A}_c = \begin{pmatrix} -\omega_{p1} & 0 \\ 0 & -\omega_{p2} \end{pmatrix}, \mathbf{B}_c = \begin{pmatrix} 1 \\ 1 \end{pmatrix},\ \ \mathbf{C}_c = \begin{pmatrix} W_{p1} \\ W_{p2} \end{pmatrix}. \tag{10}$$

3.3. The complete closed-loop state-space model

Let us define the augmented state vector $\mathbf{x} = (\mathbf{x}_p,\ \mathbf{x}_c)^\intercal$. Let the augmented matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{B}_r$ and $\mathbf{C}$ be as follows:

$$\mathbf{A} = \begin{pmatrix} \mathbf{A}_p & \mathbf{0} \\ -\mathbf{B}_c\mathbf{C}_p^\intercal & \mathbf{A}_c \end{pmatrix}, \mathbf{B} = \begin{pmatrix} \mathbf{B}_pv_g \\ \mathbf{0} \end{pmatrix}, \tag{11}$$

$$\mathbf{B}_r = \begin{pmatrix} \mathbf{0} \\ \mathbf{B}_cv_{\rm ref} \end{pmatrix},\ \mathbf{C} = -\begin{pmatrix} \mathbf{0} \\ \mathbf{C}_c \end{pmatrix}. \tag{12}$$

Then, the system with the plant model in (4a)-(4b) and the controller model in (9a)-(9b) can be described by the following state-space model together with the switching condition (19):

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u + \mathbf{B}_r, \tag{13a}$$

$$\dot{v}_i = v_{\text{ref}} - \mathbf{C}_p^{\intercal}\mathbf{x}_p, \tag{13b}$$

$$v_{\text{con}} = -\mathbf{C}^{\intercal}\mathbf{x} + W_i v_i, \tag{13c}$$

The expression of the solution $\mathbf{x}(t)$ at time t of the system starting at an initial condition $\mathbf{x}(t_0)$ at time instant t_0 takes the following form [27]:

$$\mathbf{x}(t) = e^{\mathbf{A}(t-t_0)}\mathbf{x}(t_0) + \int_{t_0}^{t} e^{\mathbf{A}(t-\tau)}\mathrm{d}\tau\mathbf{B}_u\mathbf{w}. \tag{14}$$

Remark : Because the state matrix $\mathbf{A}$ corresponding to the buck converter is invertible, we have used the following formula whenever it was necessary:

$$\int_{t_0}^{t} e^{\mathbf{A}(t-\tau)}\mathrm{d}\tau = \mathbf{A}^{-1}(e^{\mathbf{A}(t-t_0)} - \mathbf{I}). \tag{15}$$

For the integral variable $v_i(t)$ one can write:

$$v_i(t) = v_i(t_0) + \int_{t_0}^{t} v_{\text{ref}} - \mathbf{C}_p^{\intercal}\mathbf{x}_p(\tau)\mathrm{d}\tau, \tag{16}$$

where $t_0 = nT$ for $u = 1$ ($t \in (nT, nT + d_nT)$) and $t_0 = nT + d_nT$ for $u = 0$ ($t \in (nT + d_nT, (n+1)T)$). By taking into account the switching decision dictated by the PWM strategy, the closed-loop model can be obtained. This switching decision imposes the following cycle-by-cycle constraint in the time domain:

$$v_{\text{con}}(d_nT) - v_{\text{ramp}}(d_nT) = 0 \tag{17}$$

where d_n is the duty cycle of the driving signal u within the switching period $(nT, (n+1)T)$, $n \in \mathbb{N}$, defined as the ratio between the ON time duration and the entire switching period $(nT, (n+1)T)$. According to the definition of the vector $\mathbf{C}$ in (12), the control voltage can be expressed as follows:

$$v_{\text{con}}(t) = -\mathbf{C}^{\intercal}\mathbf{x}(t) + W_i v_i(t). \tag{18}$$

Hence (17) becomes as follows:

$$-\mathbf{C}^{\intercal}\mathbf{x}(d_nT) + W_i v_i(d_nT) - v_{\text{ramp}}(d_nT) = 0. \tag{19}$$

4. Analytical multi-parametric prediction of subharmonic oscillation boundary

4.1. The steady-state value of the integral variable

Let D be the steady-state duty cycle $D = \lim_{n\to\infty} d_n$. In the presence of an integrative feedback loop, the value of D is imposed by the relationship between the steady-state average output voltage (voltage reference $v_{\rm ref}$) and the input voltage v_g as will be demonstrated below. In fact, according to (16), the steady-state values of the integral variable at time instant DT within a switching cycle and at the final of the same switching cycle can be calculated as follows:

$$v_i(DT) = v_i(0) + W_i \int_0^{DT} (v_{\rm ref} - v_o(t))\mathrm{d}t, \tag{20a}$$

$$v_i(T) = v_i(DT) + W_i \int_{DT}^{T} (v_{\rm ref} - v_o(t))\mathrm{d}t. \tag{20b}$$

By substituting (20b) in (20a), one obtains

$$\begin{aligned} v_i(T) &= v_i(0) + W_i \int_0^{DT} (v_{\rm ref} - v_o(t))\mathrm{d}t + W_i \int_{DT}^{T} (v_{\rm ref} - v_o(t))\mathrm{d}t \\ &= v_i(0) + W_i \int_0^{T} (v_{\rm ref} - v_o(t))\mathrm{d}t. \end{aligned} \tag{21}$$

For the integral variable v_i to be $T-$periodic, i.e., for the equality $v_i(0) = v_i(T)$ to hold, the following condition must be fulfilled:

$$W_i \int_0^{T} (v_{\rm ref} - v_o(t))\mathrm{d}t = 0 \Rightarrow T v_{\rm ref} - \int_0^{T} v_o(t)\mathrm{d}t = 0, \tag{22}$$

which implies that:

$$v_{\rm ref} = \frac{1}{T} \int_0^{T} v_o(t)\mathrm{d}t = V_o, \tag{23}$$

where V_o stands for the average value of the output voltage v_o. This means that the DC value of the output signal is equal to the desired reference signal and that the DC component of the error signal is zero. Note that this error signal is the input to the integrator and if it is not null, the average output of the integrator will not converge to a steady state. Therefore, the DC value of the output voltage is uniquely determined by $v_{\rm ref}$. The previous analysis apply for any switching converter. In particular, for the buck converter considered in this study, according to (4a)-(4b), the steady-state duty cycle D is related to the DC component of the output voltage, demonstrated before to be equal to $v_{\rm ref}$, by the following expression:

$$V_o = \mathbf{C}_p^{\intercal}\, (s\mathbf{I} - \mathbf{A}_p)^{-1}\mathbf{B}_p\big|_{s=0}\, U_0 = -\mathbf{C}_p^{\intercal}\mathbf{A}_p^{-1}\mathbf{B}_p v_g D. \tag{24}$$

where U_0 is the DC component of the binary signal u in steady-state which coincides with the steady-state duty cycle D. Solving the previous equation for D one obtains [1]:

$$D = \frac{V_o}{-\mathbf{C}_p^\intercal \mathbf{A}_p^{-1}\mathbf{B}_p v_g} = \frac{v_{\rm ref}}{v_g}. \tag{25}$$

which agrees with steady-state analysis based on net volt-seconds assuming low ripple at the output voltage [1]. Hence, there is no need for solving the switching equation (19) to determine the operating duty cycle D in the presence of an integral action in the output voltage feedback loop such as in V^1 control. Note that there is an infinite number of solutions for $v_i(0)$ and equivalently $v_i(DT)$ if these values are to be determined from (20a)-(20b) because even if $v_o(0)$ is fixed there are infinity of values of $v_o(DT)$ that will give $v_o(0) = v_o(T)$ depending on the value of D or equivalently $v_{\rm ref}$. In fact, the value of $v_i(0) = v_i(T)$ is to be determined from the switching condition (19). From this condition, the integral variable $v_i(DT)$ at time instant DT is given by the following expression:

$$v_i(DT) = \frac{1}{W_i}(\mathbf{C}^\intercal(\mathbf{x}(DT) - v_{\rm ramp}(DT))). \tag{26}$$

Once the value of $v_i(DT)$ is obtained from the switching condition, the steady-state value $v_i(0)$ of the integral variable at the beginning of the switching period can be obtained using the equation the integrator variable dynamics:

$$v_i(0) \quad = \quad v_i(DT) + W_i \int_{DT}^{T} (v_{\rm ref} - v_o(t)) {\rm d}t. \tag{27}$$

4.2. The steady-state operating point of the non-integrative state-variables

Let us define $\mathbf{\Phi}_1 = e^{\mathbf{A}DT}$, $\mathbf{\Phi}_0 = e^{\mathbf{A}(1-D)T}$, and $\mathbf{\Psi}_1 = \int_0^{DT} e^{\mathbf{A}t}{\rm d}t(\mathbf{B}+\mathbf{B}_r) = \mathbf{A}^{-1}(\mathbf{\Phi}_1 - \mathbf{I})(\mathbf{B}+\mathbf{B}_r)$ and $\mathbf{\Psi}_0 = \int_0^{(1-D)T} e^{\mathbf{A}t}{\rm d}t\mathbf{B}_r = \mathbf{A}^{-1}(\mathbf{\Phi}_0 - \mathbf{I})\mathbf{B}_r$. Let $\mathbf{x}(0)$ and $\mathbf{x}(DT)$ be the steady-state value of the $T-$periodic orbit $\mathbf{x}(t)$ of the system at the start of each period and at the time instant DT respectively. The steady-state values of the non-integrative state variables can be obtained by enforcing periodicity and can be expressed as follows:

$$\mathbf{x}(0) = (\mathbf{I} - e^{\mathbf{A}T})^{-1}(\mathbf{\Phi}_0\mathbf{\Psi}_1 + \mathbf{\Psi}_0), \tag{28a}$$

$$\mathbf{x}(DT) = (\mathbf{I} - e^{\mathbf{A}T})^{-1}(\mathbf{\Phi}_1\mathbf{\Psi}_0 + \mathbf{\Psi}_1). \tag{28b}$$

The matrix $\mathbf{I} - e^{\mathbf{A}T}$ is nonsingular because the integrator has been excluded from the vector of the state variables $\mathbf{x}$ but has been included in the switching condition (19). Note that without excluding the integral variable from $\mathbf{x}$, the problem will be *ill-posed* and this matrix will be singular since the integral variable cannot reach a constant steady-state without closing the loop by the switching condition [16]. With the aim to avoid such an *ill-posedness* problem, in [15] and in other works by the same author

of [15], the pole of the integrator at the origin was replaced by a small pole δ hence hiding the effect of the integral action on the subharmonic oscillation boundary. Here, the nature of the integrator is maintained and its effect on this undesired phenomenon will be explicitly revealed for the case of the buck converter under V^1 control strategy.

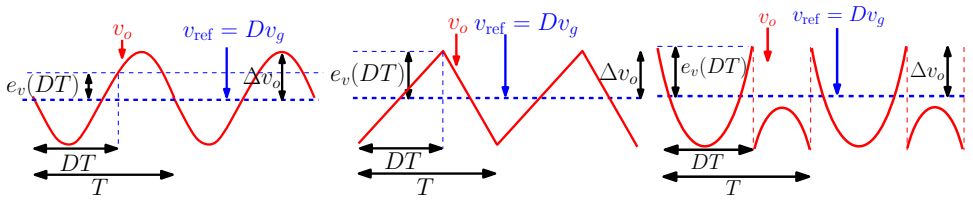
4.3. An analytical expression for multi-parametric prediction of subharmonic oscillation

Switching converters can exhibit many kinds of periodic orbits. In engineering applications of these systems, the fundamental $T-$periodic orbit is the only acceptable operation regime and hence its stability boundary has meticulously been investigated recently by many researchers [11, 20, 21]. While slow-scale low frequency stability boundaries can be detected by using an averaged approach, other fast-scale instabilities boundaries such as those corresponding to subharmonic oscillation are mainly due to the switching action which must be taken into account in order to predict this kind of instabilities. The determination of the boundary of this phenomenon can be tackled from several points of view. Although numerical approaches for multi-parameter stability boundary determination can be used to obtain the critical values of the parameters, it is more useful and more accurate to have an explicit expression for that purpose. Therefore, to accurately determine such boundaries, appropriate analytical methods must be used. Our purpose in this paper is to use an analytical matrix-form expression for predicting the stability limit of the system.

Let m_a be the slope of the ramp modulator signal $v_{\rm ramp}$. Following the same procedures as in [16], the boundary of subharmonic oscillation, as particularized for the buck converter considered in this study, is given by the following equality:

$$m_a \;=\; -\mathbf{C}^\intercal(\mathbf{I}+e^{\mathbf{A}T})^{-1}\mathbf{\Phi}_1(2\mathbf{A}\mathbf{x}(0)+(2\mathbf{B}_r+\mathbf{B})\mathbf{w})+W_i e_v(DT). \tag{29}$$

where $e_v(DT) = v_{\rm ref} - v_o(DT) = V_o - v_o(DT) = V_o - \mathbf{C}^\intercal\mathbf{x}(DT)$ is the voltage error at time instant DT and $\mathbf{x}(DT)$ and $\mathbf{x}(0)$ are given in (28a) and (28b) respectively. Derivation details are given in the appendix. Eq. (29) compresses all the parameters of the system in a single matrix-form boundary condition and can be solved for any system parameters. By neglecting the term $W_i e_v(DT)$ corresponding to the integral action in (29) we obtain the expression reported in [23] or [24] respectively. Below we demonstrate that the integral action and the associated term $W_i e_v(DT)$ have a negligible effect on the subharmonic oscillation boundaries and hence it can be dropped if only subharmonic oscillation is of concern.



(a) Ideal (b) Dominating ESR (c) Dominating ESL

Figure 3. Waveforms of the output voltage ripple of a buck converter. (a) Ideal with null or very small ESR and ESL, (b) Dominating ripple due to ESR. (c) Dominating ripple due to ESL.

4.4. The negligible effect of the integrator on subharmonic oscillation boundary in VMC

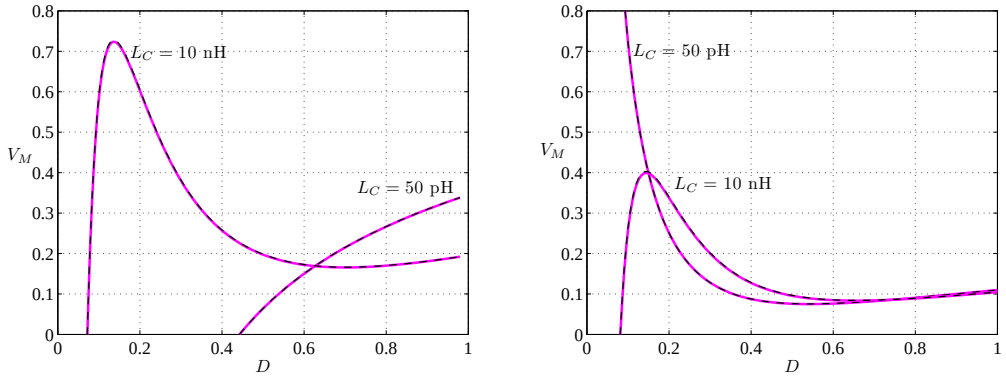
Fig. 3 shows the waveforms of the output voltage for the ideal case, with dominant ripple due to the ESR and with dominant ripple due to the ESL. In all cases, it can be observed that the upper bound of the term $e_v(DT)$ is the output voltage ripple Δv_o, i.e., $e_v(DT) < \Delta v_o$. In this paper, the ESL of the output capacitor is included in the model and the effect of this parasitic element will be studied. The analysis reported here is valid when the ESR of the output capacitor dominates its ripple and the ripple becomes triangular as well as when the ESL dominates this ripple showing a discontinuity of the output voltage at the switching instants. The output voltage ripple in the presence of an ESR and an ESL in the output capacitor can be approximated as follows [22]:

$$\Delta v_o \approx v_g \overline{D}(\alpha D + \beta). \tag{30}$$

where the coefficients α and β are given by:

$$\alpha := \frac{T}{L}\left(\frac{T}{8C} + R_C\right), \ \beta := \frac{L_C}{L} \tag{31}$$

Because in any practical design $L_C \ll L$, $T^2 \ll LC$ and $TR_C \ll L$, then $\alpha \ll 1$ and $\beta \ll 1$. Therefore, the ripple Δv_o is very small and since $e_v(DT) < \Delta v_o$, $e_v(DT)$ is also very small. Moreover, in V^1 control, $|W_{p1}| \gg W_i$ and $|W_{p2}| \gg W_i$ and therefore the term $W_i e_v(DT)$ can be neglected in (29) without a significant alteration of the results. This statement will be confirmed later in Section 5 by numerical simulations. Therefore, in V^1 control, like in all VMC schemes, the integral action has a negligible effect on the subharmonic oscillation boundary. A similar observation was reported in [13] based on a numerical study using the eigenvalues of the monodromy matrix.



(a) (b)

Figure 4. Stability boundary of the buck converter under V[1] (a) and conventional type-III (b) compensation designs. The boundaries obtained by ignoring the term corresponding to the integral action are also shown in dashed line but both lines are superimposed because they are practically identical.

5. Validation of the theoretical results by using a circuit-level switched model

Consider a buck converter under a V[1] control strategy. Let us use the same practical parameter values considered in [7]. These are: the desired output reference voltage $v_{\text{ref}} = 1.5$ V, inductance $L = 1.5$ μH, capacitance $C = 42$ μF, ESR of the capacitor R_C = 5 mΩ, switching frequency f_s = 300 kHz, $k_v = 1$, $k_i = 0.17$ Ω, output current $i_o = 8$ A ($R = 0.1875$ Ω) and $W_i = 21.23$ krad/s. In [7], the output capacitor ESL parasitic values were 50 pH and 1.2 nH in different tests. In this paper we sweep this parameter from 50 pH to 10 nH to reveal its effect on the behavior of the system. The subharmonic oscillation boundary is first studied in the parameter space (D, V_M) where $V_M = m_a T$ is the amplitude of the ramp modulator signal. The operating duty cycle D is varied by varying the input voltage v_g according to (25). To study the system under the V[1] control, the zeros and the poles are selected according to (8). Fig. 4 shows the subharmonic instability boundary from (29) for two different values of L_C. The stability area is above the curves. For low values of L_C, the stability boundary corresponding to V[1] control scheme is very similar to the one corresponding to a CMC for which a ramp modulator/compensator is needed only for duty cycle values larger than a certain critical value D_c. However, this critical value is no longer 0.5 as predicted by classical design in a pure CMC [25], but smaller and decreases when L_C increases hence implying a reduction of the stability region. For relatively large values of L_C, the ramp stabilizer is needed for almost all the range

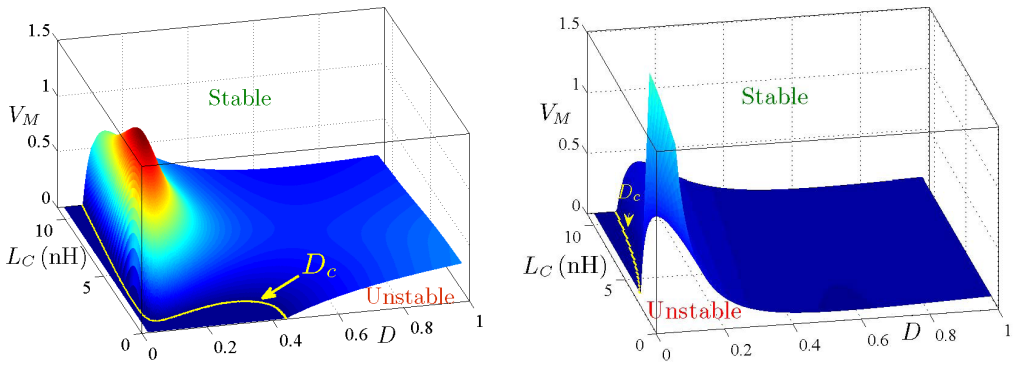
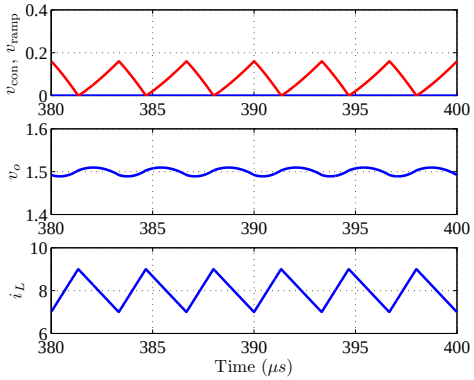


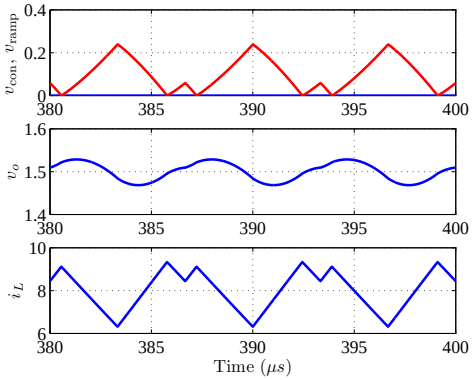
Figure 5. Stability boundary of the buck converter under V^1 (a) and conventional type-III (b) compensation designs by showing the effect of the ESL L_C on the stability boundary.

of duty cycles and the needed ramp slope could even be larger for smaller values of the operating duty cycles.

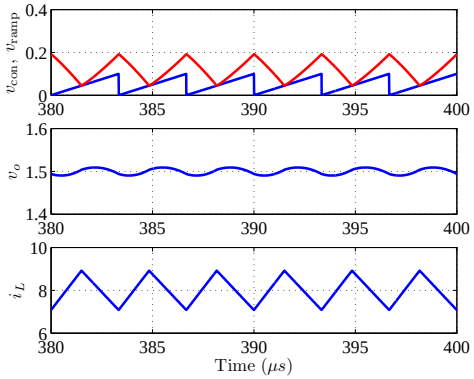
Fig. 5 shows a mesh plot of the stability region in the parameter space (D, L_C, V_M) where the critical duty cycle value D_c is also plotted in the plan (D, L_C). Compared to the conventional type-III compensation design with the same values of all other parameters, it can be observed that the converter with V^1 control design with relatively small values of L_C exhibits subharmonic oscillation only for duty cycles larger than a critical value D_c (depending on L_C) while the conventional type-III controller requires a ramp compensator for, practically, all the range of operating duty cycle values. When L_C increases, the boundary curves for both design methods are similar but the V^1 control design method requires less ramp amplitude. The dynamics of the system with V^1 control design has been checked by time-domain numerical simulations using a switched model implemented in PSIM© software and a good agreement was observed. First, let $L_C = 50$ pH (small). From Fig. 4, the converter is stable without ramp compensation ($m_a = V_M = 0$) if $D < 0.44$. Let $V_M = 0$ and $D = 0.4$. With these values of parameters, the converter is stable as predicted in Fig. 4 and confirmed by numerical simulations from the switched circuit-level model depicted in Fig. 6(a). Let $V_M = 0$ and $D = 0.45 < 0.5$. The converter exhibits subharmonic oscillation as predicted in Fig. 4 and confirmed by the numerical simulations shown in Fig. 6(b). Let $V_M = 0.1$ V and $D = 0.45$. The converter is stable as shown in Fig. 6(c). Now let $L_C = 10$ nH (large). Let $V_M = 0.6$ V and $D = 0.2$ the converter is stable as predicted in Fig. 4 and confirmed by numerical simulations from the switched circuit-level model depicted in Fig. 7(a). Let $V_M = 0.5$ V and $D = 0.2$, the converter exhibits subharmonic oscillation as



(a) $V_M = 0$, $D = 0.4$.



(b) $V_M = 0$, $D = 0.45$.



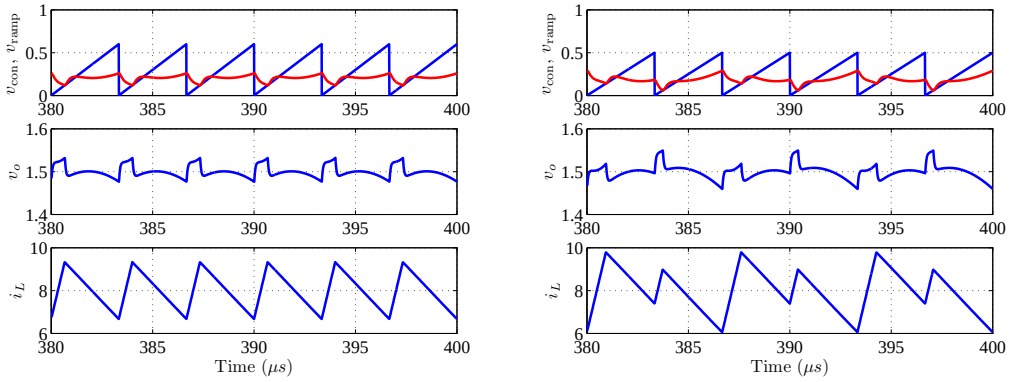
(c) $V_M = 0.1$ V, $D = 0.45$.

Figure 6. Time-domain waveforms using V[1] compensator for different values of D and V_M. L_C =50 pH.

predicted in Fig. 4 and confirmed by the numerical simulations shown in Fig. 7-b.

Appendix: derivation of subharmonic oscillation boundary for the buck converter under the V[1] control strategy

The content of this appendix is derived from the results presented in [16] by particularizing them for the case of the buck converter under the V[1] control strategy. Since we are concerned with in the occurrence of the first subharmonic oscillation boundary, consider the converter working under subharmonic regime with a $2T$-periodic orbit (see Fig. A-1). This behavior is normally characterized by



(a) $V_M = 0.6$ V, $D = 0.2$. (b) $V_M = 0.5$ V, $D = 0.2$.

Figure 7. Time-domain waveforms using V^1 compensator for $D = 0.2$ and different values of V_M. L_C =10 nH.

the exhibition, during two consecutive cycles in steady-state, of a narrow pulse, of duration $(D-\varepsilon_t)T$, and another wide pulse, of duration $(D+\varepsilon_t)T$, in the driving signal u and also in other related square-wave signals [16]. The parameter ε_t is a small quantity that vanishes at the onset of subharmonic oscillation. During two consecutive switching periods in the time interval $(0, 2T)$, let the crossing between the control signal $v_{\rm con}$ and the $T-$periodic signal $v_{\rm ramp}$ occurs at $t = (D-\varepsilon_t)T$ and at $t = (1+D+\varepsilon_t)T$ (see Fig. A-1). For the buck converter considered in this study, and during the switching cycle of duration T, the system has two phases defined by the system matrix pair $(\mathbf{A}, \mathbf{B}_1)$ and $(\mathbf{A}, \mathbf{B}_0)$ respectively, where $\mathbf{B}_1 = \mathbf{B}+\mathbf{B}_r$ and $\mathbf{B}_0 = \mathbf{B}$ while during a switching cycle of duration $2T$, the system has four phases defined by the matrix pair sequence $(\mathbf{A}, \mathbf{B}_1)$, $(\mathbf{A}, \mathbf{B}_0)$, $(\mathbf{A}, \mathbf{B}_1)$ and $(\mathbf{A}, \mathbf{B}_0)$ respectively. Exhibiting a $2T$-periodic regime, the sampled steady-state values of the state variables at the switching instants $(D-\varepsilon_t)T$ and $(1+D+\varepsilon_t)T$ can be obtained by using (14) and forcing $2T-$periodicity. In doing so, these values can be expressed as follows

$$\mathbf{x}((D-\varepsilon_t)T) = (\mathbf{I} - e^{2\mathbf{A}T})^{-1}\mathbf{\Psi}_-(\varepsilon_t) \quad \text{(A-1a)}$$

$$\mathbf{x}((1+D+\varepsilon_t)T) = (\mathbf{I} - e^{2\mathbf{A}T})^{-1}\mathbf{\Psi}_+(\varepsilon_t) \quad \text{(A-1b)}$$

where

$$\mathbf{\Psi}_-(\varepsilon_t) = \overline{\mathbf{\Phi}}_1\overline{\mathbf{\Phi}}_4\overline{\mathbf{\Phi}}_3\overline{\mathbf{\Psi}}_0 + \overline{\mathbf{\Phi}}_1\overline{\mathbf{\Phi}}_4\overline{\mathbf{\Psi}}_3 + \overline{\mathbf{\Phi}}_1\overline{\mathbf{\Psi}}_4 + \overline{\mathbf{\Psi}}_1 \quad \text{(A-2a)}$$

$$\mathbf{\Psi}_+(\varepsilon_t) = \overline{\mathbf{\Phi}}_3\overline{\mathbf{\Phi}}_0\overline{\mathbf{\Phi}}_1\overline{\mathbf{\Psi}}_4 + \overline{\mathbf{\Phi}}_3\overline{\mathbf{\Phi}}_0\overline{\mathbf{\Psi}}_1 + \overline{\mathbf{\Phi}}_3\overline{\mathbf{\Psi}}_0 + \overline{\mathbf{\Psi}}_3 \quad \text{(A-2b)}$$

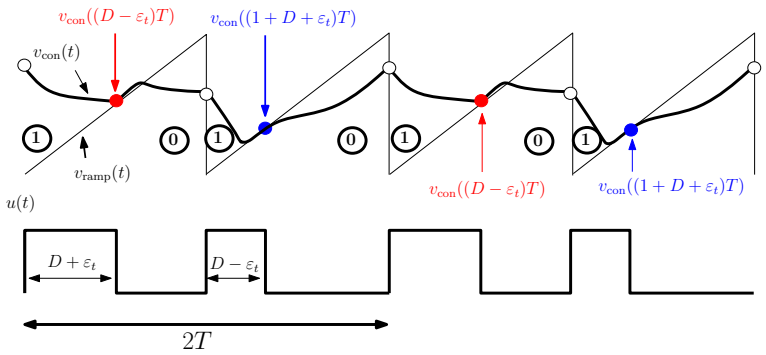


Figure A-1. The ramp signal $v_{\rm ramp}$, steady-state waveforms of the control signal $v_{\rm con}(t)$ and the driving signal u at $2T-$subharmonic regime for the buck converter under V^1 control strategy.

and

$$\overline{\mathbf{\Phi}}_1 = \mathbf{\Phi}_1 e^{-\mathbf{A}\varepsilon T},\ \overline{\mathbf{\Psi}}_1 = \int_0^{(D-\varepsilon_t)T} e^{\mathbf{A}\tau}\mathrm{d}\tau\mathbf{B}_1\mathbf{w} \tag{A-3a}$$

$$\overline{\mathbf{\Phi}}_0 = \mathbf{\Phi}_0 e^{\mathbf{A}\varepsilon T},\ \overline{\mathbf{\Psi}}_0 = \int_0^{(1-D+\varepsilon_t)T} e^{\mathbf{A}\tau}\mathrm{d}\tau\mathbf{B}_0\mathbf{w} \tag{A-3b}$$

$$\overline{\mathbf{\Phi}}_3 = \mathbf{\Phi}_1 e^{\mathbf{A}\varepsilon T},\ \overline{\mathbf{\Psi}}_3 = \int_0^{(D+\varepsilon_t)T} e^{\mathbf{A}\tau}\mathrm{d}\tau\mathbf{B}_1\mathbf{w} \tag{A-3c}$$

$$\overline{\mathbf{\Phi}}_4 = \mathbf{\Phi}_0 e^{-\mathbf{A}\varepsilon T},\ \overline{\mathbf{\Psi}}_4 = \int_0^{(1-D-\varepsilon_t)T} e^{\mathbf{A}\tau}\mathrm{d}\tau\mathbf{B}_0\mathbf{w} \tag{A-3d}$$

From the switching conditions at time instants $(D-\varepsilon_t)T$ and $(1+D+\varepsilon_t)T$, the following equalities hold:

$$-\mathbf{C}^\intercal\mathbf{x}((D-\varepsilon_t)T) + W_i x_i((D-\varepsilon_t)T) = v_{\rm ramp}((D-\varepsilon_t)T) \tag{A-4a}$$

$$-\mathbf{C}^\intercal\mathbf{x}((1+D+\varepsilon_t)T) + W_i x_i((1+D+\varepsilon_t)T) = v_{\rm ramp}((D+\varepsilon_t)T) \tag{A-4b}$$

Subtracting (A-4b) from (A-4a), one obtains:

$$-\mathbf{C}^\intercal(\mathbf{x}((1+D+\varepsilon_t)T)-\mathbf{x}((D-\varepsilon_t)T))+W_i(x_i((1+D+\varepsilon_t)T)-x_i((D-\varepsilon_t)T)) = 2m_a\varepsilon_t T \tag{A-5}$$

The expression (A-5) can be written as follows

$$m_{\rm cri}(D) = m_a \tag{A-6}$$

where $m_{\rm cri}(D)$ is the critical slope for subharmonic oscillation boundary given by

$$m_{\rm cri}(D) = -\lim_{\varepsilon_t\to 0}\frac{1}{2\varepsilon_t T}\mathbf{C}^\intercal(\mathbf{x}((1+D+\varepsilon_t)T)-\mathbf{x}((D-\varepsilon_t)T)) + m_I \tag{A-7}$$

where m_I is the term contributed by the integral variable and that can be expressed as follows:

$$m_I = W_i \lim_{\varepsilon_t \to 0} \frac{1}{2\varepsilon_t T} \int_{(D-\varepsilon_t)T}^{(1+D+\varepsilon_t)T} e_v(t)\mathrm{d}t = W_i e_v(DT). \quad \text{(A-8)}$$

On the other hand, by using (A-1a)-(A-1b), the limit expression in (A-7) becomes

$$m_{\mathrm{cri}}(D) = -\mathbf{C}^{\intercal}(\mathbf{I} - e^{2\mathbf{A}T})^{-1} \lim_{\varepsilon_t \to 0} \frac{1}{2\varepsilon_t T}(\mathbf{\Psi}_+(\varepsilon_t) - \mathbf{\Psi}_-(\varepsilon_t)) + W_i e_v(DT) \quad \text{(A-9)}$$

The difference $\mathbf{\Psi}_+(\varepsilon_t) - \mathbf{\Psi}_-(\varepsilon_t)$ can be arranged as follows

$$\begin{aligned} \mathbf{\Psi}_+(\varepsilon_t) - \mathbf{\Psi}_-(\varepsilon_t) &= \overline{\mathbf{\Phi}}_3\overline{\mathbf{\Phi}}_0\overline{\mathbf{\Phi}}_1\overline{\mathbf{\Psi}}_4 + \overline{\mathbf{\Phi}}_3\overline{\mathbf{\Phi}}_0\overline{\mathbf{\Psi}}_1 + \overline{\mathbf{\Phi}}_3\overline{\mathbf{\Psi}}_0 + \overline{\mathbf{\Psi}}_3 \\ &- \overline{\mathbf{\Phi}}_1\overline{\mathbf{\Phi}}_4\overline{\mathbf{\Phi}}_3\overline{\mathbf{\Psi}}_0 - \overline{\mathbf{\Phi}}_1\overline{\mathbf{\Phi}}_4\overline{\mathbf{\Psi}}_3 - \overline{\mathbf{\Phi}}_1\overline{\mathbf{\Psi}}_4 - \overline{\mathbf{\Psi}}_1 \quad \text{(A-10)} \end{aligned}$$

in such a way that the limit in (A-9) becomes as follows

$$\lim_{\varepsilon_t \to 0} \frac{1}{2\varepsilon_t T}(\mathbf{\Psi}_+(\varepsilon_t) - \mathbf{\Psi}_-(\varepsilon_t)) = \mathbf{\Phi}_1(2\mathbf{A}(\mathbf{\Phi}_0\mathbf{\Psi}_1 + \mathbf{\Psi}_0) + (\mathbf{I} - e^{\mathbf{A}T})(\mathbf{B_1} + \mathbf{B}_0)\mathbf{w}) \quad \text{(A-11)}$$

Using the expression of $\mathbf{x}(0)$ in (28a), the previous equation becomes

$$\lim_{\varepsilon_t \to 0} \frac{1}{2\varepsilon_t T}(\mathbf{\Psi}_+(\varepsilon_t) - \mathbf{\Psi}_-(\varepsilon_t)) = \mathbf{\Phi}_1((\mathbf{I} - e^{\mathbf{A}T}))(2\mathbf{A}\mathbf{x}(0) + (\mathbf{B_1} + \mathbf{B}_0)\mathbf{w}) \quad \text{(A-12)}$$

and the critical slope of the ramp modulator for exhibiting subharmonic oscillation is given by the following expression

$$m_{\mathrm{cri}}(D) = -\mathbf{C}^{\intercal}(\mathbf{I} - e^{2\mathbf{A}T})^{-1}(\mathbf{I} - e^{\mathbf{A}T})\mathbf{\Phi}_1(2\mathbf{A}\mathbf{x}(0) + (\mathbf{B_1} + \mathbf{B}_0)\mathbf{w}) + W_i e_v(DT) \quad \text{(A-13)}$$

Because $(\mathbf{I} - e^{2\mathbf{A}T})^{-1} = (\mathbf{I} + e^{\mathbf{A}T})^{-1}(\mathbf{I} - e^{\mathbf{A}T})^{-1}$, (A-13) can still be simplified as follows:

$$m_{\mathrm{cri}}(D) = -\mathbf{C}^{\intercal}(\mathbf{I} + e^{\mathbf{A}T})^{-1}\mathbf{\Phi}_1(2\mathbf{A}\mathbf{x}(0) + (2\mathbf{B}_r + \mathbf{B})\mathbf{w}) + W_i e_v(DT) \quad \text{(A-14)}$$

6. Conclusions

Subharmonic oscillation can be exhibited by DC-DC buck converters under the new V^1 control design approach. In this work, an exact expression for locating the stability limit in buck converters under this control strategy has been used to predict this undesired phenomenon. Generally speaking, the equivalent series inductance L_C of the output capacitor can reduce the stability region and it must be taken into account for accurate prediction of the system response. For low values of this parameter, the stability boundary corresponding to V^1 control scheme is very similar to the one associated with peak current mode control for which a ramp modulator/compensator is needed only for duty cycle values larger than a certain critical value of the operating duty cycle. However, this critical value is no longer

0.5 as predicted by a classical design approach [1, 25], but smaller and decreases when the parasitic parameter L_C increases. For relatively large values of L_C, the ramp compensator is needed for almost all the range of duty cycles and the needed ramp slope could even be larger for smaller values of the operating duty cycles. This work provides a convenient means of accurate analytical stability boundary determination of power buck converters under V^1 control for different applications and could help in selecting the parameter values of the system to avoid such undesired behavior in a practical design. As in all voltage mode control strategies, the integral action in the feedback loop is demonstrated to have a negligible effect on the subharmonic oscillation boundary. Notice also that the fixed frequency V^1 control concept can be adapted to be used with variable frequency modulation schemes like in V^2 control strategies [3, 5, 26]. The results presented here can be extended to these cases with a little additional effort.

Acknowledgments

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REFERENCES

1. R. W. Erickson and D. Maksimovic *Fundamentals of power electronics*. Lluwer, 2001.
2. K. Chen, P. Huang, and H. Ho, "Buck-boost power converter with feed-forward technique for achieving fast line response," Sep 16 2010, US Patent App. 12/720,022.
3. D. Goder and W. R. Pelletier, "V2 architecture provides ultra-fast transient response in switch power supplies," in Proc. HFPC Conf., 1996, pp. 19-23.
4. J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Transactions on Power Electronics,* vol. 21, no. 2, pp. 346-353, 2006.
5. R. Redl and J. Sun, "Ripple-based control of switching regulators: an overview," *IEEE Transactions on Power Electronics,* vol. 24 no. 12, pp. 2669-2680, 2009.
6. M. del Viejo, P. Alou, J. A. Oliver, O. García, J. A. Cobos, "V2IC control: a novel control technique with very fast response under load and voltage steps", *IEEE Applied Power Electronics Conference* APEC'll, 2011.
7. J. Cortes, V. Svikovic, P. Alou, J. Oliver, J. A. Cobos, "V^1 concept: designing a voltage mode control as current mode with near time-optimal response for Buck-type converters," *IEEE Transactions on Power Electronics,* vol. 30, no. 10, pp. 5829-5841, 2015.

8. Intersil, "Designing stable compensation networks for single phase voltage mode buck regulators," Technical Brief TB417.1. [Online]. Available: http://www.intersil. com/content/dam/Intersil/documents/tb41/tb417.pdf
9. P. Siewniak and B. Grzesik, "The piecewise-affine model of buck converter suitable for practical stability analysis," *International Journal of Circuit Theory and Applications* vol. 43, no. 1,pp. 3-21, 2015.
10. H. Zhang, Y. Zhang and X. Ma, "Dimensionless approach to multi-parametric stability analysis of nonlinear time-periodic systems: Theory and its applications to switching converters," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 60, no. 2, pp. 491-504, 2013.
11. J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, J. A. Cobos, R. Wisniewski, "Accurate analysis of subharmonic oscillations of V^2 and $V^2 I_c$ controls applied to buck converter," *IEEE Transactions on Power Electronics,* vol. 30, no. 2, pp. 1005-1018, 2015.
12. D. Giaouris, S. Banerjee, B. Zahawi, V. Pickert, "Stability analysis of the continuous-conduction-mode buck converter via Filippov's method," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 55, no. 4, pp. 1084-1096, 2008.
13. D. Giaouris, S. Maity, S. Banerjee, V. Pickert, and B. Zahawi, "Application of Filippov method for the analysis of subharmonic instability in DC-DC converters," *International Journal of Circuit Theory and Applications*, vol. 37, no. 8, pp. 899-919, 2009.
14. L. Wei-Guo, Z. Luo-Wei, L. Quan-Ming and W. Jun-Ke, "Non-invasive chaos control of DC-DC converter and its optimization," *International Journal of Circuit Theory and Applications* vol. 39, no. 2, pp. 159-174, 2011.
15. C.-C. Fang, "Instability Conditions for a Class of Switched Linear Systems With Switching Delays Based on Sampled-Data Analysis: Applications to DC-DC Converters," Nonlinear Dynamics, vol. 77, no. 1, pp. 185-208, 2014.
16. A. El Aroudi, A new approach for accurate prediction of subharmonic oscillation in switching regulators–part I: Mathematical derivations, *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5651-5651, July 2017.
17. A. El Aroudi, A., D. Giaouris, H.-C Iu, H., I. A. Hiskens,"A review on stability analysis methods for switching mode power converters," *IEEE J. on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 3, pp. 302–315, 2015.
18. L. Cheng, W.-H. Ki,, "A circuit-oriented geometrical approach in predicting subharmonic oscillation of DC-DC converters with voltage-mode control," *IEEE International Symposium on Circuits and Systems,* ISCAS'2014, pp. 962-965, 1-5 June, 2014.
19. D. J. Shortt, "The effect of capacitor equivalent series inductance on DC-DC converter performance and stability," *Fourth Annual IEEE Applied Power Electronics Conference and Exposition Conference Proceedings,* APEC'89, pp.136-142, 13-17, 1989.
20. B. Hayes, M. Condon and D. Giaouris, "Design of PID controllers using Filippov's method for stable operation of DC-DC converters," *International Journal of Circuit Theory and Applications,* vol. 44, no. 7 pp. 1437-1454, 2016.
21. M. Bradley, E. Alarcón and O. Feely, "Control of limit cycle oscillations in a multiple-sampled digitally controlled buck converter," *International Journal of Circuit Theory and Applications,* vol. 43, no. 6, pp. 691-708, 2015.
22. "Switching Regulator IC series: Capacitor Calculation for Buck converter IC," 2014, Application note No.14027ECY02, available at http://www.rohm.com.
23. A. El Aroudi, M. Al-Numay, J. Calvente, R. Giral, E. Rodriguez and E. Alarcón, "Prediction of subharmonic oscillation in switching regulators: From a slope to a ripple standpoint," *International Journal of Electronics,* vol. 103 , no. 12, pp. 2090-2109, 2016.
24. A. El Aroudi, "Prediction of subharmonic oscillation in switching converters under different control strategies," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 61, no. 11, pp. 910-914, 2014.
25. R. Redl and I. Novak, "Instabilities in current-mode controlled switching voltage regulators," in *IEEE Power Electronics Specialists Conference,* PESC'81, pp. 17–28, 1981.
26. T. Qian, "Subharmonic Analysis for buck converters with constant on-time control and ramp compensation," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 5, pp. 1780-1786, 2013.

27. K. J. Aström and B. Wittenmark. “Computer-control systems: Theory and design,” Prentice Hall, Englewood Cliffs, NJ, 3rd edition, 1997.