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Using low-cost microcontrollers to implement variable hysteresis-width comparators for switching power converters

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Abstract: Hysteretic comparators are often used to implement sliding-mode controllers or other type of discontinuous regulators for power switching converters. Their design is usually performed analogically yielding robust and fast controllers that can even allow converter operation with high values of duty cycle. A new analogue implementation based on a low-cost microcontroller is described in this study showing the mentioned advantages plus the flexibility of a programmable digital system. The proposed comparator employs some microcontroller peripherals without consuming execution time of the control algorithm and without requiring interruption management. It provides variable hysteresis width to obtain constant switching frequency in sliding-mode strategies and can be used in any type of hard switching converter. The dynamic performance of the method is verified experimentally in a boost converter-based rectifier with power factor correction and output voltage regulation in one single stage. The boost converter operates in sliding mode with constant switching frequency and results in a total harmonic distortion of the input current <1%.

1 Introduction

Hard switching self-oscillating converters are increasingly used nowadays due to the need of fast response in voltage regulator modules for microprocessors supply [1, 2], and because of the rapid penetration of sliding-mode control in the regulation of power converters [3].

Although sliding-mode control theory implies an infinite switching frequency operation, its practical implementation is carried out by means of a hysteresis comparator yielding a finite switching frequency that can be handled by the converter power devices with a high degree of efficiency. The resulting switching regulator is fast and robust, and exhibits a variable switching frequency. The last feature is a drawback when designing additional filters for the converter and when considering its capability of association in terms of interleaving or other forms of synchronisation [4, 5]. Reconciling sliding-mode control implementations and constant switching frequency is a well known research open problem as reported in [6], where sliding-mode-based pulse-width modulation (PWM) is attained through a dedicated discrete-time analysis of the system. Nonetheless, for a significant number of cases, the hysteresis implementation is the best solution and even the only alternative in certain designs requiring high values of duty cycle without risk of modulator saturation [7].

The hysteresis implementation is usually performed by means of analogue circuits resulting in an analogue controller of the power converter. A comparison on the equal basis of analogue and digital implementations for the same converters reveals that the analogue alternative requires a bigger number of active and passive components, which eventually lead to a reliability reduction and to an increment of the energy consumed and size of the controller [8]. Besides, it is difficult to modify the analogue control configuration because this implies changes in the hardware. Moreover, no complex controllers can be implemented analogically due to the limited mathematical operation capability of that type of configuration.

The previous limitations have constrained the sliding-mode control-based analogue implementations to relatively simple switching surfaces using in most of the cases linear combinations of few state variables plus proportional–integral (PI) compensators. Although this type of implementation is nowadays the only alternative for switching frequency designs above the radio-frequency band, the good performances of current digital processors make the digital approach a serious competitor of the analogue controllers for switching frequency operation in the region above the audio band up to 100 kHz. In addition to a higher capability for complex mathematical calculation, digital controllers exhibit intrinsic switching noise immunity and a great degree of versatility due to the possibility of reprogramming their control algorithms [9].

In the transition from analogue-to-digital (AD) implementations for switching frequencies above the audio band and below 100 kHz, the digital implementation of the hysteresis comparator plays a key role. A complete digital implementation of a hysteresis comparator has been reported in [10], wherein the compact and flexible configurations there described require powerful digital processors and peripherals. In a clear-cut contrast, the hysteresis comparator can be digitally approximated by predictive techniques at the expense of allowing less precision in the implementation [11].

An intermediate solution avoiding drawbacks of both analogue and digital approaches is a hybrid implementation. In this approach, converter references are digitally generated first and then analogically compared with the state variables. One of the first antecedents in the use of a hysteresis comparator hybrid implementation was reported in [12], wherein a scheme such as the one in Fig. 1*a* was used to regulate the output voltage of a boost converter by means of a two-loop control approach. A low-cost microcontroller established digitally the current reference for an inner current control loop employing an analogue hysteresis modulator. The 8-bit digital reference was transformed into an analogue signal by means of an external digital-to-analogue converter (DAC), and then compared with the inductor current by means of an analogue hysteresis circuit, which eventually provided the activation/deactivation signal to the power transistor driver.

Another solution for a hybrid implementation was reported in [13] and is illustrated in Fig. 1*b*. In that work, the need for complex references with a direct dependence on several input parameters

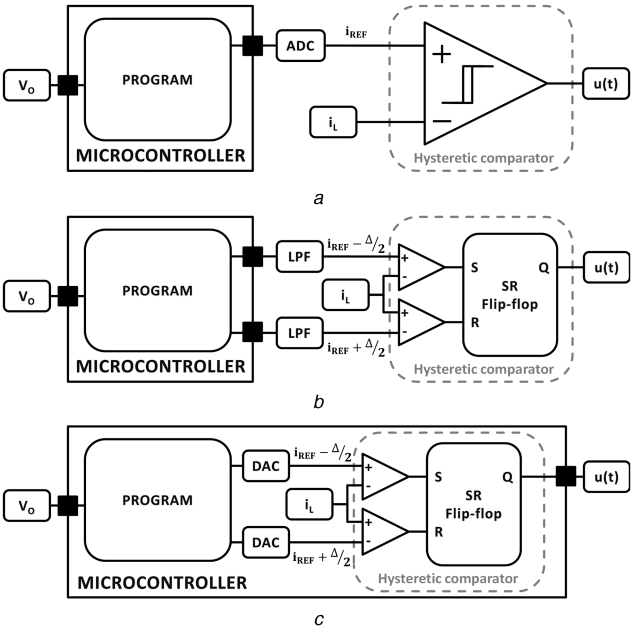


Fig. 1 *Different hybrid implementations*
(a) Analogue hysteretic comparator with a reference provided by the microcontroller, ***(b)*** Digital comparator with two low-pass filtered references provided by the microcontroller, ***(c)*** Fully integrated hysteretic comparator

justified the use of microcontrollers to generate the references. Also, each external DAC was substituted by the combination of a PWM peripheral and a low-pass filter. Since the circuit used two references, the hysteresis width could be tuned, and therefore the switching frequency could be fixed. However, an appropriate selection of the PWM switching frequency was required and a correct choice of the filter characteristics to optimise the bandwidth, filter delay, ripple and references precision.

It is worth mentioning that the hybrid solution employing two references that were reported in [14], which was based on an field-programmable gate array to generate the references to control a power converter operating at the very high switching frequency. Both references were sent time multiplexed to an external DAC to create indirectly a hysteresis effect in an analogue simple comparator. In particular, the upper reference value was sent to the comparator during the ON state to establish the switching to OFF state, while the lower reference value was similarly used to establish the transition from OFF to ON.

Moreover, an interesting approach based on low-cost microcontrollers was presented in [15], where two fully integrated hybrid hysteretic comparator configurations were reported. One configuration uses two internal comparators to trigger interrupt service routines that modify properly the digital output connected to the driver. This solution implies a significant consumption of execution time and has a slow time response. The other configuration is based on Fig. 1*c* and consists of an asynchronous operation of the PWM module, which eventually leads to an SR bistable scheme. The resulting bistable is activated by two internal analogue comparators and behaves such as an analogue hysteresis comparator. The method does not require additional external devices and is fast and reliable. Besides, since it almost consumes zero execution time, the saved time can be employed for other purposes.

This paper is focused on a hybrid approach describing an analogue implementation of a hysteresis comparator employing a low-cost microcontroller. The proposed comparator is based on the architecture of Fig. 1*c* and its main goal is to obtain a variable hysteresis width in order to implement sliding-mode control strategies with constant switching frequency. Note that so far variable hysteresis width has been successfully employed in the mitigation of zero-crossing distortion in power factor correction (PFC) by means of an analogue implementation that appropriately modulates the mentioned width, so that it tends to zero when the input voltage does [16, 17]. On the other hand, it has to be pointed out that variable hysteresis-width operation has been the subject of recent works in power converters, because it combines the rapid response of hysteresis comparators with a predicted spectral behaviour that can facilitate the design of additional filters. In this sense, it is worth mentioning the work dealing with three-phase system reported in [18]. There, the hysteresis width used in each phase leg of a voltage source inverter is modulated by its corresponding average output voltage and subsequently tuned to synchronise the zero crossings of the phase-leg current errors with a fixed reference clock signal.

The main antecedent of this paper is found in the work reported in [14], where a buck converter in DC–DC operation is controlled by means of a three-loop regulation scheme. The first loop or internal loop is built analogically to regulate the output capacitor current by means of a hysteresis comparator. The second loop regulates digitally the output voltage by modifying the two levels of the comparator hysteresis band of the first loop. Finally, the third loop regulates the switching frequency by measuring it and forcing its actual value to the desired reference by means of a PI compensator that also modifies the mentioned two levels of the comparator.

The work here reported is focused on the regulation of a boost converter for AC–DC operation with unity power factor using also a three-loop control approach. The purpose of the first loop is to guarantee a unity power factor operation by imposing a sliding regime, whose practical implementation requires the use of a hysteresis comparator. The goal of the second loop is regulating the output voltage by modifying the value of the reference current in the hysteresis comparator of the internal loop. Finally, the design of the third loop is totally decoupled from the previous loops, because the hysteresis width is only modified in this loop to ensure a constant switching frequency unlike the case in [14], where the width is modified by the action of both second and third loops.

The rest of this paper is organised as follows. The proposed solution is described in detail in Section 2 together with a verification test of the comparator performance. A boost converter-based rectifier with PFC and output voltage regulation in a single stage is used to illustrate the advantages of the method in Section 3, and the corresponding analysis is performed in Section 4. Experimental results are shown in Section 5, and finally conclusions are given in Section 6.

2 Hysteresis hybrid implementation

The fully integrated hysteretic comparator of Fig. 1*c* is used to control a power converter as shown in Fig. 2, where the organisation of the microcontroller internal peripherals illustrates the method of implementing the SR bistable. The implementation requires a microcontroller with two comparators and one PWM module, and can be directly adapted to a large number of low-cost devices of families PIC24, dsPIC30 and dsPIC33 from Microchip [19].

The power converter in Fig. 2 is controlled through a sliding surface given by expression (1), where $f_f(x_i)$ is an analogue signal that is a function of the converter fast variables x_i while $g_s(x_j)$ is the output of a zero-order hold (ZOH) and is a function of the slow variables x_j. The first function enters into the microcontroller through port CMP_x and the second one is internally calculated

$$S(x) = f_f(x_i) - g_s(x_j) \tag{1}$$

The control law is given by

$$\left.\begin{aligned} u = 0 \quad \text{if} \quad S(x) > \frac{\Delta}{2} \\ u = 1 \quad \text{if} \quad S(x) < -\frac{\Delta}{2} \end{aligned}\right\} \tag{2}$$

where Δ is the hysteresis width.

The first implication in the previous law is performed by resetting the PWM_x output, i.e. by activating the PWM fault mode, which will force the output value to zero. Conversely, the second

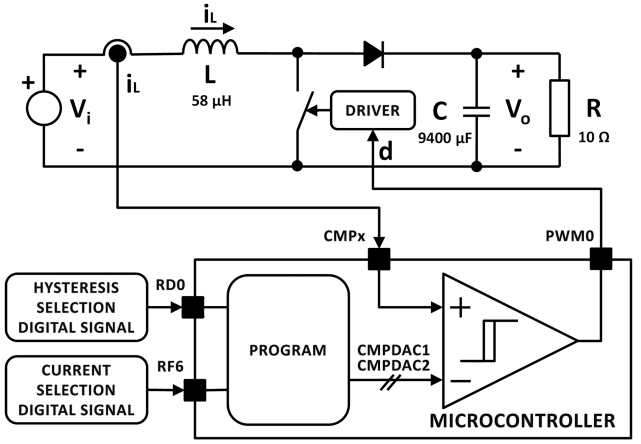


Fig. 2 *Block diagram of a generic hysteresis-based control of a power converter employing a microcontroller and description of the SR flip-flop*

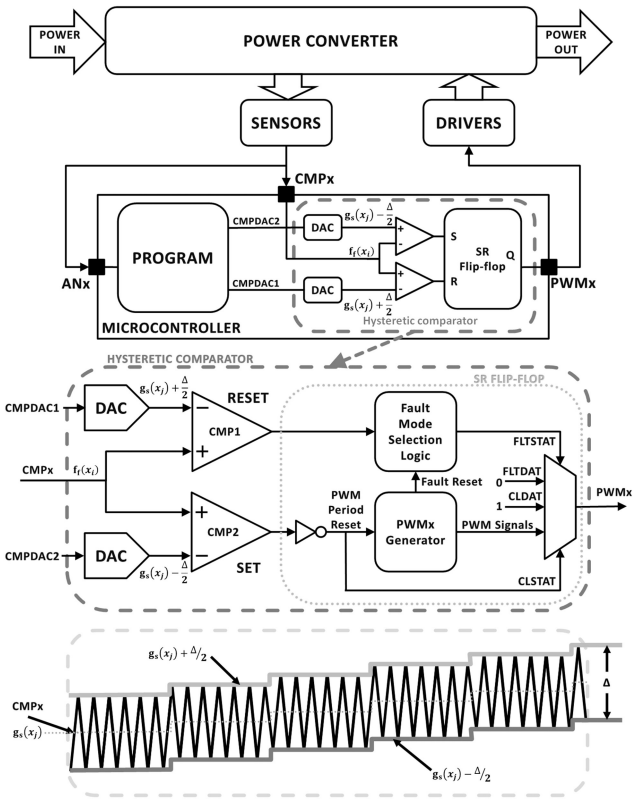


Fig. 3 *Hysteresis control based on microcontroller of the inductor current of a boost converter*

implication is performed by activating the current limit mode, which will set the PWM$_x$ output, reset the PWM counter and deactivate the PWM fault mode. A third implication requires no changes in the control action and corresponds to the case, in which the surface is within the hysteresis limits. The result of (2) is an analogue hysteresis comparator, in which the continuous-time signal entering through pin CMP$_x$ has to evolve between the bounds given by CMPDAC1 and CMPDAC2, which are digitally generated by the microcontroller. Thus, the reference signal $g_s(x_j)$ and the hysteresis width Δ can be easily modified, because they are, respectively, the mean value and the difference between the mentioned bounds as illustrated at the bottom of Fig. 2.

The microcontroller hysteresis implementation requires a peripheral initialisation, which implies the introduction of the appropriate initial values in the peripheral registers. After initialisation, executing the programme for the hysteresis implementation only requires updating the registers associated to CMPDAC1 and CMPDAC2 whenever a change either in reference $g_s(x_j)$ or in the hysteresis width Δ occurs. This results in a negligible time-consumed in the programme, so that most of the execution time can be devoted to other tasks.

Next, a practical validation of the previous procedure is performed in a single-boost converter, which is controlled by the inductor current. Two current references and two hysteresis width are considered. Fig. 3 shows the corresponding block diagram, where RF6 is a digital input to choose the average value of the inductor current. Ripple and switching frequency are established through digital input RD0. The microcontroller establishes the values for registers CMPDAC1 and CMPDAC2 once the current average value and hysteresis width are defined. The sensed inductor current enters into the microcontroller through CMP$_x$ pin.

The experimental results for four different sets of CMPDAC1 and CMPDAC2, i.e. (2300, 1800); (2450, 1650); (1350, 550); and (1200, 700) mA, are depicted in Fig. 4, where it can be observed the corresponding changes in the switching frequency and the value of the current in the equilibrium point. It can be observed in the oscilloscope captures the current inductor, output of the hysteresis comparator activating the switch driver, and the reference current. It is worth mentioning that the inductor current remains in the hysteresis band. It has to be pointed out that the current evolves between references CMPDAC1 and CMPDAC2 and that the response to a reference change is practically instantaneous.

Fig. 5*a* shows the scheme of an analogue hysteresis comparator based on the dual comparator LM319 and flip-flop CD4027, and a microcontroller based comparator, which provides the driver activation signals $u_a(t)$ and $u_m(t)$, respectively. The response of both comparators to an input step-type waveform $S(x(t))$ is illustrated in Fig. 5*b*, where it can be appreciated that both responses exhibit a similar delay of around 90 ns and similar rise time.

3 Sliding-mode-based PFC

Once that the microcontroller based hysteresis comparator has been proved to be an effective alternative to the analogue implementation, the digital version is now applied in the design of PFC in a full-bridge rectifier loaded by a boost converter as illustrated in Fig. 6. The goal of the design is to obtain a unity power factor at the input port of the converter and a DC-regulated voltage at its output port. Different solutions are considered, based on variable and constant switching frequency, for a prototype of 50 W with a regulated output voltage of 48 V, which is supplied by an input voltage of 24 V$_{rms}$ at 50 Hz. A notch filter is employed to suppress the first harmonic of the inductor current.

The controller action $u(t)$ is provided by the combination of a conventional two-loop regulation scheme [6, 7, 11, 12, 20, 21], and an additional third loop to control the hysteresis width. In the conventional part, an internal loop controls the inductor current through the hysteresis comparator, whose corresponding inputs are the inductor current $i_L(t)$ and the reference current $i_{ref}(t)$, which is modified by the hysteresis width in an additive or subtractive way. These two signals are the respective outputs of two ZOH systems, wherein the sample and hold are performed during $T_s = 1/f_s = 10$ μs. The corresponding input of each ZOH is the discretised reference current $i_{ref}(kT_s)$ plus (or minus) the discretised hysteresis width $\Delta(kT_s)/2$. The discretisation of the hysteresis width allows operating with the constant or variable width depending on the regulation objectives.

An external loop allows the PFC and establishes the reference $i_{ref}(kT_s)$ for the internal control loop. The PFC is carried out by equalling $i_{ref}(kT_s)$ and $g_a(kT_s)\cdot v_i(kT_s)$ in order to ensure proportionality at the converter input port between voltage and current. Thus, the converter will behave such as a loss-free resistor imposed by the sliding-mode control [20, 22]. The proportionality factor $g_a(kT_s)$ is also used to indirectly control the converter output voltage $v_o(kT_s)$. With this aim, the output voltage error with respect to the desired value is processed by a discrete-time PI controller in cascade with a digital filter with transfer function $H(z)$. As shown in Fig. 6*b*, this filter holds the value of an input sample of $g(kT_s)$ during the $N-1$ following samples ($N = fs/fo$ and $fo = 50$ Hz) and neglects the corresponding input samples in that interval. Thus,

$g_a(kT_s)$ is constant during each grid period assuring a perfect proportionality between input voltage and current.

The third loop employs a feed-forward control to establish the hysteresis-width reference $\Delta_1(kT_s)$. This reference is obtained using the values of input and output voltages $v_i(kT_s)$ and $v_o(kT_s)$, and the desired switching period $T_{sw\_ref}(kT_s)$. The influence of uncertainty, non-linearity and tolerances on the feed-forward performance is mitigated by adding a feedback path with an integrator.

4 Analysis of the proposed example

The boost converter in CCM is a variable structure system and two sets of state equations are required to model it. The first set describes the ON topology, when the controllable switch is active, and the second set is devoted to the OFF state, when the diode is conducting. Both equation sets can be combined into a single one (3) using the control variable $u(t)$, so that $u = 1$ during T_{ON} and $u = 0$ during T_{OFF}

$$\begin{aligned}\frac{\mathrm{d}i_L}{\mathrm{d}t} &= -\frac{v_o}{L}(1-u)+\frac{v_i}{L}\\ \frac{\mathrm{d}v_o}{\mathrm{d}t} &= \frac{i_L}{C}(1-u)-\frac{v_o}{RC}\end{aligned} \tag{3}$$

The first control loop assures a near unity power factor by imposing to the inductor current $i_L(t)$ a sliding regime given by (4), where $i_{ref}(t)$ is the output of a ZOH, whose input $i_{ref}(kT_s)$ is proportional to $v_i(kT_s)$ as shown in Fig. 6

$$S(x) = i_L - i_{ref}(t) = 0 \tag{4}$$

$$S(x)\cdot\frac{\mathrm{d}S(x)}{\mathrm{d}t} < 0 \tag{5}$$

Assuming that the sliding existence condition (5) is satisfied, the equivalent control $u_{eq}(t)$ forcing the system to evolve on the surface (4) can be obtained from (6) by imposing $\mathrm{d}S(x)/\mathrm{d}t = 0$

$$\left.\begin{aligned}\frac{\mathrm{d}i_L}{\mathrm{d}t} &= -\frac{v_o}{L}(1-u)+\frac{v_i}{L}\\ \frac{\mathrm{d}S(x)}{\mathrm{d}t} &= \frac{\mathrm{d}i_L}{\mathrm{d}t}-\frac{\mathrm{d}i_{ref}(t)}{dt}=0\end{aligned}\right\} \Rightarrow u(t) = 1-\frac{v_i}{v_o}+\frac{L}{v_o}\cdot\frac{\mathrm{d}i_{ref}(t)}{\mathrm{d}t} \tag{6}$$

The equilibrium point (7) is obtained imposing steady-state conditions on the converter equation set (3) using the previous control signal (6). As the inductor current $i_L(t)$ is forced to track $i_{ref}(t)$, the remaining ideal sliding dynamics (8) corresponds to the output capacitor voltage $v_o(t)$

$$X^* = (I_Q, V_{oQ}) = \left(I_{refQ}, \sqrt{V_{iQ}RI_{refQ}}\right) \tag{7}$$

$$\begin{cases} i_L = i_{ref}(t)\\ g(x) = \dfrac{\mathrm{d}v_o}{\mathrm{d}t} = \dfrac{1}{C}i_{ref}(t)\cdot\left[\dfrac{v_i}{v_o}-\dfrac{L}{v_o}\dfrac{\mathrm{d}i_{ref}(t)}{\mathrm{d}t}\right]-\dfrac{v_o}{RC}\end{cases} \tag{8}$$

Since the ideal sliding dynamics is non-linear, expression $g(x)$ must be linearised around the equilibrium point X^*, as seen in (9) in

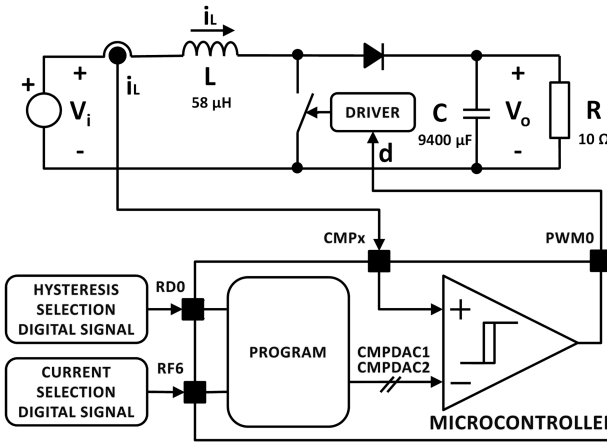
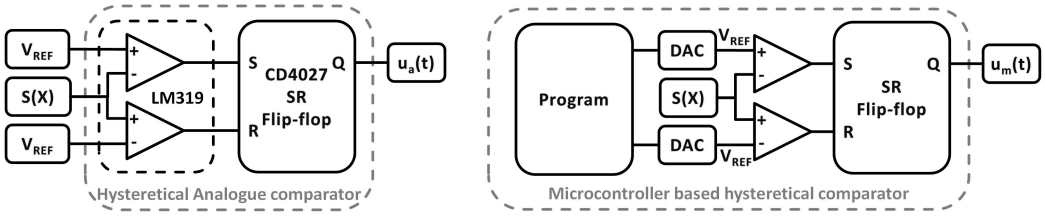
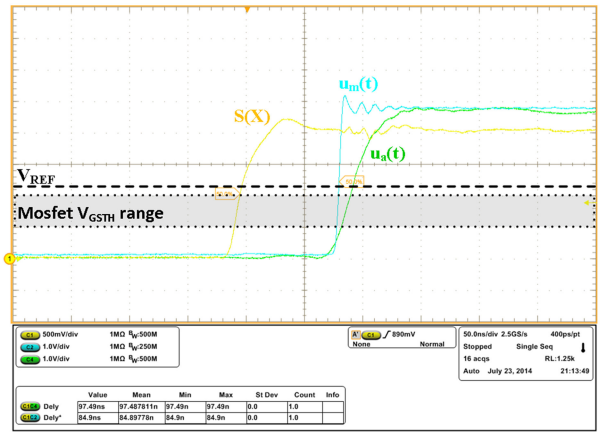


Fig. 4 *Waveforms illustrating a change of switching frequency and equilibrium point current produced by a variation of hysteresis width and reference current*



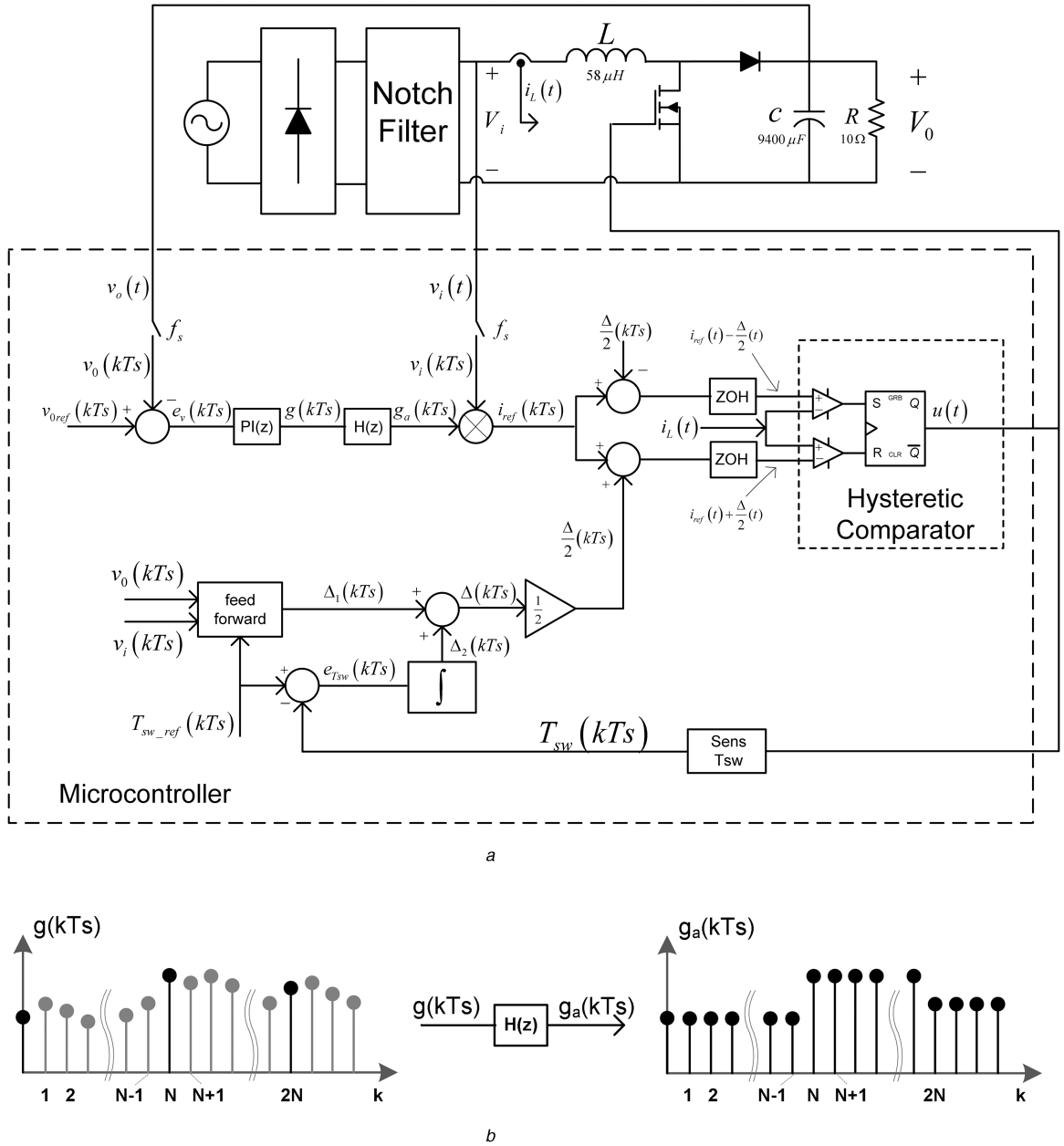
a



b

Fig. 5 *Analogue and microcontroller based hysteresis comparators comparison*

(a) Analogue and microcontroller based hysteresis comparators scheme, ***(b)*** Responses of analogue and microcontroller based hysteresis comparators to a step-type signal and gate-source voltage threshold range for a 5 V gate metal–oxide–semiconductor field-effect transistor



a

b

Fig. 6 *Sliding-mode control-based PFC in a boost converter using the proposed hysteretic controller with regulated switching frequency*
(a) Block diagram, ***(b)*** Input and output discrete-time sequences in filter $H(z)$ showing its sample–hold behaviour

order to design the output voltage controller using linear techniques. The linearised-model coefficients set $\{a, b, c, d\}$ are given in (10)

$$g(x) = \frac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} \simeq a \cdot \hat{i}_\mathrm{ref}(t) + b \cdot \hat{v}_\mathrm{i}(t) + c \cdot \hat{v}_\mathrm{o}(t) + d \cdot \hat{f}(t), \quad \text{where } f(t) = \frac{\mathrm{d}i_\mathrm{ref}(t)}{\mathrm{d}t} \tag{9}$$

$$a = \left.\frac{\partial g(x)}{\partial i_\mathrm{ref}}\right|_{X^*} = \frac{1}{C}\sqrt{\frac{V_\mathrm{i}Q}{RI_{\mathrm{ref}Q}}}, \quad b = \left.\frac{\partial g(x)}{\partial v_\mathrm{i}}\right|_{X^*} = \frac{1}{C}\sqrt{\frac{I_{\mathrm{ref}Q}}{RV_{\mathrm{i}Q}}}$$
$$c = \left.\frac{\partial g(x)}{\partial v_\mathrm{o}}\right|_{X^*} = -\frac{2}{RC}, \quad d = \left.\frac{\partial g(x)}{\partial f}\right|_{X^*} = -\frac{L}{C}\sqrt{\frac{I_{\mathrm{ref}Q}}{RV_{\mathrm{i}Q}}} \tag{10}$$

Applying the Laplace transform, the first loop is finally modelled by means of two small-signal first-order transfer functions $H_{\mathrm{ci}}(s)$ and $H_{\mathrm{cv}}(s)$ with a stable pole at $s = -2/\mathrm{RC}$. Note that only $H_{\mathrm{ci}}(s)$ is required to design the voltage regulation loop as shown in Fig. 7

$$H_{\mathrm{ci}}(s) = \frac{\hat{V}_\mathrm{o}(s)}{\hat{I}_\mathrm{ref}(s)} = \frac{a + ds}{s - c}, \quad H_{\mathrm{cv}}(s) = \frac{\hat{V}_\mathrm{o}(s)}{\hat{V}_\mathrm{i}(s)} = \frac{b}{s - c} \tag{11}$$

Fig. 7 shows the voltage regulation loop. In this figure, the gain $V_{\mathrm{i}Q}$ models the effect of the multiplier as shown in Fig. 6, $H_{\mathrm{ci}}(z)$ is the discretised transfer function previously obtained, PI(z) is a PI controller and $H(z)$ is the digital filter as shown in Fig. 6*b*

$$H_{\mathrm{ci}}(z) = \frac{\hat{V}_\mathrm{o}(z)}{\hat{I}_\mathrm{ref}(z)} = Z\left\{\left[L^{-1}\left(\frac{(1-\mathrm{e}^{-T_\mathrm{s}})}{s}\cdot H_{\mathrm{ci}}(s)\right)\right]\Big|_{t=kT_\mathrm{s}}\right\}$$
$$= \frac{1 - \left((a/c)\left(1-\mathrm{e}^{-cT_\mathrm{s}}\right) + d\right)\cdot z^{-1}}{1 - \mathrm{e}^{-cT_\mathrm{s}}z^{-1}} \tag{12}$$

$$\mathrm{PI}(z) = \frac{\hat{G}(z)}{\hat{E}_\mathrm{v}(z)} = \frac{K_1 + K_2 \cdot z^{-1}}{1 - z^{-1}} \tag{13}$$

The Z-transform of the signal $g_a(kT_S)$ represented in Fig. 6*b* will be given by

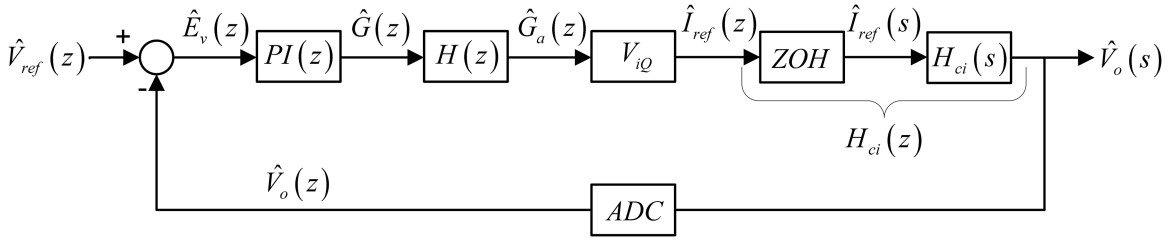


Fig. 7 *Voltage regulation loop*

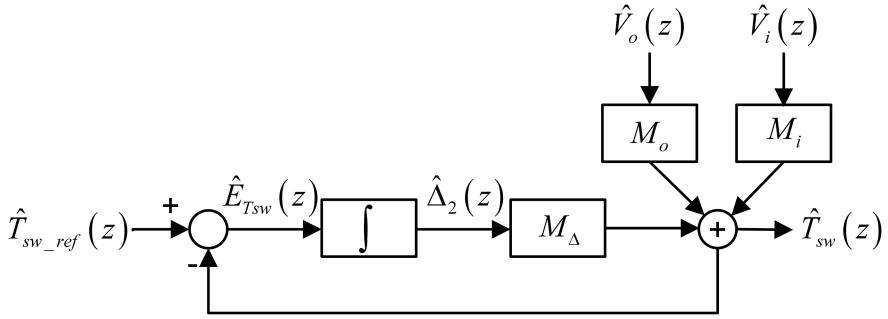


Fig. 8 *Switching period regulation loop*

$$\begin{aligned}\hat{G}_a(z) &= g(0)(1+z^{-1}+z^{-2}+z^{-3}+\cdots+z^{-(N-1)})\\ &+g(N)z^{-N}(1+z^{-1}+z^{-2}+z^{-3}+\cdots+z^{-(N-1)})\\ &+g(2N)z^{-2N}(1+z^{-1}+z^{-2}+z^{-3}+\cdots+z^{-(N-1)})\\ &+\cdots+ =\frac{1-z^{-n}}{1-z^{-1}}(g(0)+g(N)z^{-N}+g(2N)z^{-2N}+\cdots)\end{aligned} \tag{14}$$

It can be observed in (14) that the second factor is the Z-transform of a signal $g_{\text{int}}(kT_s)$ that is obtained by N-order decimation of $g(kT_s)$ [23, 24]. Therefore, signal $g_{\text{int}}(kT_s)$ can be expressed as

$$g_{\text{int}}(kT_s) = g(kT_s)\sum_{n=-\infty}^{n=\infty}\delta((k-nN)T_s) \tag{15}$$

where $\delta(\,.\,)$ stands for Kroneker's delta.

It has to be pointed out that the lower limit in the sum is $-\infty$ because $g(kT_s)$ represents the samples of a periodic signal defined in the interval $(-\infty,\infty)$.

On the other hand, expression (15) can be also represented as follows:

$$g_{\text{int}}(kT_s) = g(kT_s)\frac{1}{N}\sum_{n=0}^{N-1} w_N^{-nk}, \quad \text{where} \quad w_N = e^{-j(2\pi/N)} \tag{16}$$

Therefore, (14) can be rewritten as

$$\hat{G}_a(z) = \frac{1-z^{-N}}{1-z^{-1}}Z\{g_{\text{int}}(kT_s)\} \tag{17}$$

Besides

$$\begin{aligned}Z\{g_{\text{int}}(kT_s)\} &= \sum_{k=0}^{\infty}\left(g(kT_s)\frac{1}{N}\sum_{n=0}^{N-1}w_N^{-nk}\right)z^{-k}\\ &= \frac{1}{N}\sum_{n=0}^{N-1}\sum_{k=0}^{\infty}g(kT_s)(w_N^{-n}z)^{-k} = \frac{1}{N}\sum_{n=0}^{N-1}\hat{G}(w_N^{-n}z)\end{aligned} \tag{18}$$

where $\hat{G}(z)$ is the Z-transform of the discrete-time signal $g(kT_s)$.

Finally

$$\hat{G}_a(z) = \frac{1-z^{-N}}{1-z^{-1}}\cdot\frac{1}{N}\sum_{n=0}^{N-1}\hat{G}(w_N^{-n}z) \tag{19}$$

It can be observed that a rational function relating $\hat{G}_a(z)$ and $\hat{G}(z)$ cannot be derived from (19), so that no transfer function $H(z)$ can be used to describe the filtering action. As a consequence, the design of the PI is not straightforward. The selection of the controller parameters is simplified by approximating the filtering action by that of an equivalent low-pass filter $H_{\text{eq}}(z)$ using an iterative process. This is carried out by comparing the frequency response of expression (19) with that of a digital low-pass filter given by expression (20) until an acceptable bandwidth for control purposes is obtained

$$\hat{G}_a(z) = \hat{G}(z)H_{\text{eq}}(z) \tag{20}$$

The switching frequency regulation loop is shown in Fig. 8. The switching period T_{sw} of a boost converter controlled using a comparator with a hysteresis band Δ is given by (21). The feed-forward block in Fig. 6*a* calculates the theoretical hysteresis band Δ_1 for a given switching period reference $T_{\text{sw\_ref}}$ as expressed in (22)

$$T_{\text{sw}} = T_{\text{on}} + T_{\text{off}} = \frac{\Delta\cdot L}{V_{\text{i}}} + \frac{\Delta\cdot L}{V_{\text{i}}-V_{\text{o}}} \tag{21}$$

$$\Delta(kT_s) \simeq T_{\text{sw\_ref}}(kT_s)\cdot\frac{V_{iQ}(kT_s)\left[V_{iQ}(kT_s)-V_{oQ}(kT_s)\right]}{L\cdot\left[2V_{iQ}(kT_s)-V_{oQ}(kT_s)\right]} = \Delta_1 \tag{22}$$

(kT_s)

Nevertheless, external perturbations and inductor non-linearities can cause a substantial switching period error that must be compensated by means of the third loop as illustrated in Fig. 8. In fact, the feed-forward block gives a value Δ_1, which is used to reduce the time required by the third-loop integrator to cancel the switching period error. From expression (22), a small-signal model is derived in (23) and eventually used in the switching period regulation loop of Fig. 8. The closed-loop transfer function is given by (24)

$$M_\Delta = \left.\frac{\partial T_{\text{SW}}}{\partial\Delta}\right|_Q = \frac{L\cdot(2V_{iQ}-V_{oQ})}{V_{iQ}(V_{iQ}-V_{oQ})} \tag{23}$$

$$\frac{\hat{T}_{\text{sw}}(z)}{\hat{T}_{\text{sw\_ref}}(z)} = \frac{M_\Delta}{(M_\Delta+1)-z^{-1}}, \quad \text{where} \quad \frac{\hat{G}(z)}{\hat{E}_{\text{v}}(z)} = \frac{1}{1-z^{-1}} \tag{24}$$

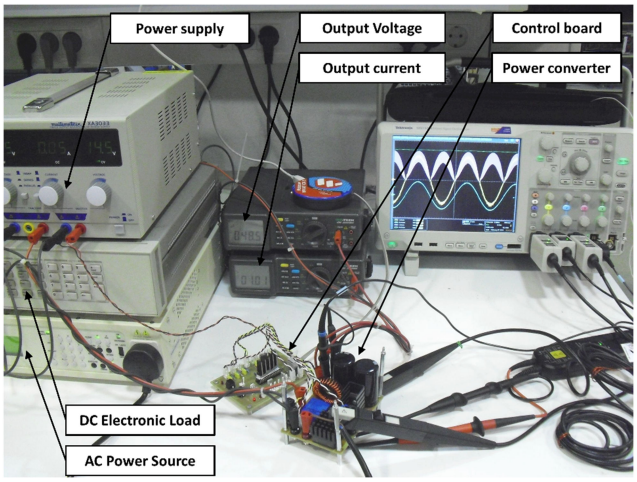


Fig. 9 *Experimental prototype and workbench*

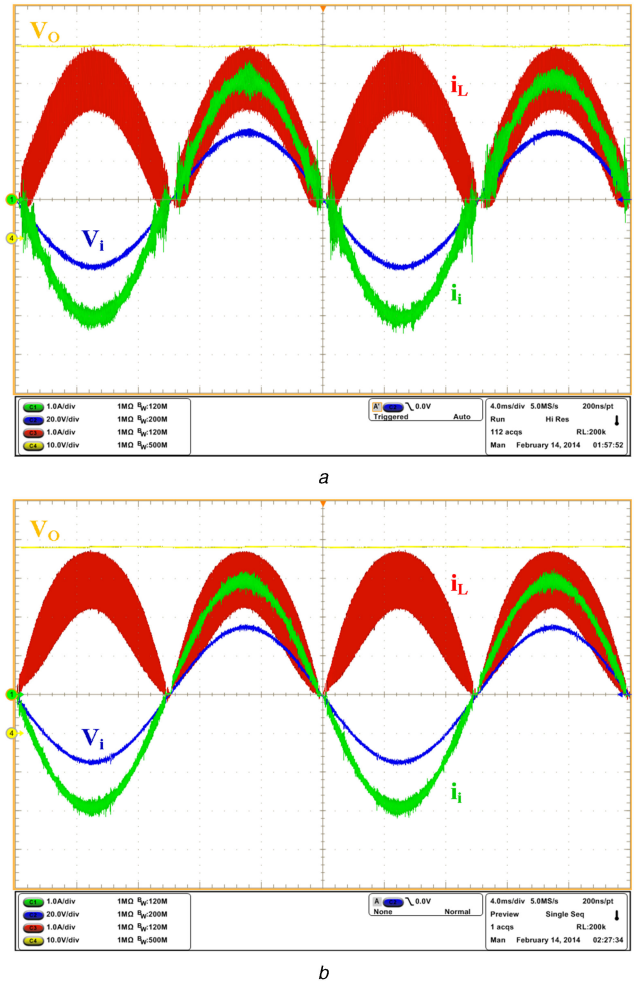


Fig. 10 *Experimental waveforms*

(a) Case 1: Measured reference and constant hysteresis width, ***(b)*** Case 4: Ideal stored reference and variable hysteresis width

Finally, note that the effective hysteresis band is the result of adding algebraically to the constant value given by (22) the corresponding corrections introduced by the switching period regulation loop.

5 Experimental results

Fig. 9 shows the workbench employed to validate the experimental prototype for the PFC system described in the block diagram of Fig. 6. The boost converter is close to the control board that contains the microcontroller dsPIC30F2020. The converter AC input voltage is 24 V_{rms}, which is supplied by an AC Pacific 118-ACX-UPC1 source. The converter output supplies an electronic load HP 6060B, which has been adjusted to absorb 1 A. Additional supply for the system circuitry is provided by a Multimetrix XA3033 source. Measurements in time and frequency domains depicted in Figs. 10 and 11, respectively, have been captured by a Tektronix MSO5204 oscilloscope. Input current and inductor current have been obtained by means of a Tektronix TCP0030 current probe, whereas input and output voltages have been measured with a high-voltage differential probe THDP0200 and a passive voltage probe TPP1000, respectively.

Table 1 summarises the experimental results in terms of power factor and total harmonic distortion (THD) in four cases. The first one corresponds to a constant hysteresis width and employs the reference $v_i(kT_s)$ provided by the AD converter to track the sinusoidal input signal. In the second case, the hysteresis width is also constant but the tracking uses a reference $v_i(kT_s)$ provided by the microcontroller, which has stored an ideal sinusoidal signal in its memory. The third case, in turn, employs a variable hysteresis width and the same reference than case 1. Finally, the fourth case is characterised by a variable hysteresis width and a reference such as in case 2.

It can be observed that case 4 exhibits the lowest harmonic distortion and the maximum power factor.

The reason for its best performance is the use of the ideal reference stored in the microcontroller memory and the effect of the variable hysteresis width that results in constant switching frequency. The notch filter is tuned at the switching frequency, which eliminates the first harmonic of the input current ripple yielding the low value of harmonic distortion shown in the table. Moreover, the zero-crossing distortion is significantly reduced in this case due to the joint action of an appropriately synchronised ideal sinusoidal reference and the variable hysteresis width that tends to zero at the crossing points. This phenomenon can be observed by comparing the inductor current i_L waveforms in Figs. 10*a* and *b*. By simple inspection of the first figure, a constant hysteresis-width operation is inferred for the whole operating range, this being the cause of a significant distortion at zero crossing. Unlikely, in Fig. 8*b* the hysteresis width is adapted in a decreasing way as the current is decaying so that it is practically zero at the zero crossings. It has to be pointed out that both figures show that the output voltage is regulated at the specified level and that the input voltage is significantly less distorted in case 4. The intermediate cases in Table 1 illustrate the advantages of introducing the ideal sinusoidal reference not only in the case of variable hysteresis width but also in the case of constant one. The conclusions of the comparison in the time domain are corroborated by the spectral measurements of inductor current i_L and input current i_i depicted in Fig. 11 for cases 1 and 4. Note that the notch filter action is more effective in case 4 because the converter is operating at the constant switching frequency.

In the case of the ideal sinusoidal reference, it is worth mentioning that the proposed algorithm can measure the grid frequency accurately and detect the frequency variations undergone by a real system so that the look-up table values can be appropriately recalculated. The calculation of the new values will take few network cycles, this resulting in a negligible transient disturbance during which the power factor slightly alters. As a matter of fact, it can be proved that for step-type changes of the grid frequency of 10%, e.g. 45 and 55 Hz, the power factor decreases temporarily to 0.9854 and 0.9793, respectively, until the look-up table values are updated.

Finally, it has to be pointed out that the advantages of using an ideal sinusoidal reference are high noise immunity and very low crossover distortion, especially in low-voltage systems where the influence of the rectifier voltage drop is important.

6 Conclusion

This paper has demonstrated that analogue hysteresis-based controllers can be implemented using a low-cost microcontroller. The resulting hybrid system combines the fast response and robustness of classical analogue hysteretic controller and the

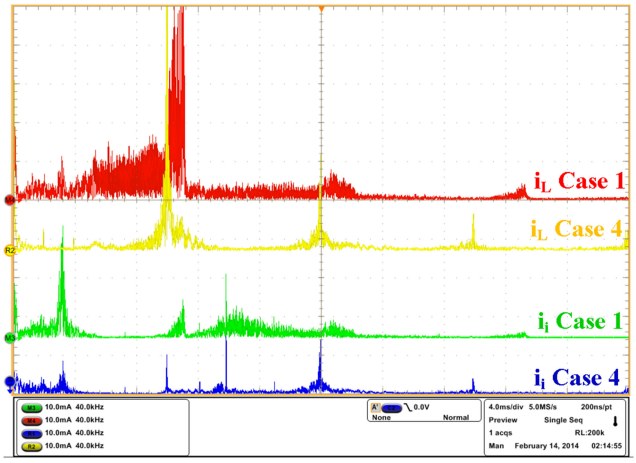


Fig. 11 *Spectral measurements of both inductor and input currents for cases 1 and 4*

Table 1 Power factor and THD in four cases defined by the type of hysteresis width and reference signal

	Implementation alternatives		Power factor	I-THD, %
case 1	measured sinusoidal reference	constant hysteresis band	0.99838	5.05149
case 2	ideal sinusoidal reference	constant hysteresis band	0.99741	3.20338
case 3	measured sinusoidal reference	variable hysteresis band	0.99841	5.02136
case 4	ideal sinusoidal reference	variable hysteresis band	0.99948	0.83276

flexibility and capability of digital devices to implement complex control laws. Besides, no execution time is consumed in the involved comparison since this is carried out by the microcontroller peripherals, which implies that the digital device can be used to generate references or to implement other algorithms.

The digital implementation of the hysteresis comparator has been contrasted in terms of rapidity with a classical analogue implementation proving that the digital one exhibits a similar performance. The versatility of the digital implementation has been demonstrated in the implementation of a PFC in a boost converter, in which a switching frequency regulation loop has been introduced. This loop has allowed the converter to work with a variable hysteresis width, which has led to a constant switching frequency operation. The design versatility has been also illustrated by the possibility of generating ideal sinusoidal references appropriately synchronised with the input signal, this feature being the key element in the reduction of the THD. It is worth mentioning the simplicity of variable hysteresis-width implementation for distortion reduction in a PFC system in comparison with the complexity of existing analogue solutions. The design of the resulting three-loop control system implies a perfect decoupling among the different loops. The inner loop has been designed by means of a continuous-time sliding-mode control approach. The second loop has been designed by means of a classical linear discrete-time approach that includes the discretisation of a transfer function derived from the first-loop study. Finally, the effect of the variable switching frequency is corrected by the action of the third loop without affecting the performance of the second and first loops.

The proposed method for a digital implementation of a hysteresis comparator could be used in the implementation of sliding-mode controllers for any type of hard switching converter operating with constant or variable switching frequency and being regulated by switching surfaces given by complex mathematical expressions. Examples of this are maximum power point trackers [25], power adaptors [26], battery chargers, motor drives etc.

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8 References

[1] Abu-Qahouq, J., Hong, M., Batarseh, I.: 'Multiphase voltage-mode hysteretic controlled DC-DC converter with novel current sharing', *IEEE Trans. Power Electron.*, 2004, **19**, (6), pp. 1397–1407

[2] Castilla, M., Guerrero, J.M., Matas, J., *et al.*: 'Comparative study of hysteretic controllers for single-phase voltage regulators', *IET Power Electron.*, 2008, **1**, (1), pp. 132–143

[3] Tan, S.-C., Lai, Y.-M., Tse, C.-K.: '*Sliding mode control of switching power converters: techniques and implementation*' (CRC Press, Boca Raton, USA, 2011)

[4] Yazici, I.: 'Robust voltage-mode controller for DC-DC boost converter', *IET Power Electron.*, 2015, **8**, (3), pp. 342–349

[5] Tan, S.C., Lai, Y.M.: 'Constant-frequency reduced-state sliding mode current controller for Cuk converters', *IET Power Electron.*, 2008, **1**, (4), pp. 466–477

[6] Vidal-Idiarte, E., Marcos-Pastor, A., Garcia, G., *et al.*: 'Discrete-time sliding-mode-based digital pulse width modulation control of a boost converter', *IET Power Electron.*, 2015, **8**, (5), pp. 708–714

[7] Lopez-Santos, O., Martinez-Salamero, L., Garcia, G., *et al.*: 'Robust sliding-mode control design for a voltage regulated quadratic boost converter', *IEEE Trans. Power Electron.*, 2015, **30**, (4), pp. 2313–2327

[8] Buccella, C., Cecati, C., Latafat, H.: 'Digital control of power converters – a survey', *IEEE Trans. Ind. Inf.*, 2012, **8**, (3), pp. 437–447

[9] Maksimovic, D., Zane, R., Erickson, R.: 'Impact of digital control in power electronics'. 16th Int. Symp. Power Semiconductor Devices and ICs 2004 Proc. ISPSD '04, 2004

[10] Singh, R.K., Mishra, S.: 'Synthetic-ripple-based digital hysteretic modulator for point-of-load converters', *IEEE Trans. Ind. Electron.*, 2013, **60**, (11), pp. 4996–5007

[11] Vidal-Idiarte, E., Carrejo, C.E., Calvente, J., *et al.*: 'Two-loop digital sliding mode control of DC-DC power converters based on predictive interpolation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (6), pp. 2491–2501

[12] Vidal-Idiarte, E., Martinez-Salamero, L., Guinjoan, F., *et al.*: 'Sliding and fuzzy control of a boost converter using an 8-bit microcontroller', *IEE Proc. Electr. Power Appl.*, 2004, **151**, (1), pp. 5–11

[13] Valderrama-Blavi, H., Bosque-Moncusi, J.M., Marroyo, L., *et al.*: 'Adapting a low voltage PEM fuel-cell to domestic grid-connected PV system'. Industrial Electronics 2009 IECON '09 35th Annual Conf. IEEE, 2009

[14] Huerta, S.C., Alou, P., Garcia, O., *et al.*: 'Hysteretic mixed-signal controller for high-frequency DC-DC converters operating at constant switching frequency', *IEEE Trans. Power Electron.*, 2012, **27**, (6), pp. 2690–2696

[15] Mamarelis, E., Petrone, G., Spagnuolo, G.: 'An hybrid digital-analog sliding mode controller for photovoltaic applications', *IEEE Trans. Ind. Inf.*, 2013, **9**, (2), pp. 1094–1103

[16] Bodetto, M., Aroudi, A.E., Cid-Pastor, A., *et al.*: 'High performance hysteresis modulation technique for high-order PFC circuits', *Electron. Lett.*, 2014, **50**, (2), pp. 113–114

[17] Bodetto, M., Aroudi, A.E., Cid-Pastor, A., *et al.*: 'Design of AC-DC PFC high-order converters with regulated output current for low-power applications', *IEEE Trans. Power Electron.*, 2016, **31**, (3), pp. 2012–2025

[18] Holmes, D.G., Davoodnezhad, R., McGrath, B.P.: 'An improved three-phase variable-band hysteresis current regulation', *IEEE Trans. Power Electron.*, 2013, **28**, (1), pp. 441–450

[19] ww1.microchip.com/downloads/en/DeviceDoc/70178C.pdf, accessed 2016

[20] Chiang, H.C., Lin, F.J., Chang, J.K., *et al.*: 'Control method for improving the response of single-phase continuous conduction mode boost power factor correction converter', *IET Power Electron.*, 2016, **9**, (9), pp. 1792–1800

[21] Albiol-Tendillo, L., Vidal-Idiarte, E., Maixe-Altes, J., *et al.*: 'Seamless sliding-mode control for bidirectional boost converter with output filter for electric vehicles applications', *IET Power Electron.*, 2015, **8**, (9), pp. 1808–1816

[22] Flores-Bahamonde, F., Valderrama-Blavi, H., Martínez-Salamero, L., *et al.*: 'Control of a three-phase AC/DC VIENNA converter based on the sliding mode loss-free resistor approach', *IET Power Electron.*, 2014, **7**, (5), pp. 1073–1082

[23] Antoniou, A.: '*Digital signal processing*' (McGraw-Hill, Columbus, USA, 2006), ISBN 0-07-145424-1

[24] Martínez, M., Gómez, L., Serrano, A.J., *et al.*: 'Filtros digitales', Open Course Lectures, Escola Tècnica Superior d'Enginyeria, Universitat València, Spain, Academic year 2009–10 (in Spanish). Available at http://ocw.uv.es/ingenieria-y-arquitectura/filtros-digitales/tema_7_modificacion_de_la_frecuencia_de_muestreo.pdf

[25] Lebron, Y., Shmilovitz, D.: 'Maximum power point tracking employing sliding mode control', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2013, **60**, (3), pp. 724–732

[26] Valderrama-blavi, H., Bosque, J.M., Guinjoan, F., *et al.*: 'Power adaptor device for domestic DC microgrids based on commercial MPPT inverters', *IEEE Trans. Ind. Electron.*, 2013, **60**, (3), pp. 1191–1203