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ADC Quantization Effects in Two-Loop Digital Current Controlled DC-DC Power Converters: Analysis and Design Guidelines

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Abstract: This paper analyzes the presence of undesired quantization-induced perturbations (QIP) in a dc-dc buck-boost converter using a two-loop digital current control. This work introduces design conditions regarding control laws gains and signal quantization to avoid the quantization effects due to the addition of the outer voltage loop in a digital current controlled converter. The two-loop controller is composed of a multisampled average current control (MACC) in the inner current-programmed loop and a proportional-integrator compensator at the external loop. QIP conditions have been evaluated through simulations and experiments using a digitally controlled pulse width modulation (DPWM) buck-boost converter. A 400 V 1.6 kW proof-of-concept converter has been used to illustrate the presence of QIP and verify the design conditions. The controller is programmed in a digital signal controller (DSC) TMS320F28377S with a DPWM with 8.96-bit equivalent resolution, a 12-bit ADC for current sampling, and a 12-bit ADC for voltage sampling or a 16-bit ADC for voltage error sampling.

Keywords: dc-dc power converter; multisampled average current control (MACC); digital control; limit-cycle oscillation (LCO); quantization-induced perturbations (QIP)

1. Introduction

Digital control in dc-dc converters is of interest because its many potential advantages such as low power consumption and flexibility to program and design advanced control strategies to improve the system performance [1–3]. Therefore, the digital closed-loop configuration is increasingly being used in dc-dc converters [4–6]. Digital control depicts an important element of power converters for renewable energy systems [7], automobile industry [8], and industrial applications [9]. However, many works report disadvantageous quantization effects related to the existence of limit cycles in digitally controlled pulse width modulation (DPWM) converters. Static and dynamic models taking into account the quantization effects are derived and used to explain the origins of limit-cycle oscillations (LCO) for voltage single-loop digital control in [10,11]. A DPWM resolution lower than ADC resolution usually causes LCO that affects the regulation of the controlled variable [12]. Therefore, DPWM with resolution higher than the ADC is usually implemented in order to reduce the effect of limit-cycle oscillations in voltage single-loop digital

control, where the difference between the voltage reference and the output voltage is quantized to a digital number to represent the error signal [13,14].

It is well known that cascade control of dc-dc converters generally offers better performance than single-loop control [15,16]. Moreover, current control strategies are always needed to connect in parallel some converters to increase power management. Therefore, two-loop digital control structures have been extensively applied last teen years [17–21]. Analysis of LCO are given in [22–24] for digital current mode control. In these works, the resolution of the DPWM is also greater than the ADC resolution in the outer voltage loop. In [22], an estimation algorithm has been applied to the average current control of a buck converter in order to reduce quantization effects in the inductor current loop and, consequently, the presence of limit cycle oscillations. A method to design a two-loop digital control is developed in [23], where the current reference is dynamically adjusted to give a solution to the LCO problem. A technique to compute the steady-state duty cycle in real-time was considered in [24], where a time-to-digital converter translates the duty ratio information into a digital code using a moving average filter and an adjustable current loop sampling frequency. At steady-state, the strategy disables the current-loop sampling and the control computation. Then, a virtual open loop configuration is used to reduce oscillations of the inductor current.

In order to improve the resolution of the DPWM in single-loop digital voltage controllers, some authors use sigma-delta modulation to eliminate the quantization noise and the LCO. In [12], a non-zero error method is used to encode the output voltage error improving the low resolution of the DPWM. A sigma delta modulation scheme and switching frequency modulation strategy are combined in [25] to increase the effective resolution of the DPWM. Nonetheless, there are not reported works that show the effects of quantization in dc-dc converter with a two-loop digital control having an integral term of its output voltage error.

This paper presents design conditions to avoid the effects of the quantization in two-loop current controlled dc-dc switching converter. LCOs conditions presented in [10] are extended to a two-loop digital control in order to obtain restrictions associated with the gains of the control laws and the quantization resolution for each control loop. When the condition proposed for the external loop is fulfilled, simulation and experimental results verify that the QIP are suppressed from the current signals.

Section 2 presents the conditions for each digital loop to observe the two-loop quantization effects. Section 3 describes the implementation of the digitally controlled buck-boost converter in order to validate the restrictions. Experimental and simulation results for a 400 V 1.6 kW digitally controlled coupled-inductor dc-dc buck-boost converter are presented in Section 4. Conclusions are given in Section 5.

2. Two-Loop Quantization Effects

Quantization effects have been deeply studied in [10,11,26], where authors studied limit cycling conditions regarding plant and controller gains besides ADC and PWM resolution in a single-loop voltage control. This section presents dynamic conditions to avoid limit cycles in a two-loop digital current controller converter.

In this case, both inner and outer small-signal representation of the control to output transfer function can be represented in general form as

$$G_p(s) = \frac{G}{s} \tag{1}$$

where G is the gain of the transfer function and $1/s$ represents the transfer function of an integrator. In the case of the inner current control (see Figure 1a), the transfer Function (1) becomes

$$G_{pin}(s) = \frac{m_1 + m_2}{s} \tag{2}$$

where m_1 is the positive slope and m_2 is the negative slope of the output current. Finally, for the voltage loop (see Figure 1b) the transfer Function (1) becomes

$$G_{pou}(s) = \frac{1}{C_o s} \tag{3}$$

where C_o represents the output filter capacitor of the converter. A standard Proportional-Integral (PI) controller is used in both control loops

$$G_{pi}(s) = K_p + \frac{K_i}{s} \tag{4}$$

where $G_{pi}(s) = G_{pii}(s)$ for the inner loop (Figure 1a) and $G_{pi}(s) = G_{piv}(s)$ for the external loop (Figure 1b).

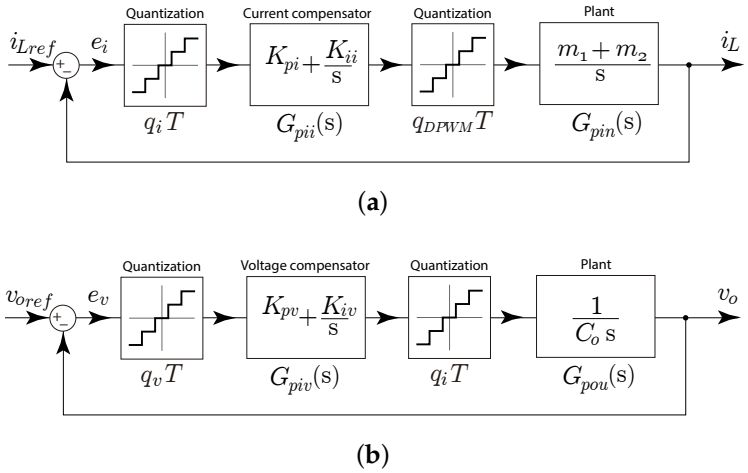

Figure 1. Proportional-integrator control block diagram of (**a**) inner loop dynamic model and (**b**) outer loop dynamic model.

The dynamic model for each loop is shown in Figure 1, where q is the quantization level for an input or an output signal. Therefore, q_i, q_v, and q_{DPWM} represent, respectively, the output current i_L, the output voltage v_o, and the DPWM quantization level. T is the switching period ($1/f_s$). Finally, e_v and e_i are the error signals of the measured voltage and current, respectively. Then, in the inner loop, $G_{pii}(s)$ generates the control variable u, taking into account the mean value of the output current converter to change the duty cycle. Nonetheless, $G_{piv}(s)$ for the output voltage gives the current reference for the inner loop based on the error voltage.

The loop gains of the linear part of the system are defined without quantization [10,26] as follows,

$$T_L(s) = G_{pi}(s)G_p(s). \tag{5}$$

Therefore, using (1) and (4) we obtain the crossover angular frequency as

$$\omega_c = K_p G, \tag{6}$$

A typical design of PI parameters usually places the zero of the controller at least one decade below of the desired crossing frequency ω_c, thus giving the following condition,

$$K_i/K_p << \omega_c, \tag{7}$$

Then, we have to adjust K_p and K_i in order to obtain the desired phase margin. Phase margin (PM) is usually adjusted to be greater than 50° by tuning K_p and satisfying (7).

2.1. Outer Loop Condition

In digital power converter operation, the static and the integral gain condition must be satisfied to avoid limit cycling due to quantization [27–29]. Then, the necessary no-limit-cycling condition that allows the existence of a steady-state solution inside ADC zero-error bin, given in [28,29], can be written for the external voltage loop in Figure 1b as

$$q_i TG < q_v. \tag{8}$$

Condition (8) indicates that the minimum output voltage variation, due to the minimum output current step change provoked by a variation in the output voltage, must be smaller than the quantization level of the output voltage. In this condition (8), the gain G is defined as $1/C_o$. The no-limit-cycling condition involving the integral gain is

$$q_v T K_{iv} < q_i. \tag{9}$$

The output current reference change provoked by a minimum error in the voltage loop is $K_{pv} q_v$. To guarantee output voltage regulation, the compensator must develop a correction action when e_v is different from 0 [29], thus giving

$$q_v K_{pv} > q_i. \tag{10}$$

Combining restrictions (9) and (10) results in the following condition,

$$K_{iv} T < \frac{q_i}{q_v} < K_{pv}. \tag{11}$$

Condition (12) is derived replacing (10) in (8)

$$K_{pv} TG < 1. \tag{12}$$

Employing Equation (6) and replacing $K_p = K_{pv}$ in (12), we obtain an upper limit for the crossing frequency

$$\omega_c < \frac{1}{T}. \tag{13}$$

2.2. Inner Loop Condition

Restriction (11) can be extended in terms of the inner loop block diagram representation of Figure 1a. Following the same procedure as in the outer loop, the condition for the inner loop is given by

$$K_{ii} T < \frac{q_{DPWM}}{q_i} < K_{pi}, \tag{14}$$

Following (7), we select $K_{ii} T = K_{pi}/10$ and adjust K_{pi} to obtain a PM greater than 50°.

3. Validation of the Restrictions

The fulfillment of Conditions (11) and (14), which guarantee a stable digital two-loop control, have been verified using a buck-boost converter with coupled inductors. The topology of the dc-dc buck-boost converter for a voltage regulation application shown in Figure 2 was introduced as an unidirectional buck-boost converter in [30] and presented for electric vehicle and high-voltage application in [31,32]. The bidirectional power stage shown in Figure 2 is composed of two coupled inductors with unitary turns ratio and magnetic coupling coefficient $k = 0.5$. Therefore, primary self-inductance L_1 is equal to secondary self-inductance L_2 ($L_1 = L_2 = L$), and their mutual inductance is $M = L/2$. The two-loop digital voltage controller proposed in Figure 3 consists of a MACC [33] inner current programmed controller and a discrete-time PI compensator at the outer voltage feedback loop. Note, in Figure 3 we also

represent two measuring approaches that allows to obtain different quantization levels of the measured output voltage error.

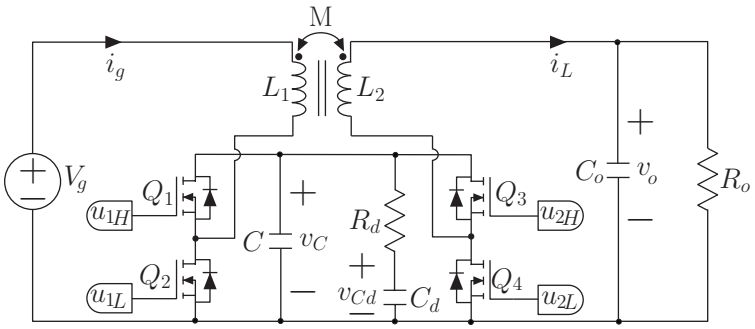

Figure 2. Power stage of a coupled-inductor buck-boost converter.

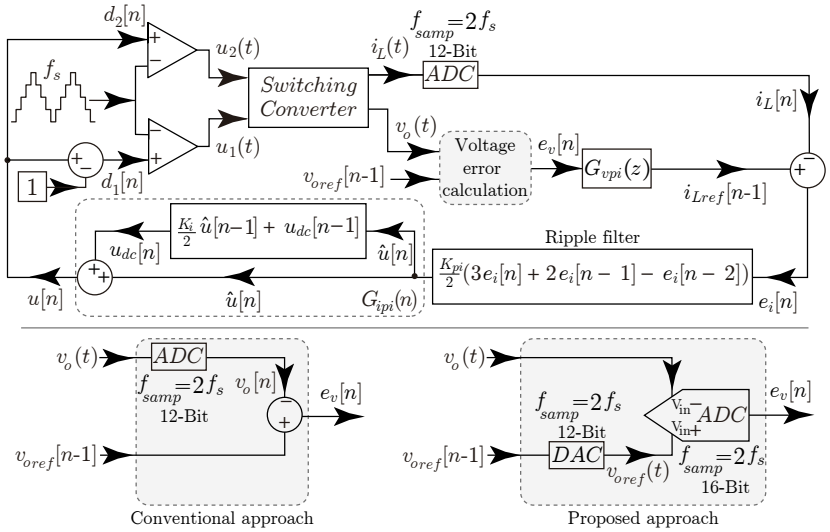

Figure 3. Block diagram of the digital controller for the voltage regulation of the buck-boost converter. Bottom Left: Conventional voltage error subcircuit. Bottom Right: Proposed improved approach subcircuit.

3.1. Multisampled Average Current Control (MACC)

The multisampled average current control for the bidirectional buck-boost converter was presented in [33]. The MACC stage generates the control variable (u) that is processed by a dual digital PWM to obtain the discrete control signals (u_1 and u_2) that activate the converter half-bridges. The external loop regulates the output voltage by providing the MACC with the output current reference through a discrete proportional-integral control transfer function $G_{vpi}(z)$, as it is seen in Figure 3. An important element of the MACC loop is the ripple filter processing the error between output current $i_L[n]$ and its desired reference $i_{Lref}[n-1]$. The ripple filter averages two consecutive samples per switching period ($f_{samp}=2f_s$) of the output current error. This strategy eliminates the switching ripple in the current loop without significant phase loss [34].

The discrete-time ripple filter transfer function can be expressed as

$$\hat{u}[n]=\frac{K_{pi}}{2}\left(3e_i[n]+2e_i[n-1]-e_i[n-2]\right). \tag{15}$$

The proportional gain can be written in terms of the output current waveform slopes as

$$K_{pi} = \frac{K_n}{(m_1 + m_2)T} \tag{16}$$

where the output current has a periodic triangular waveform with rising and falling current slopes m_1 and $-m_2$, respectively. The expression $m_1 + m_2$ is obtained for each converter operation mode, yielding

$$m_1 + m_2 = \begin{cases} \dfrac{Mv_o[n]}{L^2 - M^2} & \text{for boost mode} \\ \dfrac{LV_g}{L^2 - M^2} & \text{for buck mode.} \end{cases} \tag{17}$$

Parameter K_n has been adjusted to 0.35 to obtain a crossover frequency (CF) of approximately 11 kHz and a phase margin (PM) of 58° as in [33].

The digital PI compensator in the z-domain added to the current control loop has been implemented using forward-Euler method as follows,

$$G_{ipi}(z) = 1 + \frac{K_i}{2}\frac{1}{z-1} \tag{18}$$

Figure 3 shows the implementation of the discrete-time PI compensator, whose integral gain can be chosen as in [33].

3.2. *Digital Proportional-Integral Voltage Control*

A slower outer voltage loop providing current reference i_{Lref} is added to the inner current loop. The PI voltage controller is designed taken into account the value of the output filter capacitor (C_o) and the desired loop-gain crossover frequency (f_c). The transfer function of the PI voltage controller can be expressed in the z domain using the forward Euler method as

$$G_{vpi}(z) = K_{pv} + \frac{K_{iv}T_{samp}}{z-1}z^{-1} \tag{19}$$

where $K_{pv} = C_o 2\pi f_c$, $K_{iv} = K_{pv}/T_i$, and T_{samp} is the sample period ($1/f_{samp}$). Therefore, the bandwidth of the voltage loop depends on the proportional coefficient (K_{pv}), while the phase margin (PM) is adjusted to be greater than 50° adjusting K_{pv} after setting $T_i = 10/(2\pi f_c)$ for the integral coefficient (K_{iv}). The forward-Euler method is used to find the recurrence equations for the discrete-time PI controller as

$$\begin{aligned} i_{Lp}[n] &= K_{pv}e_v[n] \\ i_{Li}[n] &= K_{iv}T_{samp}e_v[n] + i_{Li}[n-1] \\ i_{Lref}[n] &= i_{Lp}[n] + i_{Li}[n]. \end{aligned} \tag{20}$$

4. Simulation and Experimental Results

The set-up used to carried out the different experiments with the MACC-based two-loop digital control is shown in Figure 4. It is composed of a 400 V 1.6 kW buck-boost prototype converter with the parameters described in Table 1 and the TMS320F28377S DSC. The design of the buck-boost converter is presented in [32].

The tests were carried out changing quantization values and controller parameters, as described next. Test 1 has been done using the conventional voltage error approach shown in Figure 3 using a 12 bit ADC to take the samples of output current and voltage. The external loop compensator is designed to obtain a cross-over frequency of $f_c = 4$ kHz. Test 2 also corresponds to the conventional voltage error measurement approach used in Test 1 but tuning $f_c = 2$ kHz. In order to reduce the voltage error quantization value q_v,

Test 3 has been carried out with the proposed voltage error block shown in Figure 3, using a 16 bit ADC in differential mode and $f_c = 4$ kHz for the external closed loop. In Test 4, the ADC quantization level of the output current and voltage is increased, scaling ADC resolution to 8 and 11 bits respectively for the current and voltage sampled values [35], and using the conventional approach error voltage block in Figure 3. Loop gains of the external control loop for the last test are selected to obtain $f_c = 4$ kHz.

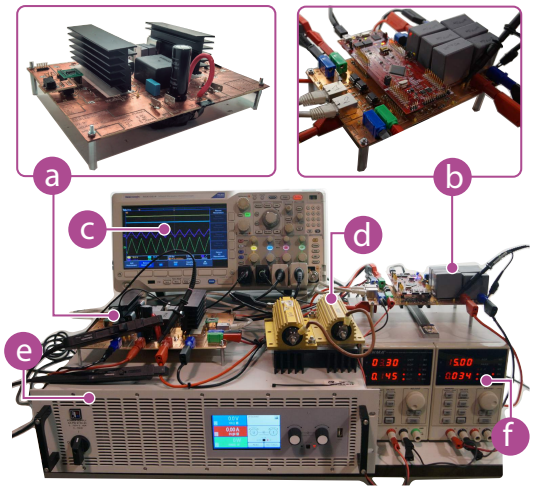

Figure 4. Experimental set-up of the buck-boost voltage regulator: (**a**) coupled-inductor buck-boost power stage, (**b**) digital signal controller with output capacitor $C_o = 28$ µF, (**c**) oscilloscope, (**d**) constant resistive load $R_o = 200$ Ω (**e**) input dc power supply, and (**f**) auxiliary power supply for DSC and MOSFET drivers.

Table 1. Parameters for the buck-boost setup.

Converter Parameters	Value
Input voltage V_g	200–400 V
Output voltage V_o	100–400 V
Rated power	1.6 kW
Switching frequency $f_s = 1/T$	100 kHz
Output capacitor C_o	28 µF
Intermediate capacitor C	1.32 µF
Mutual inductance $M = L_m$	135 µH
Self inductances $L_1 = L_2$	270 µH
Damping network R_dC_d	5 Ω, 20 µF
Load resistor R_o	200 Ω

Figure 5 shows simulated waveforms of output current reference i_{Lref}, variable control u, and voltage error e_v when the converter operates in steady-state with $V_g = 200$ V and $v_o = 300$ V.

A summary of the tests and evaluations of the fulfillment of the stability conditions for each loop, obtained by replacing the parameters of Tables 2 and 3 in the restrictions (11) and (14), are shown in Table 4. Figure 5a shows quantization-induced perturbations (QIP) in all signals for the Test 1, when neither $q_{DPWM}/q_i < K_{pi}$ for the restriction (14) of the inner current loop nor $K_{iv}T < q_i/q_v$ of the external loop are fulfilled. In Test 2, although condition (14) is not fulfilled, QIP are reduced for the output current reference as can be seen in Figure 5b. The condition for the external loop (11) is satisfied due to the reduction of the gains K_{iv} and K_{pv}, but, as the cross-over frequency depends on the proportional gain K_{pv}, the loop bandwidth is reduced. The ADC quantization level of the output voltage quantization q_v is reduced in

Test 3, where the condition for the external loop is fulfilled with a wide bandwidth, and the effects of QIP on the output current reference are significantly reduced.

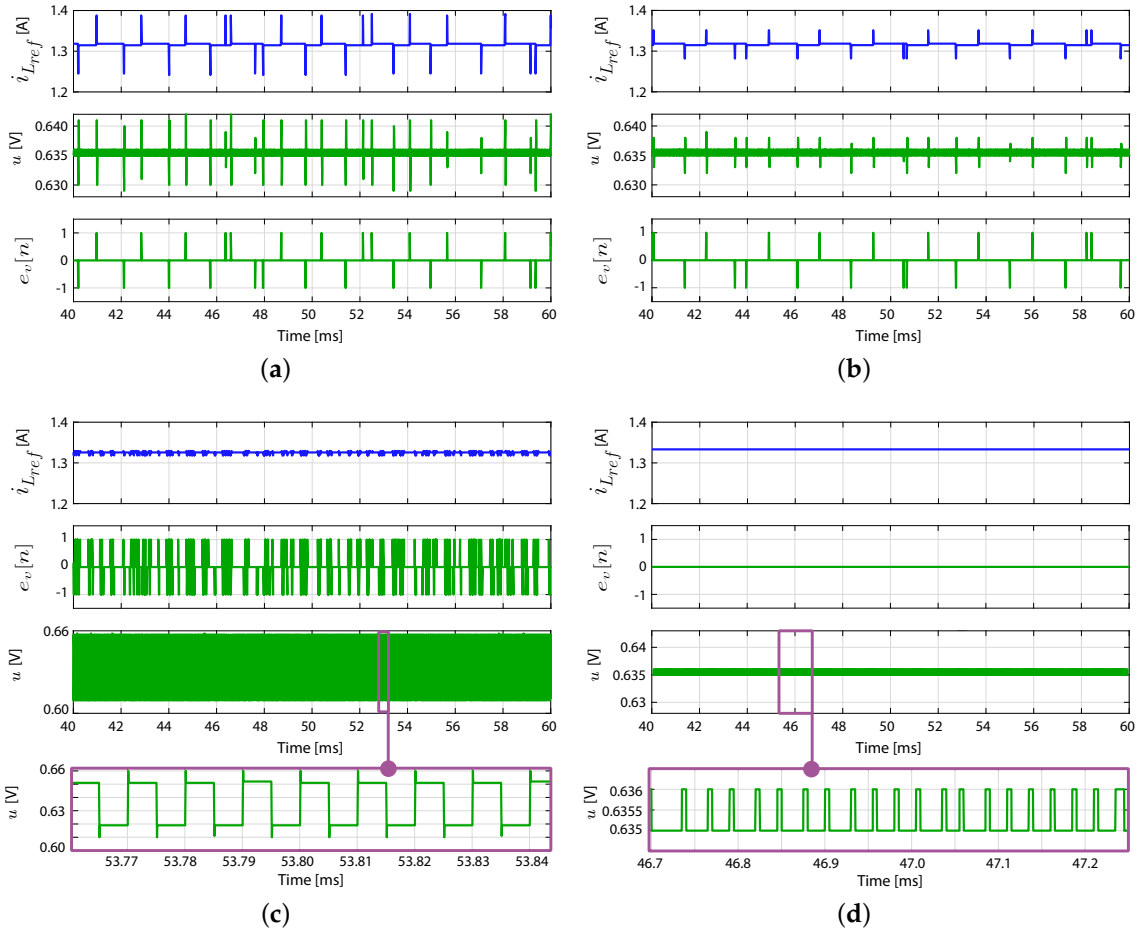

Figure 5. Simulation of output current reference i_{Lref}, signal control u, and voltage error e_v with the converter operating in steady-state: (**a**) Test 1; (**b**) Test 2; (**c**) Test 3; (**d**) Test 4.

Table 2. Analog parameters controller design.

External control parameters for $f_c = 4$ kHz	**Value**
K_{pv}	$0.7\ \frac{A}{Vs}$
$K_{iv}T$	$0.07\ \frac{A}{V}$
External control parameters for $f_c = 2$ kHz	**Value**
K_{pv}	$0.35\ \frac{A}{Vs}$
$K_{iv}T$	$0.035\ \frac{A}{V}$
Inner control parameters	**Value**
K_{pi}	$47\ \frac{1}{kAs}$
$K_{ii}T$	$4.7\ \frac{1}{kA}$

Table 3. ADC quantization parameters controller design.

Quantization Tests 1 and 2	**Value**
v_o ADC quantization level q_v	0.11 V
i_L ADC quantization level q_i	5.86 mA
DPWM quantization q_{DPWM}	0.002
Quantization Test 3	**Value**
v_o ADC quantization level q_v	0.013 V
i_L quantization level q_i	5.86 mA
DPWM quantization q_{DPWM}	0.002
Quantization Test 4	**Value**
quantization level q_v	0.22 V
quantization level q_i	93.75 mA
DPWM quantization q_{DPWM}	0.002

Table 4. Summary of the tests.

Test	$e_v[n]$ **Calculation**	f_c **[kHz]**	**Condition** (14)	**Condition** (11)
Test 1	Conventional	4	X	X
Test 2	Conventional	2	X	✓
Test 3	Proposed	4	X	✓
Test 4	Conventional	4	✓	✓

To compare the bandwidths and stability margins provided by each of the tests, the corresponding Bode plots of the voltage loop-gains for the converter operating in boost mode are provided in Figure 6, being the loop gain frequency response in a switched converter a powerful tool commonly used for the design of the controllers used in the control stage [36]. It is important to note that the results for the Test 1 have not been included in the frequency response analysis previously described. This test does not present a stable inner loop regulation which is evidenced by the presence of high current peak perturbations. This peak would be destructive for the converter if an experimental frequency response analysis is performed (please see the temporary experimental results presented below). Experimental plots in Figure 6b show that the Tests 3 and 4 with $K_{pv} = 0.7$ provide a CF of 4 kHz and a PM of 52°, while Test 2 with $K_{pv} = 0.35$ A/Vs, with smaller quantization perturbations (see Figure 5b), yields a CF = 2.16 kHz and PM = 59.58°.

Simulation tests were done using two voltage error measurement approaches shown in Figure 3. The conventional approach on the left side uses an ADC for sampling the voltage and then computes the voltage error. On the right side, the proposed method quantizes the voltage error by using an ADC in differential mode. Previously, it produces an analog voltage reference from the digital one. Through this last approach, it is possible to increase the error voltage resolution. The values of the analog control gains for the inner and for the external loop at different cross-over frequencies are shown in Table 2.

The proportional gain for the outer control is selected using the expression $K_{pv} = C_o 2\pi f_c$ for different crossover frequencies ($f_c = 2$ KHz and $f_c = 4$ kHz) and with $C_o = 28$ µF. Then, the proportional gain for the inner control is adjusted using the expression (16) with $K_n = 0.35$, employing the Equation (17) for boost mode with an output voltage of $V_o = 300$ V in Equation (16). The statement $K_i T = K_p/10$ ensures to obtain a PM greater than 50° (see Figure 6), therefore $K_{iv} T = K_{pv}/10$ for the outer loop and $K_{ii} T = K_{pi}/10$ for the inner loop. The parameters for the different tests are listed in Table 3.

Nonetheless, the condition for the inner loop is not fulfilled in this test, therefore the control variable u and voltage error e_v are not free of QIP effects as it is shown in Figure 5c. The simulated results of Test 4, in which both stability conditions are satisfied, are shown in Figure 5d, where the QIP perturbations have

disappeared from all signals. It is also noticeable that, in comparison with previous tests, the control effort has been also reduced, which is indicated by the small amplitude of control variable u.

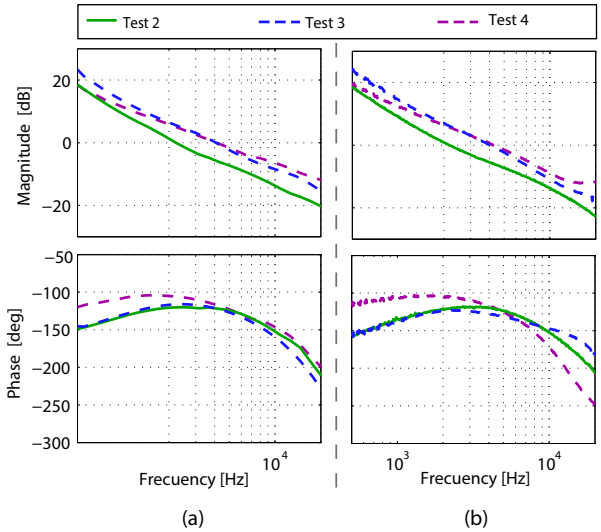

Figure 6. Voltage loop-gain Bode plots: (**a**) simulated, (**b**) experimental.

These values are in good agreement with the simulated results in Figure 6a. Despite the fact that Tests 2 and 3 do not satisfy all conditions, it is possible to operate the converter with these designs, obtaining a wider bandwidth using the proposed approach seen in Figure 3 for the Test 3.

Additional experiments and simulations have been performed to observe the current waveforms during start-up together with about 12 ms of steady-state regimes. Figure 7 depicts waveforms of input (i_g) and output (i_L) currents, as well as input (v_o) and output (V_g) voltages in the same cases previously shown in Figure 5.

In Figure 7, waveforms of the experimental results show higher QIP in relation to the simulation results due to noise in the experimental tests. In the same way, Figure 7a,b corresponds to Test 1 using the conventional approach, where the DPWM was configured for 8.96-bit. Output voltage and current ADC resolution are set to 12 bits, and the input ADC input voltage range goes from 0 V to 3 V. Figure 7a,b shows the simulated and experimental results when the proportional gain of the voltage loop is selected as $K_{pv} = 0.7$. In this case, the current waveforms present perturbations with high current overshoot and undershoot values. Results when the gain K_{pv} is reduced to the more conservative value of 0.35 in Test 2 are plotted in Figure 7c,d, showing that limiting the voltage loop bandwidth using the conventional error-calculation method reduces QIP in both currents improving the closed-loop stability. The current waveforms in Test 3 with the proposed improved error measurement approach in Figure 7e,f, show that there are no significant current perturbations when the proportional gain is again selected to $K_{pv} = 0.7$, so that a wide bandwidth voltage loop is obtained with a phase margin larger than 50°. In this case, the DPWM has been configured with 8.96-bit resolution, while the ADCs sampling the output current and the voltage error have been configured with resolutions of 12-bit and 16-bit differential mode, respectively. Figure 7g,h shows the simulated and experimental results for the Test 4, when the proportional gain is $K_{pv} = 0.7$ and both conditions (11) and (14) are fulfilled. Time domain current waveforms of the prototype for the different tests when it works in boost mode are shown in Figure 8. Figure 8a current waveforms for Test 1 present high current undershoot because conditions (11) and (14) are not fulfilled. The rest of test results show that the QIP is reduced, obtaining better results for the Test 4 with a $f_c = 4$ kHz (Figure 8d). It is important to remark that fulfilling condition (11) for the external loop is enough to reduce QIP and

LCO at the current waveforms in steady-state when the control of the converter is a two-loop with an integrator due to the external loop not cause induced perturbations in the internal loop.

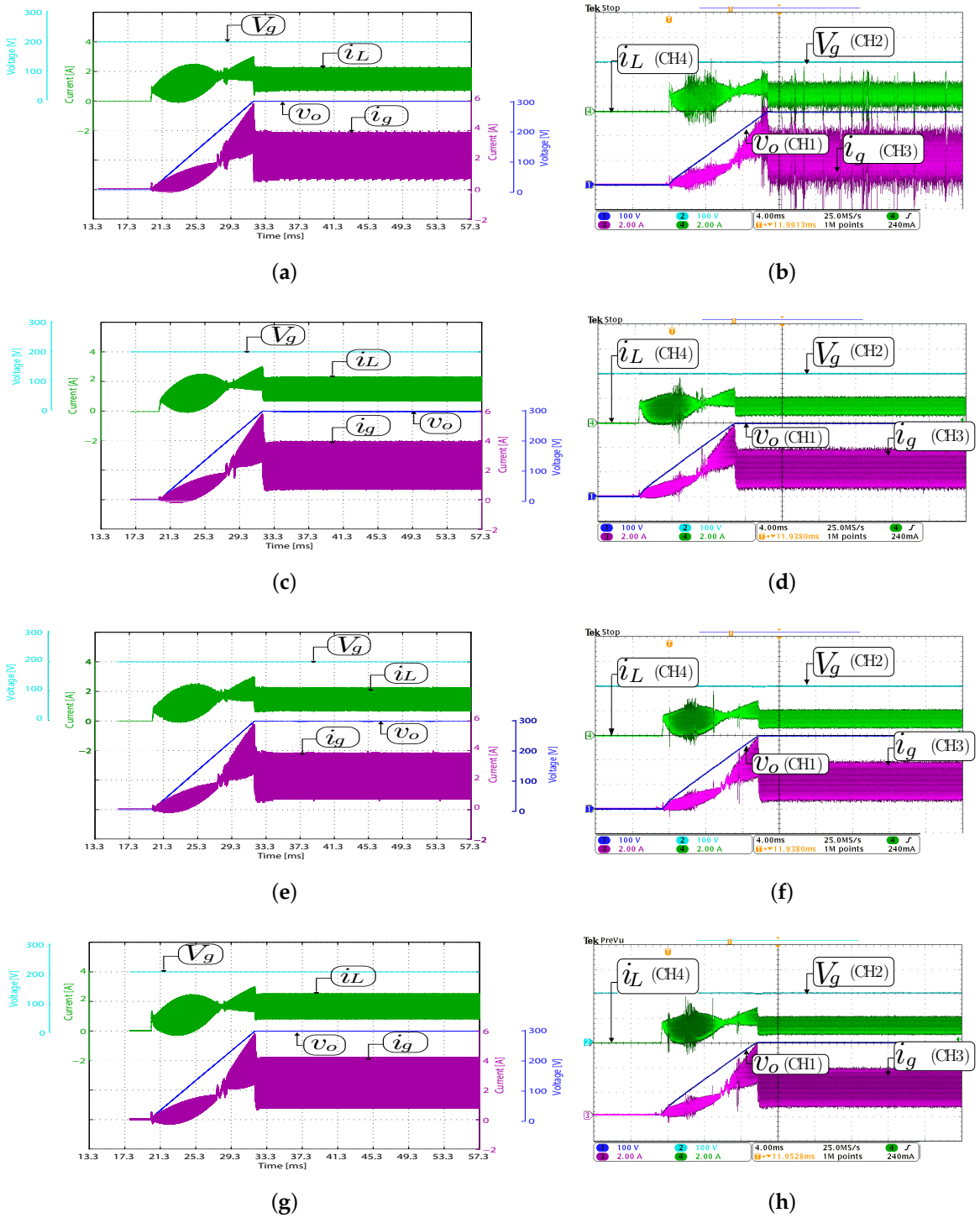

Figure 7. Simulated (**a**,**c**,**e**,**g**) and experimental (**b**,**d**,**f**,**h**) start-up waveforms: (**a**,**b**) Test 1, (**c**,**d**) Test 2, (**e**,**f**) Test 3, and (**g**,**h**) Test 4 ($V_g = 200$ V, $v_o = 300$ V, and $R_o = 200$ Ω). CH1: v_o (100 V/div). CH2: V_g (100 V/div) CH3: i_g (2 A/div), CH4: i_L (2 A/div).

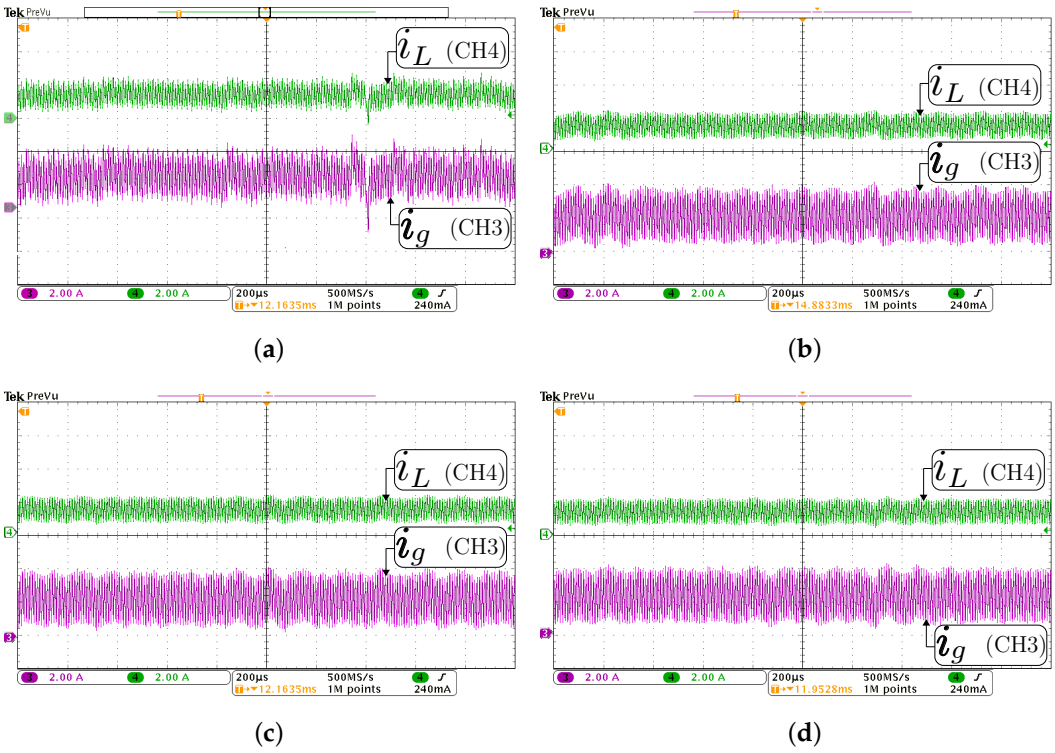

Figure 8. Time domain waveforms of i_g and i_L: (**a**) Test 1, (**b**) Test 2, (**c**) Test 3, (**d**) Test 4. CH3: i_g (2 A/div), CH4: i_L (2 A/div), and time base of 200 µs.

5. Conclusions

Limit cycle oscillations conditions due to quantization-induced perturbation in a digital two-loop current controlled converter are presented and analyzed in this paper. LCO conditions includes both loops ADCs quantization, DPWM quantization and gains of the to control laws to show the undesired quantization effects in a two-loop digital voltage regulator of a dc-dc converter with an integrator at its output. Simulation and experimental results, obtained after developing different tests on a 400 V 1.6 kW coupled-inductor buck-boost purpose-built prototype, validate that the current waveforms present perturbations when these conditions are not fulfilled. These tests also demonstrate that fulfilling the condition for the external loop is enough to reduce the quantization induced perturbations. Nevertheless, the comparison of test results suggests that fulfilling conditions for both loops is the best option to avoid LCO and QIP in the system variables. The work presents a useful guidance for the design of the PI digital controllers in DC-DC converters, in order to improve significantly the dynamic responses, increasing the voltage loop bandwidth without ADC quantization effects.

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Abbreviations

The following abbreviations are used in this manuscript.

ADC	Analog to digital converter
QIP	Quantization-induced-perturbation
MACC	Multrisampled average current control
DPWM	Digitally controlled pulse width modulation
DSC	Digital signal controller
LCO	Limit-cycle oscillations
PM	Phase margin
PI	Proportional-Integral
CF	Crossover frequency

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