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Coupled inductors design of the bidirectional non-inverting buck–boost converter for high-voltage applications

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Abstract: This work analyses the effects on the efficiency of the winding-to-winding capacitance of the coupled-inductor of the bidirectional non-inverting buck–boost converter in high-voltage applications. This converter presents many advantages that make it suitable for low-voltage hard-switching photovoltaic and fuel cell hybrid systems. However, experimental results obtained using the previously reported procedure to implement the coupled inductors show low-efficiency in high-voltage applications. A different implementation procedure of the coupled inductors, with lower winding-to-winding capacitance, is proposed. High-efficiency experimental results from a 400 V 1.6 kW prototype have been achieved over a wide operating voltage range, thanks to the use of SiC devices and the modified coupled inductors, confirming in this way its good potential as a building block also in high-voltage wide-gain-range applications.

1 Introduction

Nowadays, bidirectional converters are used as discharging–charging battery regulators, renewable energy power processors, and electric vehicles (EVs) systems. In renewable systems like photovoltaic and wind power, the bidirectional dc–dc converter operates as an interface between the high voltage source and the low voltage battery in order to optimise the efficiency. Battery discharging–charging regulators are common in telecommunication applications and space platforms. In EVs powertrain configurations, global efficiency is optimised using high-efficiency bidirectional converters able to step-up and step-down voltages [1–3].

The non-inverting dc–dc buck–boost converter with coupled inductors [4] could be a good candidate to optimise global efficiency because it can step-up or step-down voltage with high efficiency, providing smooth transitions between both modes provided that a hysteretic pulse-width modulator (PWM) control strategy is used to activate its switches [5, 6]. This converter has the same wide conversion ratio than a single inductor non-inverting buck–boost converter with better efficiency because of reduced switches stress. In addition, the placement of their coupled inductors eliminates the pulsating nature of input and output currents and reduces the associated noise levels. Moreover, the combination of coupled inductors with an RC damping network in parallel with the intermediate capacitor eliminates the right-half plane (RHP) zero usually exhibited by conventional continuous conduction dc–dc converters in step-up voltage mode [4]. The solution to the problem of the RHP zeros using coupled inductors with an RC damping network has been reported in [7, 8]. This solution allows for obtaining high efficiency and wide bandwidth boost converters for high-power low-voltage applications [9]. The topology has been used as a building block in several fuel-cell applications, such as the serial–parallel hybrid system reported in [10].

An even more versatile bidirectional version was introduced in [11, 12] where digital and analogue controls have been studied for low-voltage applications. However, to achieve ideal magnetic inductor coupling, the bifilar winding technique is used [13–16], which increases parasitic winding-to-winding capacitance. In high-voltage applications, associated losses to this parasitic capacitance have significant value and are one of the reasons of the theoretical versus experimental efficiency mismatch and the appearance of voltage switch spikes. The coupled inductor design presented in [17] has been used for the non-inverting dc–dc buck–boost converter, this design allows flexibility to adjust the coupling coefficient by connecting tightly coupled inductors ($k \simeq 1$) in series with the separate uncoupled inductor. This method is used in [4], where the peak efficiency obtained is of 97 % for an input voltage of 51 V and an output voltage of 48 V. This converter has the peak efficiency when the input and output voltages are similar. The high-efficiency voltage gain range is between 0.5 and 2.

This work presents the design of a hard-switching high-voltage bidirectional buck–boost converter with coupled inductors. The experimental results show that the implementation of the coupled inductors following the multiple-core approach used in [17] presents low efficiency in high-voltage applications. After analysing the converter power loss, it is possible to conclude that the high parasitic winding-to-winding capacitance value is the responsibility of the majority power loss in the converter. Then, a single-core design procedure of the coupled inductors is used and tested, now showing good efficiency measurements over a wide range of operating points. A summarised comparison of the peak efficiency of the dc–dc converters with coupled inductors that use both approaches of coupled inductor implementation used in this work is provided in Table 1. The coupled inductors were built in a toroidal core. The multiple-core approach design is composed of a tightly coupled inductor (with a coupling coefficient $k = 1$) in series with separate uncoupled inductors. These uncoupled inductors represent the leakage inductance for the structure. This method allows fulfilling more accurately the coupling specifications. In the case of using the single-core approach, its low core permeability coefficient leads to obtain a low coupling coefficient, as shown in Table 1. Using this methodology, the non-inverting buck–boost converter with the single-core approach has been shown a higher peak efficiency in high-voltage. The single-core method also is used in low-power low-voltage applications in order to reduce the number of magnetic elements [22]. In [20, 4], the converter presents high peak efficiency for low-voltage applications, showing the parasitic winding-to-winding capacitance in the multiple magnetic core implementation has not major effects in converter efficiency in low-voltage applications. The description of the two possibilities of implementing the coupled inductors is

Table 1 Peak efficiency of dc–dc converters with coupled inductors

Presented in	Converter type	Coupled inductor design	Input voltage, V	Output voltage, V	Switching frequency, kHz	Rated power, W	Peak efficiency, %
[18]	Cuk-SEPIC converter	Multiple-core approach, coupling coefficient: 0.89, core permeability coefficient: 60	400.0	360.0	100	4000	92.5
[19]	Interleaved high step-up converter	Single-core approach, coupling coefficient: 0.98, core permeability coefficient: 50	21.0	270.0	50	1000	97.3
[20]	Zero-voltage switching (ZVS) bidirectional step-up converter	Multiple-core approach, coupling coefficient: 0.7, core permeability coefficient: 26	48.0	100.0	100	350	94.0
[21]	High step-up dc–dc converter	Single-core approach, coupling coefficient: 0.98, core permeability coefficient: 50	40.0	400.0	50	500	96.2
[22]	Isolated resonant dc–dc ZVS	Single-core approach, coupling coefficient: 0.6, core permeability coefficient: 16	80.1	20.8	2000	30	95.7
[4]	Unidirectional non-inverting buck–boost converter	Multiple-core approach, coupling coefficient: 0.5, core permeability coefficient: 60	51.0	48.0	100	700	97.0
[23]	Bidirectional non-inverting buck–boost converter	Multiple-core approach, coupling coefficient: 0.75, core permeability coefficient: 26	200.0	175.0	100	1600	91.0
in this paper	Bidirectional non-inverting buck–boost converter	Single-core approach, coupling coefficient: 0.5, core permeability coefficient: 26	350.0	300.0	100	1600	98.0

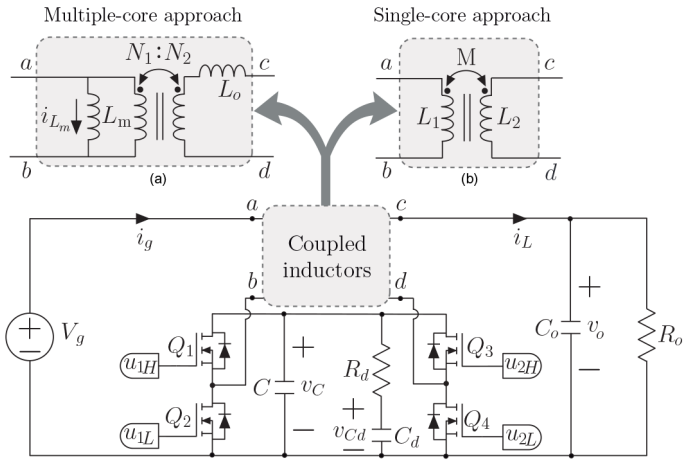


Fig. 1 *Schemes of the buck–boost power stage*
(a) Multiple-core approach, ***(b)*** Single-core approach

presented in Section 2, where the design for two power stages is presented. The proposed design of the coupled inductors and the associated damping network required to be efficient at high voltages are presented in Section 3. A comparative study of the winding-to-winding of coupled inductors is presented in Section 4. Current control is introduced in Section 5. Finally, Sections 6 and 7 provide, respectively, the experimental results and conclusions.

2 Non-inverting buck–boost converter

The topology of the bidirectional non-inverting buck–boost converter is shown in Fig. 1. It is composed by a buck–boost cell of two MOSFET half bridges, an $R_d C_d$ damping network connected in parallel with the intermediate capacitor C, and a pair of coupled inductors, one connected between the input and the middle node of the one half bridge, and the second one between the output and the middle node of the other half bridge. To achieve high efficiency, depending on the mode of operation, one of the half bridges switches at high frequency while the high-side MOSFET of the other half bridge is permanently in the ON-state and the low-side one is in the OFF-state. In the scheme of Fig. 2, the duty cycle $d_1(t)$

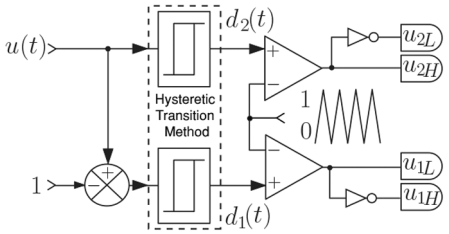


Fig. 2 *Diagram of switch signals generation*

is used to activate the switch Q_1 and Q_2 for boost mode. Q_3 and Q_4 are switched with the duty cycle $d_2(t)$ for buck mode. Activation signals u_{1H} and u_{1L} are activated in a complementary manner while u_{2H} is set at 1 and u_{2L} is set at 0, in boost mode. Otherwise, u_{2H} and u_{2L} are activated in a complementary manner while u_{1H} is set at 1 and u_{1L} is set at 0, in buck mode. The duty cycles are computed considering a variable control $u \in [0, 2]$, where $u(t) = 1 + d_1(t)$ in boost mode and $u(t) = d_2(t)$ for buck mode [4]. In addition, the digital controller allows simple incorporation of the operational

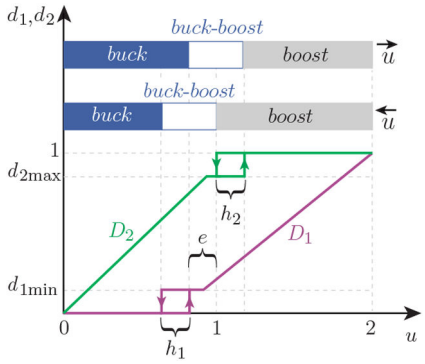


Fig. 3 *Scheme of the hysteretic transition method*

dead-zone avoidance technique [5] as shown in the switch signals generation of Fig. 2. The hysteretic method presented in [5] has been employed to avoid oscillations due to transition among different operating modes, i.e. buck, buck–boost and boost. Fig. 3 depicts the transition method. Hysteresis windows (h_1, h_2) are used to get smooth operating mode transitions. In order to operate the converter in a steady state, the duty cycles can be defined as $d_1(t) = D_1$ and $d_2(t) = D_2$. The operation modes are obtained varying u. When u is increased, the converter operates in buck mode for $0 \le u < 1 - e$, in buck–boost mode for $1 - e \le u < 1 + h_2$, in boost mode for $1 + h_2 \le u < 2$. Following the same process when u is decremented, the converter operates in boost mode for $1 \le u < 2$, in buck–boost mode for $1 - e - h_1 \le u < 1$ and buck mode for $0 \le u < 1 - e - h_1$. The following conditions should be fulfilled to set the hysteresis window widths:

$$h_1 > d_{1\min} \tag{1a}$$

$$h_2 > 1 - d_{2\max} \tag{1b}$$

$$e_{\min} = d_{1\min} + (1 - d_{2\max}) \tag{1c}$$

where $d_{1\min}$ is the minimum boost duty cycle, $d_{2\max}$ is the maximum buck duty cycle and $e_{\min}$ is the minimum value of the overlapping coefficient e.

Therefore, the converter operates either as a boost converter with output filter or as a buck converter with input filter, without the higher voltage stress on the switches of other step-up/step-down converter structures. The coupled inductors for the multiple-core approach buck–boost power stage can be designed following the transformer model in order to obtain a predictable coupling coefficient, as shown in Fig. 1*a*, where L_m is the magnetising inductance, L_o is the leakage inductance, and the coupled coefficient k is determined by $k = L_m/\sqrt{L_m(L_o + L_m)}$ [9]. In [4] coupled inductors with turns ratio $N_1/N_2 = 1$ and $k = 0.5$ resulted in identical control-to-output transfer functions for both operation modes (step-down or buck mode and step-up or boost mode). Accordingly, the dynamic characteristics of the output voltage and output current were continuous at the transition point between the boost and buck modes.

Coupled inductors can be defined and constructed in different ways. In the photovoltaic application reported in [24], the coupling coefficient is defined as $k = M/\sqrt{L_1 L_2}$, where M is the mutual inductance, and L_1 and L_2 are the self-inductances of the primary and the secondary coils, respectively. In both [24, 12], a 1:1 transformer was constructed with a pair of tightly coupled inductors of turns ratio $N_1/N_2 = 1$ and a magnetising inductance L_m. Two identical non-coupled inductors $L_a = L_b$ were connected in series with the primary and the secondary of the transformer, where $L_m = M$, $L_1 = L_a + M$ and $L_2 = L_b + M$, and therefore $L_1 = L_2$. The unusual symmetrical arrangement of three different magnetic elements was the form of mimicking two loosely coupled inductors with an equal number of turns coiled around a single core, such as the single-core approach Fig. 1*b*. It is composed of a pair of loosely coupled inductors with unitary turns ratio and magnetic coupling coefficient $k = 0.5$. Therefore, primary self-inductance L_1 is equal to secondary self-inductance L_2 ($L_1 = L_2 = L$), and their mutual inductance is $M = L/2$.

Two different power-stages correspondings with each of the coupled inductors approaches have been built. PS1 is the multiple-core bidirectional non-inverting buck–boost converter approach (Fig. 1*a*) with a pair of tightly coupled inductors $k \simeq 1$ and a non-coupled additional. On the other hand, PS2 is the proposed bidirectional non-inverting buck–boost converter with only one magnetic element (Fig. 1*b*), which is a pair of loosely coupled inductors (coupling coefficient $k = 0.5$). PS1 and PS2 are designed with the specifications of the buck–boost converter's parameters given in Table 2. The output current range is between −4 and 4 A. The input voltage range is between 200 and 400 V, and the output voltage range goes from 0 to 400 V. The switching frequency is 100 kHz. The components R_d and C_d of Fig. 1 can be calculated as in [4] with

$$R_d \simeq 0.65\sqrt{\frac{L_i}{C}}, C_d \ge 8C, \tag{2}$$

where $L_i = L_m$ for PS1 and $L_i = M$ for PS2. An important aspect affecting efficiency but required to obtain the minimum-phase desired dynamics is the power loss in R_d (P_{Rd}), which is analysed in [9]. Dissipated power P_{Rd} depends on the amplitude of the voltage ripple, Δv_c, at the intermediate capacitor as

$$P_{Rd} = \frac{\Delta v_c^2}{12R_d}, \tag{3}$$

assuming a ripple of triangular shape so that its rms value can be estimated easily. The expressions to calculate peak-to-peak ripples of currents and voltages are listed in Table 3, where T is the switching period, and D_1 and D_2 are the steady-state duty cycles in boost mode and buck mode, respectively. Table 2 shows the description and values for each power stage components selected for its implementation.

2.1 Buck–boost converter PS1 design

The design of PS1 was presented in [23] for a high-voltage application. In [23], the non-inverting dc–dc converter has been designed to regulate the power flow between the battery and the dc input of the EV inverter drive following the design procedure described in [4]. The converter is designed to regulate $V_o = 350$ V in the dc-link voltage, with $V_g = 200$ V. The value of peak-to-peak current ripples for input and output converter are calculated, taking into account the nominal power of the system, which is 1.6 kW, its values corresponding to 100% of the mean current values. The value of i_{Lm} is the difference between i_g and i_L in (Fig. 1*a*). Therefore the peak-to-peak current ripples values are: $\Delta i_L = 4$, $\Delta i_g = 7$ and $\Delta i_{Lm} = 3$ A. The peak-to-peak voltage ripple established for the intermediate capacitor is $\Delta v_c = 15$ V and the power loss desired for R_d is $P_{Rd} = 2$ W. The steps to calculate the

Table 2 Selected components and parameters for the buck–boost converter

Common parameters for PS1 and PS2	Value or type
input voltage V_g	200–400 V
output voltage V_o	100–400 V
rated power	1.6 kW
switching frequency $f_s = 1/T$	100 kHz
output capacitor C_o	28 μF
intermediate capacitor C	4 × R76PN33304030 J
multiple-core approach (PS1)	Value or type
coupled inductor	$M = L_m = 285\,\mu$H core: 77908 magnetics number of turns: 93 wire size: 18-AWG coupling coefficient 1
non-coupled inductor	$L_o = 214\,\mu$H core: 77191 magnetics number of turns: 65 wire size: 18-AWG
global coupling coefficient k_2	0.75
damping resistance R_d	BPR10100J, 10 Ω, 10 W, 500 V
damping capacitor C_d	MKP1848S61070JP2C, 700 V, 10 μF
single-core approach (PS2)	value or type
coupled inductor	$M = L_m = 135\,\mu$H core: 77908 magnetics number of turns: 80 wire size: 18-AWG $L_1 = L_2 = 270\,\mu$H
global coupling coefficient k_3	0.5
damping resistance R_d	2 × BPR10100J in parallel, 10 W, 500 V, 5 Ω
damping capacitor C_d	MKP1848S62070JP2F, 700 V, 20 μF

Table 3 Peak-to-peak ripple amplitudes for PS1 and PS2

	Buck mode	Boost mode
PS1		
Δi_L	$\frac{(V_g - V_o)V_o T}{V_g L_o}$	$\frac{V_g(V_o - V_g)T}{V_o L_o}$
Δi_{Lm}	0	$\frac{V_g(V_o - V_g)T}{V_o L_m}$
Δv_c	$\frac{(V_g - V_o)V_o^2 T}{V_g^2 R_o C}$	$\frac{(V_o - V_g)T}{R_o C}$
PS2		
Δi_L	$\frac{V_o T(V_g - V_o)L}{V_g(L^2 - M^2)}$	$\frac{V_g T(V_o - V_g)M}{V_o(L^2 - M^2)}$
Δi_g	$\frac{V_o T(V_g - V_o)M}{V_g(L^2 - M^2)}$	$\frac{V_g T(V_o - V_g)L}{V_o(L^2 - M^2)}$
Δv_c	$\frac{D_2 I_L}{C} T(D_2 - 1)$	$\frac{D_1 I_L}{C} T$

component values of the buck–boost converter are explained in Algorithm 1 (see Fig. 4).

The resulting values from Algorithm 1 (Fig. 4) are $L_m = 285\,\mu$H, $C = 1.32\,\mu$F, $R_d = 10\,\Omega$ and $C_d = 10\,\mu$F. The value of the inductor L_o is calculated following the equation for Δi_L from Table 3 in boost mode and its value is 214 μH.

The state-space averaging (SSA) method to apply PS1 (Fig. 1*a*) leads to the following set of differential equations introduced in [4]:

$$\begin{aligned}
\frac{\mathrm{d}\bar{i}_{Lm}}{\mathrm{d}t}(t) &= \frac{(\bar{v}_g - \bar{v}_c(1 - \bar{d}_1))}{L_m} \\
\frac{\mathrm{d}\bar{i}_L}{\mathrm{d}t}(t) &= \frac{(\bar{v}_g - \bar{v}_c(1 - \bar{d}_1)) - (\bar{v}_o - \bar{v}_c\bar{d}_2)}{L_o} \\
\frac{\mathrm{d}\bar{v}_c}{\mathrm{d}t}(t) &= \frac{1}{C}\left(-\bar{i}_L\bar{d}_2 + (i_{Lm} + i_L)(-\bar{d}_1 + 1) - \frac{1}{R_d}(\bar{v}_c - \bar{v}_{cd})\right) \\
\frac{\mathrm{d}\bar{v}_{cd}}{\mathrm{d}t}(t) &= \frac{\bar{v}_c - \bar{v}_{cd}}{C_d R_d} \\
\frac{\mathrm{d}\bar{v}_o}{\mathrm{d}t}(t) &= \frac{\bar{i}_L}{C_o} - \frac{\bar{v}_o}{R_o C_o}
\end{aligned} \tag{4}$$

2.2 Buck–boost converter PS2 design

The component values for the buck–boost converter PS2 from Fig. 1*b* have been selected, taking into account the parameters of the converter's specification given in Table 2. In order to compare the two power stages, the design of PS2 maintains the same characteristic of the studied converter (PS1) in terms of size, material and cost. The power losses in R_d are $P_{Rd} = 4$ W. Using (5), the damping resistor selected is $R_d = 5\,\Omega$ with $\Delta v_c = 15$ V. Keeping the same value for the intermediate capacitor of $C = 1.32\mu$F, the values for C_d and M are selected using (4), being

1: **Input:** Δi_{Lm}, P_{Rd}, V_o, V_g, f_s, Δv_c value

2: Find L_m from Δi_{Lm} equation from Table 2 in boost mode.

3: Find R_d,from Eq. 3.

4: Compute C and C_d using Eq. 2 .

5: **Output:** L_m, C, R_d and C_d values.

Fig. 4 *Algorithm 1: buck–boost PS1 design*

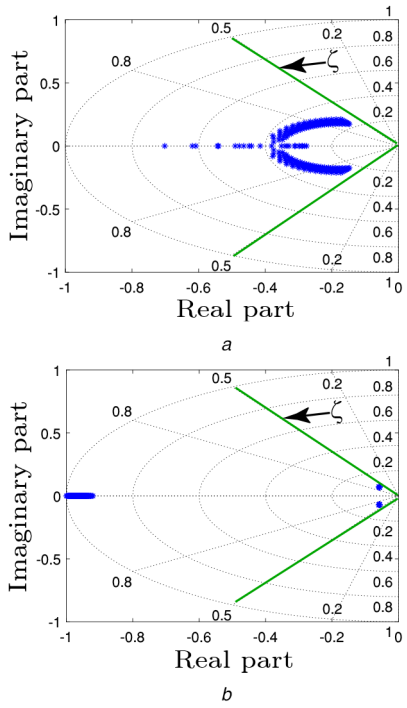


Fig. 5 *Roots of the characteristic polynomial of the PS2 converter*
(a) Boost mode, ***(b)*** Buck mode

$M = 135\,\mu$H and $C_d = 20\,\mu$F. The value for L is according with the coupled inductor design and is explained in the next section. Equations (4) and (5) have been used for the converter model studied in [4, 23]. To study the internal dynamics of the converter for the component values selected, the transfer functions from the input signals to the output voltage are found. In order to ensure that the internal system dynamics is sufficiently damped, the polynomials from the transfer functions are tested for different operating points of the converter. Therefore, the damping coefficients of the complex zeros have to be >0.5 ($\zeta > 0.5$). The small-signal state-state vector $\bar{\boldsymbol{x}}$ is defined as $\bar{\boldsymbol{x}} = [\bar{i}_g, \bar{i}_L, \bar{v}_c, \bar{v}_{cd}, \bar{v}_o]^T$, where $\bar{i}_g$ and $\bar{i}_L$ are the averaged input and output currents, respectively, $\bar{v}_c$ is the averaged voltage in the intermediate capacitor, $\bar{v}_{cd}$ is the averaged voltage in the damping capacitor and $\bar{v}_o$ is the averaged output voltage. The input vector is $\bar{\boldsymbol{d}} = [\bar{d}_1, \bar{d}_2]$. A continuous conduction mode (CCM) operation for the converter is considered in the analysis. Using the differential equations of the state variables expressed in [24] and the use of the SSA method to the following expressions for the state variables of the proposed converter from Fig. 1*b*:

$$
\begin{aligned}
\frac{\mathrm{d}\bar{i}_g}{\mathrm{d}t}(t) &= \frac{L\big(\bar{v}_g - \bar{v}_c(1-\bar{d}_1)\big) - M\big(\bar{v}_o - \bar{v}_c\bar{d}_2\big)}{L^2 - M^2} \\
\frac{\mathrm{d}\bar{i}_L}{\mathrm{d}t}(t) &= \frac{M\big(\bar{v}_g - \bar{v}_c(1-\bar{d}_1)\big) - L\big(\bar{v}_o - \bar{v}_c\bar{d}_2\big)}{L^2 - M^2} \\
\frac{\mathrm{d}\bar{v}_c}{\mathrm{d}t}(t) &= \frac{1}{C}\Big(-\bar{i}_L\bar{d}_2 + i_g\big(-\bar{d}_1 + 1\big) - \frac{1}{R_d}(\bar{v}_c - \bar{v}_{cd})\Big) \\
\frac{\mathrm{d}\bar{v}_{cd}}{\mathrm{d}t}(t) &= \frac{\bar{v}_c - \bar{v}_{cd}}{C_d R_d} \\
\frac{\mathrm{d}\bar{v}_o}{\mathrm{d}t}(t) &= \frac{\bar{i}_L}{C_o} - \frac{\bar{v}_o}{R_o C_o}
\end{aligned}
\tag{5}
$$

The transfer functions from the input signals to the output voltage are found, as follows:

$$G_{v_o d_1} = \frac{\bar{v}_o(s)}{\bar{d}_1(s)} \text{ when } D_2 = 1 \text{ in boost mode}$$

$$G_{v_o d_2} = \frac{\bar{v}_o(s)}{\bar{d}_2(s)} \text{ when } D_1 = 0 \text{ in buck mode}$$

The component values are evaluated, testing the transfer functions $G_{v_o d_1}$ and $G_{v_o d_2}$, taking into account that the zeros must be sufficiently damped. In boost mode, the numerator of $G_{v_o d_1}(s)$ is a third-degree polynomial (8)

$$s^3 + \sigma_2 s^2 + \sigma_1 s + \sigma_0 \tag{6}$$

where

$$\sigma_0 = -\frac{1}{CC_d R_d M}(D_1 - 1)$$

$$\sigma_1 = \frac{I_L}{CC_d R_d V_g}\Big(\frac{-L}{M} + (1 - D_1)\Big) + (1 - D_1)\frac{1}{MC}$$

$$\sigma_2 = \frac{1}{R_d}\Big(\frac{1}{C_d} + \frac{1}{C}\Big) + \frac{I_L}{CV_g}$$

and for buck mode, the numerator of $G_{v_o d2}(s)$ is

$$s^3 + \rho_2 s^2 + \rho_1 s + \rho_0 \tag{7}$$

where

$$
\begin{aligned}
\rho_0 &= \frac{1}{CC_d L R_d} \\
\rho_1 &= \frac{1}{CL} + \frac{I_L}{V_g R_d C_d C}\Big(\frac{M}{L} - D_2\Big) \\
\rho_2 &= \frac{1}{R_d}\Big(\frac{1}{C_d} + \frac{1}{C}\Big) + \frac{I_L}{CV_g}\Big(\frac{M}{L} - D_2\Big)
\end{aligned}
\tag{8}
$$

The components values listed in Table 2 for PS2 are used to evaluate the internal dynamics of the system. The roots of the polynomial characteristic in boost mode (8) are plotted in Fig. 5*a*, setting $V_g = 200$ V with the output current range $I_L = [1, 8]$ A and duty cycle range $D_1 = [0, 0.5]$, with step variations of 1 A and 0.003, respectively. Test for buck mode is realised with $V_g = 400$ V. The root values of the polynomial characteristic (9) for the same I_L range and duty cycle range $D_2 = [0.25, 1]$, with the same step variations, are represented in Fig. 5*b*. To plot the roots values, these were normalised respect to the natural frequency $\omega_n = 1/\sqrt{MC}$, as in [12]. The normalised converter parameters are expressed as: $C_{dn} = C_d/C$ and $R_{dn} = CR_d\omega_n$. Fig. 5 shows that the internal system dynamics is sufficiently damped for the components selected, where the complex zeros are below the upper limit for a damping coefficient higher than 0.5.

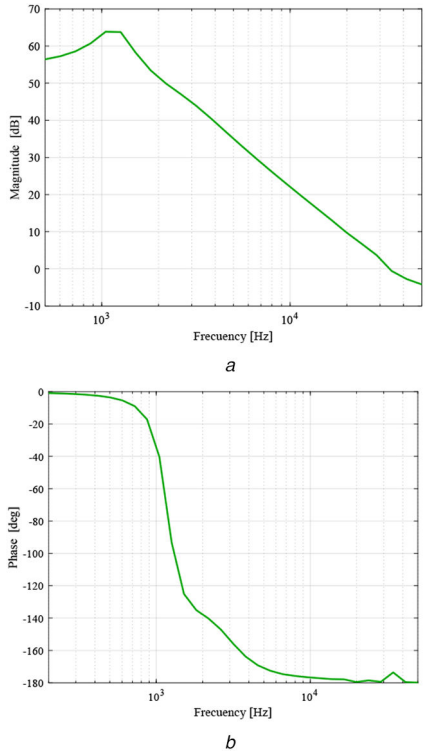


Fig. 6 *Frequency response of the small-signal control-to-output transfer function. Simulation of the switched model using PSIM in boost mode*
(a) Magnitude [dB], ***(b)*** Phase [deg]

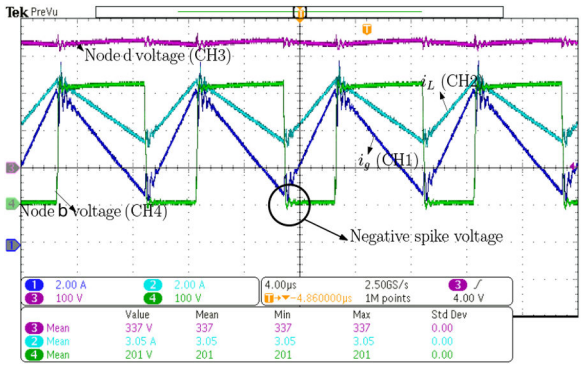


Fig. 7 *Switching node voltage in power converter*

The Bode plots of frequency responses obtained from the switched converter in PSIM are depicted in Fig. 6.

The maximum frequency plotted is half of the switching frequency. The frequency responses and the roots of the polynomial of the small-signal to output transfer function (Fig. 5) show the system with no RHP zeros, as seen in [7, 8]. Its dynamic is similar to that of a transfer function with two complex conjugate poles and no zeros, therefore the buck–boost converter can be controlled as a buck converter.

2.3 Transient voltage protection of high gate driver and MOSFETs

The MOSFET driver used in the implementation of PS1 and PS2 is the UCC27714 (high and low sides). In order to eliminate the negative return spike in the high-side floating voltage supply of pin (HS), the recommendation exposed in [25] has been followed. Fig. 7 shows the input and output currents, and the intermediate node for each half-bridge MOSFETs, when the boost node (node *b* voltage) is switching. A negative spike voltage is seen. The UCC27714 driver can keep a logical operation with negative voltage up to −8 V on HS pin. Nonetheless, a negative spike with values below this limit can cause erratic operation. Selecting a series gate resistor value of $R_1 = 10\,\Omega$, this value of resistor allows

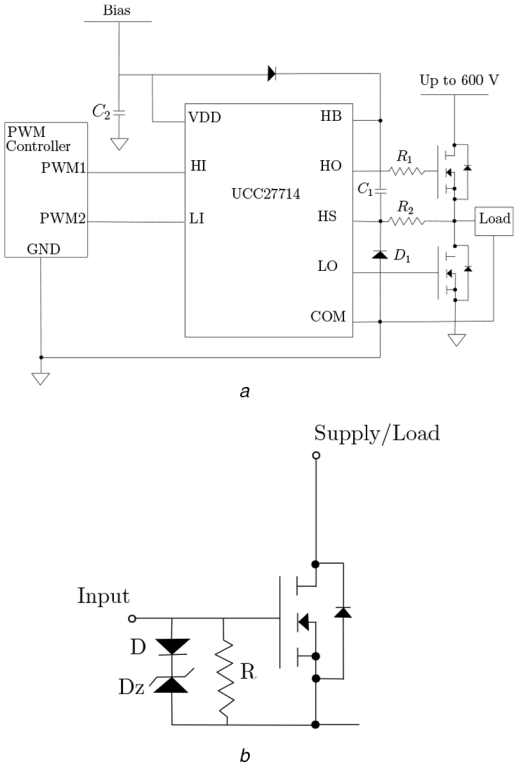


Fig. 8 *Diagram of*
(a) Circuit schematic driver, ***(b)*** Transient voltage MOSFET protection

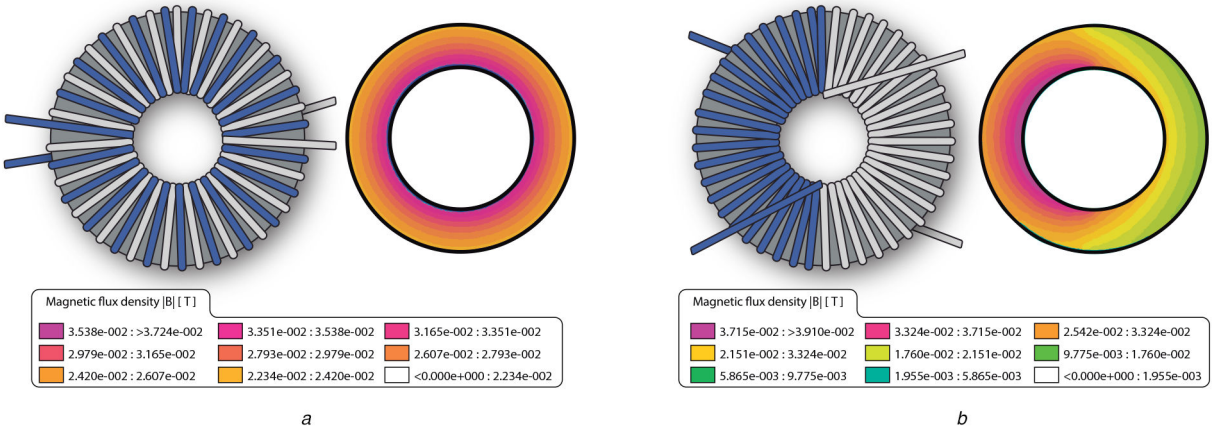
a high switch speed and a decrease in the amplitude of the negative spike. A fast power diode D1 is set between the HS and the COM pin, besides a resistor $R_2 = 5\,\Omega$ to limit the current across the diode. These elements are added to the basic schematic of the MOSFET driver, as shown in Fig. 8*a*. On the other hand, for transient voltages on the gate-source MOSFET, a diode and a Zener diode of 16 V are used, both connected in series to protect the MOSFET. Moreover, to limit the voltage in V_{gs}, $R = 47\,\text{k}\Omega$ was chosen. The schematic representation of this protection is shown in Fig. 8*b*.

3 Coupled inductors design

The transformer model parameters of the non-symmetrical coupled inductors in PS1 are $L_1 = L_m$, $L_2 = L_o + L_m$, and $M = L_m$. As shown in Fig. 9*a*, a tightly coupled inductors pair (coupling coefficient $k_1 \simeq 1$) have been built by coiling around a toroidal core, in the uniform interleaved arrangement, an equal number of turns ($N_1 = N_2 = 93$) of 18-AWG copper wire for both windings. The core is a Magnetics 77908 toroid with a relative permeability coefficient of $\mu_r = 26$. A non-coupled inductor $L_o = 214\,\mu\text{H}$ (shown in Fig. 1*a*), built by winding 65 turns of 18-AWG copper wire around a Magnetics 77191 core, has been associated in series with the secondary winding. The equivalent transformer model of the arrangement has a global coupling coefficient

$$k_2 = \frac{M}{\sqrt{L_1 L_2}} = \frac{L_m}{\sqrt{L_m(L_o + L_m)}} \simeq 0.75$$

To decrease the parasitic capacitance value between primary and secondary windings, the pair of coupled inductors of PS2 ($N_1/N_2 = 1$, $N_1 = N_2 = 80$ turns) is built, increasing the distance between the windings [26]. It has an experimental coupling coefficient $k_3 = 0.5$ and was constructed, as depicted in Fig. 9*b*, where each 18-AWG copper coil occupies one half of a Magnetics 77908 toroidal core. The flux density maps in the cores of both implementations shown in Fig. 9 have been obtained using a two-dimensional finite element method (2D-FEM) FEMM 4.2 software. For the coupled inductors of PS1, the flux linkages in the primary and secondary windings for a primary current $I_1 = 4$ A and keeping the secondary in open circuit, were $\phi_1 = 1.131$ mWb and



a *b*

Fig. 9 *Flux density map of the coupled inductors modelled using FEMM*
(a) Multiple-core approach, ***(b)*** Single-core approach

Table 4 Winding-to-winding capacitance of the coupled inductors

Frequency, kHz	Capacitance wind1-wind2	
	PS1, pF	PS2, pF
63.10	14,530	76.44
89.13	14,510	76.45
125.89	14,510	71.24
177.83	14,520	70.04

$\phi_2 = 1.124$ mWb, respectively. Therefore, the primary self-inductance is $L_1 = \phi_1/I_1 = 282\,\mu$H and the mutual inductance is $M = \phi_2/I_1 = 280\,\mu$H. A similar process was used to find the self-inductance of the secondary, getting $L_2 = 280\,\mu$H. Therefore, the simulated result of the coupling coefficient was $k \simeq 1$. As expected from the interleaved arrangement, the distribution of the flux density in the core of Fig. 9*a* is uniform, whereas it is not uniform in the core of Fig. 9*b*, where there is also an important flux leakage. Simulated values of $L_1 = L_2 = 280$ and $M = 208\,\mu$H were obtained, with a corresponding coupling coefficient of $k_3 = 0.74$. However, in this case the parameters obtained from simulations are different from those extrapolated from the slopes of the current ripples shown in Table 3 ($L_1 = L_2 = 270$, $M = 135\,\mu$H, and $k_3 = 0.5$). The common and specific parameters of the buck–boost power stages are summarised in Table 2. This is because the real flux leakage is higher than the one suggested by the 2D-FEM inductor model.

4 Parasitic winding-to-winding capacitance analysis

Measurements of the parasitic winding-to-winding capacitance of the coupled inductors were performed using a QuadTech 1910 LCR meter. The measurements taken at different frequencies are listed in Table 4. For all the frequencies, the value of the parasitic capacitor is $C_p \simeq 15$ nF for the coupled inductor with k_1, a quite large value explained by the highly interleaved winding arrangement required to have tight magnetic coupling.

Considering boost mode, in each switching cycle, the parasitic capacitor is charged up to the output voltage and discharged completely to zero volts. When the converter works in buck mode, the parasitic capacitor voltage evolves between the input voltage and zero volts. Assuming that all the energy stored in the parasitic capacitor

$$W = C_p \frac{V^2}{2} \tag{9}$$

is lost, when the voltage applied across the switch is 400 V and $f_s = 100$ kHz, the power loss reaches 120 W. On the other hand, the measured parasitic capacitance for the coupled inductors with k_3 used in PS2 is $C_p \simeq 71$ pF. Hence, the power loss will be greatly reduced using the proposed implementation in high-voltage applications. LTspice simulations have been developed to roughly predict the power loss associated to the winding-to-winding parasitic capacitance of the coupled inductors. In addition to the previous capacitance values, the simulation uses the parameters of Table 2, an almost ideal switch (SW) with only on-resistance, and $V_o = 400$ V. Fig. 10 shows the simulated results of current and voltage across SW that represents the low-side MOSFET (Q_2) when the converter is working in boost mode. Fig. 10*a* corresponds to PS1 with a parasitic capacitance of 15 nF connected between the *b* and *d* nodes (see Fig. 1). Each switching period, the 15 nF capacitor is discharged exponentially through the switch ($R_{on1} = 100\,\text{m}\Omega$, $T_{on} = 5\,\mu$s) with a peak current near to 4 kA (400 V/R_{on}) in about 8 ns, with a simulated total power loss of 159 W. The switch current and voltage in Fig. 10*b* correspond to PS2 with a 71 pF parasitic capacitor between the same nodes. Here, because of a larger on-resistance switch ($R_{on2} = 450\,\text{m}\Omega$), the current peak is reduced to 880 A. In spite of the larger on-resistance, the capacitor is discharged in just 160 ps, 50 times faster than in Fig. 10*a*. The simulated power dissipated in PS2 is 50 W, mainly due to conduction and damping resistor losses. Thermal imaging in Fig. 11 confirmed that this power is mainly dissipated by the low-side MOSFET (Q_2) of the switching half-bridge when the prototype PS1 is working in boost mode.

5 Digital current regulation

Regulation of the converter is done by means of a digital controller that integrates the hysteretic transition method. The output current of the converter is controlled using the Multisample Average Current Control (MACC) strategy [11]. The analysis for PS1 and PS2 presented for the small model in (4) and (5) allows us to find the converter's current output slope $\text{d}i_L/\text{d}t$ in each operation mode (buck or boost) for designing the digital current programmed controller (MACC). The output current has a periodic triangular waveform where the current rises with a slope of m_1 and falls with a slope $-m_2$. Table 5 presents the converter output current waveform slopes based on the equation for $\text{d}i_L/\text{d}t$ from (4) and (5) for the boost and buck modes.

The schematic diagram of the two-loop control using the MACC method is depicted in Fig. 12. The controller obtains the variable control u for the output voltage regulation; the external

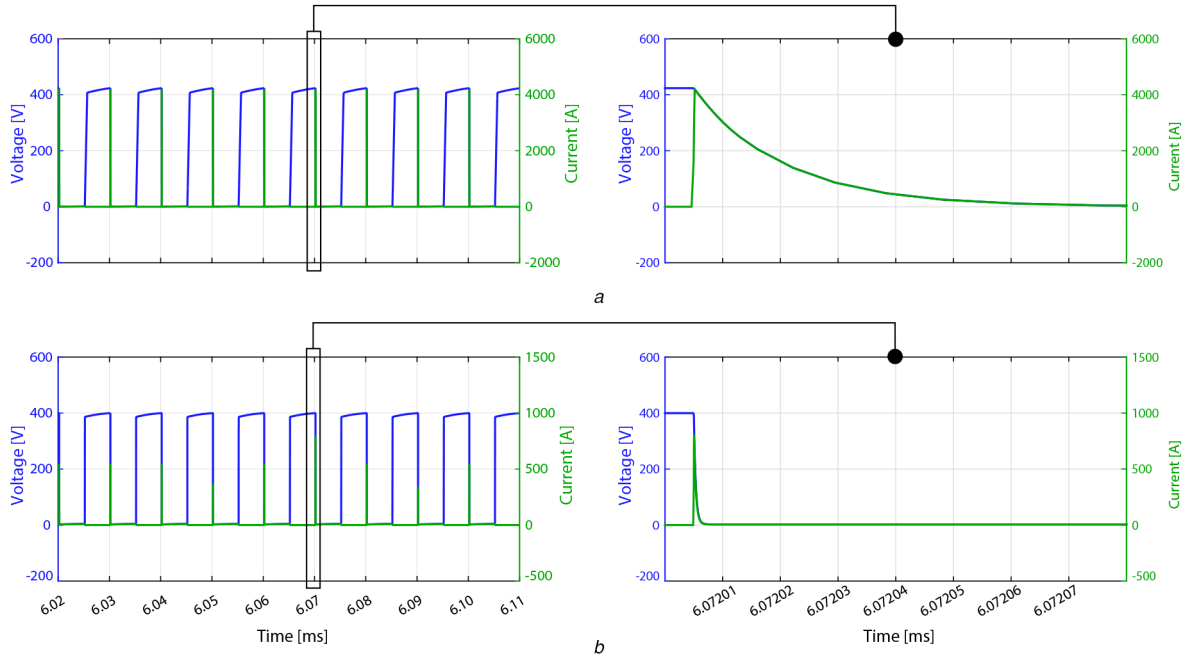


Fig. 10 *Simulated results of current and voltage across the SW Q_2 for boost mode using LTspice*
(a) Multiple-core approach (PS1), ***(b)*** Single-core approach (PS2)

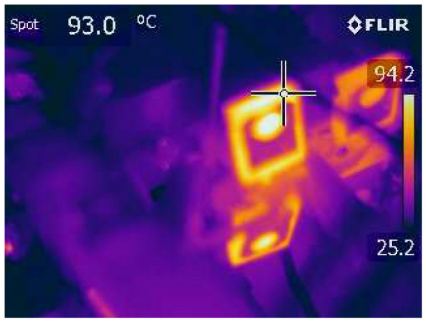


Fig. 11 *Thermal image of the half-bridge MOSFET boost side*

Table 5 Slope of the output current waveform

PS1	m_1	$-m_2$
buck	$\frac{(V_g - v_o)}{L_o}$	$\frac{(V_g - v_c - v_o}{L_o}$
boost	$\frac{V_g - v_o + v_c)}{L_o}$	$\frac{(V_g - v_o)}{L_o}$
PS2	m_1	$-m_2$
buck	$\frac{M(V_g - v_c) - L(v_o - v_c)}{L^2 - M^2}$	$\frac{M(V_g - v_c) - Lv_o}{L^2 - M^2}$
boost	$\frac{MV_g - L(v_o - v_c)}{L^2 - M^2}$	$\frac{M(V_g - v_c) - L(v_o - v_c)}{L^2 - M^2}$

loop provides the reference of the output current using a discrete PI control transfer function $G_{vpi}(z)$. In this method, a ripple filter is used to obtain an average current from the samples of the output current $i_L[n]$. The ripple filter produces the average of current error values corresponding to two samples per switching period ($f_{\text{samp}} = 2f_s$), and is used to bring the average current to their desired reference $i_{L\text{ref}}[n]$.

The expression for the ripple filter in the z-domain can be represented as follows:

$$G_f(z) = K_p\left(1 + \frac{K_a}{4}\frac{z+1}{z-1}\right)\left(1 - z^{-2}\right) \tag{10}$$

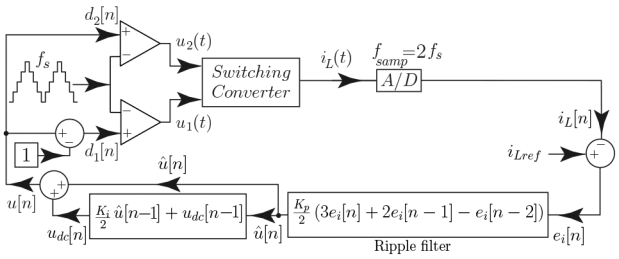


Fig. 12 *Schematic diagram of the two-loop control using MACC method*

where the value of the constant K_a is 2. This value is suggested in [11]. The resulting expression for the ripple filter replacing the value of K_a and collecting terms is

$$G_f(z) = K_p\left(\frac{3}{2} + \frac{1}{z} - \frac{1}{2z^2}\right). \tag{11}$$

This ripple filter transfer function can be expressed as a differential equation as

$$\hat{u}[n] = \frac{K_p}{2}(3e_i[n] + 2e_i[n-1] - e_i[n-2]). \tag{12}$$

The proportional gain can be written in terms of the output current waveform slopes shown in Table 5 as

$$K_p = \frac{K_n}{(m_1 + m_2)T} \tag{13}$$

where T is the switching period ($1/f_s$) and the expression $m_1 + m_2$ is obtained from Table 5 for each converter and for each operation mode, replacing $v_c = v_o$ for boost mode and $v_c = v_g$ for buck mode, obtaining for the converter PS1 the following expressions:

$$m_1 + m_2 = \begin{cases} \dfrac{V_o}{L_o} & \text{for boost mode} \\ \dfrac{V_g}{L_o} & \text{for buck mode} \end{cases} \tag{14}$$

and for the converter PS2

$$m_1 + m_2 = \begin{cases} \dfrac{MV_o}{L^2 - M^2} & \text{for boost mode} \\ \dfrac{LV_g}{L^2 - M^2} & \text{for buck mode} \end{cases} \quad (15)$$

The parameter K_n was adjusted to 0.35 to obtain a crossover frequency (CF) ~ 11 kHz as in [11].

A digital PI compensator in the z-domain is added to the current control loop and it is implemented using the forward-Euler method as follows:

$$G_{pi}(z) = 1 + \frac{K_i}{2}\frac{1}{z-1} \quad (16)$$

Fig. 12 shows the block diagram representation of the implemented difference equation corresponding to (16), where the integral gain can be chosen as in [11], hence the value for $K_i = 0.16$ was selected.

6 Experimental results

Converter prototypes controlled by a TMS320F28377S Digital Signal Control (DSC) were built with the coupled inductors and damping networks described previously. 100 mΩ ON-resistance C2M0080120D SiC MOSFETs have been used in PS1, while cheaper and faster SCT2450KEC SiC MOSFETs, with $R_{on2} = 450$ mΩ, have been used in PS2. The enhanced PWM module from Texas Instruments TMS320F28377S has been used to activate the signals for the MOSFETs switch. The parameters of the transition method (Fig. 3) used are adjusted, as follows: $d_{2max} = 0.99$, $d_{1min} = 0.01$, $e = 0.02$, $h_1 = 0.02$ and $h_2 = 0.02$.

Figs. 13*a* and *b* depict the waveforms in boost mode for the PS1 and PS2, respectively. The waveforms in buck mode for each power stage are shown in Figs. 13*c* and *d*. Peak-to-peak ripples in all waveforms are consistent with the theoretical values expected according to Table 3 and the parameters listed in Table 2. It is remarkable that the waveforms in Figs. 13*b* and *d* are free of commutation oscillations in contrast to those shown in Figs. 13*a* and *c*.

The experimental efficiencies measured at different operating points are shown in Figs. 14 and 15 for PS1 and PS2, respectively. The efficiencies were measured using a Yokogawa WT 3000 precision power analyser connected at the input and the output of the converter, and were taken with the converter working with $I_L = 4$ A. The energy conversion efficiencies are presented for two different input voltage V_g values, which correspond with 200 and 350 V. It is evident that PS2 has less power losses than PS1 in spite of using a SiC MOSFET with 4.5 times higher R_{on}, although the SCT2450KEC SiC MOSFET brings the benefit of less switching losses. The efficiency of the PS2 is higher than 95% over all the considered range of output power with a maximum value of 98% near to $v_o = 220$ V, when $V_g = 200$ V, and near to $v_o = 300$ V, when $V_g = 350$ V. Note that an efficiency decrease due to the buck–boost operation mode can be observed in Fig. 14, when $V_g = 200$ and $v_o = 220$ V. Unlike to modes buck and boost, in which only two MOSFETs are switching, in buck–boost mode, all four MOSFETs are switching, thus increasing switching losses. The same behaviour can be observed in Fig. 15 for values of the output voltage near to $v_o = 350$ V, when the input voltage is $V_g = 350$ V.

The power loss by C_p presented in Table 6 is calculated taken into account the energy stored in the parasitic capacitor using (11). In boost mode, C_p is charged at the output voltage v_o, therefore $V = v_o$ in (11) and this power is dissipated by the MOSFET Q_2. In buck mode, C_p is charged at the input voltage V_g, is $V = V_g$ in (11) and the stored energy is dissipated by the MOSFET Q_3. PS1 has a power loss of ~200 W when it works in boost mode with $V_o = 350$ and $V_g = 200$ V, and for buck mode with $V_o = 150$ and $V_g = 350$ V. The aforementioned power loss is in accordance to Fig. 16, where the power loss value of the curve with $V_g = 200$ V is similar to the power loss value of the curve with $V_g = 350$ V when the output voltage is near to 350 V. As it can be observed in Fig. 16, the power loss is nearly constant at all operating points when the converter operates on buck mode, because the parasitic winding-to-winding capacitance is always charged to V_g. When the power output of PS1 is <680 W with $V_g = 200$ V, the total power loss is minimised because C_p is charged at this input voltage, while when the converter operates below 1080 W with $V_g = 350$ V the

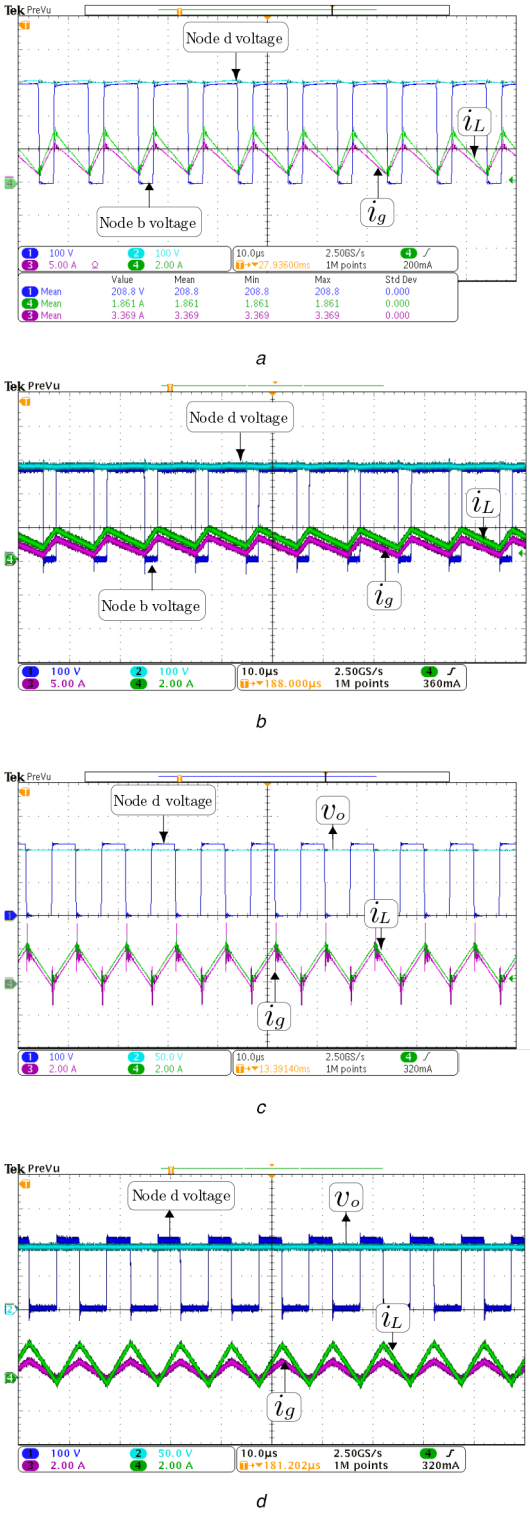


Fig. 13 *Experimental results*

(a, b) Waveforms in boost mode ($V_g = 200$ V, $v_o = 300$ V), ***(c, d)*** Waveforms in buck mode ($V_g = 200$ V, $v_o = 100$ V), ***(a)*** PS1, ***(b)*** PS2 with CH3: i_g (5 A/div), CH4: i_L (2 A/div), CH1: node *b* voltage (100 V/div), CH2: node *d* voltage (100 V/div) and time base of 10 µs, and ***(c)*** PS1, ***(d)*** PS2 with CH3: i_g (2 A/div), CH4: i_L (2 A/div), CH2: v_o (50 V/div), CH1: node *d* voltage (100 V/div) and time base of 10 µs

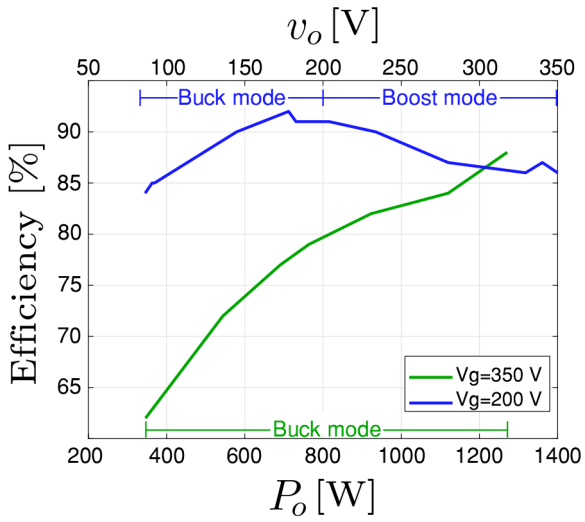


Fig. 14 *Energy conversion efficiency for two different values of V_g (200 V and 350 V) with a $I_L = 4$ A as a function of the output power P_o for PS1*

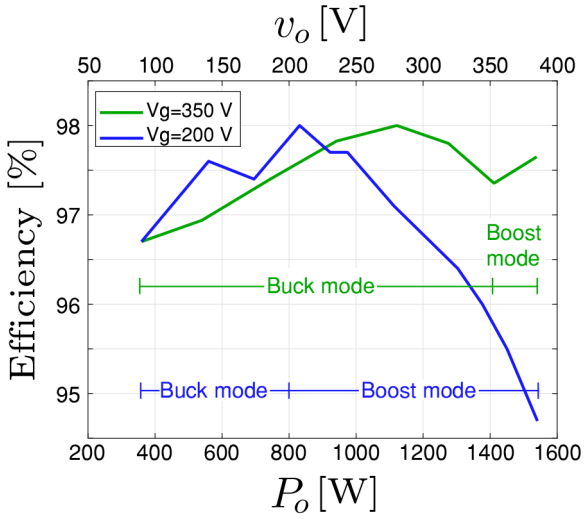


Fig. 15 *Energy conversion efficiency for two different values of V_g (200 V and 350 V) with a $I_L = 4$ A as a function of the output power P_o for PS2*

Table 6 Power loss comparison

Power loss for $V_g = 200$ V and $V_o = 150$ V	PS2	PS1
power loss experimental	14.64 W	64 W
power loss LTspice simulated	15.36 W	56 W
power loss by C_p (theoretical estimate)	142 mW	32 W
power loss for $V_g = 200$ V and $V_o = 350$ V	PS2	PS1
power loss experimental	63 W	227 W
power loss LTspice simulated	41 W	124 W
power loss by C_p (theoretical estimate)	434 mW	92 W
power loss for $V_g = 350$ V and $V_o = 150$ V	PS2	PS1
power loss experimental	17 W	213 W
power loss LTspice simulated	12 W	171 W
power loss by C_p (theoretical estimate)	434 mW	92 W

total power loss increases because C_p is charged at 350 V. Fig. 17 shows the improved performance of PS2 at high voltages, which is mainly due to the important reduction of the losses associated with the much smaller parasitic winding-to-winding capacitance.

7 Conclusion

In this paper, the non-inverting bidirectional dc–dc converter with coupled inductors is proposed for high-voltage applications in

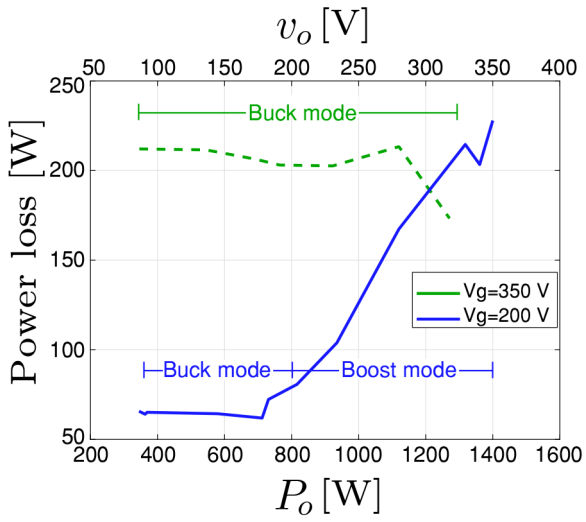


Fig. 16 *Total power loss for PS1*

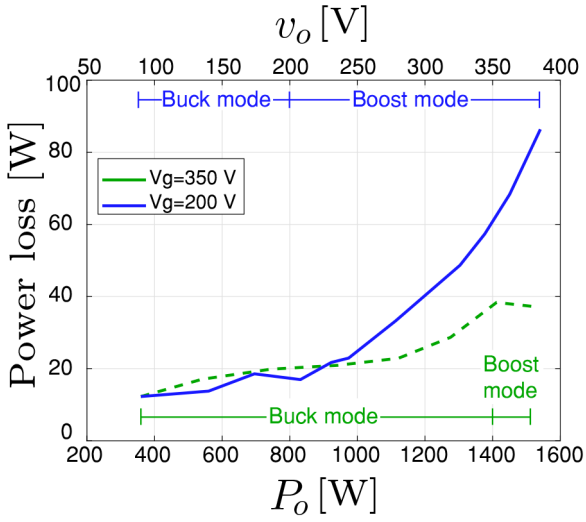


Fig. 17 *Total power loss for PS2*

which the dc–dc converter can operate either in boost mode or in buck mode with hard switching at 100 kHz. Two 1.6 kW prototypes with an input voltage range of 200–400 V, and an output voltage between 100 and 400 V have been built to analyse the efficiency of the system. Coupled inductors in the first prototype (PS1), implemented following a procedure previously reported in low-voltage applications, used two magnetic cores and exhibited high winding-to-winding capacitance that resulted in high-switching losses and, therefore low efficiency. The second prototype (PS2) has been improved to reduce the switching losses by using coupled inductors modified to achieve very low parasitic winding-to-winding capacitance and loose magnetic coupling requiring only one toroidal magnetic core. Adapting the power stage-damping network to the new parameters of the loosely coupled inductors has been straightforward. Experimental results demonstrate that the proposed converter is suitable for high efficiency, high-voltage wide-gain-range applications, thanks to the use of more appropriate SiC devices and improved coupled inductors that reduce switching losses.

8 Acknowledgment

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9 References

[1] Chen, H., Kim, H., Erickson, R., *et al.*: 'Electrified automotive powertrain architecture using composite DC–DC converters', *IEEE Trans. Power Electron.*, 2016, **3**, (1), pp. 98–116

[2] Estima, J.O., Cardoso, A.J.: 'Efficiency analysis of drive train topologies applied to electric/hybrid vehicles', *IEEE Trans. Power Electron.*, 2012, **61**, (3), pp. 1021–1031

[3] Zhang, Y., Gao, Y., Zhou, L., *et al.*: 'A switched-capacitor bidirectional DC–DC converter with wide voltage gain range for electric vehicles with hybrid energy sources', *IEEE Trans. Power Electron.*, 2018, **33**, (11), pp. 9459–9469

[4] Restrepo, C., Calvente, J., Cid-Pastor, A., *et al.*: 'A non-inverting buck-boost dc-dc switching converter with high efficiency and wide bandwidth', *IEEE Trans. Power Electron.*, 2011, **26**, (9), pp. 2490–2503

[5] Restrepo, C., Konjedic, T., Calvente, J., *et al.*: 'Hysteretic transition method for avoiding the dead-zone effect and subharmonics in a non-inverting buck–boost converter', *IEEE Trans. Power Electron.*, 2015, **30**, (6), pp. 3418–3430

[6] Jin, X., Wang, L., Yu, D., *et al.*: 'Pulse train controlled single-input dual-output buck converter with coupled inductors', *IEEE Access*, 2018, **6**, pp. 341–504o–41 517

[7] Calvente, J., Martinez-Salamero, L., Valderrama, H., *et al.*: 'Using magnetic coupling to eliminate right half-plane zeros in boost converters', *IEEE Power Electron. Lett.*, 2004, **2**, (2), pp. 58–62

[8] Calvente, J., Martinez-Salamero, L., Garces, P., *et al.*: 'Zero dynamics-based design of damping networks for switching converters', *IEEE Trans. Aerosp. Electron. Syst.*, 2003, **39**, (4), pp. 1292–1303

[9] Sanchis, E., Maset, E., Ferreres, A., *et al.*: 'Bidirectional high-efficiency nonisolated step-up battery regulator', *IEEE Trans. Aerosp. Electron. Syst.*, 2011, **47**, (3), pp. 2230–2239

[10] Ramírez-Murillo, H., Restrepo, C., Calvente, J., *et al.*: 'Energy management of a fuel-cell serial-parallel hybrid system', *IEEE Trans. Ind. Electron.*, 2015, **62**, (8), pp. 5227–5235

[11] Restrepo, C., Konjedic, T., Flores-Bahamonde, F., *et al.*: 'Multisampled digital average current controls of the versatile buck-boost converter', *IEEE J. Emerging Sel. Topics Power Electron.*, 2018, **7**, (2), pp. 879–890

[12] Mendez-Diaz, F., Pico, B., Vidal-Idiarte, E., *et al.*: 'HM/PWM seamless control of a bidirectional buck-boost converter for a photovoltaic application', *IEEE Trans. Power Electron.*, 2019, **34**, (3), pp. 2887–2899

[13] Wang, H., Wu, W., Gao, N., *et al.*: 'Modified dual buck–boost AC/DC converter with self-balanced DC output voltages', *IET Power Electron.*, 2019, **12**, (10), pp. 1170–1178

[14] Narasimharaju, B.L., Dubey, S.P., Singh, S.P.: 'Design and analysis of coupled inductor bidirectional DC–DC convertor for high-voltage diversity applications', *IET Power Electron.*, 2012, **5**, (7), pp. 998–1007

[15] Hwu, K.I., Peng, T.J.: 'High-voltage-boosting converter with charge pump capacitor and coupling inductor combined with buck–boost converter', *IET Power Electron.*, 2014, **7**, (1), pp. 177–188

[16] Yang, C., Shaojun, X.I.E., Mao, L., *et al.*: 'Efficiency improvement on two-switch buck-boost converter with coupled inductor for high-voltage applications', *IET Power Electron.*, 2014, **7**, (11), pp. 12846–12856

[17] Restrepo, C., Calvente, J., Romero, A., *et al.*: 'Current-mode control of a coupled-inductor buck–boost dc–dc switching converter', *IEEE Trans. Power Electron.*, 2011, **27**, (5), pp. 2536–2549

[18] Nathan, K., Ghosh, S., Siwakoti, Y., *et al.*: 'A new DC–DC converter for photovoltaic systems: coupled-inductors combined cuk-SEPIC converter', *IEEE Trans. Energy Convers.*, 2018, **34**, (1), pp. 191–201

[19] He, L., Xu, X., Chen, J., *et al.*: 'A plug-play active resonant soft switching for current-auto-balance interleaved high step-up DC/DC converter', *IEEE Trans. Power Electron.*, 2018, **34**, (8), pp. 7603–7616

[20] Zhang, Y., Cheng, X.F., Yin, C., *et al.*: 'A soft-switching bidirectional DC–DC converter for the battery super-capacitor hybrid energy storage system', *IEEE Trans. Ind. Electron.*, 2018, **65**, (10), pp. 7856–7865

[21] He, L., Zheng, Z., Guo, D.: 'High step-up DC–DC converter with active soft-switching and voltage-clamping for renewable energy systems', *IEEE Trans. Power Electron.*, 2018, **33**, (11), pp. 9496–9505

[22] Park, S., Rivas-Davila, J.: 'Isolated resonant dc-dc converters with a loosely coupled transformer'. 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), Stanford, CA, USA, 2017, pp. 1–7

[23] González-Castaño, C., Vidal-Idiarte, E., Calvente, J.: 'Design of a bidirectional dc/dc converter with coupled inductor for an electric vehicle application'. IEEE Int. Symp. Industrial Electronics (ISIE), Edinburgh, UK, June 2017, pp. 688–693

[24] Mendez-Diaz, F., Ramirez-Murillo, H., Calvente, J., *et al.*: 'Input voltage sliding mode control of the versatile buck-boost converter for photovoltaic applications'. IEEE Int. Conf. Industrial Technology (ICIT), Seville, Spain, March 2015, pp. 1053–1058

[25] Kiraly, L.: 'Solving noise problems in high power, high frequency control IC driven power stages'. International Rectifier Design Tips

[26] Nguyen-Duy, K., Ouyang, Z., Knott, A., *et al.*: 'Minimization of the transformer inter-winding parasitic capacitance for modular stacking power supply applications'. 16th European Conf. on Power Electronics and Applications, Lappeenranta, Finland, August 2014, pp. 1–10