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Dynamic Simulation of a-IGZO TFT Circuits Using the Analytical Full Capacitance Model (AFCM)

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ABSTRACT The Analytical Full Capacitance Model (AFCM) for amorphous oxide semiconductors thin film transistors (AOSTFTs) is first validated, using a 19-stages Ring Oscillator (RO) fabricated and measured. The model was described in Verilog-A language to use it in a circuit simulator in this case SmartSpice from Silvaco. The model includes the extrinsic effects related to specific overlap capacitances present in bottom-gate AOSTFT structures. The dynamic behavior of the simulated circuit, when the TFT internal capacitances are increased or decreased and for different supply voltages of 10, 15 and 20 V, is compared with measured characteristics, obtaining a very good agreement. Afterwards, the AFCM is used to simulate the dynamic behavior of a pixel control circuit for a light emitting diode active matrix display (AMOLED), using an AOSTFT.

INDEX TERMS Circuit simulator, dynamic model, Verilog-A, capacitances model.

I. INTRODUCTION

Amorphous oxide semiconductors thin film transistors, (AOSTFTs) are already replacing other TFT devices, in applications as flat panel displays controllers. Among these TFTs, a-IGZO TFTs present important advantages, with high mobility values, above 10 cm^2/Vs, maintaining lower fabrication cost [1]–[4]. The AOSTFTs have also been studied for other digital, as well as analog applications. For these reasons, it is very important to develop specific AC/DC models for these TFTs, capable of reproducing with sufficient precision, their behavior under different conditions.

order to simulate real circuits based in the new and promise devices.

Recently, we presented and validated a current-voltage (I-V) model [5] as well as, a specific analytical full capacitance-voltage model (AFCM) for bottom gate staggered AOSTFTs configuration, using an etch stopper layer structure [6], while in this work, we focus on its dynamic validation. Both models were described in Verilog-A language for using them in commercial circuit simulators, that allow the compilation of external models.

It is well known that the Ring Oscillators (RO) are used as a test circuit to determine the operation frequency of a device or circuit. In this work we used a 19-stages RO circuit (each stage is an inverter with a saturated load configuration based on a-IGZO TFTs) and one inverter for the dynamic validation of our model.

The device geometry of the TFTs is very important to determine the oscillator performance, among which the overlap capacitance becomes a very important feature [7]. The developed AFCM considers, not only the typical overlap capacitance between the gate and drain contact (OV), but also, the top overlap associated to the part of the drain contact on top of the ESL layer in the structure (TOV) [6]. Other aspects, as the effect of the internal capacitances of

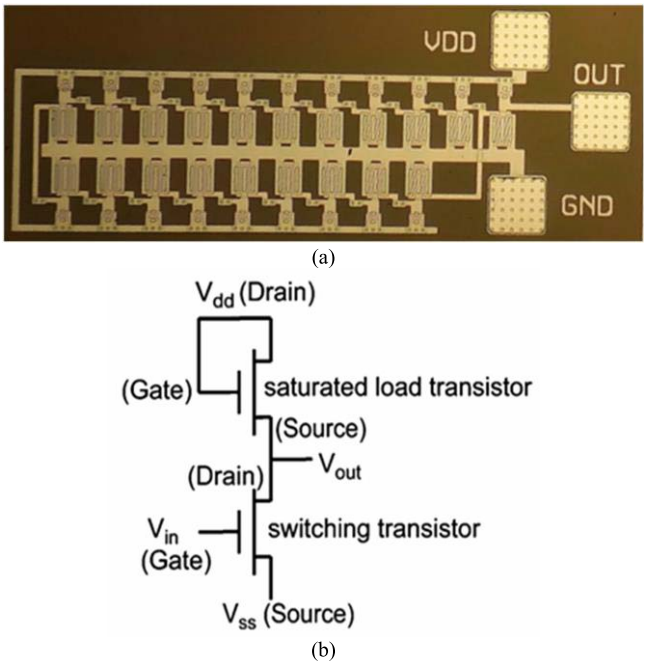

FIGURE 1. **(a) RO fabricated and measured (b) Configuration of the 19 inverters in the RO and the output buffer.**

the transistors, as well as variation of the supply voltage, are taken into account.

II. EXPERIMENTAL PART

A photo of one of the fabricated and measured Ring Oscillator (RO), consisting of 19 a-IGZO TFTs inverters is shown in Fig. 1 a). The inverters with a saturated load configuration (stages), are shown in Fig. 1 b). The output buffer circuit consists of an additional inverter with the same configuration. The fabricated load TFTs had a width of W = 15μm and a channel length of L = 15 μm, while the drivers had a width of W = 150 μm with the same channel length of L = 15 μm.

Figure 2 a) shows the cross section of an a-IGZO TFTs. The gate dielectric layer consists of a stack of Si_3N_4/SiO_2, with a thickness of 200 nm and an equivalent dielectric constant of 5.2. The IGZO layer used as semiconductor material is 45 nm thick, with a relative dielectric constant of 9. As metal contacts for *D, G* and *S,* a stack of Mo/Cr was used.

As etch stopper layer (ESL) another stack of Si_3N_4/SiO_2 was used. In Figure 2 b), the length of the typical overlap L_{ov} associated to the D/S contacts is indicated, as well as, the top overlap TOV corresponding to the part of the D/S contacts located on top the ESL layer. The effects on the electrical performance of these geometrical overlaps in the devices are considered in the full capacitance model for AOSTFTs reported in [6].

A Keithley 4200 Semiconductor voltage source for the supply voltage, an Agilent Waveform Generator for the input signal and a Tektronix TDS 3032 Oscilloscope were used

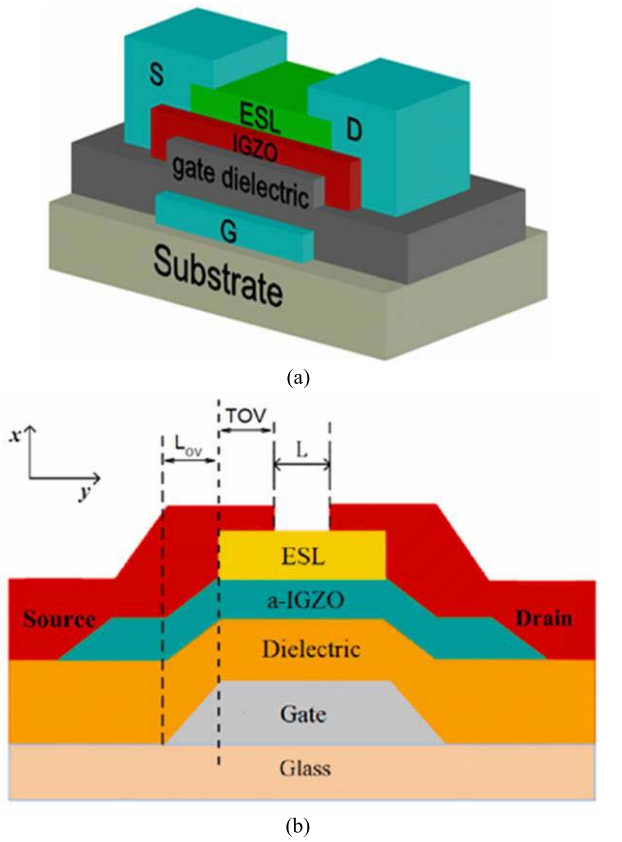

FIGURE 2. **Cross section of a) a-IGZO Devices; b) Schematic representation of the overlaps of the devices structure.**

to obtain the DC, AC and transient measurements of the analyzed circuits.

III. ANALYSIS AND DISCUSSION OF THE RESULTS

The AFCM, including the current-voltage and the capacitance-voltage models [5] and [6], respectively, was described in Verilog-A language, and used in SmartSpice from Silvaco, to simulate the analyzed circuits. As already indicated, the AFCM includes the extrinsic effects of the overlaps on the internal capacitances of the transistors shown in Fig. 2 (b), also allowing the calculation of the internal current through the device capacitances.

The equivalent circuit to represent the TFT with their internal nodes and contacts used in the simulations is shown in Fig. 3. The values of R_d and R_s are used to represent the respective conductance associated to the drain and source contact of the device. As usual, of the 9 capacitances in the device, the most significant for the dynamic behavior of the transistors are C_{gd}, C_{gs}. To represent the effect of these capacitances in the dynamic regime, the variation of the capacitances with time is calculated as the internal currents (I_{gs}, I_{gd}) represented as the derivate of the charge associated to the capacitances (Q_{gs}, Q_{gd}) with respect to the time as (in Verilog-A language):

$$Igs = TYPE * ddt(Qgs);$$

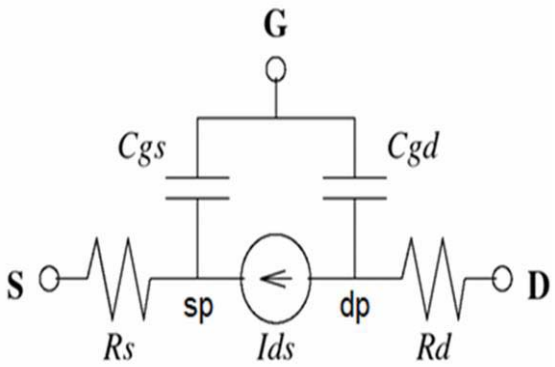

FIGURE 3. Equivalent circuit of the AOSTFTs used in the simulations.

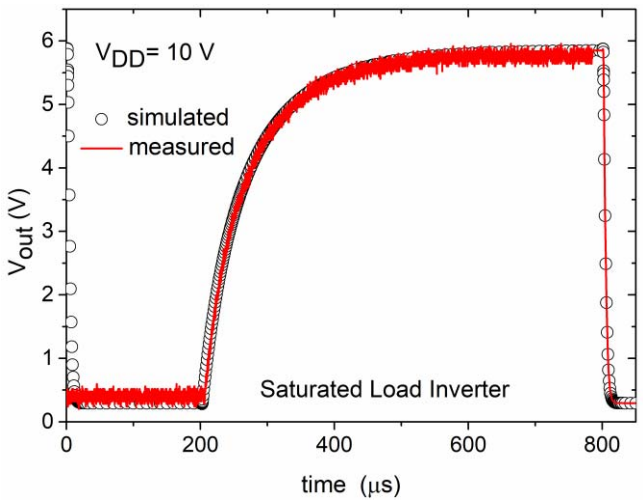

FIGURE 4. Comparison of the output signal measured and simulated of the saturated load inverter from one of stage of the RO from Fig. 1. a) at V_{DD}= 10 V.

TABLE 1. Extracted model parameters.

Parameter	Symbol	Value	Symbol	Value
TFT	LOAD TFT		SWITCHING TFT	
Threshold voltage	V_T	0.53	V_T	0.53
Mobility parameter	γ_a	0.3	γ_a	0.3
Series Resistance	R_S	3 k	R_S	3 k
Flat band voltage	V_{FB}	0.3	V_{FB}	0.3
Saturation parameter	α_S	0.4	α_S	0.4
Mobility at V_G-V_T= 1	μ1	7	μ1	7
Fit parameter	Q1	10	Q1	10
Fit Parameter	Q2	100	Q2	100
Fit parameter	V1	0.01	V1	0.01
Fit parameter	V2	1.3	V2	1.3
Subthreshold swing parameter	S	0.35	S	0.35
V_D voltage in linear region	V_{DS}lin	0.1	V_{DS}lin	0.1
Channel length modulation	λ	-1 m	λ	-1 m
Knee output curve parameter	m	2.4	m	2.4
Subthreshold Mobility Param.	γ_b	0.56	γ_b	0.56
Fit parameter	V3	0.5	V3	0.5
Fit parameter	Q3	2	Q3	2
Capacitance in depletion	CggD	0.26pF	CggD	1 pF
Capacitance in accumulation	CggA	0.3pF	CggA	1.3pF
Fit parameter	MM	0.035	MM	0.035
Fit parameter	A	0.02	A	0.02
Fit voltage	VAC	0.1	VAC	0.1
Fit saturation parameter	α_{SS}	1.25	α_{SS}	1.25
Parasitic capacitance	C_{par}	2.2fF	C_{par}	0.4pF
Fit parameter	DD	0.1	DD	0.1

$$Igd = TYPE * ddt(Qgd);$$
$$I(G, dp) <+ Igd;$$
$$I(G, sp) <+ Igs;$$

The charges Q_{GS} and Q_{GD} are calculated as:

$$Qgd = Cgd * V(G, dp);$$
$$Qgs = Cgs * V(G, sp);$$

where *dp* and *sp* are the internal nodes of the capacitances for the transistors, as can be seen in Fig. 3.

The extraction of the required model parameters was done as reported in [5], [6], after which obtained parameters were introduced in the simulator. The extracted values are shown on Table 1.

Fig. 4 shows the comparison of the output signal measured and simulated using the AFCM, for one of the saturated load inverters of the RO. The amplitude of the input pulse was 10 V. The value of the external load capacitance is 46 pF due to the superposition of the capacitance of the measurement probe of the oscilloscope and the measurement system in general, verified with a Boonton Capacitance Meter.

The maximum voltage that the output signal of our saturated load inverter should ideally reach would be approximately 9.5 V. However, our devices present an output resistance in the order of MΩ, which causes that a voltage divisor appears between the resistance of the measurement probe of the oscilloscope, which is of 10 MΩ, and the output resistance of the circuit, decreasing the maximum output voltage. These measurement conditions were considered in the simulations. As can be seen, the simulation reproduced the dynamic behavior of the output signal of the inverter for both the rise time and the fall time.

The dynamic model was also validated using the 19-stages RO from Fig. 1 a). Figure 5 shows the measured and simulated output signal of the Ring Oscillator formed by 19 inverters and one output buffer (additional inverter). The measured oscillation frequency was 22 kHz. The oscillator output signal simulated has an excellent coincidence with the ring oscillator output signal measured.

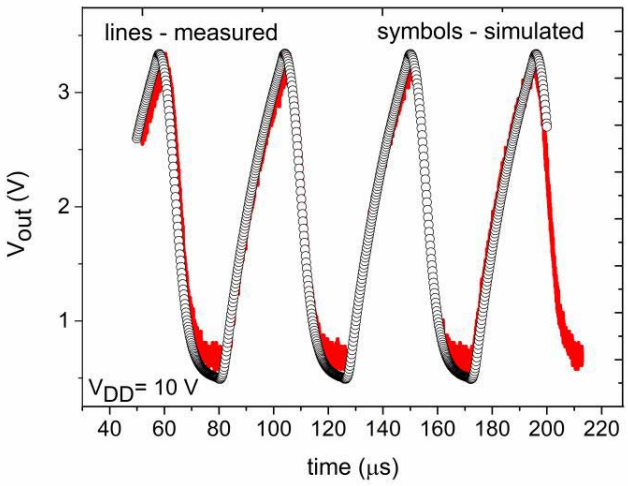

FIGURE 5. **Comparison between the output signals (measured and simulated) of the 19-stages ring oscillator from Fig. 1. a) at V_{DD}= 10 V.**

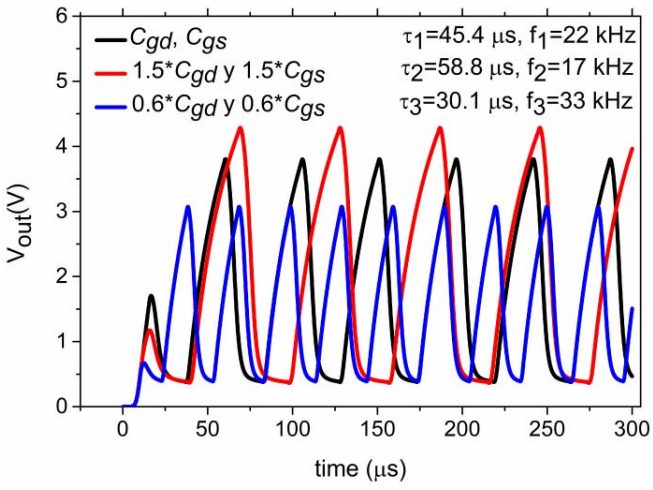

FIGURE 6. **Different RO output signals simulated changing the value of the internal capacitances C_{GD} and C_{GS} of the transistors in the Verilog-A code of the model, in order to verify the behavior of the output signal of the circuit.**

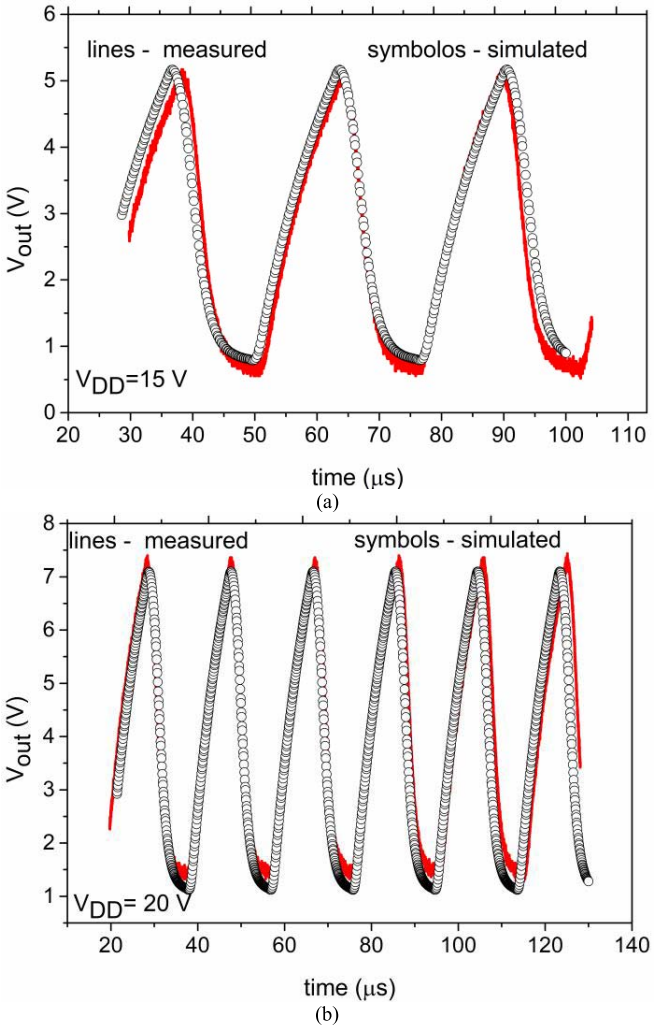

FIGURE 7. **Comparison between the output signals (measured and simulated) of the 19-stages ring oscillator from Fig. 1. a) at (a) V_{DD}= 15 V and (b) V_{DD}= 20 V.**

The effect at different internal capacitance values of the transistors on the oscillation frequency is clearly observed in the simulated output signal. The oscillation frequency is inversely proportional to the inverter delay time, that is, to the capacitance. When C_{gd}=C_{gs} was increased 1.5 times, the frequency reduced to 17 kHz, as can be seen in the Fig. 6. When C_{gd}=C_{gs} was reduced to half its value, the frequency, as expected, increased from 22 kHz to 33 kHz.

Since the operation frequency and hence, the propagation delay per stage, are function of the supply voltage (V_{DD}), Fig. 7 (a) and (b), show that the oscillation frequency of the circuit increases with the applied V_{DD}, reaching a maximum value around 60 kHz for a V_{DD}=20 V.

Finally, we evaluate and compare the dynamic response of the a-IGZO TFT circuit shown in Fig. 8 a). Fig. 8 b) and c) show the simulation of the circuit, which corresponds to a pixel control circuit used in a light emitting diode active matrix displays (AMOLED). The waveforms applied to the transistors follows the specifications for Ultra High Definition resolution on displays given by the pulse width or load time margin (t_{cm}) applied to the gate of 16 μs, for others two t_{cm} values of 30 and 40 μs, in order to determine the maximum load value of the storage capacitor (C_{st}).

Fig. 8 b) shows the expected behavior of the pixel control circuit for t_{cm}. When the voltage applied to the gate of the transistor commute from a high state to low state the output voltage remains constant. This voltage value is due the capacitor C_{st} and it is called feedback voltage (ΔV).

With the aim to see the impact of the capacitor C_{st} on the dynamic response of the pixel control circuit we obtained by simulation the output voltage of the same circuit at different values of C_{st} as can be seen in Fig. 8 c). For these simulations

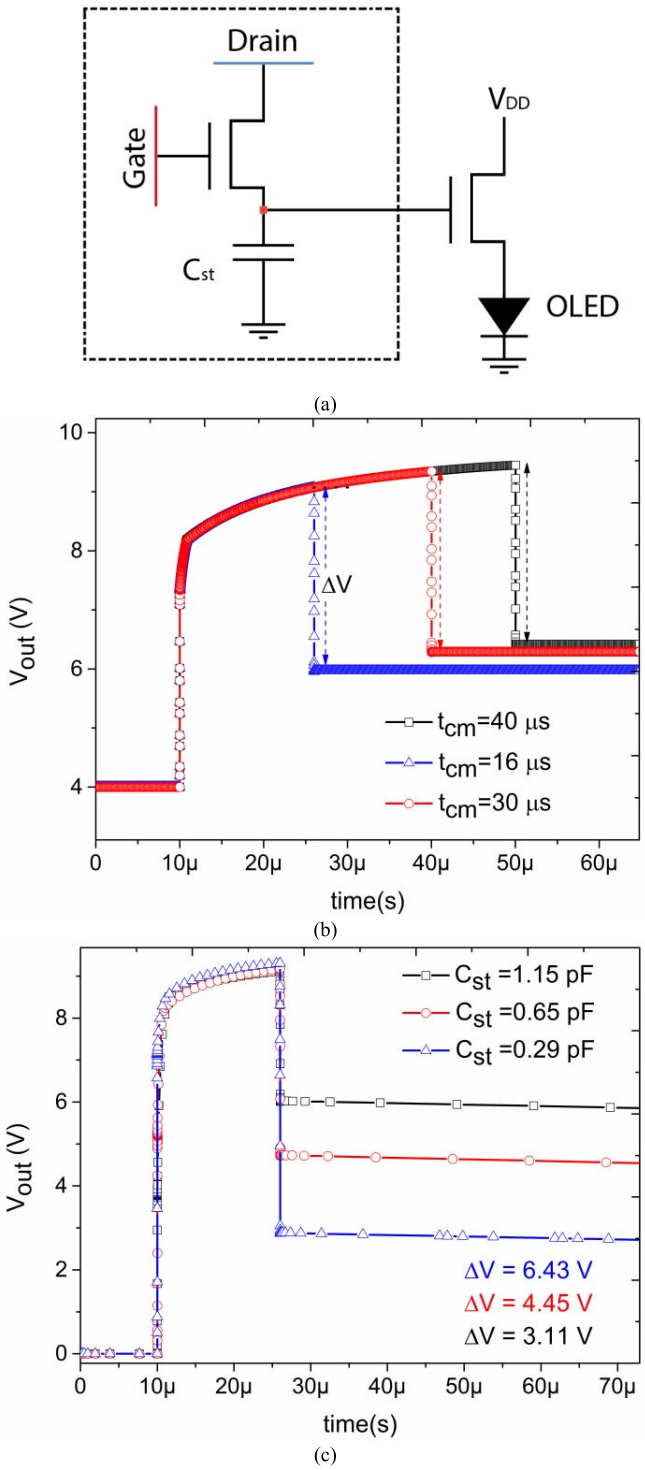

FIGURE 8. (a) Pixel control circuit simulated and circuit response for: (b) different load time margin (t_{cm}) and (c) different values of storage capacitance (C_{st}).

only a $t_{cm} = 16\ \mu s$ was considered. The results showed a substantial variation on ΔV while for a lower capacitor the load time is faster, as expected.

IV. CONCLUSION

Using the AFCM for AOSTFTs described in Verilog-a language we reproduced the dynamic behavior of a 19-stages ring oscillator and a saturated load inverter based on a-IGZO TFTs. In the case of the ring oscillator circuit the model was validated for different supply voltages obtaining the expected behavior of the output signal. The oscillation frequencies obtained for 10 V was 22 kHz, for 15 V was 37 kHz and for 20 V was around of 60 kHz. The model was also capable to reproduce the expected dynamic behavior when the internal capacitances values of the transistors were changed. On the other hand, the output voltage for an inverter with a saturated load configuration in both rise time and fall time was obtained with an excellent agreement between the simulated and measured characteristic.

A pixel control circuit for AMOLEDs was simulated. The results obtained were the expected and they were able to describe the behavior of the feedback voltage (ΔV), which is the voltage related to the storage capacitance (C_{st}), one of the most important parameters to control in this kind of circuits.

The results obtained in this work are very a good evidence that the AFCM is ready for using in the design circuits based on AOSTFTs.

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