A Large-Signal Model for a Peak Current Mode Controlled Boost Converter with Constant Power Loads

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***Abstract*—A large-signal averaged model is obtained to analyze the startup response of a boost converter loaded with a Constant Power Load (CPL) and peak Current Mode Control (CMC). An analytical methodology is developed for stability analysis during both startup and steady-state. The proposed model corresponds to two operating modes: 1) a reduced-order saturated model during startup mode and 2) an unsaturated full-order model taking place when the system reaches the vicinity of the steady-state. The duration of the starup period is also determined using the same model. To verify the validity of the derived large-signal model and the theoretical results derived from it, numerical simulation results from this model are compared with those obtained from a detailed switched model and experimental measurements demonstrating that the model can faithfully predict both the large-signal dynamic response during startup as as well as the steady-state regime of the system.**

***Index Terms*—large-signal model, switching converters, nonlinear load, constant power load, stability analysis,**

I. Introduction

PEAK Current Mode Control (CMC) is a control scheme that is commonly used for dc-dc switching converters due to several advantages such as inherent current limiting, easier outer voltage loop control design and inherent current sharing capability [1]. Since its introduction in the 70's, it has been widely used in many industrial applications and has increasingly motivated the scientific and engineering communities around the world. Namely, averaged models of switching converters peak under CMC have been the research topic of many researchers during a long period [2]–[11]. The modeling, small-signal analysis and design of switching converters with linear loads have undergone fundamental changes in their approach starting with the averaged framework and finishing with discrete-time formulation advocated decades later. In the existing literature about modeling of switching converters under CMC, most of the focus is on obtaining models for accurately predicting the converter behavior within a wide frequency range hence they all take into account the switching details. The simulation time using the resulting models significantly increases. Furthermore, the switching details are not significant for output voltage control design. Therefore, for large-signal simulation or for the outer loop controller design, the previous switching details are not necessary and obtaining a computationally efficient large-signal model becomes important.

Nonlinear large-signal averaged models of dc-dc converters under CMC have been widely considered in the literature [12]–[18]. These models are used to large-signal simulations under larger parametric variations. After their linearization in the vicinity of an operating point, the corresponding small-signal linear model is obtained and this can be used for controller design. In [12], [13] these nonlinear models were derived specifically for performing circuit simulations using commercial software. In [18], a large-signal averaged model was derived for switching converters and a general nonlinear continuous formulation procedure for large-signal simulation is presented.

All previous models were developed for power converters with linear resistive loads. Furthermore, the aforementioned models focus on accurate modeling under parametric change and rarely deals with the analysis of system behavior under operating regimes corresponding to the startup and the regulation phases. The derived models are merely used for numerical simulation purposes not for mathematical analysis. Therefore, they are based on numerical analysis and no symbolic expression can be extracted for stability boundary and very little insight is provided for the system response during startup. Moreover, a part from the widely considered resistive or constant impedance load in switching converters, the load could also be capacitive impedance [11], constant voltage (battery), constant current or an inductive impedance [19]. When the output voltage of a power converter is tightly regulated, it behaves like a constant power load (CPL) for its feeder converter in a cascade connection of two switching converters.

CPL behavior is very common in multi-converter cascading energy systems used in many industrial applications [20]–[32]. Due to the nonlinearity of the CPL, the large-signal response of a switching converter with CPL is different from

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that of the same converter with a resistive load. Large-signal averaged models for a dc-dc buck switching converter with CPL have been obtained in the past [31]. The analysis of the large-signal model has been addressed in [33] where the startup process and step response of an average current mode controlled buck converter with CPL were graphically analyzed based on the phase portrait method. Some design rules have also been proposed to achieve system stability during startup and in front of load change. The current limit value is determined accordingly to avoid the instability for the considered converter.

Therefore, although the modeling method used in this work is well known, to best of the authors' knowledge, it has not previously been used to model the large-signal behavior of dc-dc boost converter with a CPL neither to obtain analytically the expression of the system response during the startup regime nor to analytically obtain the duration of this regime. Therefore, more research effort is still required for a thorough understanding of the system behavior during startup and the transition from the saturated startup regime to the non saturated regulation regime under constant power loading conditions.

The research goal, hence, is to provide a large-signal modeling under the previous conditions and its validation by both detailed numerical simulation using the switched model and by experimental measurements. The derived nonlinear large-signal averaged model can be used for fast numerical simulation of energy systems while taking into account all the possible dynamics under different saturation regimes that could take place during startup phase. During this phase an estimate value of the startup duration and the expression of the state variables are also provided. The results from the derived model about stability and dynamical behavior will be compared to those obtained from the switched large-signal model and experimental measurements using a laboratory prototype showing a good accuracy when compared to the detailed switched model and and experimental measurements.

The rest of this paper is organized as follows. After this introduction, Section II presents the description of the system under study which consists of a dc-dc boost converter under CMC and with a CPL. Section III addresses the detailed modeling of the converter using the switched model. In Section IV, the large-signal averaged model is derived and then used to analyze the startup response. The evolution of the inductor current and the output capacitor voltage as well as the duration of the startup period are derived analytically. Large-signal simulation results from the derived model will be compared to the ones obtained from a detailed switched model of the system demonstrating that the model can be used to faithfully predict the large-signal behavior of the system. The stability domain of the desired equilibrium point in terms of the system parameters is determined in Section V. Section VI deals with the validation of the model and the derived theoretical results using numerical simulations. Experimental validation of the results is provided in Section VII. Finally concluding remarks are given in Section VIII.

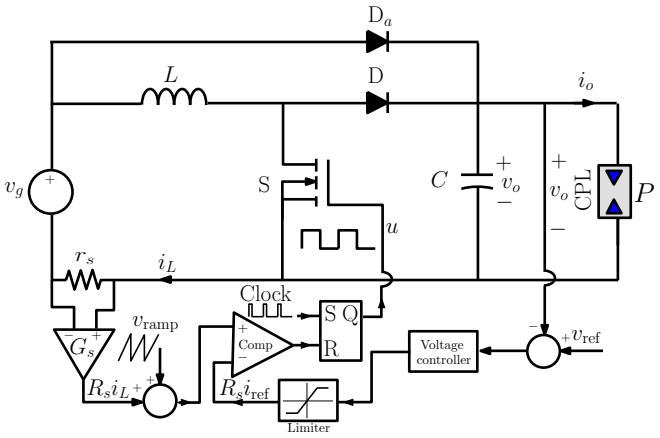


Fig. 1. Schematic circuit diagram of a boost converter under current mode control with a PWM strategy and loaded by a CPL.

II. The Boost Converter Loaded by a CPL

A. System description

The system under study is presented in Fig. 1. The power processing unit is a dc-dc boost converter with a constant input voltage and loaded by a CPL.

The power converter stage is controlled using CMC and a two-loop strategy where the outer voltage loop provides the reference signal for the inner current loop using fixed frequency PWM strategy. The ON/OFF binary driving signal u for the switch S is generated by a comparator and a set-reset (SR) latch as shown in Fig. 1. Its duty cycle d is generated by comparing the sensed signal $R_s i_L$ and the signal $R_s i_{\rm ref} - v_{\rm ramp}$, where $R_s i_{\rm ref}$ is the desired current reference and $v_{\rm ramp}$ is ramp compensating signal whose amplitude is V_M and period is T. If $R_s i_L$ reaches $R_s i_{\rm ref} - v_{\rm ramp}$, the switch S is turned OFF.

The reference signal $R_s i_{\rm ref}$ is provided by the outer voltage loop regulating the CPL voltage v_o to a desired voltage $v_{\rm ref}$. The voltage controller is used to compensate for the error $v_{\rm ref} - v_o$ detected between a fixed reference voltage level $v_{\rm ref}$ and the output voltage v_o with the aim to regulate v_o to $v_{\rm ref}$. In this work, the voltage controller is a PI compensator with a pole at the origin, a time constant τ and a proportional gain κ_p.

During start-up, a dc-dc converter may exhibit an unacceptable inrush current. To avoid inrush current during startup, a limiter is placed at the output of the PI compensator. However even with this limiter block at the output of the voltage controller, the inductor current during startup can overpass the established current limit if the initial voltage of the output capacitor is less than the input voltage [34]. To overcome this problem in the boost converter, its output voltage must start-up at an initial voltage different from zero which requires an amount of energy to be stored in the output capacitor before the converter starts operating. In the particular case of a CPL, the situation is worse because a zero capacitor voltage will imply, theoretically, an infinite current flowing through the load. In dc-dc boost converters, it is possible to provide the initial condition for the output capacitor voltage by connecting

an additional diode D_a between the input and the output ports as shown in Fig. 1.

III. Mathematical continuous-time nonlinear switched model

By applying Kirchhoff's voltage and current laws to the power stage of the circuit depicted in Fig. 1, the following set of differential equations describing the power stage is obtained:

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = -\frac{P}{Cv_o} + \frac{i_L}{C}(1-u), \tag{1a}$$

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = -\frac{v_o}{L}(1-u) + \frac{v_g}{L}, \tag{1b}$$

$$v_o(0) = v_g, \qquad i_L(0) = 0. \tag{1c}$$

The initial condition of the output voltage is due to the direct path between the input and the output imposed by the auxiliary diode D_a. The sensing resistance r_s as well as many other parasitic parameters were neglected in the modeling for simplicity. The state equations corresponding to the PI compensator of the outer voltage loop can be expressed as follows:

$$\frac{\mathrm{d}v_i}{\mathrm{d}t} = \varepsilon, \tag{2a}$$

$$v_i(0) = 0, \tag{2b}$$

where $v_i := \int \varepsilon(t)\mathrm{d}t$ is the integral state variable and $\varepsilon = v_{\mathrm{ref}} - v_o$ is the voltage error. To avoid the windup phenomenon, the integral variable v_i is also limited to an upper bound $R_s I_{\lim}$ and the expression of the integral variable becomes as follows

$$v_i = \begin{cases} \frac{1}{\tau}\int \varepsilon(t)\mathrm{d}t & \text{if } \frac{1}{\tau}\int \varepsilon(t)\mathrm{d}t < R_s I_{\lim} \\ R_s I_{\lim} & \text{if } \frac{1}{\tau}\int \varepsilon(t)\mathrm{d}t \geq R_s I_{\lim}. \end{cases} \tag{3}$$

With both inner current and outer voltage loops closed, the current reference $R_s i_{\mathrm{ref}}$ for the inner loop is provided by the output of the voltage controller according to the following expression:

$$R_s i_{\mathrm{ref}} = \kappa_p \varepsilon + W_i v_i, \tag{4}$$

where $W_i = \kappa_p/\tau$ is the integral gain of the PI compensator, τ being its time constant. The set of equations (1a)-(1b) together with (2a) establish the nonlinear switched model of the system. The closed loop model can be obtained by taking into account the switching condition which dictates the duty cycle cyclically. This condition is imposed by the intersection of the control voltage v_{con} with the ramp signal v_{ramp} and can be written as follows:

$$R_s i_L = R_s i_{\mathrm{ref}} - v_{\mathrm{ramp}}, \tag{5}$$

where $v_{\mathrm{ramp}} = m_a t \bmod T$, where $m_a = V_M/T$ is the slope of the ramp compensator, V_M being its amplitude and T its period. In order to complete the model, the limiter at the output of the voltage controller must be taken into account and the current reference must be limited according to the following expression

$$i_{\mathrm{ref}} = \begin{cases} \frac{1}{R_s}(\kappa_p \varepsilon + W_i v_i) & \text{if } \frac{1}{R_s}(\kappa_p \varepsilon + W_i v_i) < I_{\lim} \\ I_{\lim} & \text{if } \frac{1}{R_s}(\kappa_p \varepsilon + W_i v_i) \geq I_{\lim}. \end{cases} \tag{6}$$

The previous model can be used for performing accurate numerical simulations. However, it cannot be used for a mathematical analysis of the transient response during startup. Moroever, since the switching action is taken into account, large-signal simulations will be very time consuming. In order to overcome these problems a large-signal averaged model is derived and then used to analyze the large-signal behavior of the system during the start-up phase.

IV. Large-signal average model and analysis of the start-up response

A. Large-signal average model

The mathematical model developed here can be used for predicting the system start-up and transient behavior at the low frequency or slow scale. The averaged model of the boost converter under current mode control with voltage loop closed and with a CPL can be written as follows

$$\frac{\mathrm{d}\overline{v}_o}{\mathrm{d}t} = -\frac{P}{C\overline{v}_o} + \frac{\overline{i}_L}{C}(1-d), \tag{7a}$$

$$\frac{\mathrm{d}\overline{i}_L}{\mathrm{d}t} = -\frac{\overline{v}_o}{L}(1-d) + \frac{v_g}{L}, \tag{7b}$$

$$\frac{\mathrm{d}\overline{v}_i}{\mathrm{d}t} = \overline{\varepsilon} \tag{7c}$$

$$\overline{v}_o(0) = v_g, \qquad \overline{i}_L(0) = 0, \qquad \overline{v}_i(0) = 0. \tag{7d}$$

where the overline stands for averaging within a switching period. The large-signal closed-loop model can be obtained by replacing the duty cycle d by its expression corresponding to CMC. It is possible to determine the duty cycle expression under peak CMC with ramp compensation in terms of the sensed current $R_s i_L$, the reference current $R_s i_{\mathrm{ref}}$ and the following constraint due to the switching decision [1]

$$\overline{i}_L(t) = R_s \overline{i}_{\mathrm{ref}}(t) - (m_a + \frac{m_1}{2})dT, \tag{8}$$

where $m_1 = R_s v_g/L$ is the slope of the signal $R_s i_L$ during the ON subinterval. In terms of the averaged current, and taking into account possible saturation of the duty cycle d, this can be expressed as follows

$$d = \begin{cases} \frac{R_s(\overline{i}_{\mathrm{ref}}(t) - \overline{i}_L(t))}{(m_a + \frac{m_1}{2})T} & \text{if } 0 < \frac{R_s(\overline{i}_{\mathrm{ref}}(t) - \overline{i}_L(t))}{(m_a + \frac{m_1}{2})T} < 1, \\ 1 & \text{if } \frac{R_s(\overline{i}_{\mathrm{ref}}(t) - \overline{i}_L(t))}{(m_a + \frac{m_1}{2})T} \geq 1, \\ 0 & \text{if } \frac{R_s(\overline{i}_{\mathrm{ref}}(t) - \overline{i}_L(t))}{(m_a + \frac{m_1}{2})T} \leq 0. \end{cases} \tag{9}$$

The saturation of the duty cycle will not take place whenever the following condition is satisfied:

$$\overline{i}_{\mathrm{ref}} < \overline{i}_L + \frac{1}{R_s}(m_a + \frac{m_1}{2})T. \tag{10}$$

According to (3) and (6), the averaged value $\bar{i}_{\rm ref}$ of the current reference $i_{\rm ref}$ and the averaged value $\overline{v}_i$ of the state variable v_i are also limited according to the following expressions

$$\bar{i}_{\rm ref} = \begin{cases} \frac{1}{R_s}(\kappa_p\bar{\varepsilon} + W_i\overline{v}_i) & \text{if } \frac{1}{R_s}(\kappa_p\bar{\varepsilon} + W_i\overline{v}_i) < I_{\rm lim}, \\ I_{\rm lim} & \text{if } \frac{1}{R_s}(\kappa_p\bar{\varepsilon} + W_i\overline{v}_i) \geq I_{\rm lim} \end{cases} \tag{11a}$$

$$\overline{v}_i(t) = \begin{cases} \frac{1}{\tau}\int \bar{\varepsilon}(t)\mathrm{d}t & \text{if } \frac{1}{\tau}\int \bar{\varepsilon}(t)\mathrm{d}t < R_sI_{\rm lim}, \\ R_sI_{\rm lim} & \text{if } \frac{1}{\tau}\int \bar{\varepsilon}(t)\mathrm{d}t \geq R_sI_{\rm lim}. \end{cases} \tag{11b}$$

The expression of the duty cycle as given by (9) together with the expressions of $\overline{v}_i$ and $\bar{i}_{\rm ref}$ given in (11a)-(11b) can then be used in (7d) of the system to obtain the closed large-signal model.

B. Order-reduction during startup with current reference saturated

The full-order average model given by (7a)-(7c) and (9)-(11b) describes the large-signal dynamical behavior of the converter at the slow scale. It is worth to note that the system is designed in such a way that saturation do not take place under stable steady-state regime. However, during startup, saturation of the current reference provided by the PI compensator could take place to avoid unacceptable high inrush current. In particular, in the presence of the auxiliary diode D_a, according to (11a) the saturation of the reference current $i_{\rm ref}$ and consequently its averaged value $\bar{i}_{\rm ref}$ will take place from the initial starting time if the following condition is fulfilled

$$\frac{1}{R_s}(\kappa_p(v_{\rm ref} - v_g)) \geq I_{\rm lim}. \tag{12}$$

This condition is usually satisfied under normal operating conditions of the converter. Therefore with (12) fulfilled, an order reduction takes place and the integral variable v_i will be constrained according to $v_i = R_sI_{\rm lim}$. It is worth to note that the reduced-order model is only valid under saturation regime and cannot be used for predicting the overall dynamics of the system.

C. Asymptotic behavior of the reduced-order model

During startup, if (12) is satisfied, the converter will start operating under CMC with voltage loop open and with a current limit $I_{\rm lim}$ and the equation describing the integral variable can be omitted. Under this operating mode, the coordinates of the supposed equilibrium point of the average model of the system are as follows

$$I_L = \frac{P}{v_g}, \tag{13a}$$

$$V_o = \frac{v_g}{1-D}, \tag{13b}$$

$$D = \frac{R_s(I_{\rm lim} - I_L)}{(m_a + \frac{m_1}{2})T}. \tag{13c}$$

But, depending on the values of $I_{\rm lim}$, T, L, P, m_a and v_g, the resulting steady-state duty cycle D could be saturated to its maximum value 1 and therefore the previous equilibrium point could be virtual and the system will not present a real equilibrium point since the voltage coordinate is at infinity[1]. Note that saturation of D at 0 requires that $I_{\rm lim} < I_L$ which does not make sense. Saturation of D at 1 takes place if the following condition holds

$$\frac{P}{v_g} + \frac{1}{R_s}(m_a + \frac{m_1}{2})T < I_{\rm lim}. \tag{14}$$

This condition is also usually satisfied under normal operating conditions of the converter. The reduced-order averaged model with $i_{\rm ref}$ saturated will exhibit a real equilibrium point if the following condition is satisfied

$$\frac{P}{v_g} < I_{\rm lim} < \frac{P}{v_g} + \frac{1}{R_s}(m_a + \frac{m_1}{2})T \tag{15}$$

The stability of this equilibrium point can be investigated by linearizing the previous averaged model with $i_{\rm ref}$ saturated in the vicinity of an operating point. If the duty cycle is not saturated, the large-signal model can be expressed as follows

$$\dot{\overline{\mathbf{x}}} = \mathbf{f}(\overline{\mathbf{x}}, d) \tag{16}$$

$$d = R_s\frac{I_{\rm lim} - \bar{i}_L(t)}{(m_a + \frac{m_1}{2})T}, \tag{17}$$

where $\overline{\mathbf{x}} = (\overline{v}_o \quad \bar{i}_L)^\intercal$ and $\mathbf{f}$ is as follows

$$\mathbf{f}(\overline{\mathbf{x}}) = \begin{pmatrix} \frac{\mathrm{d}\overline{v}_o}{\mathrm{d}t}, \\ \frac{\mathrm{d}\bar{i}_L}{\mathrm{d}t}. \end{pmatrix} \tag{18}$$

Let $\hat{v}_o = \overline{v}_o - V_o$, $\hat{i}_L = \bar{i}_L - I_L$ and $\hat{d} = d - D$ the small deviations of the average output voltage $\overline{v}_o$, the average inductor current $\bar{i}_L$ and the average duty cycle d with respect to their steady-state values V_o, I_L and D respectively. Therefore, the small-signal model of the system under CMC with current reference saturated can be written as follows

$$\dot{\hat{\mathbf{x}}} = \mathbf{J}\hat{\mathbf{x}}, \tag{19}$$

where $\mathbf{J}$ is the Jacobian matrix of the system that can be computed from the following expression

$$\mathbf{J} = \frac{\partial f}{\partial \overline{\mathbf{x}}} + \frac{\partial f}{\partial d}\frac{\partial d}{\partial \overline{\mathbf{x}}}. \tag{20}$$

The calculation of the different partial derivatives leads to the following expression of $\mathbf{J}$

$$\mathbf{J} = \begin{pmatrix} \frac{P}{V_o^2C} & \frac{\alpha I_L}{C} + \frac{1-D}{C} \\ -\frac{1-D}{L} & -\frac{\alpha V_o}{L} \end{pmatrix}, \tag{21}$$

where α is given by

$$\alpha = \frac{R_s}{(m_a + \frac{m_1}{2})T}. \tag{22}$$

[1]The voltage will increase starting from its initial condition v_g and as soon as the voltage error ε changes its sign, the PI compensator comes into play and under stability conditions of the closed loop system to be derived later, the output voltage v_o will be regulated to its desired value.

The characteristic polynomial of the system under this operating mode can be expressed as follows

$$p(\mu) = \mu^2 + \left(\frac{\alpha V_o}{L} - \frac{P}{CV_o^2}\right)\mu + \frac{1}{LC}. \tag{23}$$

Therefore the equilibrium point will be stable with $i_{\rm ref}$ saturated whenever the following condition holds

$$\frac{\alpha V_o}{L} - \frac{P}{CV_o^2} > 0. \tag{24}$$

If (24) is not satisfied, the equilibrium point will be unstable and the system will exhibit low frequency oscillation under saturated regime. Therefore, it can be concluded that the slow scale dynamic properties of the boost converter with a CPL under CMC differs from those of the same converter loaded by resistive load. In particular, the averaged model of a peak current mode controlled boost converter is always stable with a resistive load. It is not the case for the boost converter with CMC and CPL. In fact, the useful case is the unstable one with $i_{\rm ref} = I_{\rm lim}$ during the start-up phase because with closed voltage loop, once $\overline{v}_o$ reaches $v_{\rm ref}$ the voltage controller will come into play and the dynamics will be governed by the full-order model that can be obtained by replacing $I_{\rm lim}$ by $\overline{i}_{\rm ref}$, making this current reference the unsaturated output of the PI voltage controller and augmenting the previous model by taking into account the integral variable.

D. Analysis of the start-up response

Under a tight current mode control leading to an order reduction like in sliding mode control [35], the large-signal model will be of first order duding startup. In this case an expression for the output voltage during the startup period can be obtained in closed form [35]. Unfortunately, this is not the case with fixed frequency peak current mode control and ramp compensation since this order reduction do not take place. Although in this case it cannot be exactly obtained, the expression of the output voltage during the startup period in this case can be modified from [35] and approximated as follows

$$\overline{v}_o(t) \approx \begin{cases} v_g & \text{if } t < t_r, \\ \sqrt{v_g^2 + 2\dfrac{v_g(I_{\rm lim} - \frac{m_a T}{R_s}) - P}{C}(t - t_r)} & \text{if } t > t_r. \end{cases} \tag{25}$$

where t_r is the time instant at which the signal $R_s i_L$ reaches the value $I_{\rm lim} - m_a dT$ for the first time.

E. Calculation of the current reaching time t_r

During the start-up phase, the inductor current is limited to its maximum permitted value $I_{\rm lim}$ and the duty cycle is saturated to 1. Therefore, the inductor current i_L and its averaged value $\overline{i}_L$ will increase linearly according to the equation $i_L(t) = m_1 t$. Under these conditions, the reaching time t_r when the signal $R_s i_L$ reaches the $R_s I_{\rm lim} - m_a T$ for the first time can be obtained by solving the following equation

$$R_s m_1 t_r = R_s I_{\rm lim} - m_a T \tag{26}$$

which results in

$$t_r = \frac{R_s I_{\rm lim} - m_a T}{R_s m_1} \tag{27}$$

Depending on the values of $I_{\rm lim}$, T, L, R_s, m_a and v_g, the duty cycle will be saturated during a number of switching cycles $N_{\rm sat}$ given by the following expression

$$N_{\rm sat} = \left\lfloor \frac{R_s I_{\rm lim} - m_a T}{R_s m_1 T} \right\rfloor, \tag{28}$$

where $\lfloor \cdot \rfloor$ stands for the floor function.

F. Voltage reaching time t_c and the theoretical evolution of the inductor current ripple during start-up

The time instant at which the voltage $\overline{v}_o$ reaches the desired voltage $V_{\rm ref}$ can be obtained by solving the equation $\overline{v}_o = V_{\rm ref}$ using (25) which leads to

$$t_c = t_r + \frac{R_s C}{2((R_s I_{\rm lim} - m_a T)v_g - R_s P)}(V_{\rm ref}^2 - v_g^2). \tag{29}$$

At $t = t_c$, the averaged load voltage $\overline{v}_o$ reaches the reference voltage $V_{\rm ref}$. For $t > t_c$, the system will evolve according to the performances imposed by the voltage loop controller.

The time evolution of the switching ripple amplitude $\Delta i_L(t)$ in a boost converter with CPL and under saturated startup regime can be expressed as follows [35]

$$\Delta i_L(t) = \frac{T v_g\left(\sqrt{v_g^2 + 2\dfrac{v_g I_{\rm lim} - P}{C}(t - t_r)} - v_g\right)}{2L\sqrt{v_g^2 + 2\dfrac{v_g I_{\rm lim} - P}{C}(t - t_r)}}. \tag{30}$$

The derived expression for the time evolution of the inductor current ripple will be validated in Section VI by detailed numerical simulations using the switched model.

V. Local Slow Scale Stability Domain of the Closed-Loop Full-Order Model

Performing a similar small-signal analysis like in subsection IV-C taking the integral variable as an additional state variable, hence the state vector being $\overline{\mathbf{x}} = (\overline{v}_o \quad \overline{i}_L \quad \overline{v}_i)^\intercal$, the Jacobian matrix of the system with voltage loop closed becomes as follows

$$\mathbf{J} = \begin{pmatrix} \dfrac{P}{V_o^2 C} + \dfrac{\kappa_p I_L}{C} & \dfrac{\alpha I_L}{C} + \dfrac{1-D}{C} & \dfrac{\kappa_p I_L}{C} \\ -\dfrac{1-D}{L} - \dfrac{\kappa_p V_o}{L} & -\dfrac{\alpha V_o}{L} & -\dfrac{\kappa_p V_o}{C} \\ -1 & 0 & 0 \end{pmatrix}. \tag{31}$$

Now, the characteristic polynomial depends on the proportional gain κ_p and the time constant τ of the PI controller. But it is a third order equation making it difficult to obtain a clear analytical expression for stability boundary. Ignoring the effect of the integral variable, it is obtained that the boundary of the slow scale instability is the manifold $\{\mu_{\rm ss} = 0\}$ in the parameter space, where $\mu_{\rm ss}$ is given by

$$\mu_{\rm ss} = \kappa_p - \frac{R_s C v_g^2}{LP(1-D)} + \frac{(1-D)^2 T(m_2 + 2m_a)}{2v_g}. \tag{32}$$

For instance, in terms of the proportional gain κ_p of the PI compensator, the system will be stable at the slow scale if this parameter is selected lower than the critical value $\kappa_{\rm cri}$ given by the following expression

$$\kappa_{p,\rm cri} \approx \frac{R_s C v_g^2}{LP(1-D)} - \frac{(1-D)^2 T(m_2+2m_a)}{2v_g}. \qquad (33)$$

This stability limit will be validated later by numerical simulations and experimental measurements from a laboratory prototype.

It is worth to note that since the previous stability limit was obtained by using an averaged model that ignores the real switching behavior of the system, a discrepancy is expected to exist between the results obtained from the closed-form expression (33) and those obtained numerically from the detailed switched model.

VI. Large-signal simulation performance and model validation

The simulated and measured large-signal waveforms for the output voltage and the inductor current were used to validate the previously derived model. Time-domain waveforms during startup and steady-state operation are useful in illustrating the large-signal characteristics of the system. The parameters used are the ones listed in Table I. The rest of parameters to be varied to get different large-signal behaviors are shown in the captions of the figures.

TABLE I
The fixed parameter values

$V_{\rm ref}$	L	C	P	V_M	T	τ
48 V	200 μH	130 μF	48 W	1 V	25 μs	1 ms

Fig. 2 shows the time-domain response of the inductor current and the output capacitor voltage for different values of input voltage $v_g = 16$ V and $v_g = 32$ V. For $v_g = 16$ V, the critical value of the proportional gain κ for slow scale instability to take place is $\kappa_{\rm cri} \approx 10.4$ and for $v_g = 32$ V, one has $\kappa_{\rm cri} \approx 20.77$. The used value of the proportional gain is $\kappa_p = 3$ which is less than $\kappa_{\rm cri}$ in both cases. The corresponding values of the left hand side of (12) are equal to 96 A and 48 A respectively. The current is limited to $I_{\rm lim} = 6.5$ A. Therefore (12) is fulfilled in both cases and the system current reference is saturated from at the initial starting time instant. The peak $\bar{i}_L + \Delta i_L/2$ and valley $\bar{i}_L - \Delta i_L/2$ values of the inductor current, where Δi_L is predicted from (30), are also depicted in dashed lines together with the average current $\bar{i}_L$ in Fig. 2-a and Fig. 2-b. It can be observed that similar responses are obtained from both the detailed switched model and the derived large-signal model during startup and in steady-state regimes. During startup, condition (24) is fulfilled and the system is stable but the equilibrium point is virtual and will not be reached in steady-state. In fact, as soon as the output voltage is in the vicinity of its desired value, the PI compensator comes into play and because $\kappa_p < \kappa_{\rm cri}$, the system is stable hence the desired equilibrium point is reached.

The results were obtained from the exact switched model implemented in PSIM© and from the full-order large-signal model derived in the previous section. The analytical expression of the output voltage given in (25) is also plotted during the startup interval $(0, t_r)$. The curves cannot be distinguished from each other during this interval hence confirming the accuracy of the derived expressions. The calculated values of the reaching times t_r and t_c as predicted by (27) and (29) agree very well with those obtained by numerical simulations from the switched model and the large-signal model. For $v_g = 32$ V, $t_c \approx 38$ μs and $t_r \approx 654.6$ μs and for $v_g = 16$ V, the voltage reaching time is $t_c \approx 71$ μs and the current reaching time is $t_r \approx 2.5$ ms. In both cases, one has that $t_c \ll t_r$.

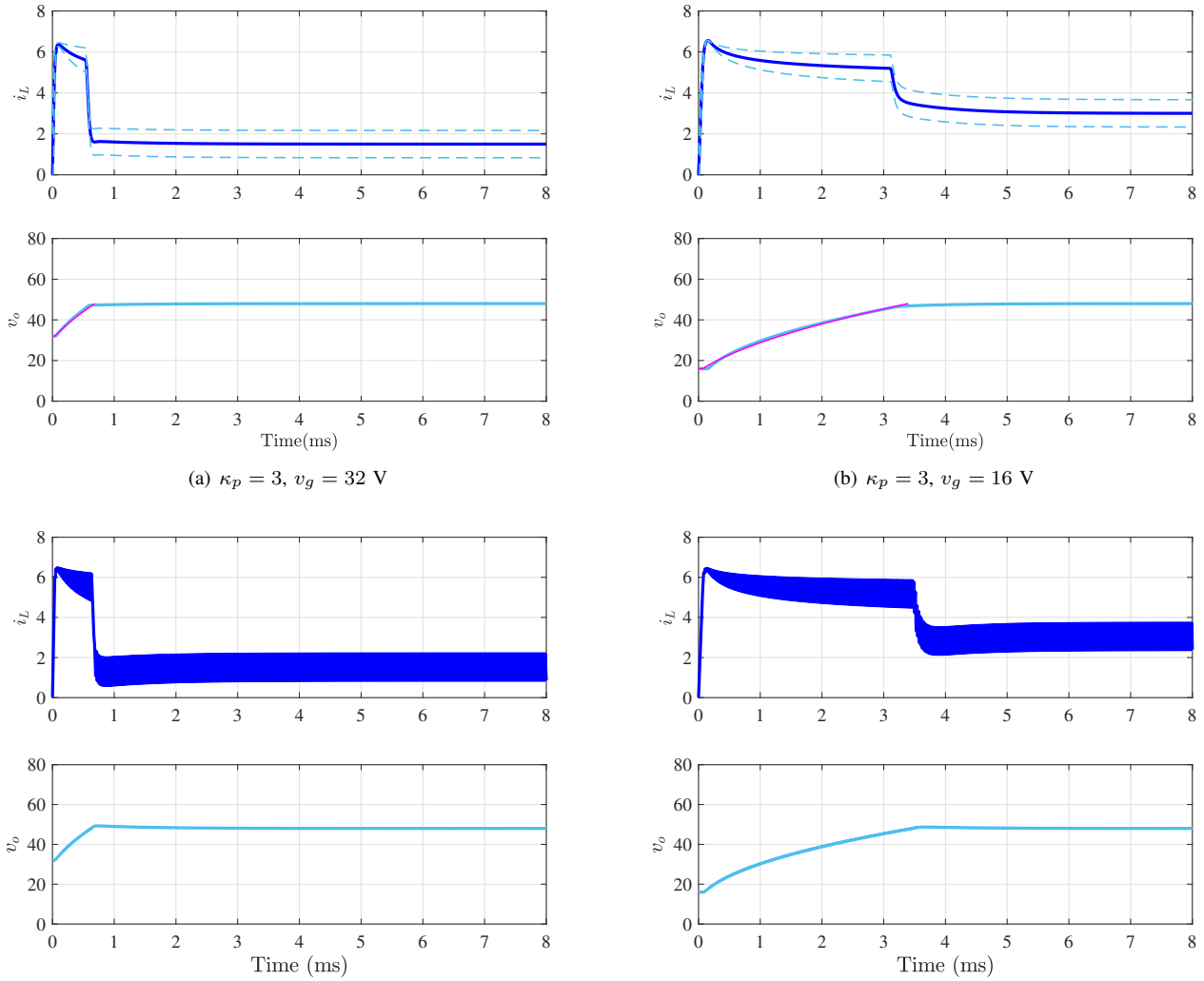
The number of the initial saturated switching cycles predicted from (28) also agree well with the one obtained from numerical simulation from the detailed switched model. For $v_g = 32$ V, $N_{\rm sat} = 1$ and for $v_g = 16$ V, $N_{\rm sat} = 2$.

It can be seen that for the case of $v_g = 32$ V, the duration of the transient time is short as predicted by (29). In this case, state variables respond quickly during startup. Similar responses of the inductor current and output voltage take place for $v_g = 16$. However, the transient time is larger in this case as predicted by (29). In both cases, the inductor current i_L is controlled to its desired value and the output voltage evolves approximately according to (25) during the startup period. In steady-state operation, the output voltage is well regulated to $v_{\rm ref} = 48$ V and the inductor current average value is settled down on its theoretical value $I_L = P/v_g = 3$ A for $v_g = 16$ V and $I_L = P/v_g = 1.5$ A for $v_g = 32$ V. It is worth to note that a small discrepancy can be observed between the voltage reaching time obtained from the switched model and the large-signal model. This discrepancy is mainly due to switching ripple not taken into account in the large-signal average model.

Fig. 3 shows the time-domain evolutions of the inductor current and the output capacitor voltage for input voltage $v_g = 16$ V and for $\kappa_p = 11 > \kappa_{\rm cri}$. Now, since $\kappa_p > \kappa_{\rm cri} \approx 10.4$ and the system is unstable when it reaches the regulation phase, exhibiting low frequency oscillations. In Fig. 3-b, the peak and valley values of the inductor current predicted from (30) and the evolution of the output voltage from (25) are also shown. The corresponding value of the left hand side of (12) is equal to 176 A. The current is limited to $I_{\rm lim}$ =6.5 A as before. Therefore (12) is fulfilled and the system current reference is also saturated from the initial starting instant. During startup, the equilibrium point is also virtual in this case and will not be reached in steady-state. These oscillations can interact with the saturation limit leading to large-signal limit cycles. Typical corresponding waveforms are shown in Fig. 3. It can be observed that the matching between the results from the detailed switched model and from the derived large-signal model is again remarkable.

VII. Experimental validation

A comparison between the responses from numerical simulation using the proposed large-signal model and the ones obtained from prototype measurements was also conducted. The experimental setup used for validating the theoretical



(a) $\kappa_p = 3$, $v_g = 32$ V

(b) $\kappa_p = 3$, $v_g = 16$ V

(c) $\kappa_p = 3$, $v_g = 32$ V

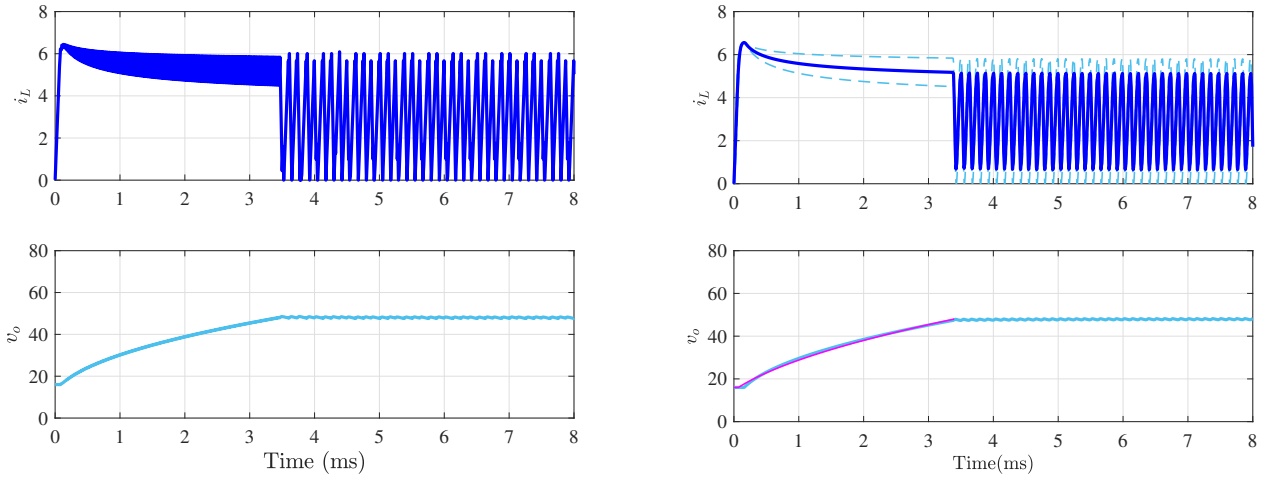
(d) $\kappa_p = 3$, $v_g = 16$ V

Fig. 2. Simulated time-domain waveforms showing the inductor current i_L and the output capacitor voltage v_o during startup for two different values of v_g. Top: from the derived large-signal averaged model. The predicted peak $\bar{i}_L + \Delta i_L/2$ and valley $\bar{i}_L - \Delta i_L/2$ values of the inductor current, where Δi_L is given in (30), are also depicted in dashed lines together with the average current $\bar{i}_L$. The analytical expression of the output voltage given in (25) is also plotted during the startup interval $(0, t_r)$. The curves cannot be distinguished from each other during this interval hence confirming the accuracy of the derived expressions. Bottom: from the detailed full order switched model.

predictions and the numerical simulations is depicted in Fig. 4 where the boost converter, its control board, the constant power sink, the power sources and signal generators can be identified. The parameters values are the same as those used in numerical simulations (Table I). The corresponding schematics diagram is shown Fig. 5. In order to emulate an ideal constant power load at the converter output, an electronic load (ELEKTRO-AUTOMATIK EL3400-25) was used. The inductor was built using toroidal Magnetics Kool-mu© core. The output capacitor is the parallel connection of 5 metallized polyester (MKT) capacitors each has a capacitance of 10 μF and 36 ceramic (X7R) capacitors each has a capacitance of 2.2 μF. The total capacitance is about 129 μF. The switch used is an IRFP4110PBF Silicon MOSFET and the diode is an MBR30H100CTG Silicon Schottky diode. The steady-state duty cycle was varied by adjusting the input voltage while maintaining constant reference voltage for all the experiments. The voltage error is processed by a PI controller implemented using standard OA devices. The proportional gain of the PI controller can be adjusted using a potentiometer. A 40 kHz sawtooth ramp signal provided from the signal generator Tektronix AFG2021 is subtracted from the output of PI voltage controller and the result is compared to the signal $R_s i_L$. The current is sensed using the hall effect current sensor LEM LA25NP with total conversion ratio 1 volt per ampere and an equivalent resistance $r_s = 6.3$ mΩ ($G_s r_s = R_s$).

The comparator used is LM319N. The output of the SR latch CD4027BE is the switch driving signal using the driver MCP1407-E/P. The results, shown below, were measured by using the oscilloscope Tektronix TDS 754C and the probes TEKTRONIX TCP202 for illustrating the current waveforms.

Fig. 6 illustrates the startup response from the experimental prototype for the same values of parameters used in simulations illustraed in Fig. 2. It can be observed from these figures



(a) Switched model (b) Large-signal averaged model

Fig. 3. Simulated time-domain waveforms showing the inductor current i_L and the output capacitor voltage v_o during startup. (a) from the detailed full order switched model. (b) from the large-signal averaged model. The predicted peak $\bar{i}_L + \Delta i_L/2$ and valley $\bar{i}_L - \Delta i_L/2$ values of the inductor current, where Δi_L is given in (30), are also depicted in dashed lines together with the average current $\bar{i}_L$. The analytical expression of the output voltage given in (25) is also plotted during the startup interval $(0, t_r)$. The curves cannot be distinguished from each other during this interval hence confirming the accuracy of the derived expressions. .

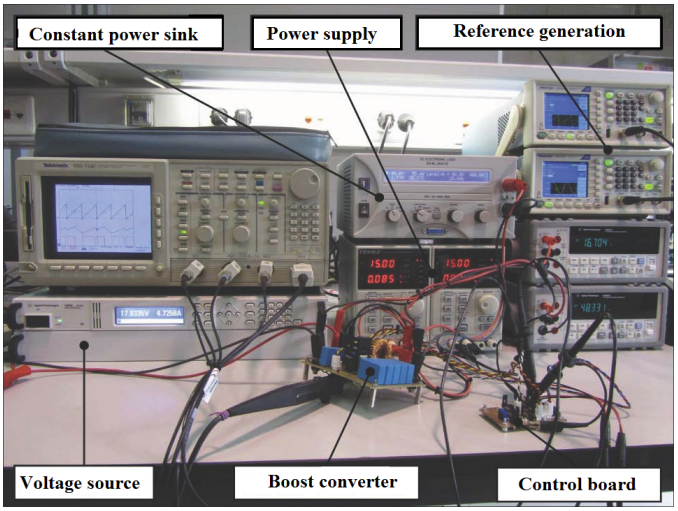


Fig. 4. The experimental setup used to validate the theoretical and the simulation results.

that the transient waveforms obtained from the simulation and experimental results match quite well with each other although some discrepancies between the experimental results and those from the switched model can still be appreciated. These discrepancies are mainly due to parasitic parameters such as the losses in the reactive and the switching devices that were not taken into account in the analysis. This demonstrates that the proposed large-signal model and the derived analytical expressions for the startup period duration and the expression of the state variables can faithfully predict the response of the boost converter with peak current mode control and loaded by a CPL with voltage loop closed.

Fig. 7 shows the startup response from the experimental prototype when the system exhibits low frequency oscillation in the regulation phase corresponding to Fig. 3. A good matching can again be observed between the experimental response and the two simulated responses from both models which demonstrate the validity of the approximate stability condition given in (33).

VIII. Conclusions

A large-signal averaged model for a dc-dc boost converter operating under peak current-mode control and loaded with a constant power load is presented in this paper. The developed model is nonlinear and can be used either in the voltage loop controller design after linearization or for large-signal simulations. Expressions for the state variables during startup time interval as well as the duration of this interval are derived analytically. Although the modeling method used in this work is well known, according to the authors' knowledge, it has not previously been used to model the large-signal behavior of power converters with constant power load neither to obtain analytically the expression of the state variables during the startup regime nor to analytically obtain the duration of this regime. The theoretical results have been validated by means of numerical simulations from the detailed circuit-based switched model implemented in PSIM© software and also by measurements from a boost converter prototype. It has been shown that the derived model accurately predicts the slow scale low frequency behavior in large-signal transients during startup as well as the stability boundary in terms of the system parameters if it is linearized in the vicinity of the desired equilibrium point. Therefore, under continuous conduction mode operation, the model predicts the converter dynamic behavior with great accuracy in different operating points. Like many other conventional averaged models, one of the limitation of the derived large-signal model is its inability to predict the fast scale behavior of the converter. A

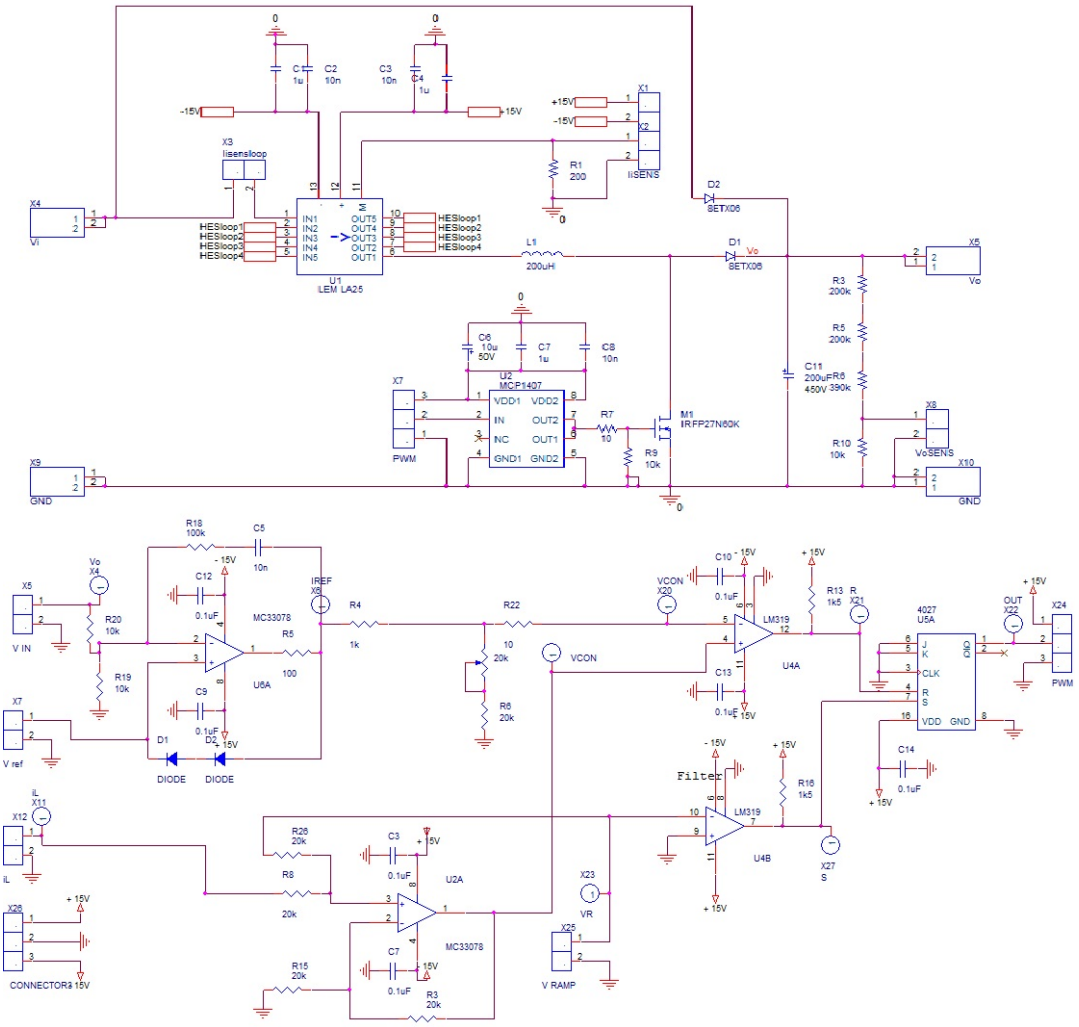
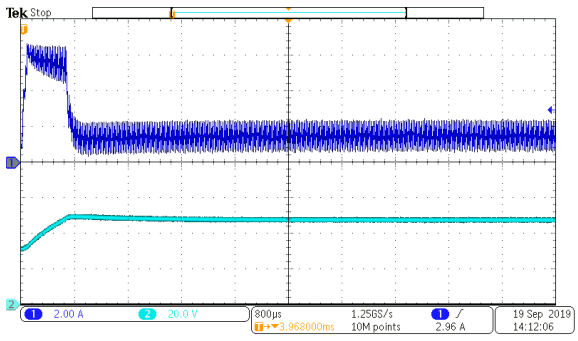
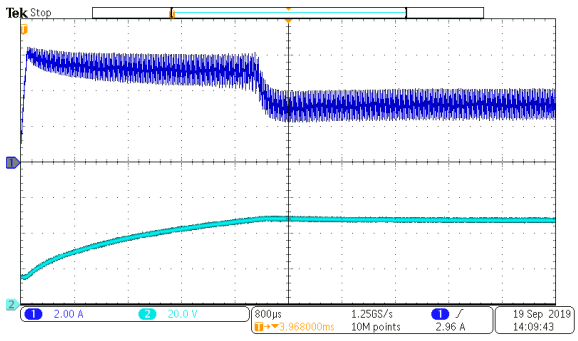


Fig. 5. Schematic diagram of the imlemented control scheme for the converter with CPL.



(a) $\kappa_p = 3$, $v_g = 32$ V ($D < 0.5$)



(b) $\kappa_p = 3$, $v_g = 16$ V ($D < 0.5$)

Fig. 6. Experimental time-domain waveforms showing the inductor current i_L and the output voltage for two different values of input voltage v_g.

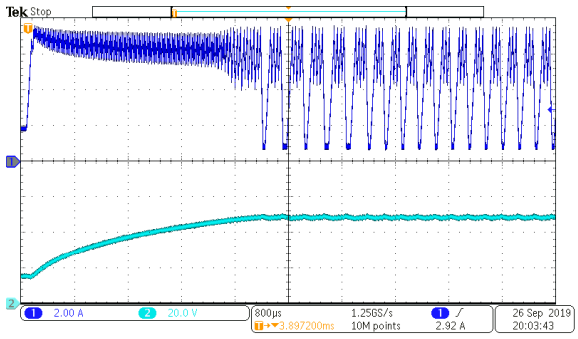


Fig. 7. Experimental time-domain waveforms showing the inductor current i_L and the output voltage for $\kappa_p = 8.6$.

separate paper submitted to the same special issue is dedicated to a methodology to accurately predict fast scale instability in switching converters with constant power load. Further research will be dedicated to extending the presented work to other converter topologies.

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