Piecewise Quadratic Slope Compensation Technique for DC-DC Switching Converters

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***Abstract*—In this paper, a piecewise quadratic slope compensation technique for eliminating subharmonic oscillations in dc-dc switching converters is studied. With this technique, a self-generated signal is used in the compensation scheme resulting in a naturally full duty cycle stability domain. The expression of the piecewise quadratic compensating signal within a switching cycle is derived. It is obtained that the steady-state value of the amplitude of this signal is the same as in the conventional linear slope compensation scheme that guarantees stability for all values of the duty cycle. However, in the piecewise quadratic scheme this is achieved without exact knowledge of the inductance value nor sensing the input and the output voltages. The stability of the converter under the considered compensation scheme is also guaranteed for all values of the duty cycle with voltage loop open. A boost converter under peak current mode control is used to validate the theoretical results both by numerical simulations and by experiments. Simulation results are analyzed and compared to the performances of the state-of-art techniques with voltage loop closed.**

***Index Terms*—dc-dc power converters, subharmonic oscillation, slope compensation, current mode control.**

I. Introduction

SLOPE compensation using an external sawtooth periodic signal with a constant slope is the conventional strategy used by power electronics engineers for stabilizing switching converters under peak CMC [1], [2]. With this technique a periodic sawtooth signal is subtracted from the reference signal such that by adequately adjusting its slope, the system is stabilized. The larger the slope of the ramp the wider is the stability range in terms of the duty cycle [3]–[5]. In order to have a stable system for all values of duty cycles, the slope must be equal to one half the absolute value of the falling slope of the sensed inductor current.

In addition to the constant slope compensation, many control methods have been proposed to suppress subharmonic oscillations. Roughly speaking, the suppression of this undesired behavior can be performed either by shaping the frequency response of the controller [6], [7], by updating the amplitude of the compensation signal in the time domain [8]–[17] or by injecting external stabilizing signals leading to resonant parametric perturbation (RPP) [18], [19]. Time delayed feedback control (TDFC) stabilizes unstable periodic orbits in nonlinear systems by shaping the frequency response of the controller and was applied to suppress subharmonic oscillation in dc-dc converters [20]–[22]. Nevertheless, TDFC cannot be implemented using analog devices. Filter-based stabilization techniques approximating the TDFC using implementable filters were proposed in [6], [7], [23], [24] to stabilize switching converters.

In order to eliminate subharmonic oscillation in a dc-dc buck converter under VMC, RPP method was applied in [18] and it was empirically observed that a sinusoidal perturbation can stabilize the system and the effects of phase shift frequency mismatches in the stabilizing signal have been studied. It was also shown that the control effort can be significantly reduced if the stabilizing signal is applied with an appropriate phase shift.

In [19], RPP was used for stabilizing a PFC boost converter under peak CMC by superposing an external sinusoidal signal to the reference current. The authors have analytically explained why the technique in [18] works, and developed methods for obtaining optimal choice for the stabilizing signal. The main advantage of the RPP technique with phase shift over the RPP method is that the stabilizing signal in the second case is zero if the phase shift is optimized. This also leads to the conservation of the desired peak reference value of the inductor current while having the same stabilizing effect as the RPP. However, the generation of a stabilizing signal with an optimum phase shift and its synchronization with the clock signal is hard from implementation point of view.

The zero-perturbation dynamic slope compensation (ZPDC) scheme was proposed to suppress subharmonic oscillation while accurately tracking the current reference by the peak value of the inductor current in a buck converter [8]. This technique was further developed for a boost converter and

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a hybrid dynamic compensation (HDC) was proposed for PFC in [16]. The HDC is a combination of ZPDC and ripple compensation and achieves the accurate tracking of the average inductor current instead of its peak making it suitable for PFC applications while inheriting the advantage of ZPDC in eliminating subharmonic oscillation.

To overcome the problem related to the implementation of an RPP scheme with an optimum phase shift and its synchronization with the clock signal, a Dynamic Resonant Perturbation (DRP) technique was proposed in [17] to stabilize a buck converter under peak CMC. In that work, the stabilizing signal is generated from the ac component of the output voltage achieving the same stabilizing effect of the phase shifted RPP technique. The technique leads naturally to zero perturbation at the switching instant and it consists of extracting the compensation signal from the output voltage after differentiating the output voltage to remove its dc component, integrating the result and resetting it to zero at the end of each switching cycle. The resulting compensation signal has a time-varying slope that reaches an optimum value at the switching instant. However, the technique, using the output voltage for extracting the compensating signal, can only be applied to the buck converter for which the derivative of the output voltage is continuous. For the vast majority of switching converters, the derivative of this voltage is discontinuous and the previous technique would result in serious noise problems.

II. Motivation, main contribution and organization of the study

The basic principle to generate a conventional linear ramp compensating signal is to integrate a constant voltage within a switching cycle. To avoid subharmonic oscillation in switching converters under peak CMC with a conventional linear compensation for all values of duty cycle, the slope m_a of the compensating signal must satisfy the inequality $m_a > R_s m_0/2$, where R_s is current sensing resistance, $R_s m_0$ is the slope of the sensed current during the discharging (OFF) interval. To provide the suitable slope compensation, it is necessary to know m_0 beforehand and this depends on either both the input and output voltages in the boost converter or on the output voltage in the buck converter. By sensing the input and the output voltages make the control circuitry not only complex but also costly. Moreover, in all the cases, m_0 depends also on the inductance L which is not a constant parameter that may change it value according to its operating current especially where weight and size are major constraints and working with saturable inductors becomes a necessity to achieve compact switched mode power supplies [25]. In this particular case, no practical hints are available in the literature on how to select the slope of the compensating slope for switching converters.

Hence, the most important limitation of the conventional slope compensation scheme and some state-of-art strategies is that they cannot provide an adaptive way for selecting the appropriate slope which can guaranty of robust stability for all inductance and duty cycle values. In most of the designs, the worst case approach, which in peak CMC, corresponds to the maximum duty cycle and the minimum inductance values, leads to overcompensation for other operating points.

The method proposed in [26] is based on a simple and practical idea of generating the compensating signal from the error between the inductor current and its reference leading to a Piecewise Quadratic (PWQ) compensating signal with a cycle-by-cycle time-varying amplitude. Although the main idea of the compensation strategy has been published in [26] and presented in [27], more research effort is still required for a thorough understanding of its operation. Hence, the research goal in this paper is to provide a detailed analysis of the technique proposed in [26] and its experimental validation. The expression of the PWQ variable amplitude slope compensating signal and the corresponding duty cycle are derived in closed form for the fist time. The steady-state amplitude of the PWQ compensating signal is also determined. It is shown that it is equal to the constant amplitude of the ramp signal in the conventional linear slope compensation scheme that guarantees stability for all values of the duty cycle. However, with the PWQ compensation scheme, this is achieved without exact knowledge of the inductance value nor sensing the input and the output voltages. It will be shown that the technique significantly improve the main drawbacks of both conventional and the state-of-art compensation techniques without extra complexity hence enabling wider operation range ensuring stability of the current loop even for reduced values of inductance. Experimental results show that the idea works well hence it could be useful for some applications especially for those requiring small size and high performance in miniaturized power converters.

The paper is structured in eight different sections. After this introduction, Section II presents the Piecewise Quadratic (PWQ) slope compensation technique for dc-dc switching converters under peak CMC. Section III deals with a unified approach for stability analysis of a switching converter under peak CMC with the PWQ slope compensation technique. Using a reduced-order model that considers the inductor current as the only state variable of the power stage, it has been demonstrated that stability can be guaranteed for all duty cycle values considering the voltage loop open. The technique is applied in Section IV to a dc-dc boost converter where both numerical simulations and experimental measurements demonstrate the validity of the PWQ slope compensation technique. A comparison between the conventional and the ZPDC compensation schemes from one hand and the PWQ technique from the other hand is presented in Section VI. A discussion is given in Section VII. Finally, concluding remarks are drawn in the last section.

III. Piecewise quadratic slope compensation technique for switching converters under CMC

A. Unified inductor current model in switching converters

Fig. 1 shows the unified three-terminal circuit diagram of a switching converter under peak CMC. The terminals designations a, p, and c refer to active, passive and common respectively. The common node between the switches S and $\overline{\text{S}}$ connects to the inductor whose inductance is L. The switching element $\overline{\text{S}}$ is a diode in unidirectional converters while it is a transistor in bidirectional and synchronous converters.

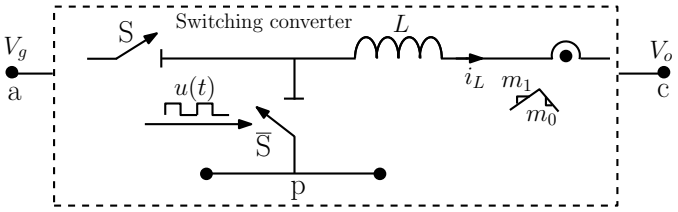


Fig. 1. Unified three terminal circuit diagram of an elementary switching converter under CMC.

TABLE I
INPUT, OUTPUT TERMINAL VOLTAGES AND INDUCTOR CURRENT RISING AND FALLING SLOPES m_1 AND m_0 FOR THE ELEMENTARY SWITCHING CONVERTERS.

Parameter	Buck	Boost	Buck-Boost
V_g	V_{ap}	v_{ca}	V_{ac}
V_o	v_{cp}	v_{pa}	V_{pc}
m_1	$\frac{V_g - V_o}{L}$	$\frac{V_g}{L}$	$\frac{V_g}{L}$
m_0	$-\frac{V_o}{L}$	$\frac{V_g - V_o}{L}$	$\frac{V_o}{L}$

Table I shows the input and the output voltages for the three elementary converters in terms of the voltage between the terminals a, p, and c. The ripple of the output voltage V_o is much smaller than the inductor current ripple. It can be considered constant during a switching period without losing accuracy. In Continuous Conduction Mode (CCM) operation, the inductor current in a switching converter is described by a piecewise linear state-space model that can be written in the following form:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \begin{cases} m_1 & \text{if } u=1 \\ m_0 & \text{if } u=0 \end{cases} \tag{1}$$

where m_1 and m_0 are the raising and falling slopes of the inductor current i_L that are detailed in Table I for elementary switching converters.

B. Description and analysis of the piecewise quadratic slope compensation scheme

Under peak CMC, the switch S is closed ($u = 1$) at the beginning of each switching cycle and it opens ($u=0$) when the inductor current (scaled by a gain R_s) reaches the signal $R_s i_{\mathrm{ref}} - v_m$, where v_m is the compensating signal. The state of the switch $\overline{\mathrm{S}}$ is complementary to that of S. The current is sensed by a small shunt resistance r_s and then amplified by a gain A, hence $R_s = Ar_s$. The resulting amplified signal is a voltage $R_s i_L$, is connected to one input of a comparator while the voltage $R_s i_{\mathrm{ref}}$, is connected to its other input. When the converter is under constant switching frequency operation, slope compensation is required to ensure the stability of the converter and to avoid subharmonic oscillations. In this case, a compensating signal v_m is subtracted from $R_s i_{\mathrm{ref}}$ before connecting it to the corresponding comparator pin. It is well-known that in order to guarantee stability of a switching converter under peak CMC for all duty cycle values in a switching converter with a conventional linear slope compensation scheme, the added slope m_a has to be one-half the absolute value $-R_s m_0/2$ of the falling slope of the sensed inductor current $R_s i_L$ [2]. As in the conventional compensation scheme, the clock signal determines the fixed switching frequency. In Fig. 2, the signal $R_s i_{\mathrm{ref}}$ is provided by the external voltage loop controller. The output voltage v_o is subtracted from its desired reference signal V_o to form the error signal which is processed by the voltage controller to provide the reference signal $R_s i_{\mathrm{ref}}$. The voltage controller is usually a PI compensator followed by a low pass filter. The bandwidth of this loop is typically much lower than the current loop bandwidth in such a way that the output of the outer loop can be considered a dc signal. Therefore, for the sake of simplicity, this signal is considered constant in the mathematical analysis given below.

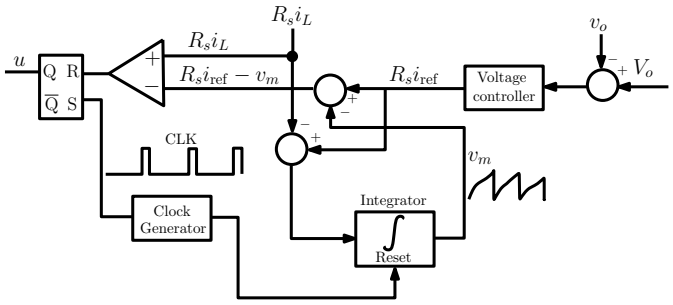


Fig. 2. The block diagram of the PWQ slope compensation technique together with the pulse width modulator and the outer voltage controller.

The current error signal in dc-dc switching converters under peak CMC always includes a dc component and a piecewise linear (triangular) ac switching ripple. This error signal has been used in [26] to generate a slope compensating signal to eliminate subharmonic and chaotic instabilities. The expression of the slope generated compensation signal is governed by the following expression [26]:

$$v_m(t) = \rho \int_0^{t \bmod T} (i_{\mathrm{ref}} - i_L(\zeta))\mathrm{d}\zeta \tag{2}$$

where $\rho = R_s/T$. The integral is reset to zero at the beginning of each switching cycle of time period T. Let $i_L(nT) := i_L[n]$ be the value of the inductor current at time instant nT. During the switching cycle $(nT, (n+1)T)$, and according to (1), the expression of the inductor current can be expressed as follows:

$$i_L(t) = \begin{cases} i_L[n] + m_1 t & \text{if } u = 1 \\ i_p[n] + m_0(t - (n + d[n])T) & \text{if } u = 0 \end{cases} \tag{3}$$

where $i_p[n] := i_L((n + d[n])T)$ is the peak value of the inductor current within the switching cycle $(nT, (n+1)T)$. Let $v_m[n] := v_m((n+1)T)$ be the value of the compensating signal v_m at the end of the cycle $(nT, (n+1)T)$ and $\nu[n] := v_m(n+d_nT)$ be its at the switching time instant $d[n]T$. Therefore, $i_p[n] = i_{\mathrm{ref}} - \nu[n]/R_s$ and hence similarly to the conventional linear ramp compensation scheme, the value of the peak current i_p is smaller than the desired value i_{ref}. Fig. 3 shows the key waveforms of the control signals $R_s i_{\mathrm{ref}} - v_m$ and $R_s i_L$ together with the generated compensating signal v_m.

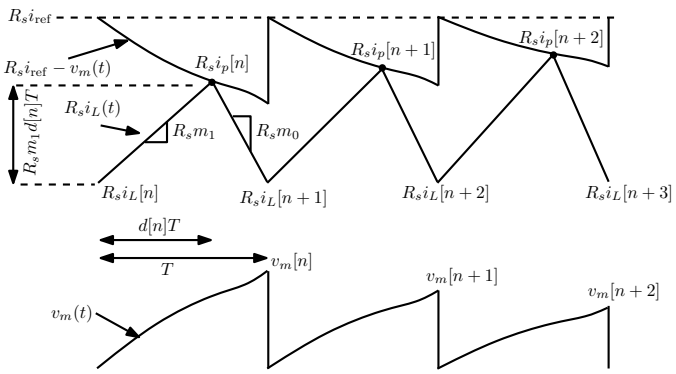


Fig. 3. The key waveforms of the control signals with the PWQ compensation technique.

From (2)-(3), the expression of the PWQ compensation signal during the switching cycle $(nT, (n+1)T)$, becomes as follows

$$v_m(t) = \begin{cases} \mu_1[n]t - \rho\dfrac{m_1}{2}t^2 & \text{if } u = 1 \\ \nu[n] + \mu_0[n](t - d[n]T) & \\ -\rho\dfrac{m_0}{2}(t - d[n]T)^2 & \text{if } u = 0 \end{cases} \tag{4}$$

where $\mu_1[n]$, $\mu_0[n]$ and $\nu[n]$ are given by the following expressions

$$\mu_1[n] = \rho(i_{\rm ref} - i_L[n]) \tag{5a}$$
$$\mu_0[n] = \mu_1[n] - \rho m_1 d[n]T \tag{5b}$$
$$\nu[n] = \mu_1[n]d[n]T - \rho\frac{m_1}{2}(d[n]T)^2 \tag{5c}$$

It can be observed that the generated PWQ compensating signal contains both linear and quadratic terms. Note also that its amplitude is cyclically time-varying. At the start of a switching period, the compensation signal is zero and at the end of the same period it reaches the cycle-by-cycle time-varying value $v_m[n]$ given by

$$v_m[n] = \nu[n] + \mu_0[n](1 - d[n])T - \rho\frac{m_0}{2}(1 - d[n])T)^2 \tag{6}$$

where $\overline{d}[n] = 1 - d[n]$. Next, the expression of the duty cycle resulting from the use of the PWQ compensation strategy and the steady-state amplitude of the compensating signal will be derived.

C. The duty cycle expression under the PWQ piecewise quadratic slope compensation scheme

The duty cycle $d[n]$ during the switching cycle $(nT, (n+1)T)$ is decided by the intersection of the signal $R_s i_{\rm ref} - v_m$ and the voltage $R_s i_L$ within that cycle (see Fig. 3). Therefore, the switching condition with the PWQ slope compensation strategy can be expressed in terms of the duty cycle and the sampled values of the previous signals as follows

$$R_s(i_L[n] + m_1 d[n]T) - (R_s i_{\rm ref} - \nu[n]) = 0 \tag{7}$$

Equation (7) has two solutions for the duty cycle $d[n]$ with the acceptable one given by

$$d[n] = 1 - \frac{\sqrt{m_1^2 + \mu_1^2[n]} - \mu_1[n]}{m_1} \tag{8}$$

Note that under peak CMC one has that $i_L[n] < i_{\rm ref}$ which implies that $\mu_1[n] > 0$ and the condition $0 < d[n] < 1$ will always hold since in this case the following inequalities are always satisfied

$$-m_1 < \mu_1[n] - \sqrt{m_1^2 + \mu_1[n]^2} < 0 \tag{9}$$

D. The steady-state amplitude of the piecewise quadratic compensating signal

As mentioned before the amplitude $v_m[n]$ of the compensating signal is cyclically time-varying according to (6). In steady-state, its value $v_m[\infty] := V_M$ is given by the following expression

$$V_M = \nu[\infty] + \mu_0[\infty](1 - D)T - \rho\frac{m_0}{2}((1 - D)T)^2 \tag{10}$$

The value of $\nu[\infty]$ and $\mu_0[\infty]$ can be derived by solving (7) for $i_L[\infty]$, taking into account that in steady-state one has $Dm_1 = -(1 - D)m_0$, and substituting in (5a)-(5c) which results in:

$$i_L[\infty] = i_{\rm ref} - \frac{1}{2}m_0(D - 2)T \tag{11a}$$
$$\mu_1[\infty] = \frac{1}{2}\rho m_0(D - 2)T \tag{11b}$$
$$\mu_0[\infty] = -\frac{1}{2}\rho m_0 DT \tag{11c}$$
$$\nu[\infty] = -\frac{1}{2}\rho m_0 DT^2 \tag{11d}$$

Therefore by using (10) and (11c)-(11d), V_M becomes

$$V_M = -\frac{1}{2}\rho m_0 T^2(D + D(1 - D) + (1 - D)^2) = -\frac{1}{2}R_s T m_0 \tag{12}$$

which is the same amplitude guaranteeing stability for all duty cycles for a conventional linear slope compensation scheme [2]. Note, however, that while with the PWQ technique (12) is naturally fulfilled, this will need an offline tuning in terms of the system input and output voltages and inductance value in the conventional scheme. As mentioned before, the effective peak value of the inductor current $i_p[n] = i_{\rm ref} - \nu[n]/R_s$ is smaller than the desired value $i_{\rm ref}$ similarly to the conventional linear ramp compensation scheme. In steady-state, one has $i_p[\infty] := I_p$ given by

$$I_p = i_{\rm ref} - \frac{\nu[\infty]}{R_s} = i_{\rm ref} + \frac{1}{2}m_0 DT, \tag{13}$$

The steady-state tracking error ε is given by the difference between $i_{\rm ref}$ and I_p. This can be expressed as follows

$$\varepsilon = i_{\rm ref} - I_p = -\frac{1}{2}m_0 DT = D\frac{V_M}{R_s} \tag{14}$$

It can be observed that the error ε increases with the duty cycle D.

IV. Stability analysis of switching converters with the PWQ slope compensation scheme

A. Continuous-time switched model

To perform an accurate stability analysis of the system we use Floquet theory combined with Filippov method to study the behaviour of the system during the switching events [28], [29]. The analysis provided in this section uses a reduced-order model considering the inductor current to be the dominant state variable of the power stage circuit, similarly to what is conventionally done when subharmonic oscillation is of concern [2]. The equation generating the slope compensating signal is also considered in the analysis. Therefore, the state-space model of the closed-loop system is as follows

$$\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t} = \mathbf{m}_u(\mathbf{x}), \tag{15}$$

where $\mathbf{x} = (i_L, \quad v_m)^\intercal$ is the vector of state variables of the closed loop system, $\mathbf{m}_u(\mathbf{x}) = \mathbf{A_u x} + \mathbf{B_u}$ is the switched vector field and $\mathbf{A}_1$, $\mathbf{A}_0$, $\mathbf{B}_1$ and $\mathbf{B}_0$ are the state matrices and input vectors corresponding to $u = 1$ and $u = 0$ respectively and that are given by

$$\mathbf{A}_1 = \mathbf{A}_0 = \begin{pmatrix} 0 & 0 \\ -\rho & 0 \end{pmatrix} \tag{16}$$

$$\mathbf{B}_1 = \begin{pmatrix} \frac{V_g}{L} \\ \rho i_{\mathrm{ref}} \end{pmatrix} = \begin{pmatrix} m_1 \\ \rho i_{\mathrm{ref}} \end{pmatrix}, \tag{17}$$

$$\mathbf{B}_0 = \begin{pmatrix} \frac{v_g - V_o}{L} \\ \rho i_{\mathrm{ref}} \end{pmatrix} = \begin{pmatrix} m_0 \\ \rho i_{\mathrm{ref}} \end{pmatrix} \tag{18}$$

The conditions governing the switching from the model with $u = 1$ to the one with $u = 0$ are given by the following expressions

$$h_1(\mathbf{x}, t) := R_s(i_{\mathrm{ref}} - i_L) - v_m = 0, \tag{19}$$

$$h_0(\mathbf{x}, t) := \frac{t}{T} \bmod 1 = 0. \tag{20}$$

With the state-space switched model and the switching conditions available, Floquet theory combined with Filippov technique can readily be applied for performing stability analysis of the system [28]. This analysis can be carried out by using the monodromy matrix which is an effective tool to accurately analyze the stability of dc-dc switching converters [28]. The different kinds of instabilities can be identified by using the eigenvalues of this matrix. Subharmonic oscillation is exhibited when one of the eigenvalues crosses the unit disk from the point $(-1, 0)$ in the complex plane.

B. Monodromy matrix

The monodromy matrix is given by [28]

$$\mathbf{M} = \mathbf{S}_0 e^{\mathbf{A}_0(1-D)T} \mathbf{S}_1 e^{\mathbf{A}_1 DT}, \tag{21}$$

where $e^{\mathbf{A}_1(DT)}$ and $e^{\mathbf{A}_0(1-D)T}$ are the state transition matrices through ON and OFF periods during which $u = 1$ and $u = 0$ respectively given by

$$e^{\mathbf{A}_1(DT)} = \begin{pmatrix} 1 & 0 \\ -DT & 1 \end{pmatrix}, \quad e^{\mathbf{A}_0(1-D)T} = \begin{pmatrix} 1 & 0 \\ -(1-D)T & 1 \end{pmatrix}. \tag{22}$$

The state transition matrices across switching (also called saltation matrices) are given by [28]

$$\mathbf{S}_1 = \mathbf{I} + \frac{(\mathbf{m}_0 - \mathbf{m}_1)\mathbf{n}_1^\intercal}{\mathbf{n}_1^\intercal \mathbf{m}_1 + \frac{\partial h_1}{\partial t}}, \quad \mathbf{S}_0 = \mathbf{R} + \frac{(\mathbf{m}_0 - \mathbf{R}\mathbf{m}_1)\mathbf{n}_0^\intercal}{\mathbf{n}_0^\intercal \mathbf{m}_1 + \frac{\partial h_0}{\partial t}}, \tag{23}$$

where $\mathbf{I}$ is the identity matrix and $\mathbf{n}_1$ and $\mathbf{n}_0$ are the gradients of the switching surfaces for the saltation matrices that are given by [28]

$$\mathbf{n}_1 = \frac{\partial h_1}{\partial \mathbf{x}} = -[1, 1]^\intercal, \quad \frac{\partial h_1}{\partial t} = 0 \tag{24}$$

$$\mathbf{n}_0 = \frac{\partial h_0}{\partial \mathbf{x}} = [0, 0]^\intercal, \quad \frac{\partial h_0}{\partial t} = \infty \tag{25}$$

$\mathbf{R}$ stands for a projection operator that can be expressed as follows

$$\mathbf{R} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}. \tag{26}$$

It is important to note that the state v_m is reset to zero at the end of each clock. That is why we need to consider $\mathbf{S}_0$ at the reset point. The expression of the saltation matrix $\mathbf{S}_0$ is obtained like in impacting system [30]. At the reset point $t = T$, the impact law relates the state after switching ($\mathbf{x}^+$) to the state before switching ($\mathbf{x}^-$) and given by $\mathbf{x}^+ = \mathbf{R}\,\mathbf{x}^-$.

Taking into account the previous equations, the expression of the saltation matrices $\mathbf{S}_1$ and $\mathbf{S}_0$ are given by

$$\mathbf{S}_1 = \begin{pmatrix} 1 + \frac{m_0 - m_1}{m_1 + \mu_1[\infty]} & \frac{m_0 - m_1}{m_1 + \mu_1[\infty]} \\ 0 & 1 \end{pmatrix}, \ \mathbf{S}_0 = \mathbf{R}. \tag{27}$$

After some algebra, the expression for Monodromy matrix becomes as follows

$$\mathbf{M} = \begin{pmatrix} 1 + \frac{(m_0 - m_1)(1-D)}{m_1 + \mu_1[\infty]} & \frac{m_0 - m_1}{m_1 + \mu_1[\infty])} \\ 0 & 0 \end{pmatrix}$$

The stability of the system can be analyzed by monitoring the eigenvalues of the matrix $\mathbf{M}$. Since the signal v_m is reset to zero at the start of every switching cycle, one of the eigenvalues is zero and the remaining one is given by

$$\lambda = 1 + \frac{(m_0 - m_1)(1-D)}{m_1 + \mu_1[\infty]} \tag{28}$$

Using the expression of $\mu_1[\infty] = \rho(i_{\mathrm{ref}} - i_L[\infty]) = m_1 D(2-D)/(2-2D) = m_0(D/2-1)$ and taking into account the steady-sate condition $Dm_1 = -(1-D)m_0$ one gets

$$\lambda = \frac{D(2-D)}{2-D^2} \tag{29}$$

The eigenvalue λ is always positive and subharmonic oscillation cannot take place in the switching converter with the PWQ compensation scheme. Furthermore, this eigenvalue takes its maximum value 1 for $D = 1$ and the system is free

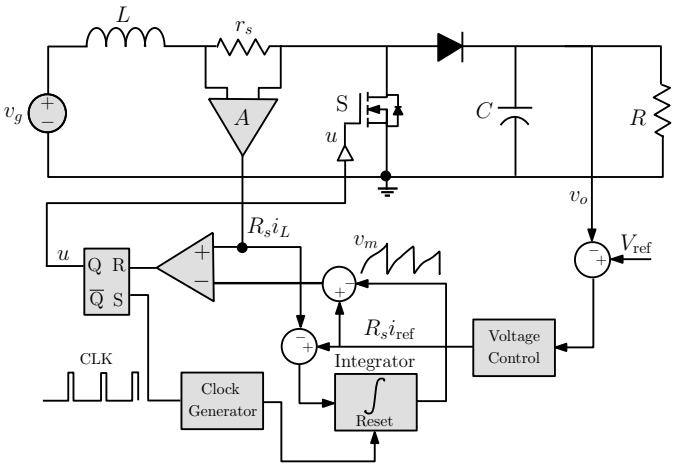


Fig. 4. Schematic circuit diagram of a boost converter under peak CMC with the PWQ slope compensation scheme.

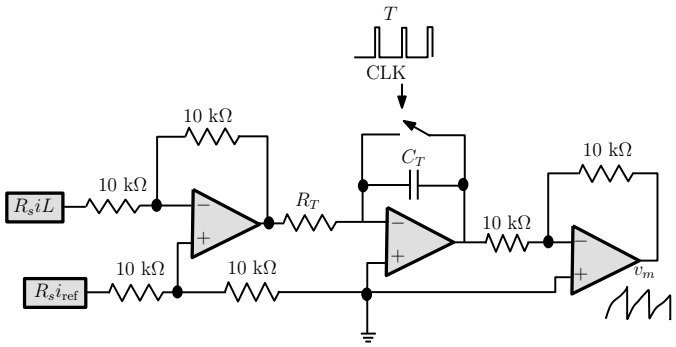


Fig. 5. Circuit diagram of the practical implementation of the signal generator for the PWQ slope slope-compensation scheme in CMC.

from any kind of instability for all values of the steady-state duty cycle D within the interval (0,1) with voltage loop open[1].

It is worth to note that the previous analysis is applicable to any switching converter under CMC since no specification of the converter topology has been made. Below, the technique presented in the previous section is applied to a boost converter under peak CMC.

[1]It well known that, by ignoring the outer voltage loop feedback in a switching converter under peak CMC, subharmonic oscillation is avoided with a conventional slope compensation if the compensating ramp slope m_a is selected such that [2]

$$-\frac{m_0 + m_a}{m_1 + m_a} < 1 \tag{30}$$

where $m_1 > 0$ and $m_0 < 0$ are the slopes of the sensed inductor current during the discharging (ON) and discharging (OFF) phases respectively and $m_a > 0$ is the slope of the ramp compensator. From (30) it can be observed that with $m_a = 0$, the previous condition becomes $-m_0/m_1 = -D/(1-D) < 1$ which is met for $D < 1/2$ and therefore, subharmonic oscillation will not take place in this case. However, with voltage loop closed, the voltage ripple can interact with the PWM process and provoke subharmonic oscillation even for duty cycle values less than $1/2$ or it can stabilize the system for duty cycle values larger than $1/2$. For the PWQ strategy, the converter is stable for all values of the duty cycle with voltage loop open. However, like in the case of conventional ramp compensation, with voltage loop closed, the voltage ripple can cause or suppress subharmonic oscillation. The focus in this work is on the current loop stability. Further research is needed to understand the effect of the voltage ripple with voltage loop closed.

TABLE II
PARAMETERS FOR BOOST CONVERTER USED IN THE NUMERICAL SIMULATIONS AND THE EXPERIMENTAL VALIDATION.

Power-stage	Control-stage
Input voltage, $V_g = 5$ V	i_{ref} variable
Output voltage, V_o Variable	$R_s = 1\ \Omega$
Inductance, $L = 1$ mH	$R_T = 40$ kΩ
Capacitance, $C = 200\ \mu$F	$C_T = 1$ nF
Switching frequency, $f_s = 25$ kHz	

V. APPLICATION TO A BOOST CONVERTER UNDER CMC

First, numerical simulations will be performed and then an experimental validation will be provided. The parameter values are the ones shown in Table II.

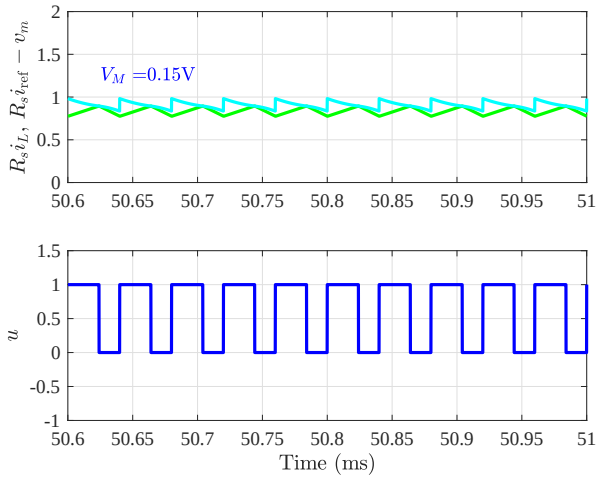
A. Validation of the slope compensation technique by numerical simulations

The circuit schematic used in the simulations is depicted in Fig. 4. Numerical simulations are performed using PSIM© software to validate the theoretical results related to the PWQ slope compensation scheme which can be implemented by the analog circuit diagram depicted in Fig. 5 where a resettable integrator has been used. Without loss of generality, the resistance R_T and the capacitance C_T are selected in such a way that $R_T C_T = T$, where T is the switching period. All parameter values used are listed in Table II.

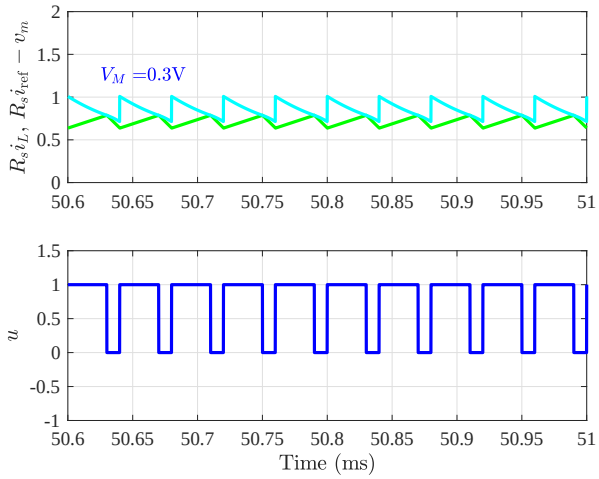
The voltage is regulated to its desired reference V_o using a PI compensator having a proportional gain $k_p = 1.5$ black and a time constant $\tau = 2$ ms. The corner frequency of the low pass filter at its output was fixed to $f_b = 2$ kHz. The average value $\overline{I}_L$ of the inductor current i_L is imposed according to the power balance between the input and the output of the converter implying $\overline{I}_L = V_o/(R(1-D))$. The peak value is $I_p = \overline{I}_L + m_1 DT/2$. The values of the load resistance used are selected in such a way that the average value $\overline{I}_L$ is equal to 0.8 A and 1.6 A for $R = 100\ \Omega$ and $R = 50\ \Omega$ respectively.

Fig. 6 shows the time-domain response of the converter under peak CMC with the PWQ compensation scheme in steady-state operation. The system is operated with two different steady-state duty cycle values which have been obtained by varying the desired output voltage V_o of the converter while maintaining the input voltage V_g constant. It can be observed that the stability is guaranteed for both duty cycle values used. Furthermore, the amplitude V_M of the compensation signal in steady-state evolves according to the theoretical expression (12). According to (12), the amplitude V_M for $D = 0.6$ is $V_M|_{D=0.6} = 0.15$ V agreed with the simulation result in Fig. 6-a. The tracking error in this case is $\varepsilon|_{D=0.6} = 0.09$ A. According to the same equation, the amplitude V_M for $D = 0.75$ is $V_M|_{D=0.75} = 0.3$ V agreed with the simulation result in Fig. 6-b. The tracking error in this case is $\varepsilon|_{D=0.75} = 0.22$ A.

Next, the results will be compared with the ZPDC technique [16] with a gain $k = 0.03$ s/H under input voltage, load resistance and inductance changes. The minimum value of k for stabilizing the system using ZPDC is $k_{\min} = T/(2L) = 0.02$ s/H [16]. A total time interval starting at 40 ms and

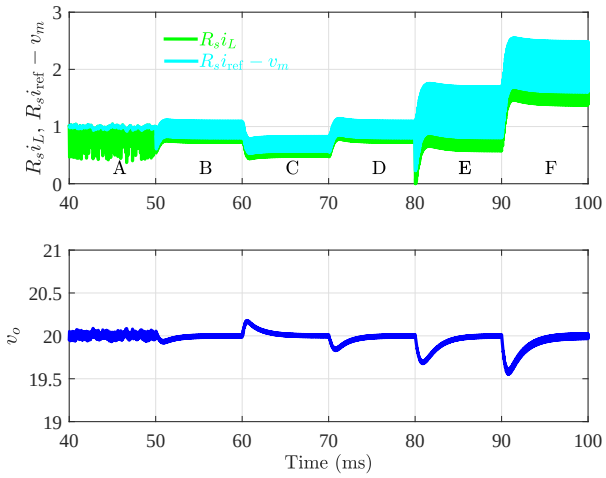


(a) $D = 0.6 \rightarrow V_o = 12.5$ V, $V_g = 5$ V and $R = 36.76\ \Omega$.

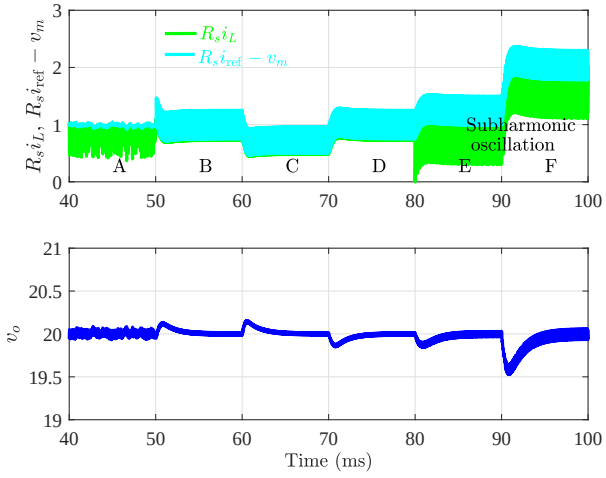


(b) $D = 0.75 \rightarrow V_o = 20$ V, $V_g = 5$ V and $R = 114.28\ \Omega$.

Fig. 6. PSIM© numerical simulations of the system response under the PWQ slope compensation with voltage loop closed. In this case the current reference is provided by an external PI voltage controller. The reference voltage V_o was varied to get the different values of the duty cycles and the load resistance R was adapted accordingly to maintain the same current reference ($i_{\rm ref} = 1$ A) for both steady-duty cycle values.



(a) PWQ.

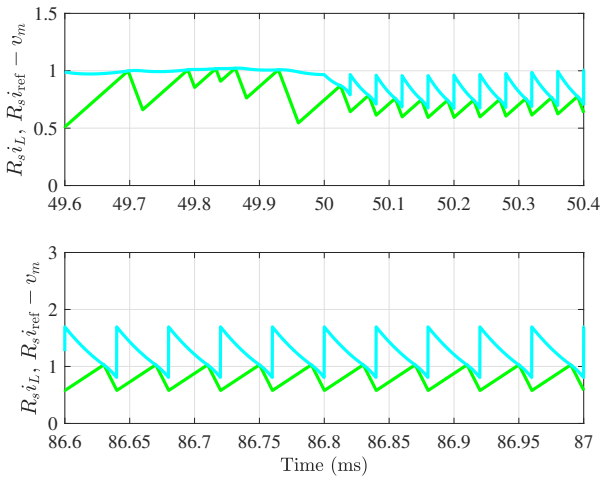


(b) ZPDC.

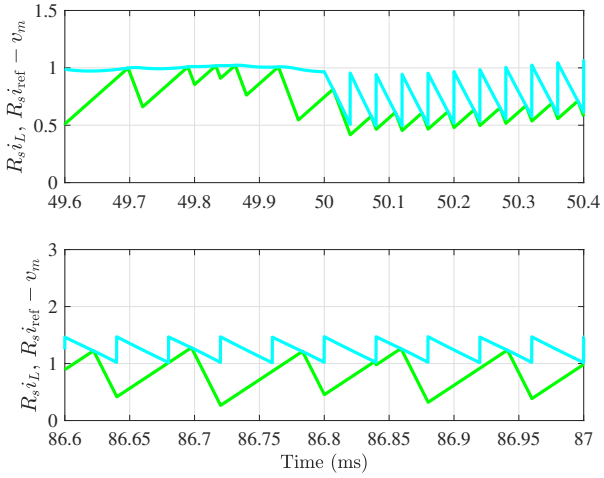
Fig. 7. The transient response under input voltage V_g, inductance L and load resistance R changes with the PWQ and the ZPDC compensation schemes.

ending at 100 ms was selected to perform the numerical simulations. This total interval is divided into 6 sub-intervals labeled A, B, C, D, E and F. Fig. 7 shows the time-domain response of the converter under peak CMC with the PWQ compensation scheme and the ZPDC technique during the total time interval (40,100) ms. In both cases, before the time instant $t_1 = 50$ ms (during sub-interval A), the system is operated with $V_g = 5$ V, $V_o = 20$ V ($D = 0.75$) $L = 1$ mH and $R = 100\ \Omega$ and without slope compensation hence the system exhibits subharmonic oscillations. The previous load resistance value was selected to give an average value of the inductor current of 0.8 A. At the time instant $t_1 = 50$ ms and during sub-interval B, the control strategies are activated and the system is stabilized in both cases. A zoomed view including the end of sub-interval A and the beginning of sub-interval B is depicted in Fig. 8-a where the stabilizing effect of both compensation schemes can be clearly observed.

At the time instant $t_1 = 60$ ms and during sub-interval C, a step change of 2 V is applied to the input voltage V_g and at the time instant $t_2 = 70$ ms and during sub-interval D, the original value of V_g is recovered. With both compensating schemes, the system presents a stable behavior free from subharmonic oscillation under this input voltage step change. At the time instant $t_3 = 80$ ms and during and during sub-interval E the value of inductance L is reduced to 0.33 mH. It can be observed that while the PWQ technique still maintains stable behavior, the ZPDC technique cannot stabilize the system with this reduced value of L and subharmonic oscillation is exhibited leading to a noticeable increase in the inductor current and output capacitor voltage ripples. It is worth to note here that the system can still be stabilized using the ZPDC technique if an updated value of gain k is used. With the PWQ scheme such a parameter re-tuning is not needed because the amplitude of the modulating signal is naturally adapted in terms of the new inductance value. Furthermore, since



(a) PWQ.



(b) ZPDC.

Fig. 8. Zoomed views of Fig. 7 showing the effect of the PWQ and the ZPDC compensation schemes.

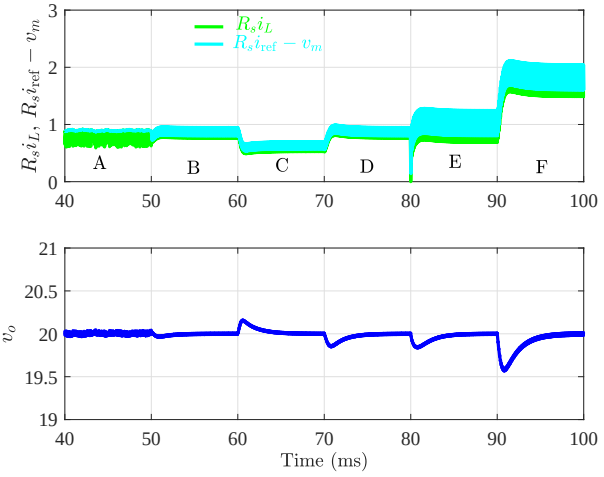


Fig. 9. The transient response under input voltage V_g, inductance L and load resistance R changes under the PWQ with switching frequency $f_s = 50$ kHz.

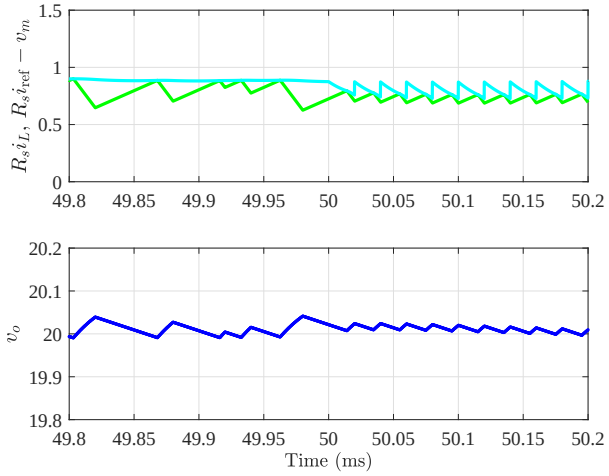


Fig. 10. Zoomed view of Fig. 9 showing the stabilizing effect of the PWQ compensation scheme with switching frequency $f_s = 50$ kHz.

the value of the inductance current is inherently taken into account in the PWQ compensation process, the stability of the converter will be guaranteed even for small inductance values. Therefore, the operation of the converter under the PWQ compensation scheme could allow a significant reduction of the size of the inductor which could result in an improvement of the power density. Finally, at the time instant $t_4 = 90$ ms and during sub-interval F, the load resistance R was reduced to 50 Ω leading to an average value of the inductor current of 1.6 A while the same reduced value of L is still used. The PWQ technique is still able to suppress subharmonic and maintains stability and robustness under the load changes while the ZPDC technique cannot stabilize the system under the same conditions. To clearly show the system behavior in steady state and the advantage of the PWQ compensation strategy, Fig. 8 depicts a zoomed view of Fig. 7-b showing the steady-state responses of the converter under peak CMC with the PWQ compensation scheme and the ZPDC technique during a small portion between intervals A and B and another small portion at the beginning of sub-interval F.

The previous numerical tests depicted in Fig. 7-b have been reproduced with a higher switching frequency $f_s = 50$ kHz and the results are depicted in Fig. 9. As can be observed, for all the tests, similar performances to those shown in Fig. 7-b are obtained with the new value of f_s. Note however that because of a larger switching frequency, the ripple of the state variables and accordingly the resulting PWQ signal amplitude are smaller in Fig. 9. Fig. 10 illustrates a zoomed view of Fig. 9 showing the steady-state responses of the boost converter under the PWQ compensation during a small time duration between intervals A and B clearly revealing the stabilizing effect of the PWQ compensation scheme with the new value of the switching frequency $f_s = 50$ kHz.

B. Experimental validation of the PWQ slope compensation technique

In this section, the theoretical results and the numerical simulations corresponding to the boost converter under peak

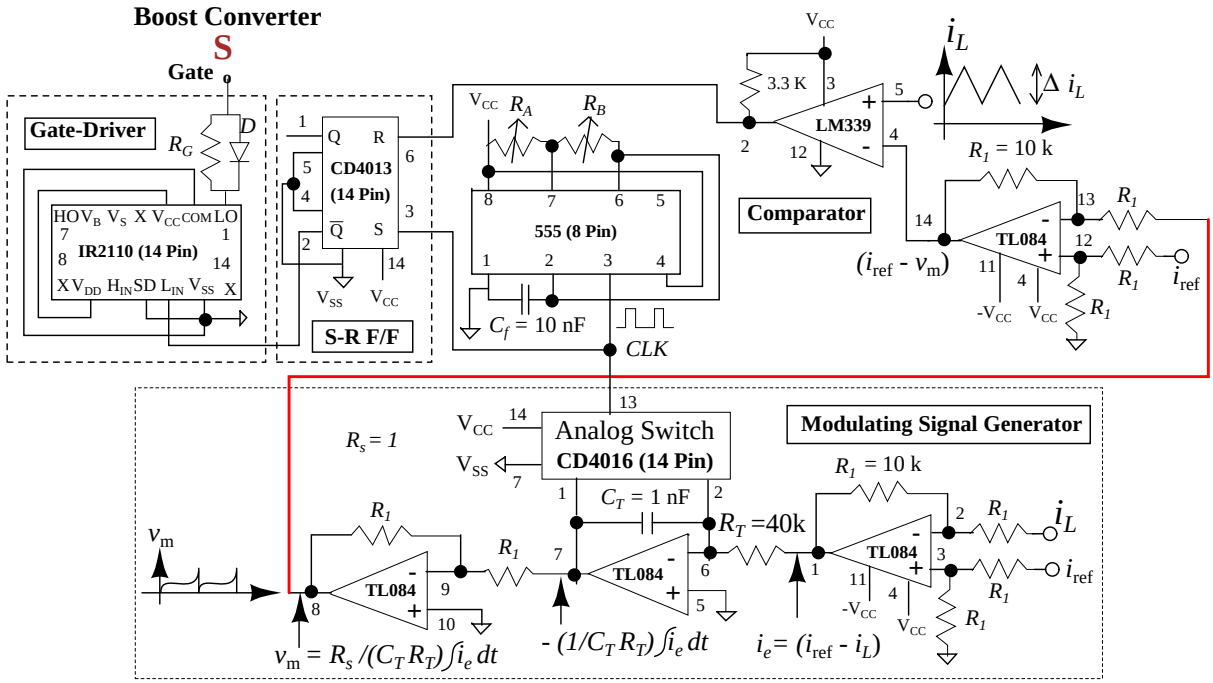


Fig. 11. Detailed schematic circuit diagram for generating the PWQ slope compensating signal together with control circuitry for the boost converter under current mode control using discrete IC chips.

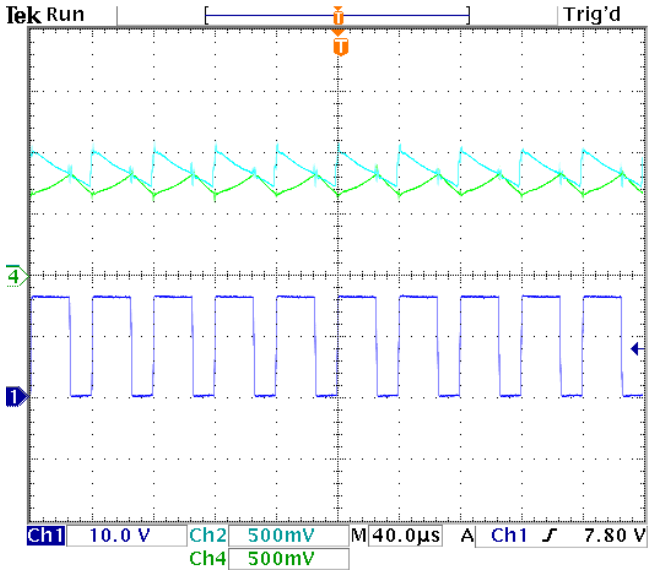
CMC are validated experimentally. For that purpose, an experimental prototype of a boost converter has been built using the same parameters as given in Table II. Fig. 11 shows the schematic circuit diagram of the implemented compensating signal generator. The switch is implemented by the MOSFET IRF640 ($R_{\mathrm{DS(ON)}} = 0.15\ \Omega$) where the driver IR2110 is used to drive the gate of the switch. Ferrite core (E-type) inductor of 1 mH ($r_L = 0.23\ \Omega$) with maximum 1 A current rating was fabricated. The diodes are realized by low forward voltage drop (0.5 V) schottky diode SR240 with a forward voltage $V_f = 0.5$ V. The control circuit uses the 555 timer IC to provide clock signal. To realize analog switch for reset purpose IC4016 is used. The quadruple operational amplifier TL084 is used for various purposes, like the error amplifier, the controller etc. The comparator LM339 compares the current through inductor (using a current sensor LA 55-P with bandwidth 200 kHz) with the control signal $R_s i_{\mathrm{ref}} - v_m$. For S-R latch, flip-flop CD4013 is used. The input voltage was fixed to 5 V. A dc voltage source was connected at the output of the converter. Two different values were used $V_o = 12.5$ ($D = 0.6$) V and $V_o = 20$ V ($D = 0.75$). The signal $R_s i_{\mathrm{ref}}$ was fixed to 1 V. The overall efficiency of the system was measured as 90% at $D = 0.6$ and 86% at $D = 0.75$ being all the losses attributed to the $R_{\mathrm{DS(ON)}}$, r_L and the forward voltage drop $V_f = 0.5$ V of the schottky diode SR240.

Fig. 12 shows the experimental results corresponding to Fig. 6. As in the case of the numerical simulations, the system is operated with different steady-state duty cycle values by varying the output voltage V_o of the converter. It can be observed that using the PWQ compensation technique the system is stable for both values of D. Other measurements not shown here allowed to check that the stability is guaranteed up to $D = 0.9$. The amplitude of the compensation signal in steady-state does not exactly evolve according to the theoretical prediction (12). The measured amplitude V_M of the compensation signal for $D = 0.6$ is 0.3 V while for $D = 0.75$ it is 0.4 V. The measured tracking error for $D = 0.6$ is 0.2 A and it is 0.25 A for $D = 0.75$. The discrepancy between the theoretical results and the experimental measurements is mainly due to factors not taken into account in the theoretical analysis. Among others, this is the case, for instance, of losses in the switching and reactive components and the limited bandwidth of the current sensor.

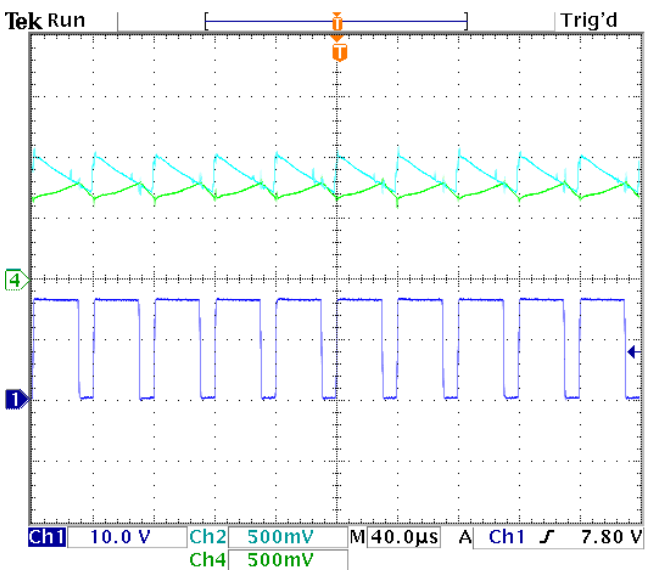
VI. Discussion about the advantages of the PWQ compensation strategy

In the PWQ compensation scheme, the stabilizing signal is generated internally and does not need any appropriate phase shifting so that the system is free from synchronization problems resulting from externally injected signals such as frequency and phase shift mismatches. In [8], [16]–[19], it has been demonstrated that the injection of external signals, appropriately phase shifted, can eliminate subharmonic oscillations in different type of switching converters. It has been also shown that the control success and its effort strongly depend on the phase shift of the stabilizing signal. In order to make a benchmarking comparison of the PWQ compensation with the current state-of-the-art, we provide some of the Figures of Merits (FoM) corresponding to the PWQ together with those of some of the most recent techniques proposed recently for eliminating subharmonic oscillation in dc-dc converters.

The most relevant FoM are summarized in Table III. Other FoM of the converter such as efficiency, current rating, temperature rating, voltage regulation, complexity of implemen-



(a) $D = 0.6 \rightarrow V_o = 12.5$ V.



(b) $D = 0.75 \rightarrow V_o = 20$ V.

Fig. 12. Experimental response of the system under the PWQ slope compensation strategy for different values of the operating duty cycle.

TABLE III
COMPARISON BETWEEN THE CONVENTIONAL, THE PWQ TECHNIQUE IN THIS WORK AND THE RECENTLY PROPOSED TECHNIQUES FOR SUPPRESSING SUBHARMONIC OSCILLATION IN SWITCHING CONVERTERS.

Contribution	**Stabilizing technique**	**Analog implementation**	**Synchronization problems**	**Need for parameter tuning for guaranteeing current loop stability**
[21], [22]	TDFC	No	No	Yes, the feedback gain and the time delay must be appropriately tuned otherwise the current loop may be unstable for some duty cycle values and loading conditions.
[23], [24]	Fiter-based control	Yes	No	Yes, the feedback gain and the cut-off frequency of the filter must be appropriately tuned otherwise the current loop may be unstable for some duty cycle values and loading conditions.
[18], [19]	RPP	Yes	Yes	Yes, the amplitude of the sinusoidal signal must be tuned appropriately otherwise the current loop may be unstable for some duty cycle values and loading conditions.
[18]	Phase shifted RPP	Yes	No	Yes, the phase shift of the sinusoidal signal must be appropriately tuned otherwise the current loop may be unstable for some duty cycle values and loading conditions.
[17]	DPR	Yes	No	Yes, the feedback gain must be appropriately tuned otherwise the current loop will may be unstable for some duty cycle values and loading conditions.
[8], [16]	ZPDC	Yes	No	Yes, the feedback gain must be appropriately tuned otherwise the current loop may be unstable for some duty cycle values and loading conditions.
[8], [16]	HDC	Yes	No	Yes, the feedback gain must be appropriately tuned otherwise the current loop may be unstable for some duty cycle values and loading conditions.
This work	PWQ	Yes	No	No, the current loop is stable under all loading conditions and for all duty cycle values.

tation, accuracy, reliability and external voltage loop transient response are not altered by the PWQ compensation strategy.

VII. CONCLUSIONS

This paper presented a piecewise quadratic slope compensation technique for eliminating subharmonic and chaotic oscillations in dc-dc switching converters under CMC. The amplitude of the modulating signal is self-adapted in terms of the inductance such that any drift due to aging or nonlinearity of the inductance is automatically taken into account. Therefore, the operation of the converter under the PWQ compensation scheme could allow a significant reduction of the size of the inductor which could result in an improvement of the power density. Moreover, since the stabilizing signal is generated from its own state variables, frequency mismatch and phase shift problems, arising in practical situations when an external signal is injected for stabilization, are naturally avoided with the PWQ technique. The theoretical analysis shows that the technique can stabilize the system for all values of the duty cycles. Compared with the conventional slope compensation, the strategy does not require an external signal generation and extracts a compensation signal directly from the error between the inductor current and its reference. The PWQ strategy has the same stabilizing effect as the conventional slope compensation technique with ramp slope guaranteeing stability for all duty cycle values but with the

PWQ compensation technique this is achieved without the need for knowledge of the inductance value and sensing the input and output voltages. Future works will deal with the effect of the external voltage loop as well as that of the limited bandwidth of current sensor on the results presented in this study. The extension of the technique to other control methods, such as average current mode control and voltage mode control, could also be a topic of a further study.

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