



HIGH VOLTAGE EFFICIENT LIGHTING BASED ON THE LOSS-FREE RESISTOR CONCEPT.

Antonio León Masich

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Antonio León-Masich

High Voltage Efficient Lighting based on the Loss-Free Resistor Concept

Doctoral Thesis

Departament d'Enginyeria Electrònica, Elèctrica i Automàtica



UNIVERSITAT ROVIRA I VIRGILI

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I STATE that the present study, entitled "High Voltage Efficient Lighting based on the Loss-Free Resistor Concept", presented by Antonio León-Masich for the award of the degree of Doctor, has been carried out under my supervision at the Department of Electrics, Electronics, and Automatic Engineering of this university.

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*Perquè només van ser necessaris set anys per mostrar-me
tot allò que es necessita al llarg d'una vida sencera.*

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List of abbreviations

AR	Acoustic resonances.
ADC	Analogue to digital converter
SiC	Silicon carbide.
Si	Silicon.
C	Converter output capacitor
CRI	Colour rendering index
CCM	Continuous conduction mode.
C_{DS}	Drain to source parasitic capacitance
C_{GS}	Gate to source MOSFET/JFET parasitic capacitance
C_{iss}	MOSFET/JFET input capacitance
C_j	Diode junction capacitance
D	Converter duty-cycle
DCM	Discontinuous conduction mode.
D_1	Converter diode
E_{off}	Energy losses in the JFET “off” transient
E_{on}	Energy losses in the JFET “on” transient
f_{sw}	Boost converter switching frequency
FL	Fluorescent lamp.
$FPGA$	Field programmable gate array
g_{fs}	MOSFET/JFET transconductance
$HFSW$	High-frequency sinusoidal waveform.
HID	High-intensity discharge.
$IEFL$	Induction electrodeless fluorescent lamps.
i_D	Diode instantaneous current
I_D	Diode average current
i_{DS}	Drain to source MOSFET/JFET instantaneous current
I_{DS}	Drain to source MOSFET/JFET average current
i_L	Instantaneous inductor current
I_L	Average inductor current
i_M	MOSFET/JFET instantaneous current
$I_{M(rms)}$	MOSFET/JFET root mean square current
i_o	Converter instantaneous output current
I_o	Converter average output current
I_{ref}	Control reference current
L	Converter inductance
LED	Light-emitting diode.
LFR	Loss-free resistor.
$LFSW$	Low-frequency square waveform.
PWM	Pulse-width modulation.
r_C	Capacitor series resistance
$R_{ds(on)}$	MOSFET/JFET on resistance
r_L	Inductor series resistance

R_O	Load resistance
R_{SENSE}	Input current sensor resistance
S_I	Converter main switch
t_{off}	MOSFET “off” switching transient duration
t_{on}	MOSFET “on” switching transient duration
V_{DS}	Drain to source MOSFET/JFET average voltage
v_F	Diode instantaneous forward voltage
V_F	Diode average forward voltage
V_{GG}	Average differential voltage applied to the MOSFET/JFET gate
v_o	Converter instantaneous output voltage
V_o	Converter average output voltage
V_S	Converter input voltage

Abstract

In this thesis, the notion of loss-free resistor (LFR) is used systematically to design power supplies for efficient lighting, namely light emitting diodes (LEDs), high intensity-discharge lamps (HID) and induction electrode-less fluorescent lamps (IEFLs) with the aim of reducing the electrical energy consumption in domestic or industrial applications.

The different lamps previously mentioned are supplied at constant power independently of the lamp type and impedance, taking advantage of the LFR nature, i.e. an emulated resistance in the input port and a power source in the output port.

The sliding -mode control technique is applied in the boost converter to impose the LFR behaviour in continuous conduction mode (CCM) in some cases, and in the boundary between CCM and discontinuous conduction mode (DCM) in other cases. This control technique has been implemented throughout the thesis by either analogue or digital controllers and allows regulating the light emitted by the lamps.

LFR behaviour is indirectly achieved in the case of LEDs lighting, in which a high voltage is obtained from both a low DC voltage (12 V) and the electrical grid. With only one boost converter and a 12 V battery, voltage gains around 100 are attained resulting in an output voltage of 1.2 kV. In the case of grid supply, two operation modes are realized, i.e. the normal mode like in battery supply and the burst mode, which intends to improve the efficiency without introducing changes in the converter and control.

Regarding the HID lamps a double-stage converter is presented in order to supply this type of lamps by a DC voltage. The first stage is a boost converter with LFR behaviour, and the second one a switched-capacitor boost converter. When the lamp is off, the two converters are operating in cascade sharing the same control signal and achieving voltages around 6 kV from a 12 V battery. Once the lamp is on, only the boost converter with LFR is working, delivering always the selected power to the HID in the warm-up and in steady-state operation irrespective of the lamp impedance. As a consequence, both output voltage and current values are automatically adjusted by the lamp impedance level.

Supplying HID lamps from a high-frequency AC voltage is also investigated by studying a boost converter with LFR behaviour in cascade with a full bridge *LCC* resonant inverter. In this case, the control technique is realized in the boost converter by means of a FPGA-based digital controller. The full bridge resonant inverter is used to generate the necessary gain to provoke the lamp start-up. Subsequently, the inverter operates at high frequency avoiding acoustic resonances (AR).

Finally, a boost converter with LFR behaviour in cascade with a full bridge *LCC* inverter is presented in order to supply an IEFL lamp by means of a high-frequency AC voltage. As in the previous cases, the converter supplies the lamp at constant power irrespective of the lamp

impedance. In this case, due to the IEFL operation, the full bridge resonant inverter is always working at high frequency.

All the converters presented in the thesis are first analysed, then simulated and finally tested experimentally showing the feasibility of LFR-based switching regulators in the field of efficient lighting.



1 Switched-Power Converters Used in Efficient Lighting

1.1 Why using of efficient lighting?

Nowadays, in addition to electricity generation by means of renewable energies, an important way to contribute to CO_2 reduction is an efficient transformation of electricity in other types of energy. This is the case of using efficient lighting sources, as light emitting diodes (LED), high intensity discharge lamps (HID) or induction electrode-less fluorescent lamps (IEFL), which are increasingly employed in domestic or industrial applications. Some of the additional advantages of using efficient lighting are low energy consumption, low maintenance cost and better light quality. Some of these features are shown in Table I, obtained from the main manufacturer datasheets (namely Venture Lighting, OSRAM, Phillips Lighting and SYLVANIA).



Fig 1. Illumination level in Europe illustrated by the European Space Agency (ESA).

In this context, the light regulation is the subject of many research papers, because the dimming operation in different kind of lamps can provide about 50% - 60% of energy saving [1, 2]. Nonetheless, these systems are expensive and normally require a more complex circuitry than the traditional systems without light regulation. However these drawbacks are compensated by the energy potential saving, and hence power electronics for efficient lighting is still an open subject wherein it is possible to find relevant contributions dealing with light regulation in LED systems [3], HID lamps [4], as well as fluorescent lamps (FL) [5, 6].



Table I. Types of lamps and corresponding features

Category	IEFL Lamp	Fluorescent	High Pressure Mercury Vapour	High Pressure Sodium Vapour	Metal Halide Lamp	LED
Light Efficiency (lm/W)	70-80	25-70	30-50	90-110	85	20-80
Effective Light Efficiency (PM/W) (lumens measurement for human pupil)	113-130	40-110	26-43	51-63	126	50-100
Color Rendering index (CRI)	>80	50-80	30-40	<40	65	70-80
Power Factor	0.98	0.38-0.95	0.44-0.67	0.44	0.4-0.6	1
Cold Start Time	Instantaneous	<3"	4-10'	4-10'	4-10'	Instantaneous
Restart Time	Instantaneous	<1"	10-15'	10-15'	10-15'	Instantaneous
Stroboscopic Effect	NO	Sometime	Sometime	Sometime	Sometime	NO
Lamp Life (hours)	100000	5000-10000	3500-6000	8000-14000	10000	50000-80000

The role of power converters for efficient light, as it is inferred from the main publications, consists in transferring the energy to the lamps as efficiently as possible with the highest power density and with light regulation capability. Also, they must be adaptable to the electrical characteristics of each kind of lamp.

The next subsections are focused on the description of the state of the art of the different drivers or electronic ballasts reported in the literature, dealing with light regulation in LED, HID, and IEFL lamps.

1.2 Electronic drivers used to supply Light Emitting Diodes (LEDs).

LEDs are an important actor in efficient lighting due to their high efficiency, high reliability, chromatic variety, and potential light regulation reducing the lamp consumption in different environments. For this reason, in recent years LED lighting has increasingly attracted researchers attention in different fields of applications, such as backlighting applications [7], street-lighting [8], automotive applications [3], and emergency lights [9] among other [10, 11].



Nonetheless, it is necessary to design and develop different power supplies taking into account the LED behaviour and taking advantage of all the LED characteristics.

The configuration of such power converters depends on the typical requirements of the application, but despite of specific specifications of each possible scenario, these are at least three main issues that have to be always addressed when dealing with LED drivers: circuit complexity, efficiency and cost.



Fig 2. Types of LED lighting in the market.

The main control techniques for LED light regulation are described in the following paragraphs by emphasizing the influence of LED characteristics in the design of the power supplies.

One of the main important aspects is that LEDs are fast lighting devices in comparison with incandescent lamps. This means that the light emitted by a LED is proportional to the current that flows through it. The main disadvantage of this is that the current ripple affects directly the light emitted by the LED. Therefore, special efforts have to be made in order to supply the LEDs with free current ripple.

In order to achieve light regulation in LED systems, two main techniques are proposed in the literature, the analogue dimming and the Pulse-Width Modulation (PWM) technique, as depicted in Figs. 3 (a), and 3 (b) respectively.

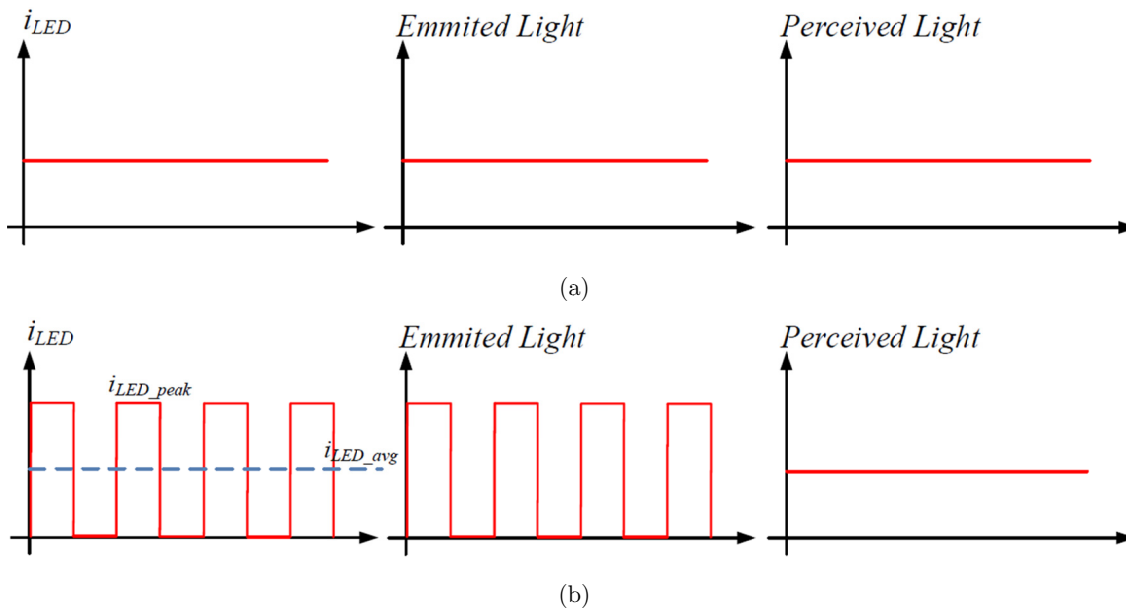


Fig 3. (a) Analogue dimming, (b) PWM dimming.

The first aforementioned dimming technique, namely the analogue method (Fig. 3(a)), is based on the DC current regulation that flows through the LED string with the aim of reaching the desired brightness level taking advantage of the existing linearity between the injected DC current in a LED and its luminosity. This technique is very simple and cost-effective but it can cause some colour variation during the LED life time. According to the circuit topology of the current regulator stage, it is possible to find two analogue dimming topologies, one based on linear regulators [12], and another one on switching regulators [13, 14].

The second dimming technique (Fig. 3 (b)), is based on switching the LED current “on” and “off” with relatively high frequency with a PWM- controlled current with a certain duty cycle and peak value, so the human eye integrates the light pulses perceiving continuous light. This PWM current control must switch at frequencies higher than 400Hz to avoid the flicker phenomena [15, 16]. As in the previous case, two dimming methods are found in the literature dealing with the PWM dimming ,i.e. systems employing linear regulators [17] , and systems using switching regulators [18-20].

1.3 Electronic ballasts to supply High-Intensity Discharge (HID) lamps.

Other important devices for efficient lighting are the high-intensity discharge (HID) lamps. Due to its high lighting efficiency (more than 100 lm/W), long lifetime, and high luminous efficacy [21], this kind of lamps is widely used in commercial lighting systems, stadiums, and street lighting among others [22].



Fig 4. Diverse types of HID lamps available in the market.

In the past, electromagnetic ballasts were used to supply HID lamps but they present some drawbacks in many applications where the size and weight of the power supply is an important factor to consider. The main disadvantages are large size, heavy weight, poor power regulation, sensitivity to line voltage sags, low efficiency, audible noise, flicker and stroboscopic effect [23].

Thus, nowadays several studies discuss the design of electronic ballasts to supply HID lamps with the highest efficiency and power density. The proposed ballasts should be capable to develop diverse functions such as generating the necessary ignition voltage to start the lamp, performing the warm-up from zero power to full power, and achieving a safe and stable operation at the desired power level. Besides, they should improve the attributes of the electromagnetic ballasts by competing in terms of cost and volume and exhibiting high power factors, efficiencies, and good power regulation [4, 24-26]. All the lamp characteristics, as ignition voltages, warm-up and steady-state operations are depending on the gas composition, arc tube length, and other constructive elements. [27, 28]

Some works dealing with the ignition transients in the HID lamps show that the value of the ignition voltage depends on the physical characteristics of each lamp. This means that this value is specific of each lamp. Typical ignition voltages of an HID lamp are greater than 3.5 kV. Diverse solutions reported in the literature to obtain these high voltages employ external ignition circuits [29-31], or resonant converter stages for resonant ignition [32], integrate new stages in the electronic ballasts [33] or include a controlled ramp of the applied voltage during the ignition to reduce the voltage peak [26, 34-36].

Moreover, these ballasts have to be designed considering the HID dynamic response. These lamps present a negative incremental impedance and during the warm-up its static



impedance varies in a wide range ($10 - 150 \Omega$) [26]. In this context, some papers present equivalent circuits to obtain simulations of the lamp behaviour during the warm-up operation [37, 38].

Besides, some reports discuss some physic phenomena that are associated with the lamp functionality in steady-state and warm-up operation [33, 39]. The most representative is the so-called Acoustic Resonance (AR), which is produced by the pressure waves within the arc tube. This phenomenon occurs for a certain range of frequencies (from 1 kHz up to 100 kHz) [23, 39], that depend on the size of the arc tube, gas pressure and composition, and that may change with the lamp aging. Therefore, operating the lamp at these frequencies can produce unstable operation causing visible flicker, and in some cases damage the lamp among other effects [40-42].

Nevertheless, it is possible to find in the literature three main solutions to supply HID lamps by means of electronic ballasts in steady-state operation mitigating the AR effects. The first-one is the simplest solution and consists in driving the lamp with a DC current. However, this results in a degradation of the electrode material because the lamp current is always flowing in the same sense and the resulting electric field may shorten the lamp life. The second-one is based on supplying the lamp with a low frequency current/voltage square waveform (LFSW) (below 1 kHz) [25, 26, 34, 41]. The LFSW approach has been proven to be robust against the uncertainty of AR models as far as the harmonics of the lamp power are maintained below 5% of the fundamental [43]. Finally, the last technique is the High Frequency Sinusoidal Waveform (HFSW) that consists in supplying the lamp far away from AR bands (above 100 kHz) by means of a resonant topology. This high-frequency approach is highly dependent on the lamp type and operating point and is not robust against lamp and aging variations in comparison with the LFSW approach. In addition, it has been demonstrated that a stable HID operation is necessary to supply these lamps by means of current or power control [38, 44].

To conclude, designing these electronic ballasts is an interesting challenge in the field of power electronics in order to guarantee a stable operation during start-up, warm-up and steady-state together with an easy and efficient light regulation.

1.4 Electronic ballasts for supplying Induction Electrode-less Fluorescent Lamps (IEFL).

Although the IEFL operation principle goes back in time to 1891 when Nikola Tesla demonstrated a “wireless” illumination in a lecture given at Columbia in New York [45], and the first patent of lighting source was registered in 1907 by Hewitt [46], nowadays IEFL continues to be the most innovative lighting source in comparison with LED and HID lamps.

The most attractive feature in IEFL lamps is the absence of electrodes. For this reason this kind of lamps will play an important role in a near future efficient lighting because they ensure a longer lifetime up to 100000 hours approximately with both low lumen depreciation and low maintenance cost [47, 48]. They exhibit in addition other lamp properties such as a



luminance efficiency higher than 110 lm/W, higher colour rendering index (CRI), wide range of colour temperatures, harmless start, instantaneous re-start and easy dimming [49, 50].

There are two types of IEFLs as illustrated in Fig. 5, namely, the external- inductor lamp (Fig. 5 (a)) and the internal inductor lamp (Fig. 5(b)), each one working at different frequencies but employing the same operation principle [51]. The magnetic coils enclosed to the discharge tube act as a transformer, in which the secondary winding is immerse in the plasma inside the lamp. An energy transfer exists from the coils provoking an electrical discharge and generating a luminous radiation.

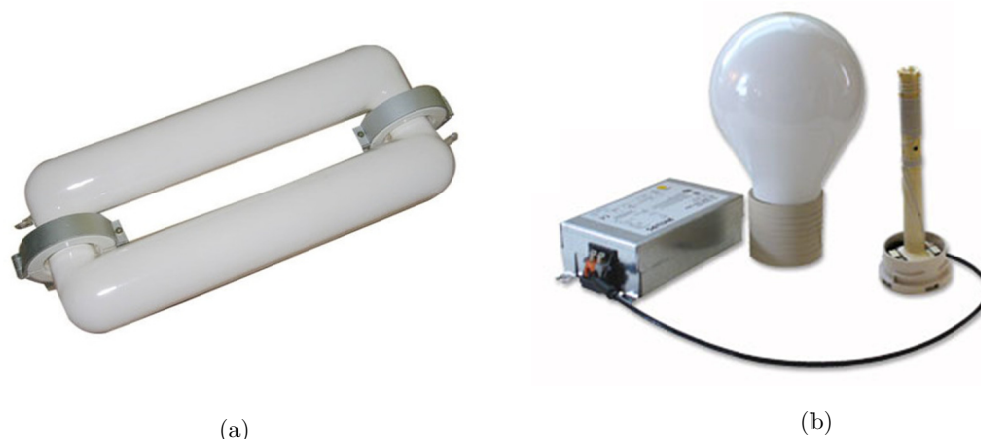


Fig 5. IEFL lamps. (a) External-inductor lamp. (b) Internal-inductor lamp.

Some papers have undertaken the study of electronic ballasts for external -inductor electrode-less fluorescent lamps (Fig. 5(a)) showing that they also have a negative incremental impedance characteristic [52]. Moreover, as indicated by the manufacturer, these lamps are designed for an HFSW operation at 250 kHz [53] and for this reason it is possible to find in the literature some papers presenting electronic ballast with several stages. In this type of power supplies, the first stage is used to obtain a power factor correction (PFC), if the ballast is supplied from the grid, while another stage is employed to control indirectly the lamp power by means of adjusting the voltage/current delivered to the third stage. Finally, an open loop resonant inverter stage provides the HFSW operation at 250 kHz to the lamp [54].

As previously mentioned, these lamps are convenient for dimming so that different techniques to provide this feature have been reported, e.g. the work of J. Tae-Kun et alt. [55] presenting a comparison between two dimming control methods. These methods are based on variable switching frequency control and variable dc-link voltage or current control method respectively , wherein either input voltage or current of the resonant stage is controlled. Later, J. Fraytag et alt. presented several converter topologies dedicated to regulate IEFL light [54, 56-58] with the aim to perform a comparative analysis for all the used converters. In all these cases the dimming control is carried out by adjusting the dc-link voltage.

Note that in all the previous publications is mandatory to know all the IEFL electrical characteristics for different power ratings [59], in order to control accurately the dc-link voltage or current delivered to the resonant stage for a good light regulation.



In this thesis, a new light regulation method is presented to supply IEFL lamps, in which the lamp power can be easily adjusted without controlling the input current or voltage of the resonant inverter stage. Therefore, the ballast here proposed will always deliver the desired power to the IEFL independently of the load characteristics, i.e. regardless of the IEFL impedance.

1.5 Motivation and goal of the thesis.

The common characteristic in all the previous works is the need to understand exactly the behaviour of the different lamps, i.e., the electrical characteristics of each one at different power levels with the aim to control accurately the supplied voltage or current required by the device. A general approach leading to a flexible ballast with common elements for the three classes of lamps would be desirable.

The main hypothesis of this work is that power supplies for efficient lighting employing LEDs, HIDs or IEFLs, can have in common a converter stage supplying a constant power irrespective of the connected stage at its output. This idea is closely related to the work presented by S. Singer et al. in references [60, 61], where a two-port power-conservative network capable to supply a constant power regardless of the connected output impedance was proposed. In this type of systems, the output voltage and current values are the coordinates of an equilibrium point determined by the output impedance and the power handled by the circuit. The two-port was called loss-free resistor (LFR), and was proposed as a possible solution to implement a non-dissipative electronic ballast supplying diverse gas discharge lamps [62].

Therefore, this thesis explores the use of different circuits with LFR characteristics in the construction of power supplies for efficient lighting employing LEDs, HIDs or IEFL lamps.

1.5.1 Loss-Free Resistor (LFR) approach applied to the efficient lighting.

The Loss Free Resistive (LFR) principles were presented by S.Singer [60, 63] from the notion of a time -variable transformer (TVT) [64] controlled by a signal processing circuit [65].

The LFR is an ideal two- port power processing element of *POPI* type [66] , i.e. input and output powers are equal , which can be modelled [67] by means of an emulated resistance R_e at the input port and a power source at the output port as shown Fig. 6 (a). The power source was defined as an element that delivers power to the output, irrespective of the load features. The total power provided in the output is equal to the total power absorbed by the resistive input port. The equilibrium point in Fig. 6 (b) is the intersection of a power constant curve (hyperbola) and a straight line defining the load resistance.

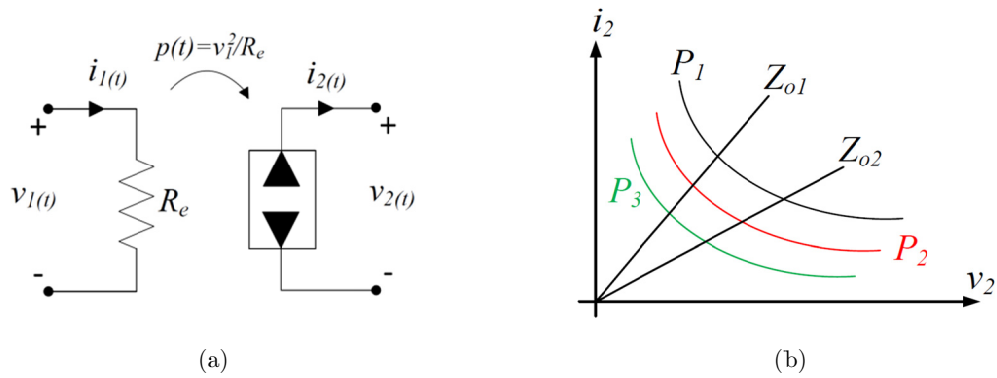


Fig 6. (a)Two port model of the LFR. (b) Power source characteristics.

The notion of LFR was originally limited to the recognition that certain switching converters exhibit input resistive impedance in steady-state when operating in discontinuous conduction mode (DCM) under pulse width modulation techniques [62], this being the case of buck-boost SEPIC, and Ćuk converters. Diverse applications using these circuits can be found in the literature in high quality rectification [68], and power interface in DC impedance matching in photovoltaic systems [69].

Nevertheless, buck-boost, SEPIC, and Ćuk converters in PWM-DCM are not the only way to implement a LFR. A well know method for the realization of the LFR is the induction of certain sliding motions in the appropriate converters [70-72]. As an example, a LFR can also be implemented by imposing a sliding mode control with a control surface given by $s(x) = V_S - R_e \cdot I_L$, as depicted in Fig. 7.

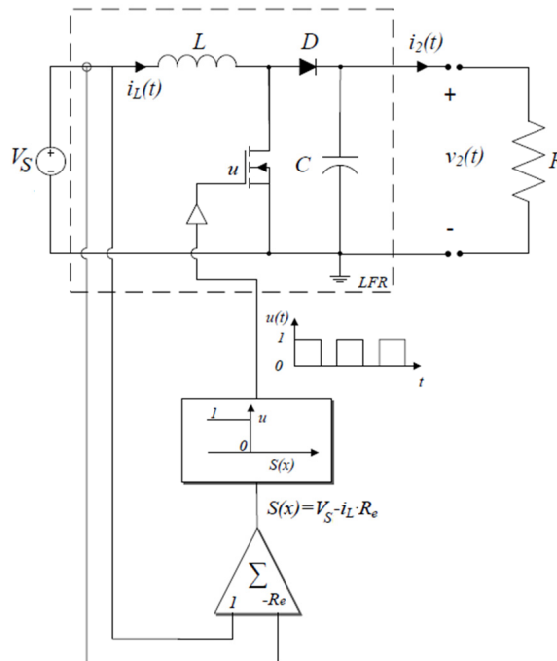


Fig 7. Boost converter with LFR behaviour controlled by means of sliding mode control.

This type of LFR synthesis is studied in this work, i.e. the employ of sliding mode control based-LFR as a common element for efficient lighting of LED, HID of IEFL lamps is closely



examined. It is expected that the processed power can be easily controlled by adjusting the value of the emulated input resistance R_e of the LFR.

1.5.2 Sliding-mode control in switched power converters.

The notion of discontinuous control goes back in time to 1920s in the Soviet Union, and was enriched later with theoretical generalizations and a great diversity of analysis and design methods for relay systems. Sliding-mode control is a particular case of discontinuous control, its main pioneers being S.V. Emelyanov [73], V.I. Utkin [74], and U. Itkis [75]. Its introduction in switching power converters was mainly due to H. Sira-Ramirez [76, 77].

The power converters are variable structure systems whose associated sliding-mode control theory is the natural way to regulate them. This is due to the fact that input signals for switching devices are continuous functions of the converter state and the resulting dynamic models are described by differential equations with discontinuous right-hand sides. In this context, sliding-modes can be induced with state trajectories over the surfaces in the system state that establish the discontinuity of the right hand sides of the differential equations [78]. Moreover, since the production of chattering is intrinsic to the nature of switching power converters, first-order sliding-mode controllers [79-81] are preferred to high-order sliding-mode controllers [82], which, in turn, are increasingly used in the regulation of electrical drives [83-85].

To summarize, power switching converters are controlled by a discontinuous signal u , assuming values of “0” or “1”, which correspond respectively to ON and OFF states of the converter. Hence, it is possible to consider a control law or switching logic as follows:

$$u = \begin{cases} 1 & s(x) > 0 \\ 0 & s(x) < 0 \end{cases} \quad (1)$$

where the function $s(x)$ is the previously mentioned surface.

Nevertheless, control law (1) cannot be physically implemented because this would imply an infinite switching frequency. A practical solution to carry out this switching logic with finite frequency is employing a hysteretic modulator [86].

When dealing with a hysteretic modulator in a feedback controlled system, there are three possible methods to tackle the analysis, i.e. describing function, Tsytkin’s method and sliding-mode control. The first two methods are performed in a frequency domain and exhibit complementary properties. While the describing function is an analytical approach giving enough insight on the influence of the different parameters in the system self-oscillation, its prediction of limit cycles is inaccurate. On the contrary, Tsytkin’s method is an accurate numerical procedure requiring some complex computations that cannot give sufficient information on the role of the different parameters in the system performance. In a clear-cut contrast, sliding-mode control is a time-domain analytical method that provides not only a good insight but also an accurate prediction of the dynamical behaviour of hysteresis-based feedback controlled systems such as self-oscillating power converters [87].



2 LFR-based ballasts for high-voltage low-power LED lighting.

This chapter presents a solution to supply high-voltage LED lamps based on a LFR stage synthesized by means of sliding- mode control.

Moreover, Silicon Carbide (SiC) devices are employed in a single stage boost converter capable to obtain high-voltages for LED lighting applications in order to maximize the efficiency.

Thus, this section is divided in three parts. Firstly, the analysis and design of a very-high gain single-stage boost converter operating at the boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is presented. The converter is supplied by a 12 V car-battery and attains 1200 V, i.e. it exhibits a voltage gain of 100. The use of a hysteretic comparator in the control loop precludes the risk of modulator saturation and facilitates the operation at the mentioned boundary. Sliding- mode control theory is applied to analyse the dynamic behaviour of the switching regulator and to establish the system stability conditions.

Secondly, an efficiency comparison is presented between the previous boost converter implemented with Silicon (Si) devices and the same converter made of two combinations of Silicon Carbide (SiC) devices and a mixture of Si and SiC elements. The comparison is performed on equal basis and discusses the influence on the converter efficiency of the semiconductor power devices and the passive components.

Finally, the same converter is redesigned in order to obtain an AC-DC grid supplied single-stage boost converter for LED applications. In this case, the converter can operate in normal mode, in which all the input current semi-cycles are employed, and in burst mode where only a fraction of all the input current semi-cycles is used in order to increase the efficiency without changing the converter parameters. In this case the power switch is realized with SiC devices to improve the performance of low-power LED-based lighting systems supplied by the grid.

2.1 Sliding-mode control-based boost converter for high-voltage-low power applications.

Converters operating at high voltage are widely used in many industrial applications, as in HID lamps requiring several kV in their start-up [88], front edge stage circuits for renewable energy [89, 90], and telecommunication applications [91].

Voltage step-up converters can be isolated and non-isolated. The isolated converters, such as flyback, push-pull, forward, or tapped boost, can provide high output voltages at the expense of an efficiency degradation provoked by the losses associated with the leakage



inductance, which cause high voltage stress, large switching losses and serious electromagnetic interference (EMI) problems [92]. These converters often require active or passive snubbers for recycling or dissipate leakage energy [93]. Moreover, using a transformer, although contributes to the voltage gain, increases the cost, volume and losses.

There are many options to achieve a high-voltage gain with non-isolated topologies, most of them derived from a single-stage boost converter. It is worthy to remark that the boost converter by itself is a poor candidate for high-voltage-gain applications because many factors can degrade its efficiency limiting also the converter power rating [94] and precluding the employ of high duty ratios that can saturate the pulse-width modulator (PWM).

Among the non-isolated topologies, high voltage gain can be achieved by connecting several step-up converters in cascade [95]. The resulting topology can supply high output voltages with a relatively high efficiency and a progressive reduction of the duty-ratios. The main drawbacks are the stability [96], the complexity, and the high cost caused by interconnecting different DC-DC converters in cascade as well as the need of synchronization in all the power switches to avoid beat frequencies. Another alternative is the employ of quadratic or cubic converters that can be derived from the cascade circuits by using a single driven transistor [97] at the expense of incorporating several additional diodes. At the same time, the single active switch must be designed to block the whole output voltage in the off-state and the entire input current at the on state.

In order to avoid the extreme duty cycles of the converters without magnetic isolation, another option is using switched- capacitors converters [98], wherein it is possible to increase the gain by introducing several stages, thus reducing the duty cycle and the devices stress. However, the current flowing through the devices increases in the switches turn ON impairing the efficiency due to the conduction loss increment. In this kind of converters, increasing the output voltage requires several switching capacitor stages, which also increases the overall cost and the complexity of the converter and reduces its reliability.

An extension of Luo's converters was reported in [99] by integrating various switched inductor stages [100] thus avoiding high duty-cycles. However, the gain of the converter is not higher than that of quadratic or cubic converters, but the complexity of the circuit, its cost and volume increase.

Other possibilities are the converters with coupled inductors, where the switching devices have to block a smaller voltage, so that devices with lower on resistance can be used, and the problem of the reverse recovery peak in the diode can be neglected. However, the coupled inductor needs a snubber to eliminate the voltage peaks generated by the leakage inductance, and this fact tends to increase the losses, cost, and volume of the converter [101]. Some efficiency improvement of these topologies combining coupled inductors with switched capacitors is found in [102] where the efficiency increment is obtained by mixing the single stage boost converter with transformers at the expense of increasing the complexity of the converter and its control.



The goal of this subsection is to demonstrate that a high voltage gain can be achieved in a single boost stage without transformers, leading to a competitive converter in the field of LED-based lighting power supplies. The proposed converter requires duty cycles near unity, so that a PWM approach is disregarded because of the risk of saturation for duty cycles bigger than 0.7. Instead, a hysteresis modulator with a variable width is employed to regulate the converter, which operates at the boundary between CCM and DCM in order to minimize the power losses.

It is well-known that a turn-off operation of the bipolar diode at zero current minimizes the switching losses. This fact imposes DCM operation, which, in turn, implies current peaks much higher than those in CCM operation for the same value of the input average current. This trade-off is solved by operating in the boundary between both modes, so that the converter has both diode turn-off at zero current and the minimum peaks and RMS values of current of a DCM performance.

The highly nonlinear behaviour introduced by the hysteretic comparator is tackled by means of the sliding-mode control theory, which provides an averaged dynamic model of the converter in spite of the variable switching frequency produced by the comparator. The converter is controlled through the inductor current since the current dynamic behaviour with respect to the control variations is of minimum-phase type. A subsequent linearization of this model allows the design of an appropriate compensating network.

From the technological point of view, the extreme conditions of high voltage operation are counteracted by the use of SiC power devices, what eventually results in a good global efficiency. The design of a specific driver for a SiC normally off JFET used in the power switch implementation is also presented.

2.1.1 Converter description and operation.

The switching converter and its control loop are depicted in Fig.8, where parasitic resistances in the reactive components together with an ON resistance for the transistor, and a voltage source for the diode are included in order to study the influence of the conduction losses in the converter performance.

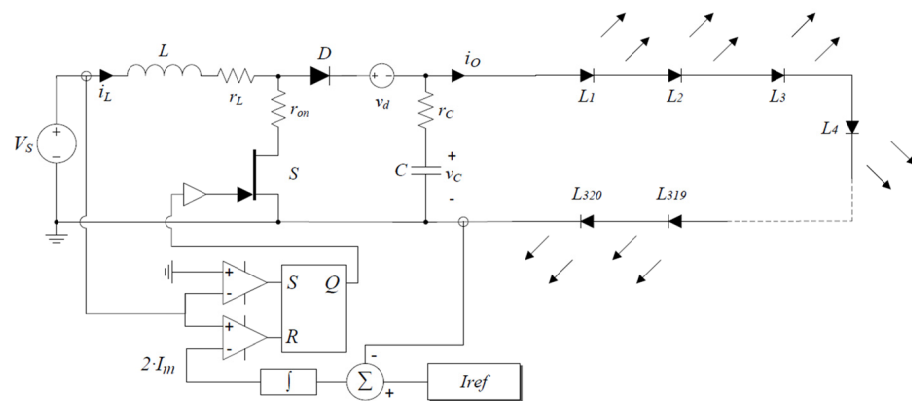


Fig 8. Boost regulator with parasitic elements for LED lighting



2.1.1.1 DCM-CCM boundary operation.

Switching losses can be minimized if the turn-OFF of the bipolar diode occurs at zero current, which imposes DCM operation. However, preserving in DCM the value of the CCM input average current to satisfy the load requirements requires current peaks much higher, this increasing the RMS value of the current in all devices, and therefore, the conduction losses of transistor and diode as illustrated in Fig. 9 and Table II. The deeper the DCM operation is, the higher the current stress is, and therefore the higher conduction losses are. Consequently, the DCM-CCM boundary appears as the working zone that combines the lowest conduction losses with minimum switching losses by keeping the diode turn-OFF at zero current.

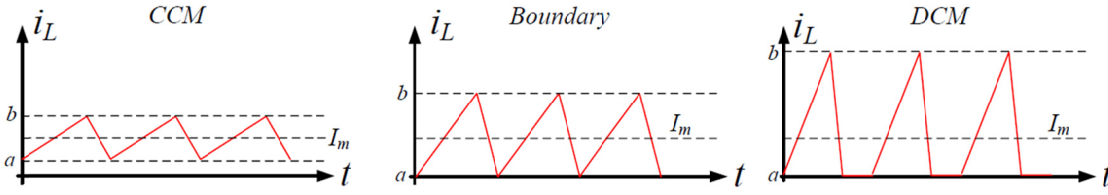


Fig 9. Inductor current at CCM, boundary, and DCM operation.

Table II. Inductor RMS currents in different conduction modes.

DCM	$\frac{2}{\sqrt{3 \cdot D}} I_m$
Boundary	$\frac{2}{\sqrt{3}} I_m$
CCM	$I_m < I_m^2 + \frac{(b-a)^2}{12} < \frac{2}{\sqrt{3}} I_m$

To calculate the averaged input current I_m , depicted in Fig. 9, the only data required is the switching period T_s , because for a high duty cycle D , such that $0.99 < D < 1$, at DCM-CCM boundary, we obtain

$$I_m \approx \frac{V_s}{2 \cdot L} \cdot D \cdot T_s \approx \frac{V_s}{2 \cdot L} \cdot T_s \quad (2)$$

$$I_m = \frac{P_o}{\eta \cdot V_s} \Rightarrow P_o = \frac{\eta \cdot V_s^2 \cdot T_s}{2 \cdot L} \quad (3)$$

where P_o is the output power and η is the converter efficiency.

Neglecting the efficiency η effect, the input current I_m , and the output power P_o are both proportional to the switching period T_s and can be controlled by adjusting the value of T_s . It can be observed that, for a constant value of the switching period, the converter behaves like a Loss Free Resistor (LFR) [60] because the input current I_m is also proportional to the supply voltage V_s .

2.1.1.2 High-gain analysis.

Disregarding the voltage drop of the diode v_d because this device is only conducting in a negligible OFF interval, the following DC gain is obtained.



$$\frac{V_o}{V_s} = \frac{R_o(1-D)}{R_o(1-D)^2 + \frac{D(1-D) R_o \cdot r_C}{R_o + r_C} + r_{ON_EFF} + r_L} \quad (4)$$

$$r_{ON_EFF} = r_{ON} + R_{SENSE1} \quad (5)$$

Fig. 10 shows the graphical representation of the DC gain as a function of the duty cycle taking values between 0.980 and 1, for different resistive output loads. The r_{ON} value of the power transistor (a JFET) has been obtained from the corresponding data sheet. It can be observed that the ideal gain $1/(1-D)$ constitutes the upper bound of the family of curves representing (4).

It can be observed in Fig.10 that the DC gain increases with the value of the resistive load and it can be deduced that the maximum gain corresponds to the maximum value of the duty cycle given by

$$d_{MAX} = \frac{R_o^2 + 2 \cdot R_o \cdot r_C - \sqrt{2} \cdot \sqrt{(R_o + 2 \cdot r_C) \cdot R_o \cdot \left(\left(\frac{1}{2} r_L + \frac{1}{2} r_{ON_EFF} + r_C \right) R_o + \frac{1}{2} r_C (r_L + r_{ON_EFF}) \right)}}{R_o \cdot (R_o + 2 \cdot r_C)} \quad (6)$$

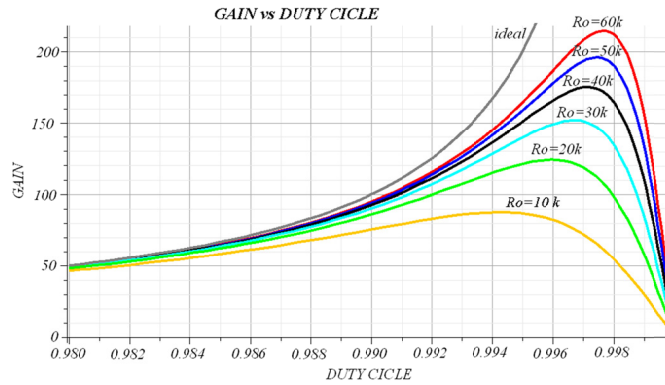


Fig 10. DC gain of the boost converter for different output loads.

From (4) and (6), it can be concluded that very high values of DC gain require extreme values of the duty cycle in the region $0.93 < D < 0.9925$. These values can be supplied by the hysteresis comparator without a risk of modulator saturation.

2.1.2 Sliding-mode control analysis.

In DCM-CCM border, the converter (Fig.11 (a)) has two structural changes within a switching period, i.e., ON state (Fig.11 (b)) and OFF state (Fig.11 (c)), and therefore it can be represented by means of two linear vector differential equations.

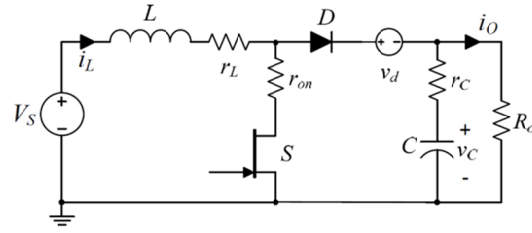
$$\dot{x}(t) = A_1 x(t) + B_1 \quad \text{for } u = 1 \quad (ON \text{ state}) \quad (7)$$

$$\dot{x}(t) = A_2 x(t) + B_2 \quad \text{for } u = 0 \quad (OFF \text{ state}) \quad (8)$$

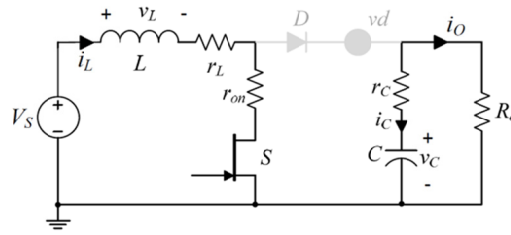
where $x(t)$ is the state vector corresponding to the state variables of the power stage.



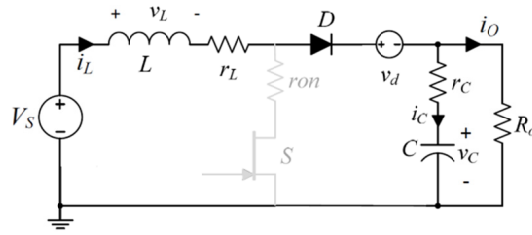
$$x(t) = [i_L, v_C]^T \quad (9)$$



a)



b)



c)

Fig 11. a) Boost converter with parasitic elements, b) ON state, c) OFF state

Matrices A_1 , A_2 , B_1 and B_2 are given respectively by

$$A_1 = \begin{bmatrix} \frac{-r_L - r_{ON}}{L} & 0 \\ 0 & -\frac{1}{(R_o + r_C)C} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{V_S}{L} \\ 0 \end{bmatrix} \quad (10)$$

$$A_2 = \begin{bmatrix} \frac{r_L}{L} - \frac{r_C \cdot R_o}{(R_o + r_C)L} & -\frac{1}{L} - \frac{r_C}{(R_o + r_C)L} \\ \frac{R_o}{(R_o + r_C)C} & -\frac{1}{(R_o + r_C)C} \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{V_S - v_D}{L} \\ 0 \end{bmatrix} \quad (11)$$

The control technique applied to the converter requires the use of a switching surface $s(x)$ to induce sliding motions in the converter by forcing the input current to track a slow varying signal $k(t)$.

$$s(x) = i_L - k(t) \quad (12)$$

where $k(t)$ is given by



$$k(t) = \frac{1}{2} \int_{-\infty}^t (I_{REF} - i_o(\lambda)) \cdot d\lambda = I_m(t) \quad (13)$$

and where, I_{REF} is the output current constant reference, $i_o(t)$ is the output current and $I_m(t)$ is the average input current, imposed by the hysteresis comparator.

Introducing the invariance conditions [78] $s(x)=0$ and $ds(x)/dt=0$ in (7)-(12) yields the equivalent control $u_{eq}(t)$, which is bounded by both maximum and minimum values of $u(t)$.

$$0 < u_{eq}(t) < 1 \quad (14)$$

Moreover, a switching law of the type

$$u(t) = 0 \quad \text{if} \quad s(x) > 0 \quad (15)$$

$$u(t) = 1 \quad \text{if} \quad s(x) < 0 \quad (16)$$

will induce a sliding regime on the switching surface ensuring the sliding-mode existence conditions because

$$s(x) \frac{ds(x)}{dt} < 0 \quad (17)$$

In order to find the equilibrium point of the resulting sliding dynamics, we will decompose $k(t)$ in two terms, namely, a positive constant K and a superposed time-varying component $\hat{k}(t)$. We will first assume a switching surface of the type $S(x)=i_L-K$, which will result in an equilibrium point X^* of constant coordinates. The influence of the term $\hat{k}(t)$ will be predicted next in a closed-loop model of the converter dynamics after linearization around X^* by assuming $\hat{k}(t) \ll K$.

The resulting equivalent control for $S(x)=i_L-K$, and the corresponding ideal sliding dynamics are given by expressions (18)-(20) respectively, as follows

$$u_{eq} = 1 - \frac{V_S - (r_{ON} + r_L) \cdot K}{-K \cdot r_{ON} + \frac{r_C \cdot R_o \cdot K}{R_o + r_C} + v_C \frac{R_o}{R_o + r_C} + v_D} \quad (18)$$

$$i_L = K \quad (19)$$

$$\frac{dv_C}{dt} = \frac{R_o}{C(R_o + r_C)} K \cdot (1 - u_{eq}) - \frac{v_C}{C(R_o + r_C)} \quad (20)$$

Therefore, the coordinates of the equilibrium point $X^*=[I_L^* \ V_C^*]$ are given by (21)-(22)

$$I_L^* = K \quad (21)$$

$$V_C^* = \frac{\sqrt{4 \cdot K \cdot ((-r_L - r_{ON}) \cdot K + V_S) R_o^3 + \left[(r_C^2 + (-6 \cdot r_{ON} - 4 \cdot r_L) r_C + r_{ON}^2) K^2 + ((2 \cdot v_D + 4 \cdot V_S) \cdot r_C - 2 \cdot v_D \cdot r_{ON}) \cdot K + v_D^2 \right] \cdot R_o^2}}{2 \cdot R_o} + \frac{\sqrt{-2 \cdot r_C \cdot (-v_C + K \cdot r_{ON}) - ((r_{ON} + r_C) \cdot K + v_D) \cdot R_o + r_C^2 \cdot (-v_D + K \cdot r_{ON})^2}}{2 \cdot R_o} + \frac{1}{2 \cdot R_o} \left[((r_{ON} - r_C) \cdot K - v_D) \cdot R_o - v_D \cdot r_C + K \cdot r_{ON} \cdot r_C \right] \quad (22)$$



Assuming now that $k(t)$ is time-varying, the corresponding equivalent control will be given by

$$u_{eq} = \frac{L \frac{dk(t)}{dt} - V_S + r_L \cdot k(t) + \frac{k(t) \cdot r_C \cdot R_o}{R_o + r_C} + v_C \frac{R_o}{R_o + r_C} + v_D}{-k(t) \cdot r_{ON} + \frac{r_C \cdot R_o \cdot k(t)}{R_o + r_C} + v_C \frac{R_o}{R_o + r_C} + v_D} \quad (23)$$

Therefore, the ideal sliding dynamics can be expressed as (24)-(25)

$$i_L(t) = k(t) \quad (24)$$

$$f(x) = \frac{dv_C}{dt} = \frac{R_o \cdot k(t) - v_C}{C(R_o + r_C)} - \frac{\left(\frac{-dk(t)}{dt} + \left(-\frac{r_L}{L} - \frac{r_C \cdot R_o}{(R_o + r_C)L} \right) k(t) + \left(-\frac{1}{L} + \frac{r_C}{(R_o + r_C)L} \right) v_C + \frac{V_S - v_D}{L} \right) R_o \cdot k(t)}{\left(\left(\frac{r_{ON}}{L} - \frac{r_C \cdot R_o}{(R_o + r_C)L} \right) k(t) - \left(\frac{1}{L} - \frac{r_C}{(R_o + r_C)L} \right) v_C - \frac{v_D}{L} \right) \cdot C \cdot (R_o + r_C)} \quad (25)$$

Linearizing equation (25) around the equilibrium point $X^* = [I_L^* \ V_C^*]$ leads to the following expression

$$\frac{d\hat{v}_C}{dt} = a \cdot \hat{k}(t) + b \cdot \hat{v}_C + c \cdot \frac{d\hat{k}(t)}{dt} + d \cdot \hat{v}_S \quad (26)$$

where coefficients a , b , c and d are given by expressions (27)-(30), respectively, for the case of no losses for the sake of simplicity.

$$a = \left. \frac{\partial f(x)}{\partial k} \right|_{x^*} = \frac{1}{C} \sqrt{\frac{V_S}{R_o \cdot K}} \quad (27)$$

$$b = \left. \frac{\partial f(x)}{\partial v_C} \right|_{x^*} = -\frac{2}{R_o \cdot C} \quad (28)$$

$$c = \left. \frac{\partial f(x)}{\partial y} \right|_{y = \frac{dK(t)}{dt}, x^*} = -\frac{L}{C} \sqrt{\frac{K}{R_o \cdot V_S}} \quad (29)$$

$$d = \left. \frac{\partial f(x)}{\partial V_S} \right|_{x^*} = -\frac{1}{C} \sqrt{\frac{K}{R_o \cdot V_S}} \quad (30)$$

Fig.12 illustrates the block diagram of the boost converter controlled through the switching surface $S(x)$. It can be observed that the ideal comparator required by the sliding – mode control theory has been implemented by a hysteretic comparator based on a flip-flop that activates the switch when the inductor current is zero, and turns OFF the MOSFET/JFET when the inductor current reaches $2 \cdot I_m$. This is equivalent to force the average input current to take the appropriate value I_m in order to fulfil the output requirements.

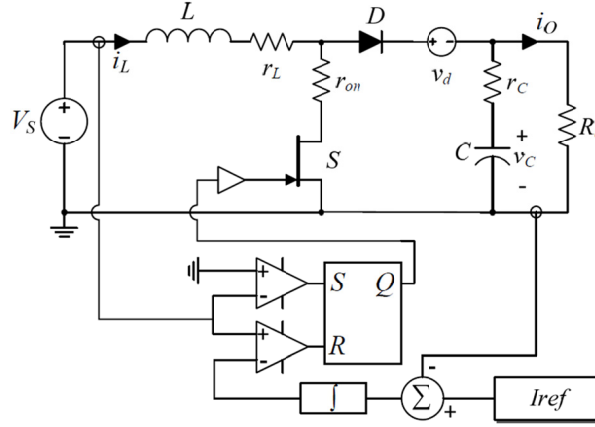


Fig 12. Boost converter with hysteretic control of the input current

Fig. 13 illustrates the closed-loop dynamic model of the switching regulator depicted in Fig.8 where the expression of $H(s)$ is derived from expression (26) by assuming $\hat{V}_S = 0$. Hence,

$$H(s) = \frac{\hat{V}_C(s)}{\hat{K}(s)} = \frac{a + c \cdot s}{s - b} \quad (31)$$

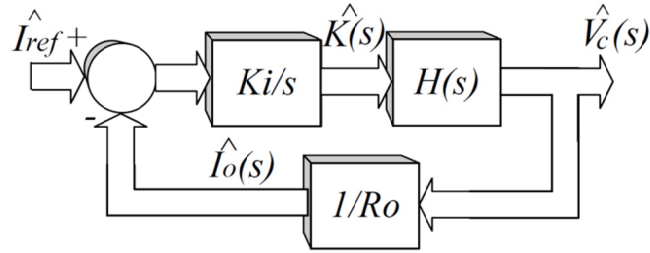


Fig 13. Dynamic model of the switching regulator depicted in Fig. 9.

The system loop gain can be expressed as

$$T(s) = H(s) \cdot \frac{1}{R_o} \cdot \frac{k_i}{s} = \frac{k_i \cdot c}{R_o} \cdot \frac{s + (a/c)}{s \cdot (s - b)} \quad (32)$$

and the characteristic equation of the system will be given by

$$s^2 + s \left(\frac{k_i \cdot c}{R_o} - b \right) + \frac{k_i \cdot a}{R_o} = 0 \quad (33)$$

that will correspond to a stable system provided that following condition is satisfied.

$$0 < k_i < \frac{2}{L} \sqrt{\frac{R_o \cdot V_S}{K}} \quad (34)$$

Therefore, k_i can be found using classical Bode techniques in (32) or by pole assignment in expression (33).



2.1.3 Single-stage boost converter implementation.

2.1.3.1 Power stage.

Figs. 14 and 15 illustrate the circuit scheme of power stage and sliding-mode controller respectively.

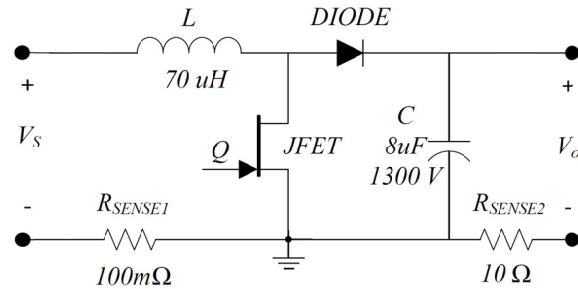


Fig 14. Power stage scheme.

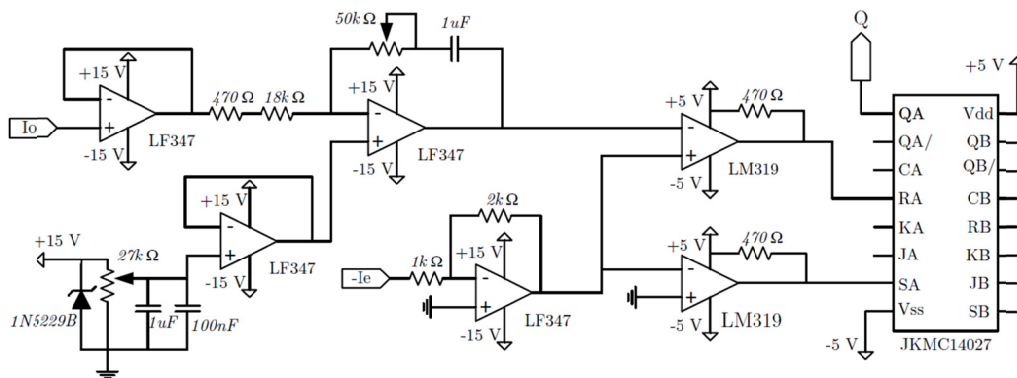


Fig 15. Control implementation schematic circuit.

With the aim of achieving a single stage boost converter with the highest efficiency, the converter has been implemented with SiC devices.

In our case, the power diode is a SiC Schottky non-commercial device that has been specifically fabricated for our application by the National Center for Research in Microelectronics under the series name ALS11. The power transistor is the normally OFF JFET SJEP12R063 that has required the design of a specific driver as it is described below in this section.

The input series inductor of 70 μ H has been realized with 11 wires of 0.07 mm² by making 37 turns around the Kool M μ 773244-A7 core, which has a relative permeability of 90. It has to be pointed out that the use of 11 wires instead of 1 intends to reduce the skin effect when the switching frequency of the converter increases beyond 40 kHz.

The output capacitor is of ceramic type with a capacity of 8 μ F and an equivalent series resistance (ESR) of 8 m Ω and a breaking voltage of 1.3 kV.



The input current sensor is made of an SMD resistance of 100 m Ω and 5 W while the output current sensor is an E24 resistor of 10 Ω and 0.25 W. Signals $-I_e$ and I_{out} are proportional to inductor current i_L and output current i_o respectively.

2.1.3.2 Control stage.

Fig. 15 shows the two main blocks of the sliding-mode controller, namely, integrator of the output current error and hysteretic comparator. The integrator has been implemented with a circuit based on LF347 operational amplifier while the hysteretic circuit employs two LM319 comparators with a response time of 80 ns, and a JKMC14027 flip flop with a bandwidth of 13 MHz. The inputs of the hysteretic comparator are $k(t)$ and I_e , which are respectively given by the output of the integrator and the output of an inverting amplifier based on LF347. The output of the hysteretic comparator is a digital signal Q which activates the driver to turn on or turn off the power transistor. The transistor turn on corresponds to the high level of Q , which is the result of a zero input current while the turn off is produced by the low level of Q , which is obtained when $k(t)$ is bigger than $2 \cdot I_m$.

2.1.3.3 Driver implementation.

The driving circuit of the normally-OFF JFET has to provide a negative voltage to turn-OFF the JFET and a positive voltage to turning it ON.

Although normally-ON JFET SiC devices and drivers are quite common, normally-OFF JFETs and MOSFETs are less available. The ON-JFET, is a majority carrier device that typically has normally ON characteristics requiring a negative bias applied to the gate pinch off channel, the pinch off voltage level being determined by the design of the channel [103]. The OFF-JFET has complementary characteristics, which implies that different drivers for each type of SiC JFET are needed. In Fig.16 the basic circuit differences between normally-OFF and normally-ON JFET drivers are shown.

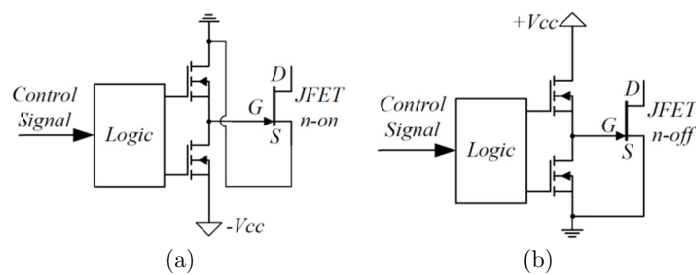


Fig 16. Typically JFET driver. (a) n-on (b) n-off.

The resulting driver prototype employed in our case for the SJEP12R063 normally OFF JFET is depicted in Fig. 17. The driver is composed by a simple push-pull output driver, a series gate resistance R_S and a parallel connection of a capacitor C , diode D_1 and resistance R_P , and a diode D_2 . The output of the parallel combination is directly connected to the JFET. The resulting driver prototype is illustrated in Fig.18. It has to be pointed out that signal Q in Fig.14 is the output of the hysteretic comparator previously described. It can be observed that



the driver is realized by two bipolar transistors, a npn transistor (ZTX 653) with an V_{br} of 100 V and a collector current of 2 A, and a pnp transistor (ZTX 753) with an V_{br} of 100 V and a collector current of -2 A.

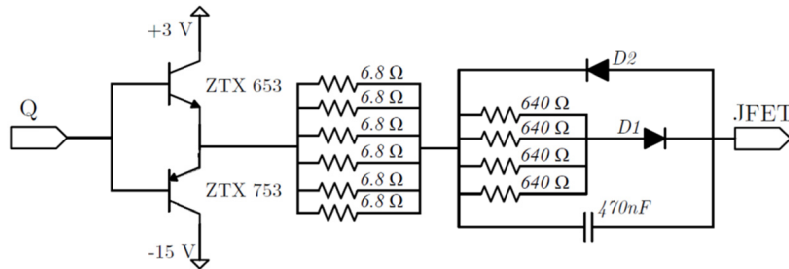


Fig 17. Implementation of the driver prototype circuit.

The R_S resistor has been realized by means 6 E24 resistors of $6.8\ \Omega$ in parallel while the R_P resistor has been implemented by 4 E24 resistors of $640\ \Omega$. Diodes D_1 and D_2 are of schottky type (SD103-A) of 40 V and 15 A. Finally, capacitor C has been implemented by a ceramic capacitor of 470 nF 16 V.

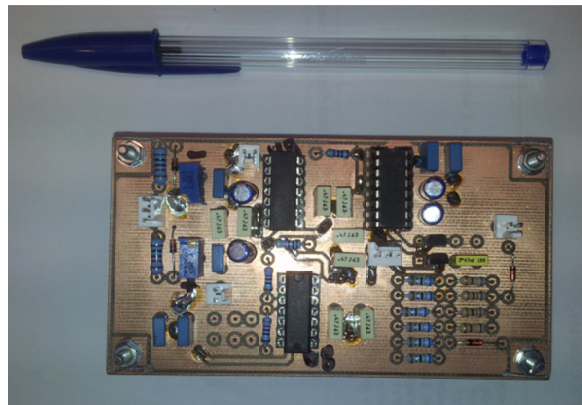


Fig 18. Driver prototype.

2.1.4 Experimental results.

Table III shows the characteristics of the semiconductor devices described in subsection 2.1.3.1 in terms of blocking voltage for both transistor and diode. As regards the power transistor, the values of on resistance, threshold voltage V_{th} , gate voltage V_g , gate charge Q_g and gate current I_g are also depicted. Information about forward current, on voltage drop, and total capacitance charge Q_C of the diode is also given. The experimental prototype has been supplied with three different voltages (9, 12, and 14 V) and for each input voltage different loads have been tested (10 k Ω , 20 k Ω , 30 k Ω , 40 k Ω , 50 k Ω , 60 k Ω). The measured parasitic resistances are r_L , namely, $140\ m\Omega < r_L < 155\ m\Omega$ for a range of switching frequency between 20 kHz and 40 kHz, and $r_C = 8\ m\Omega$. The control parameter k_i is 102.



Table III. Power switches used in the single stage boost converter.

ALS11	SiC	1.2kV	5 A	V _{on} 1.8-2.3V	Q _c 30nC		
SJEP120R063 Semisouth	SiC	1.2kV	63mΩ (30A)	V _{th} 1V	V _g -15 3V	Q _g 60nC	I _g 0.4A

2.1.4.1 SiC diode and SiC JFET.

The efficiency curves and the resulting switching frequency are depicted in Fig. 19. It can be observed that as the output voltage increases, the switching frequency decreases. In addition, it has to be pointed out that below 1000 V in the output voltage, the dominant losses are of switching type, the conduction losses being preponderant beyond the mentioned value. Therefore, the converter exhibits a higher efficiency for the lowest input voltage in all the output voltage range up to 1000 V.

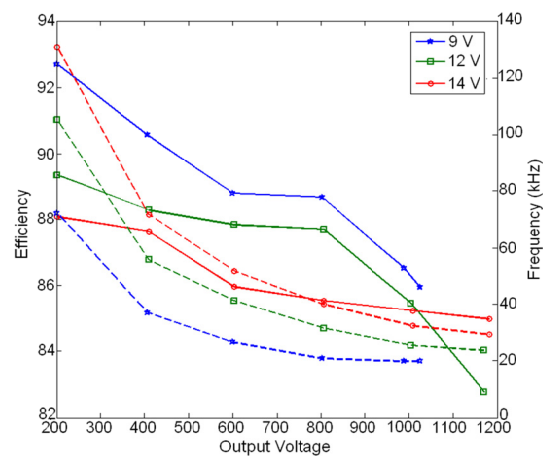


Fig 19. Efficiency (cont.line) and switching frequency (dis. ine).

As illustrated in Fig. 20, the output voltage reaches 1.2 kV DC (CH.3) from a 12 V DC (CH.1) input supply in the case of a resistive load of 60 kΩ. The input current (CH.2) exhibits a switching frequency of 23 kHz in the DCM-CCM boundary. The average value of the current flowing through the output load (CH.4) is 20mA approximately.

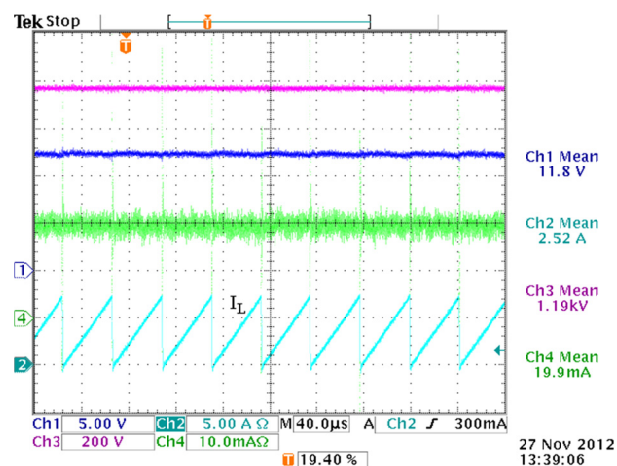


Fig 20. Converter waveforms for a resistive load of 60 kΩ.

The SiC-based converter has been also loaded with a LED spot consisting of 320 LEDs connected in series as it is illustrated in the picture shown in Fig. 21. The corresponding steady-state results are illustrated in Fig. 22, where it can be seen that the output voltage reaches 956 V (CH.3) for an input voltage of 12 V (CH.1). This voltage corresponds to the voltage drop produced by the circulation of an output current of 21.6 mA (CH.4) through the 320 LEDs.

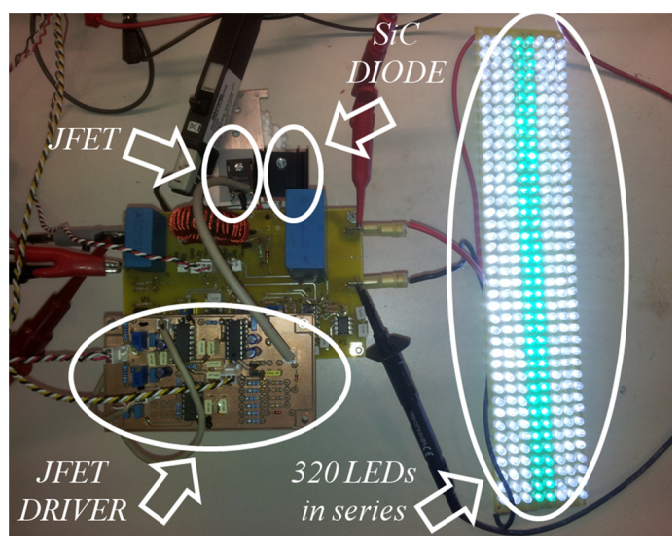


Fig 21. LED-based Spot light and boost converter with SiC devices.

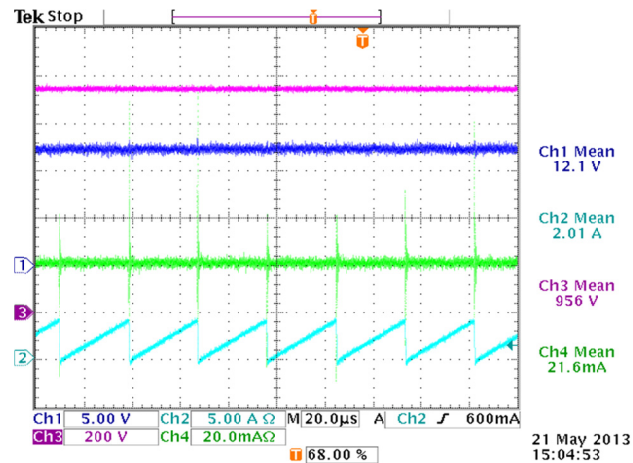


Fig 22. Converter waveforms for a 320 LEDs load.

2.1.4.2 Driver's results.

Figs. 23-25 corroborate the correct behaviour of the driver designed in subsection 2.1.3.3 by showing the turn-on and turn-off of the normally-OFF JFET. Fig. 23 shows the OFF-state of the JFET with a $I_{GS}=0$. Next, the JFET is first activated with a gate current peak of 600 mA, so that I_{GS} reaches its final value of approximately 10 mA after a short transient. Hence, according to the data-sheet, the estimated value of r_{ON} is 60 m Ω . The value of the current peak (600 mA) can be observed in detail in Fig. 24. Finally, the turn-OFF transient is illustrated in Fig. 25. It can be seen in the three figures that the gate voltage is 3.3 V in the ON-state and -15 V in the OFF-state.

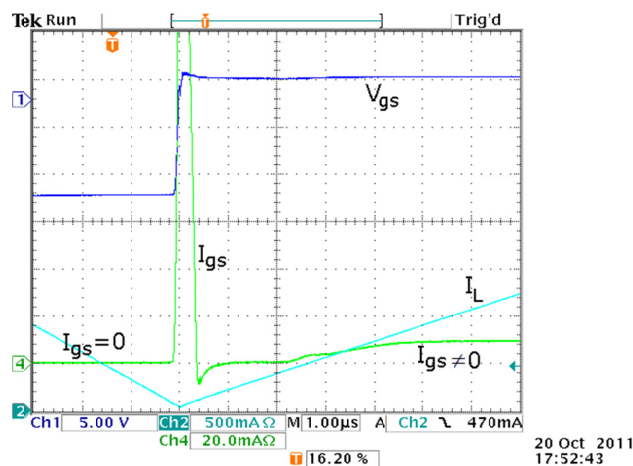


Fig 23. Start-Up transient of SiC JFET device.

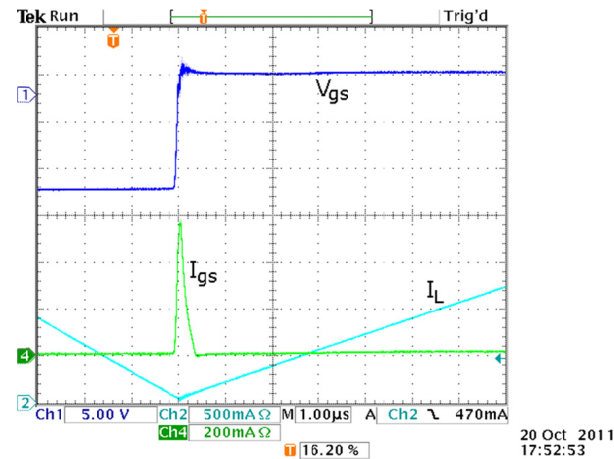


Fig 24. Peak current in start-up transient of SiC JFET.

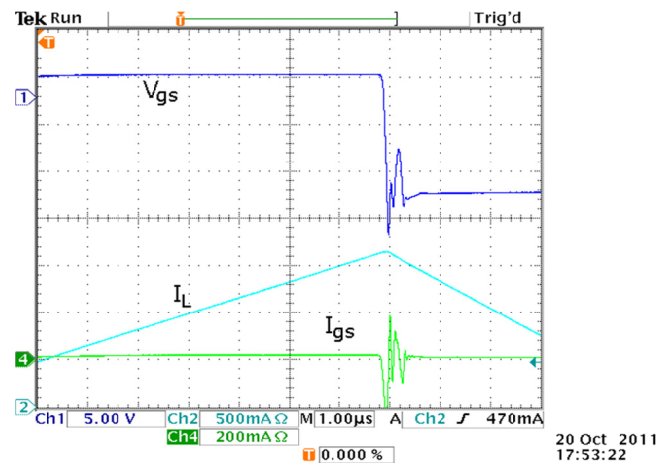


Fig 25. Turn-off transient of SiC JFET device.

2.1.5 Conclusion of the high-gain single stage boost converter.

The design of a very high voltage-gain single stage boost converter has been investigated. A voltage gain around 100 has been obtained with duty cycles near 1 without risk of saturation due to the use of a hysteretic modulator. The converter has been controlled through the inductor current whose reference is given by the integral of the output current error. The dynamic behaviour of the system has been studied by means of the sliding-mode control theory to establish the stability conditions.

The system operates at the boundary of CCM and DCM to make compatible a high output load and a high duty cycle operation with minimum losses. The experimental results are in good agreement with the theoretical predictions and show the expected variation of the switching frequency with the coordinates of the equilibrium point.

The performance of the converter supplying a LED-based spot light has been also studied and shows promising results for future lightning applications. The converter has been implemented by means of a normally-OFF JFET and a Schottky diode, which has been



specifically fabricated for the application. The use of SiC devices has allowed yielding 1200V with a DC gain of 100 and an efficiency of 83% operating at 24 kHz.

2.2 Efficiency comparison between Si and SiC-based implementations in a High-Gain DC-DC boost converter.

As previously mentioned this subsection presents an efficiency comparison between the boost converter presented in the subsection 2.1 implemented with Silicon (Si) devices and the same converter implemented in other three cases, i.e., employing two combinations of Silicon Carbide (SiC) devices and a mixture of Si and SiC elements. The experiments are carried out in the single stage boost converter prototype delivering a maximum output voltage of 1200 V when is supplied by a 12 V battery. The measurements show that the highest efficiency is obtained when the power transistor is implemented by a normally-off junction field-effect transistor (JFET) and the diode by a SiC Schottky device with a small parasitic capacitance.

The implementation with the highest efficiency has been selected for supplying a light spot of 320 LEDs in series, which results in an output voltage of 956 V and an output power of 20.6 W.

2.2.1 Use of SiC devices in power converters.

Silicon carbide (SiC) devices are increasingly replacing Silicon (Si) components in the design of power converters due to their attractive characteristics such as high electrical breakdown field, big thermal conductivity, large electron saturated drift velocity and great irradiation tolerance, which make them capable to work at higher voltages and frequencies with lower losses compared with their Si counterparts [104-108]. Different studies and experiments over the last years demonstrate the progressive penetration of SiC devices in switching converters and show that some of these components have already reached enough technological maturity to constitute their own market niche.

One of the most representative examples of this maturity is the junction field-effect transistor (JFET) , whose behaviour has been the subject of recent publications [109-113], some reports having disclosed specific gate drivers for JFETs [103, 114], and shown its utility in cascode rectifier structures [115, 116]. Other reports demonstrate that JFETs can work with higher power densities and higher switching frequencies and result in better efficiencies than the Si equivalent implementations [117]. This is the case of a boost converter tested at elevated temperatures [118], the development of multilevel converters [119], and the implementation of rectifier systems with power factor correction [120], isolated bidirectional DC-DC converters [121], dual active bridges [122], DC-DC converters for hybrid-electric-vehicle [123], quasi-resonant inverters for induction heating systems [124], and sparse matrix converters [125].

The previous implementations have been developed for high power converters, their applications ranging from several to hundreds of kilowatts. There are, nevertheless, some emerging applications like lighting supplies that do not involve high power but require high



voltage in their operation. This is the case of high-intensity discharge (HID) lamps needing high voltages to start-up [88, 126, 127], the supply of LED -based spot lights with the LEDs connected in series [128], or the converters for induction electrode-less fluorescent lamps (IEFL) powered at high frequencies [54].

2.2.2 Developed application and comparison efficiency.

Note that the application of our research is implementing a 25 W LED-spot with conventional LEDs and there are three possible solutions, namely, a) array of a series connection of LEDs b) array of parallel connection and c) array of series-parallel connection. Combination (b) requires balancing the currents circulating for each branch. The equalization can be performed by means of passive or active techniques. In the passive case, an important number of resistances have to be inserted, what results in an important decrease of the efficiency. In the active case, the equalization has to be performed by means of circuits emulating the behaviour of current sources, this implying complexity and efficiency decrease due to the additional power supply required by the current sources. Hence, it is expected that the series -parallel solution will present the same drawbacks than the parallel connection. As a conclusion, series connection seems the least complex in terms of equalization and inclusion of additional components. Besides, the risk of collapse inherent to all series connections, provoked by an element in open circuit, is mitigated in the prototype by connecting a Zener bypass diode for each 4 LEDs. In a clear-cut contrast with the permanent operation of the resistances in the case of passive equalization in the parallel connection, the bypass diodes are only in conduction state in an emergency situation.

From the technological point of view, our first goal is to demonstrate that the use of SiC devices can be beneficial in the low -power high voltage applications required by LED-based lighting systems. Different SiC-based implementations are studied and their performances compared among them and with a Si-based implementation in a boost converter supplying a series connection of LED devices as shown in Fig. 26, wherein the switching cell is defined as the combination of the power diode and the power transistor, which in turn is activated by the driver. The converter operates in the boundary between discontinuous and continuous conduction mode (DCM-CCM) , employs a hysteretic modulator to avoid the risk of saturation [129] with the associated sliding-mode control law previously discussed.

The different technological combinations of power devices are depicted in Fig. 27. Four cases are considered, namely, 1) Si MOSFET and Si bipolar diode, 2) SiC JFET and Si bipolar diode 3) SiC JFET and SiC Schottky diode (A) and 4) SiC JFET and SiC Schottky diode (B). Hence, a second objective of the technological study is to choose the switching cell yielding the highest efficiency in this high -voltage low power application.

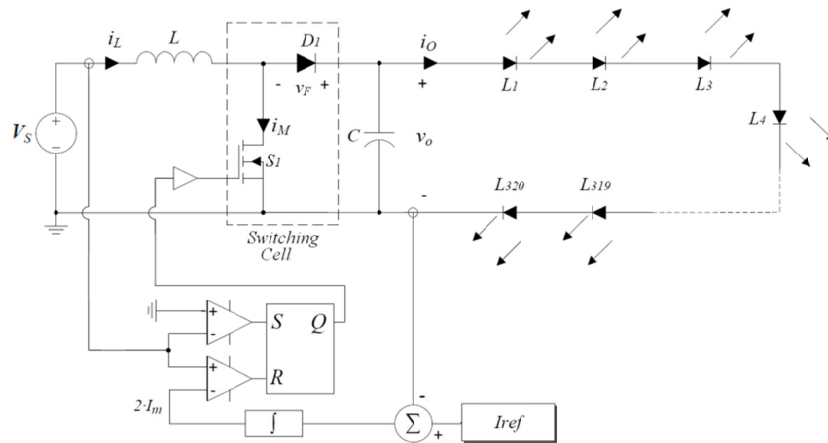


Fig 26. Boost converter supplying a series connection of LEDs.

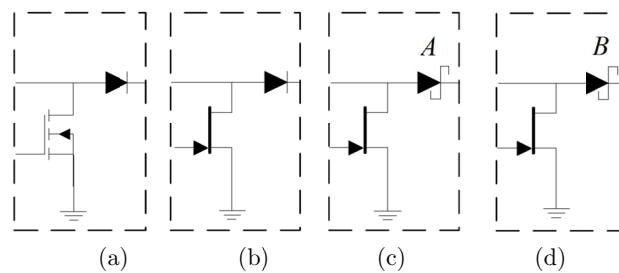


Fig 27. Tested switching cells. A) Si MOSFET/Si diode. B) SiC JFET/Si diode. c) SiC JFET/SiC Schottky (A), d) JFET/ SiC Schottky (B).

2.2.3 Experimental set-up.

The aim of the comparison is to find the main cause of losses in the converter and to determine which device limits the voltage gain. Without loss of generalization, the output load in the test is of resistive type absorbing the same level of current than an equivalent load made of series connected LEDs. With this goal, the set-up illustrated in Fig.28 has been employed to carry out the measurements. It consists of an auxiliary DC power supply, the boost converter using Si or SiC devices, an input voltage probe, an additional power supply for converter control circuitry, an oscilloscope, an output voltage probe, a resistive output load, an output voltage multimeter and a LED spot load with 320 LEDs in series.

The steady-state waveforms of the high -voltage low-power experiments in this research are of the type depicted in Fig. 29. In this case the converter employs a 12.2 V input voltage and a 60 k Ω output load and results in a DCM-CCM boundary operation with 1160 V output voltage and a switching frequency of 25 kHz.

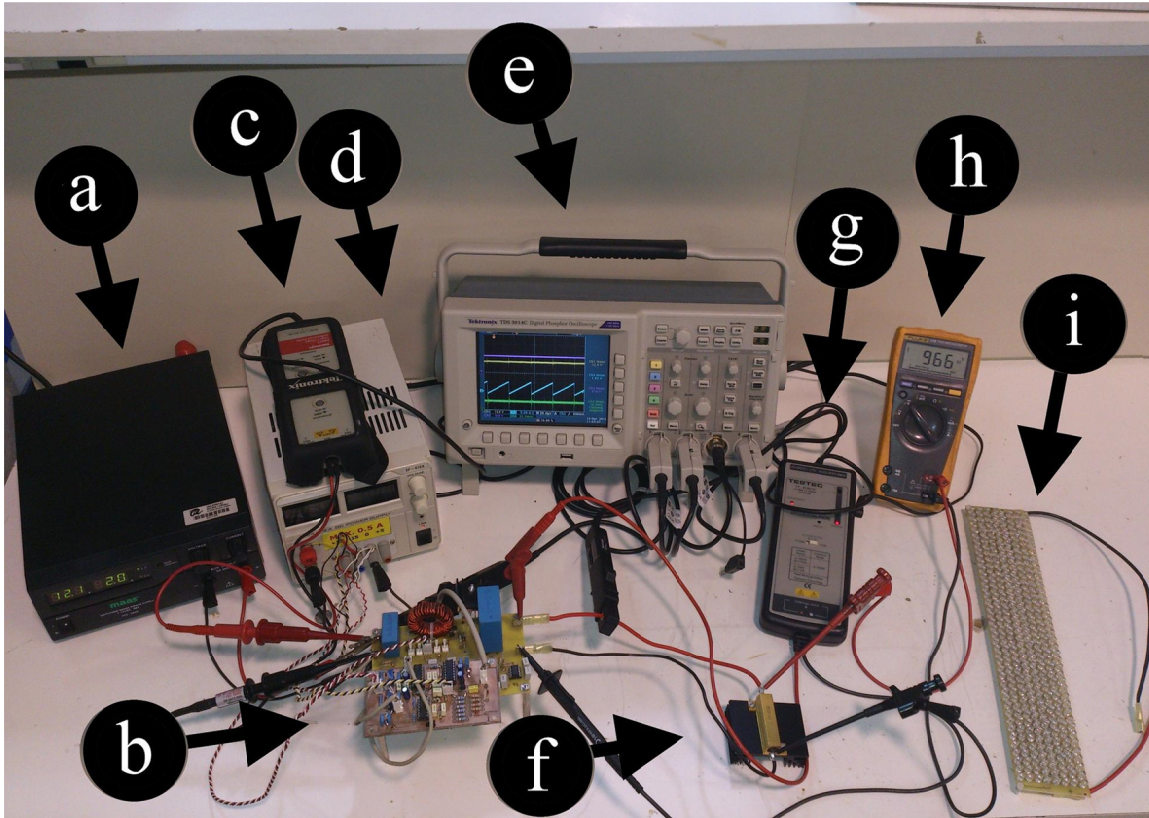


Fig 28. Experimental set-up: a) boost converter b) Input voltage probe c) DC power supply d) Power supply for control circuitry e) Oscilloscope f) Output resistive load g) Output voltage probe h) Output voltage multi-meter i) LED spot load with 320 LEDs in series.

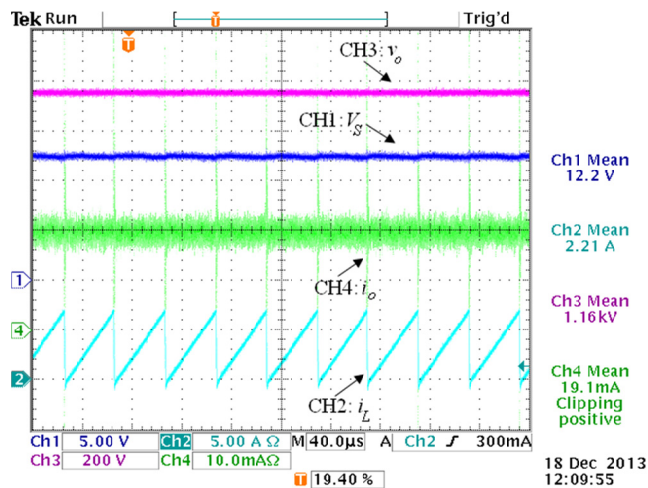


Fig 29. Steady-state waveforms of high-voltage low-power experiment in a boost converter operating in the DCM-CCM boundary.

Table IV shows the characteristics of the semiconductor devices employed in the converter implementation in terms of type of material (Si or SiC) for both transistor and diode. The power diode is DSEP30-12AR in cases 1 and 2 and SDP30S120 and ALS 11 in cases 3 and 4 respectively. The power transistor is IPW90R1200 (Si-MOSFET) in case 1 and SJEP120R063



normally OFF SiC JFET in cases 2, 3, and 4. ALS11 is a power diode fabricated by the Spanish National Centre of Microelectronics (CNM) in the frame of a joint research project with our group ⁽¹⁾. The normally OFF JFET employed in cases 2-4 has required the design of a specific driver.

In the experiments, the converter prototype has been supplied by three different input voltages (9 V, 12 V and 14 V) and for each input voltage different loads have been tested (10 kΩ, 20 kΩ, 30 kΩ, 40 kΩ, 50k Ω, and 60 kΩ) for each switching cell. The output current is regulated at 20 mA level, which is the rated current for the 5 mm diameter LEDs which will constitute later the converter output load.

Table IV. Parameters of the evaluated devices

Parameter	Symbol	Devices					Unit
		Cool MOS	SiC n-off JFET	Si Diode	SiC Diode	SiC Diode	
Manufacturer		Infineon	Semisouth	IXYS	Semisouth	CNM	
Part No.		IPW90R120C3	SJEP120R063	DSEP30-12AR	SDP30S120	ALS-11	
Type		CoolMOS	SiC n-off JFET	Soft-recovery	SiC Schottky	SiC Schottky	
Breakdown Voltage	V_{BD}	900	1200	1200	1200	1200	V
Rated Current	I_{RATED}	23	20	30	30	5	A
Max. Junction Temperature	$T_{J,max}$	150	150	175	175	150	°C
Thermal Resistance, J-C	R_{thJC}	0.3	0.6	1.1	0.48		K/W
On Resistance	$R_{ds,on}$	120	63	--	--	--	mΩ
Total Gate charge	Q_g	270	60	--	--	--	nC
Input Capacitance	C_{ISS}	6800	1220	--	--	--	pF
Output Capacitance	$C_{OSS}^{(2)}$	63	80	--	--	--	pF
Reverse Transfer Capacitance	$C_{RSS}^{(2)}$	3	69	--	--	--	pF
Transconductance	g_{fs}	20	30	--	--	--	S
Forward Voltage	V_F	--	--	1.7-2.7	1.6-2.4	1.8-2.3	V
Total Capacitance	C_j	--	--	47	80	39	pF
Package		TO-247	TO-247	TO-247 AD	TO-247 AD	TO-220	

⁽¹⁾RUE –Advanced Wide Band Gap Semiconductor Devices for Rational Use of Energy CSD2009-0046.

⁽²⁾These values have been extracted from the corresponding graph datasheet

2.2.4 Losses estimation.

There are two main causes of losses in the converter, namely, semiconductor and passive losses. In the first case, losses can be provoked during the switching transition and during the



power device conduction interval, while in the second case losses are produced by parasitic resistances in both inductor and capacitor and by magnetizing phenomena in the inductor core.

Also, it is worth noting that the output voltage is limited to 900 V in the Si-based converter implementation because this value is the breakdown voltage of the MOSFET used in the experiments. Therefore, the output power has an upper bound of 18 W in this case because the output current is regulated at 20 mA. On the contrary, the JFET-based converter can reach an upper bound of 1200V, which results in a maximum output power of 24 W for the same level of output current. Besides, the use of a hysteretic modulator in the control loop yields a switching frequency whose value depends on the coordinates of the equilibrium point [129], this having ranged from 20 kHz to 120 kHz in the tests.

The losses estimation procedure is based on the classical approach reported in [130] and is described next by illustrating the calculation of both conduction and switching losses in semiconductors together with the assessment of losses in the reactive devices.

2.2.4.1 Semiconductor conduction losses.

The conduction losses for both MOSFET/JFET and diode are given by P_{M_con} and P_{D_con} respectively, and are expressed in terms of averaged dissipated power per switching period as follows:

$$P_{M_con} = I_{M(rms)}^2 \cdot R_{ds(on)} = I_L^2 \cdot R_{ds(on)} \cdot D \cdot \frac{4}{3} \quad (35)$$

$$P_{D_con} = V_F \cdot I_D = V_F \cdot I_o \quad (36)$$

2.2.4.2 Semiconductor switching losses.

The switching losses in the power diode are proportional to the switching frequency, the square of the output voltage and the diode junction capacitance and are given by:

$$P_{D_sw} = \frac{1}{2} \cdot C_j \cdot V_o^2 \cdot f_{sw} \quad (37)$$

As regards the MOSFET switching losses, they can be expressed by (38) and (39) for the turn-off and turn-on transitions respectively:

$$P_{M_off} = \frac{1}{2} \cdot I_L \cdot V_o \cdot t_{off} \cdot f_{sw} \quad (38)$$

$$P_{M_on} = \frac{1}{2} \cdot I_L \cdot V_o \cdot t_{on} \cdot f_{sw} \quad (39)$$

In the JFET, the switching losses are not calculated considering the coexistence times (t_{on} , t_{off}) between voltages and currents because the on and off transient waveforms differ significantly from the MOSFET case and are more complex [131]. For this reason, the manufacturer provides graphical information in a data-sheet showing the switching energy losses E_{ON} and E_{OFF} in terms of current I_{Ds} . However, it has to be pointed out that the minimum current value is 4 A in the manufacturer's graph and our converter works with lower currents. Therefore, we have extrapolated the manufacturer's curve by means of a polynomial function of



I_{DS} in order to obtain the values of E_{ON} and E_{OFF} at low current levels. Equations (40)-(41) show the respective polynomial functions for $E_{ON}(I_{DS})$ and $E_{OFF}(I_{DS})$, that are calculated using a polynomial fitting with MATLAB, which yields the values of the coefficients shown in Table V:

$$E_{ON}(I_{DS}) = A_3 \cdot I_{DS}^3 + A_2 \cdot I_{DS}^2 + A_1 \cdot I_{DS} + A_0 \quad (40)$$

$$E_{OFF}(I_{DS}) = B_3 \cdot I_{DS}^3 + B_2 \cdot I_{DS}^2 + B_1 \cdot I_{DS} + B_0 \quad (41)$$

Table V. Coefficients for the polynomial fitting of $E_{ON}(I_{DS})$ and $E_{OFF}(I_{DS})$

Coefficients	Values	Coefficients	Values
A_0	15.1563 μJ	B_0	1.7763 μJ
A_1	7.1808 $\mu\text{J}/\text{A}^1$	B_1	5.3357 $\mu\text{J}/\text{A}^1$
A_2	-0.1959 $\mu\text{J}/\text{A}^2$	B_2	0.2218 $\mu\text{J}/\text{A}^2$
A_3	5.697 nJ/A^3	B_3	-0.7241 nJ/A^3

Thus, the effective switching power loss in the JFET is given by expressions (42) and (43) for on and off transitions respectively:

$$P_{J_{on}} = E_{ON} \cdot f_{sw} \quad (42)$$

$$P_{J_{off}} = E_{OFF} \cdot f_{sw} \quad (43)$$

Note that the output capacitances of the MOSFET and JFET can also produce switching losses which are proportional to the drain to source capacitance C_{DS} and can be expressed as follows:

$$P_{M_{ds}} = \frac{2}{3} C_{DS} \cdot V_{DS}^2 \cdot f_{sw} \quad (44)$$

Besides, the energy lost in the gate must be included in the switching losses in the JFET and MOSFET:

$$P_{M_{gs}} = \frac{1}{2} C_{iss} \cdot V_{GG}^2 \cdot f_{sw} \quad (45)$$

From (37)-(39), it is apparent that fast devices imply low values of transition times t_{on} and t_{off} and therefore low switching losses. This is also the case of the capacitances of the power transistor, which are small for fast devices yielding a low value of power loss in (42) – (43).

Moreover, an indirect index to predict comparatively the switching losses in MOSFET/JFET is the transconductance (g_{fs}), which is given by:

$$g_{fs} = \frac{\Delta I_{DS}}{\Delta V_{GS}} \quad (46)$$

and is usually measured at saturation region for constant value of V_{DS} [132].

From Table IV, it can be expected that the JFET exhibits smaller switching losses than the MOSFET because it has a higher transconductance g_{fs} .



2.2.4.3 Semiconductor switching losses.

Table VI summarizes the estimated losses in the semiconductor devices of the boost converter by applying expressions (35)-(45) in the four switching cells depicted in Fig.27 for an input voltage of 12 V , a switching frequency of 20 KHz and an output voltage of 900 V and 1200 V in MOSFET and JFET –based converters respectively. Similar predictions have been obtained for 9 V and 14 V input voltages and will be used later to estimate the total losses of the converter for the three different values of the input voltage.

Table VI. Estimated semiconductor losses in the boost converter at DCM-CCM operation

Operating Conditions: V_S =12 V, $V_{o(JFET)}$ =1.2 kV, $P_{IN(JFET)}$ = 24W, f_{sw} = 20 kHz $V_{o(MOSFET)}$ =900 V, $P_{IN(MOSFET)}$ = 18W			Switching Cell				Unit
			Si/Si (18 W)	SiC/Si (24 W)	SiC/SiC (A)(24 W)	SiC/SiC (B)(24 W)	
Transistor	Conduction losses	P_{M_con}	0.399	0.195	0.195	0.195	W
	Turn-on losses	P_{M_on}, P_{J_on}	0.270	0.3	0.3	0.3	W
	Turn-off losses	P_{M_off}, P_{J_off}	0.338	0.543	0.543	0.543	W
	Parasitic cap. losses	P_{M_ds}	0.648	0.211	0.211	0.211	W
	Gate source par. cap. losses	P_{M_gs}	0.015	0.003	0.003	0.003	W
	Transistor total losses	P_{M_T}	1.669	1.251	1.251	1.251	W
Diode	Conduction losses	P_{D_con}	0.054	0.054	0.048	0.046	W
	Switching losses	P_{D_SW}	0.381	0.381	1.152	0.562	W
	Diode total losses	P_{D_T}	0.435	0.435	1.200	0.608	W
Switching cell total losses		P_{TOT_cell}	2.104	1.686	2.451	1.859	W

2.2.4.4 Inductor losses.

An input inductor of 70 μ H has been chosen to fulfil the design specifications for an output power between 0 and 24 W and DCM-CCM boundary operation and it has been implemented by means of 37 turns around the core Kool M μ 773244-A7 of Magnetics ® of 11 wires of 0.07mm². Note that the use of 11 wires instead of 1 intends to reduce both the skin effect for switching frequencies beyond 40 kHz and the value of the parasitic series resistance (r_L). Fig. 30 (a) and (b) show respectively the experimental dependence of both inductance and parasitic series resistance on the switching frequency considering input voltages of 9 V, 12 V, and 14 V and the same input power of 24 W in the three cases.

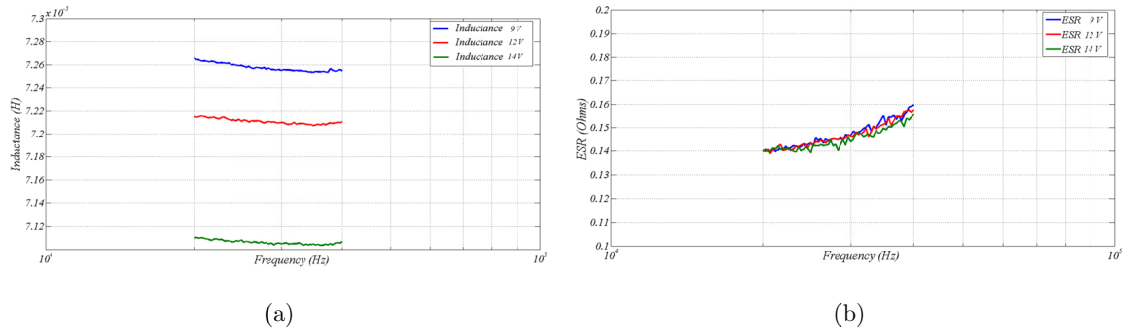


Fig 30. (a) inductance vs. frequency. (b) Parasitic resistance vs. frequency



It can be observed that the inductance remains practically constant in the range between 20 kHz and 40 kHz for a given value of the input voltage. The parasitic resistance in turn has the same value for the three input voltages and is practically constant in the whole frequency range. The resulting average values for 51 measures at 20 kHz yields 71.52μH and 147.36 mΩ for the inductance and the parasitic resistance respectively.

Therefore the copper losses are given by $P_{cooper} = I_{L(rms)}^2 \cdot r_L$, which results in 0.589 W for an input and output voltage of 12 V and 1200 V respectively, switching at 20 kHz. Besides, 0.418 W core losses are estimated by the manufacturer, so that the total predicted losses in the inductor are 1.008 W.

2.2.4.5 Capacitor losses.

The capacitor employed in the converter implementation is of ceramic type with a capacity of 8 uF and an equivalent series resistance of 8 mΩ according to the manufacturer datasheet. The losses associated to the capacitor are produced by this resistance [133] and can be expressed as follows:

$$P_{CAP} = \left(\frac{D}{1-D} \right) \cdot r_C \cdot I_o^2 \quad (47)$$

2.2.4.6 Total losses estimation.

The total converter losses and the corresponding efficiency are estimated taking into account the previous partial losses prediction. Tables VII, VIII and IX show respectively the expected results for each switching cell in Fig.27 considering an input voltage of 9 V, 12 V and 14 V respectively. Observe that the predictions are made for all cells delivering an output voltage of 900 V, which is established by the MOSFET breakdown voltage, and also for cells a, b and c delivering an output voltage of 1.2 kV that corresponds to the JFET breakdown voltage. It has to be pointed out that in the case of an input voltage of 9 V, switching cell d, i.e., SiC/SiC (B), is the only combination that is capable to deliver 1000 V at the output as it is illustrated at the bottom of Table VII. It is apparent that the best results are predicted by the SiC/SiC (B) configuration because it allows reaching 1000 V at the output from an input voltage of 9 V and its expected efficiency is the highest one when the converter delivers 900 V at the output. However, when the converter delivers 1200 V at the output port, switching cell b, i.e., SiC/Si configuration would exhibit a slightly higher efficiency at the expense of a smaller switching frequency, which in the case of an input voltage of 12 V is still within the audio band.

It can be easily verified by means of expressions (35)-(45) that the efficiency in case SiC/Si for a switching frequency of 30 kHz is the biggest one (86.457%), as appears in Table VIII. However, our comparison has been carried out on the basis of equal output power, this implying in the case SiC/SiC (B) a switching frequency of 39 kHz, which results in smaller efficiency (83.709%).



Table VII. Total system losses at $V_S=9$ V.

$V_{o(JFET/MOSFET)}= 900$ V, $P_{IN(JFET/MOSFET)} = 18$ W		Switching Cell				Unit
		Si/Si $f=23kHz$	SiC/Si $f=19kHz$	SiC/SiC (A) $f=20kHz$	SiC/SiC (B) $f=21kHz$	
Total Switching cell loss	P_{TOT_cell}	2.897	1.603	1.855	1.585	W
Total Inductor losses	P_{IND}	1.008	1.008	1.008	1.008	W
Total Capacitor losses	P_{CAP}	0.0003168	0.0003168	0.0003168	0.0003168	
Total Converter losses	$P_{CONVERTER}$	3.905	2.611	2.863	2.593	W
Estimated Highest Efficiency	η	78.305	85.496	84.094	85.594	%
$V_{o(JFET)}= 1000$ V, $P_{IN(JFET)} = 20$ W			SiC/Si	SiC/SiC (A)	SiC/SiC (B) $f=20kHz$	
Total Switching cell loss	P_{TOT_cell}				1.725	W
Total Inductor losses	P_{IND}				1.146	W
Total Capacitor losses	P_{CAP}				0.0003524	
Total Converter losses	$P_{CONVERTER}$				2.872	W
Estimated Highest Efficiency	η				85.642	%

Table VIII. Total system losses at $V_S=12$ V.

$V_{o(JFET/MOSFET)}= 900$ V, $P_{IN(JFET/MOSFET)} = 18$ W		Switching Cell				Unit
		Si/Si $f=35$ kHz	SiC/Si $f=28$ kHz	SiC/SiC (A) $f=23$ kHz	SiC/SiC (B) $f=27$ kHz	
Total Switching cell loss	P_{TOT_cell}	3.343	2.078	1.866	1.713	W
Total Inductor losses	P_{IND}	0.750	0.750	0.750	0.750	W
Total Capacitor losses	P_{CAP}	0.0002368	0.0002368	0.0002368	0.0002368	W
Total Converter losses	$P_{CONVERTER}$	4.093	2.829	2.616	2.463	W
Estimated Highest Efficiency	η	77.261	84.285	85.466	86.317	%
$V_{o(JFET)}= 1200$ V, $P_{IN(JFET)} = 24$ W			SiC/Si $f=19kHz$	SiC/SiC (A) $f=20kHz$	SiC/SiC (B) $f=22kHz$	
Total Switching cell loss	P_{TOT_cell}		1.919	2.451	2.021	W
Total Inductor losses	P_{IND}		1.008	1.008	1.008	W
Total Capacitor losses	P_{CAP}		0.0003168	0.0003168	0.0003168	W
Total Converter losses	$P_{CONVERTER}$		2.927	3.5460	3.029	W
Estimated Highest Efficiency	η		87.804	85.585	87.379	%



Table IX. Total system losses at $V_s=14$ V.

$V_{o(JFET/MOSFET)} = 900$ V, $P_{IN(JFET/MOSFET)} = 18$ W		Switching Cell				Unit
		Si/Si $f=39kHz$	SiC/Si $f=30kHz$	SiC/SiC (A) $f=30kHz$	SiC/SiC (B) $f=39kHz$	
Total Switching cell loss	P_{TOT_cell}	3.397	2.052	2.275	2.270	W
Total Inductor losses	P_{IND}	0.662	0.662	0.662	0.662	W
Total Capacitor losses	P_{CAP}	0.0002025	0.00020251	0.000202514	0.0002025	
Total Converter losses	$P_{CONVERTER}$	4.060	2.714	2.938	2.932	W
Estimated Highest Efficiency	η	77.446	84.921	83.679	83.709	%
$V_{o(JFET)} = 1200$ V, $P_{IN(JFET)} = 24$ W			SiC/Si $f=22kHz$	SiC/SiC (A) $f=22kHz$	SiC/SiC (B) $f=30kHz$	
Total Switching cell loss	P_{TOT_cell}		2.022	2.541	2.508	W
Total Inductor losses	P_{IND}		0.851	0.851	0.851	W
Total Capacitor losses	P_{CAP}		0.00027109	0.000271086	0.0002711	
Total Converter losses	$P_{CONVERTER}$		2.874	3.393	3.359	W
Estimated Highest Efficiency	η		88.026	85.864	86.002	%

2.2.4.7 Limited gain converter due to the parasitic elements in the devices.

The parasitic resistances have a direct effect in the limitation of the converter DC gain. Disregarding the diode voltage drop because this device conduct during a non-significant time interval, the resulting DC gain is the one given by expression (48), which would correspond to the one of an ideal boost converter $1/(1-D)$ if the parasitic resistances were neglected.

$$\frac{V_o}{V_s} = \frac{R_o(1-D)}{R_o(1-D)^2 + \frac{D(1-D)}{R_o + r_C} R_o \cdot r_C + R_{ds(on)} + R_{SENSE} + r_L} \quad (48)$$

2.2.5 Experimental results.

Figs. 31 (a), 31 (b), 31 (c) and 31 (d) show respectively the experimental results of the boost converter implemented with switching cells *a*, *b*, *c*, and *d* in terms of efficiency and switching frequency for the same output power for a given output voltage and different levels of input voltages. The difference between the measured efficiency and the theoretical prediction ranges from 1 % in the minimum case to 6 % in the maximum one. This discrepancy has different causes, namely, i) parasitic resistances, capacitances and inductances in the layout paths not considered in the model, ii) the variable nature of the switching frequency whose experimental value is sensitive to unmodelled parasitic elements and therefore does not result exactly in the expected theoretical value, and iii) the fact that the datasheets predictions used in the estimations have been obtained by the manufacturer for an specific working point and not for all the operating range of the switching converter. The experimental behaviour of each switching cell is discussed next in terms of efficiency and switching frequency measurements and losses interpretation.

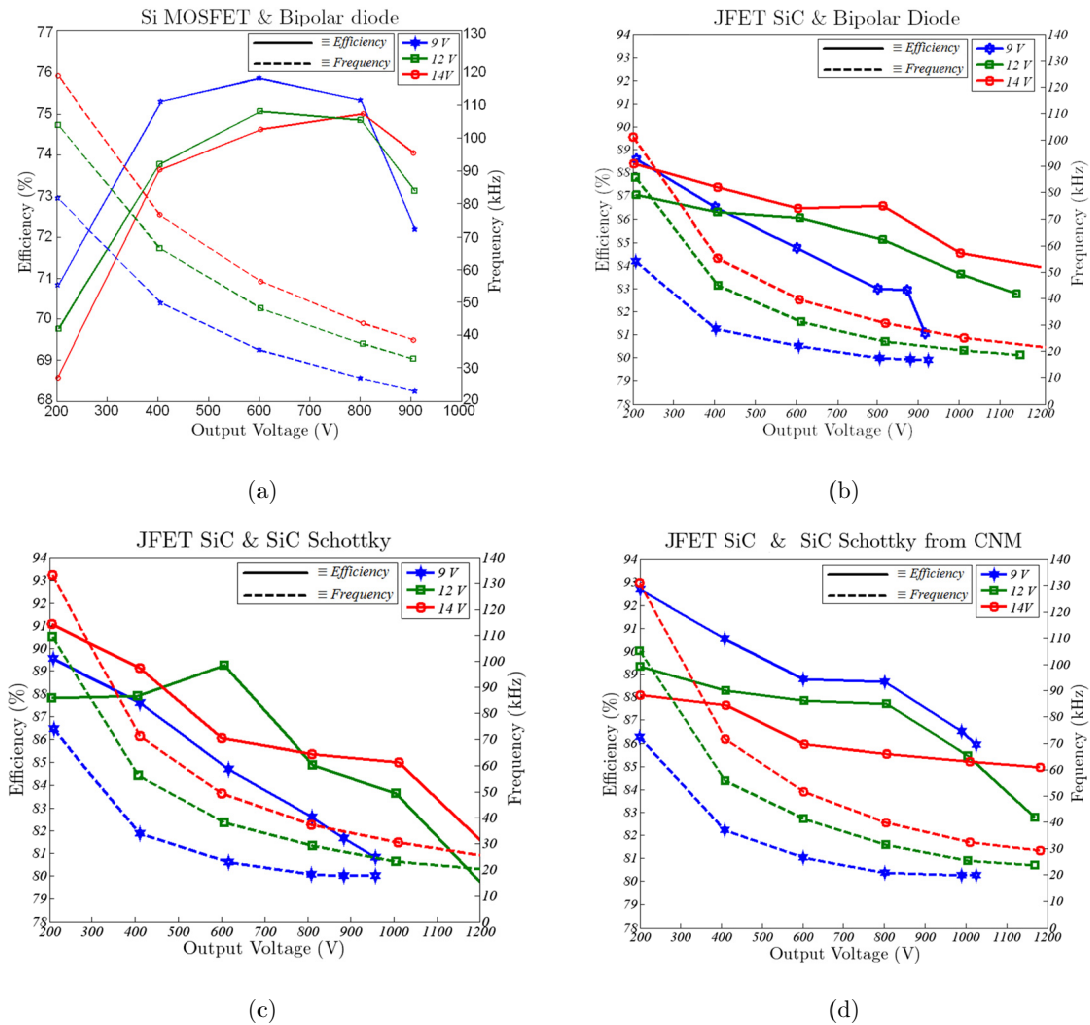


Fig 31. Efficiency and switching frequency with different switching cells. (a) Si/Si, (b) SiC/Si, (c) SiC/SiC A, (d) SiC/SiC B.

2.2.5.1 Si diode and Si MOSFET.

The efficiency curves and the resulting switching frequency in Si/Si are depicted in Fig.31 (a). It can be observed that the switching frequency decreases as the output voltage increases and that the measured efficiency is between 3 and 6% below the theoretical predictions. It can be concluded that below 800 V in the output voltage, the dominant losses are of switching type, the conduction losses being preponderant beyond the mentioned value. The converter exhibits the highest efficiency in the region of the output voltage below 800 V in the case of the lowest input voltage.

2.2.5.2 Si diode and SiC JFET.

The corresponding efficiency curves and the resulting switching frequency in this case are depicted in Fig.31 (b). It can be observed that the converter exhibits a much higher efficiency than in the previous case in all operating range and for the different input voltages as expected



from the theoretical analysis. The measured efficiency is between 3 % and 5 % below the estimated value.

2.2.5.3 Si diode and SiC JFET (A).

Fig. 31 (c) shows the efficiency curves and the resulting switching frequency for switching cell c, which has been implemented with the same JFET as in the previous case and the SiC diode SDP30S120. It can be observed that the measured efficiency is between 3 and 5% below the estimated value and is smaller than in the previous case in perfect agreement with the theoretical predictions.

2.2.5.4 Si diode and SiC JFET (B).

Fig. 31 (d) shows the efficiency curves and the resulting switching frequency for the same SiC JFET as in previous cases and the SiC diode ALS11. A significant improvement in efficiency is observed now with measured values between 1 and 3% below the theoretical prediction.

Fig. 32 (a) shows the experimental waveforms corresponding to the steady-state behaviour of the SiC/Si switching cell based converter for an output voltage around 670 V and a resulting switching frequency of 62.3 kHz. Similar waveforms have been obtained in the other three cases but are not shown here for simplicity reasons. Note that, besides the output voltage v_o and the inductor current i_L , Fig.32 (a) also shows both drain to source instantaneous voltage and current and its product $P_{sw}(t)$, which is the switching losses instantaneous power waveform in the transistor. The switching losses mechanism is illustrated in Fig. 32 (b), which is a detailed zoom in an interval of 1 μ s of similar steady-state behaviour of that of Fig. 32 (a), and where it can be seen the turn-off transients of both, transistor and diode and the waveform $P_{sw}(t)$ in the JFET during the ON and OFF transient.

Similarly, in terms of zoom description, Fig. 32 (c) shows the reason of smaller efficiency in switching cell SiC/SiC (A) than in switching cell SiC/Si as mentioned above. Note that in switching cell SiC/SiC(A) the discharge of the SiC diode parasitic capacitance through the JFET provokes a bigger peak of $P_{sw}(t)$ than the one depicted in Fig. 32 (b) , which corresponds to switching cell SiC/Si. It has to be pointed out that the experiment has been carried out in similar conditions of output voltage and switching frequency than those corresponding to the experiment in Fig. 32 (b).

The smallest value of the diode parasitic capacitance is the reason of the significant improvement in efficiency observed above in the case of switching cell SiC/SiC(B) as illustrated in Fig 32 (d), where the discharge through the JFET provokes the smallest peak of $P_{sw}(t)$ for the same operation conditions than those in the experiment of Fig. 32 (b). The small value of the parasitic capacitance is due to the small surface of the device because this one has been ad hoc fabricated to handle low currents in a clear-cut contrast with the commercial devices in cases Si/Si, SiC/Si, and SiC/SiC(A), which have been designed to support six times higher values of current, and therefore their respective surfaces are considerably higher. It has to be



pointed out that measurements corresponding to Figures 32 (b), 32 (c), 32 (d) have been carried out by means of a Lecroy PP009 voltage probe and a Tektronix TCP202 current probe together with a Tektronix TDS3042B oscilloscope of 200 MHz bandwidth, which guarantees a sufficient precision without requiring an specific set-up as described in [134]. Nevertheless, it can be observed that the worst case corresponds to the fastest signal with duration around 20 ns, which would require a probe with a bandwidth exceeding 50 MHz, this value being the upper limit of the Tektronix probe.

Therefore, the switching cell SiC/SiC (B) implementation, presents the highest efficiency both theoretically and experimentally and allows the converter to achieve DC gains higher than 100. For this reason, switching cell SiC/SiC(B) has been selected to implement a boost converter to supply a high-voltage low-power LED-spot light, as illustrated in Fig 33. The prototype parameters set are $V_s=12$ V, $L=71.52$ μ H, $C=8$ μ F. The converter has been tested with a spot of 320 LEDs in series, this resulting in an output voltage of 956 V and an output current of 21.6 mA. The input voltage and inductor current in this test are 12.1 V and 1.97 A respectively, so that an efficiency of 86.5 % has been obtained.

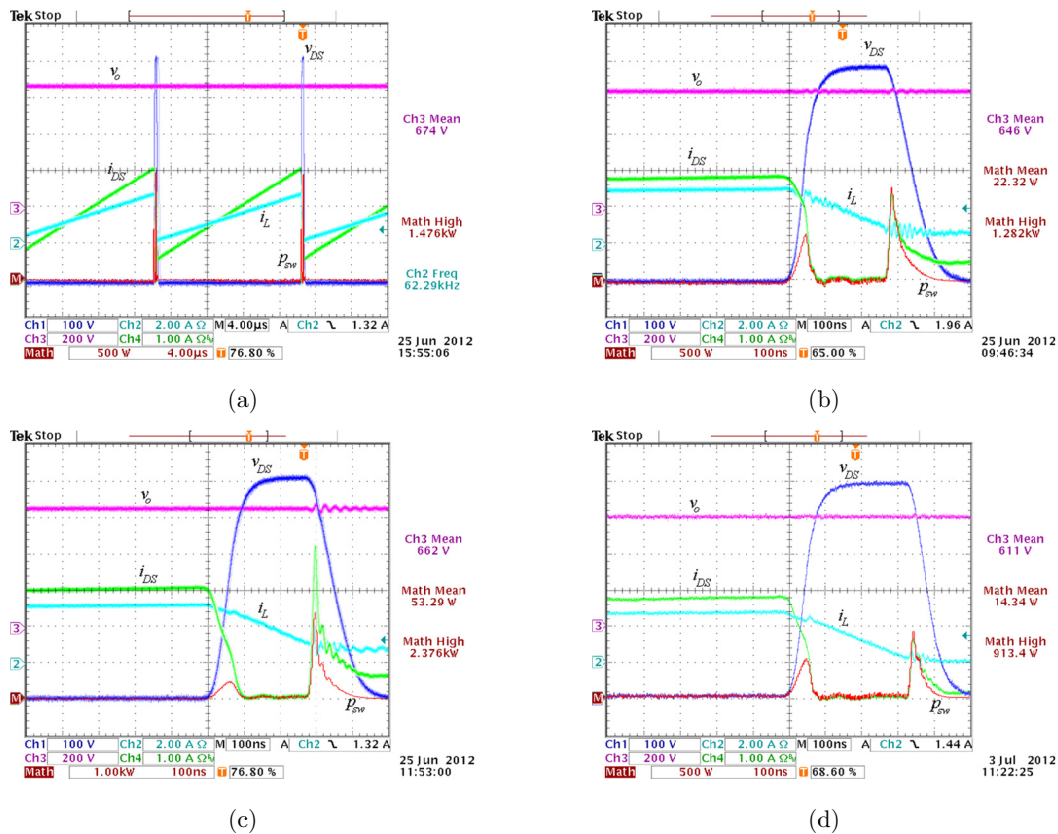


Fig 32. Switching losses illustration. (a) Steady-state for SiC/Si and detailed zoom for (b) SiC/Si, (c) SiC/SiC A, (d) SiC/SiC B.

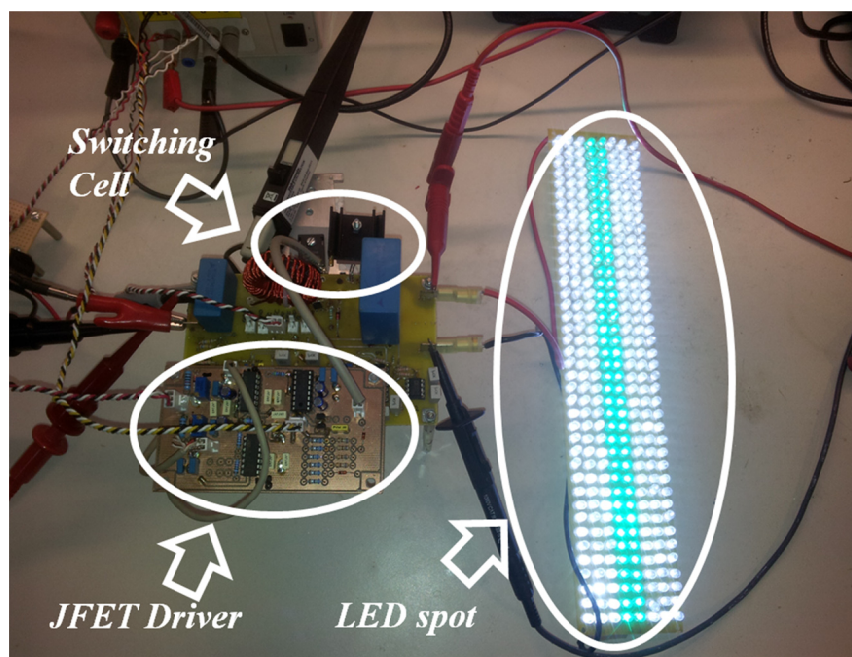


Fig 33. SiC-SiC (B)-based boost converter supplying a high voltage LED-spot.

2.2.6 Conclusions of the efficiency investigation in the single-stage boost converter.

Four different switching cells have been studied both theoretically and experimentally in terms of efficiency and switching frequency. The first one employs exclusively Si devices, while the third and four ones only use SiC components. The second cell mixes both technologies and consists in a SiC JFET and a Si diode. The Si-based converter has the smallest efficiency while the SiC-based converter with the diode with the least parasitic capacitance has led to the best efficiency and the most appropriate switching frequency in the whole operating range.

The switching cell with the highest efficiency has been employed in the implementation of a power supply for a spot of 320 LEDs in series, which results in an output voltage of 956 V and an output power of 20.6 W. The power supply for LED-based lighting systems has been recently patented [135].

It can be also observed that the converter acts as a loss-free resistor [60], so that the input port has a resistive behaviour and the output port is a power source supplying to the load all the power absorbed by the emulated resistance in an ideal case of maximum efficiency. As the actual efficiency of the converter is not 100%, the input power and the switching frequency must be different in each case in order to ensure the same value of output power.



2.3 A high voltage SiC-based boost PFC for LED applications.

This subsection covers the analysis and design of a single-stage grid-supplied boost converter with power factor correction (PFC) for LED-applications using Silicon-Carbide (SiC) and operating at the boundary between continuous and discontinuous conduction modes (CCM-DCM) to reduce switching losses. The converter is supplied by a 230 V_{RMS} grid voltage, and attains 1200 V DC at the output port, where a-spot of 320 LEDs connected in series is supplied at constant current. Sliding-mode control is employed to synthesize a two-port with almost LFR characteristics at the input port and a high degree of output current regulation at the output port. The controller is easily implemented by means of a hysteretic comparator avoiding the risk of modulator saturation. The converter can operate in a normal mode, in which all the input current semi-cycles are employed, and in a burst mode where only a fraction of all the current semi-cycles is used. The power switch is realized with silicon carbide (SiC) devices to improve the performance of low-power -grid -supplied LED-based lighting systems. The experimental results are in perfect agreement with the theoretical predictions and demonstrate the feasibility of the proposed approach.

2.3.1 Grid-supplied lighting systems.

In the field of LED lighting, several on-grid single-stage active topologies with PFC can be found in the literature [136]. They consist in a rectifier in cascade with a DC-DC converter. This DC-DC converter is introduced to regulate the current through the LEDs with two different options. The first option implies the inclusion of a capacitor between the rectifier and the converter. This solution assures a constant LED current with a negligible ripple as the converter control-loop is dedicated to regulate such current. Nonetheless, the power factor correction cannot be realized. In the second option, PFC is possible because the capacitor is transferred to the output of the DC-DC converter, this resulting in a significant ripple increment in the LEDs current. To solve this problem, some authors have proposed a two-stage converter [137], where the first stage assures the PFC, and the second one regulates the output current at a constant level with no ripple, avoiding LED-light flicker problems.

The goal of this section is to implement a single-stage SiC -based PFC boost converter operating as a current source with a negligible output ripple without losing PFC capability. An additional objective is applying the previous implementation in the supply of a high-voltage LED spot using SiC power devices. The converter control is based on the sliding mode control theory applied to the input current, and is implemented with a hysteretic comparator. The converter is studied in normal and burst operations modes. The output of the converter is loaded with a LED-spot with 320 LED devices connected in series. The risk of failing provoked by an element in open circuit is mitigated by connecting a Zener bypass diode for each 4 LEDs. The spot luminosity is regulated changing the I_{ref} value in Fig 34.

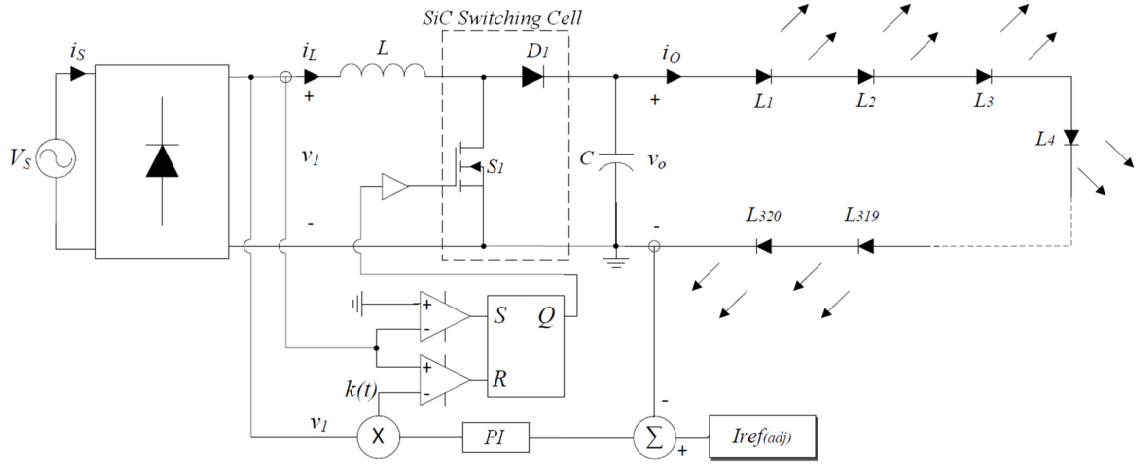


Fig 34. Boost converter with a hysteretic control of the input current.

2.3.2 Sliding-mode operation analysis in the PFC-boost converter.

The circuit description of the converter working in the DCM-CCM boundary is depicted in Fig. 35. The PFC-boost converter has two structural changes within a period, i.e. ON state, Fig. 35 (a), and OFF state Fig. 35 (b), and therefore it can be represented by means of two linear vector differential equations.

$$\dot{x}(t) = A_1 x(t) + B_1 \quad \text{for } u = 1 \quad (ON \text{ state}) \quad (49)$$

$$\dot{x}(t) = A_2 x(t) + B_2 \quad \text{for } u = 0 \quad (OFF \text{ state}) \quad (50)$$

where $x(t)$ is the state vector corresponding to the state variables of the power stage

$$x(t) = [i_L, v_C]^T \quad (51)$$

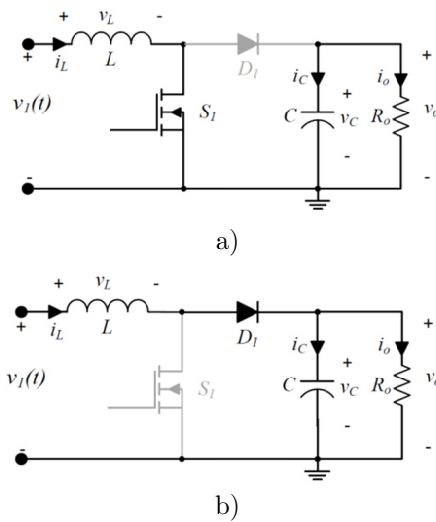


Fig 35. Boost converter states. A) ON-state; and b) OFF-state

Matrices A_1 , B_1 , A_2 , and B_2 are given respectively by



$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_o C} \end{bmatrix}; \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_o C} \end{bmatrix}; \quad B_1 = B_2 = \begin{bmatrix} \frac{v_i(t)}{L} \\ 0 \end{bmatrix} \quad (52)$$

Now, the sliding-mode control is used to design a single-stage PFC boost converter supplied by the grid voltage with a regulated DC output current of 20 mA. The fulfilment of both goals, i.e. PFC at the input port and DC output current regulation at the output port is intended by a single switching surface given by

$$s(x) = i_L - k(t) \quad (53)$$

where

$$k(t) = g(t) \cdot v_i(t) \quad (54)$$

and

$$g(t) = \left(K_P (I_{REF} - i_o(t)) + K_I \int_{-\infty}^t (I_{REF} - i_o(t)) \cdot dt \right) \quad (55)$$

where I_{REF} is the output current reference, $i_o(t)$ is the output current, and $v_i(t)$ is the rectified input voltage of 230 V_{RMS} .

It is apparent that there is a trade-off between attaining PFC at the input port (pure LFR behaviour) and obtaining DC current regulation at the output port. As a matter of fact, PFC can only be achieved if $g(t)$ is constant because in that case the inductor current and the input voltage are proportional when the converter reaches the sliding mode regime. On the contrary, output current regulation can be obtained only when the *PI* compensator is working, this implying that $g(t)$ is a time varying signal. Therefore, the output current regulation degrades the PFC but a good parameter choice could provide a high degree of both antagonist requirements.

Besides, it is important to remark that the converter has to operate in the DCM-CCM boundary because this is the best trade-off between suppressing the reverse recovery peak of the diode and minimizing the conduction losses inherent to the DCM [128]. For this reason, as illustrated in Fig.36, the constant $k(t)$ must be twice the average input current value I_m .

$$2 \cdot I_m = k(t) = g(t) \cdot v_i(t) \quad (56)$$

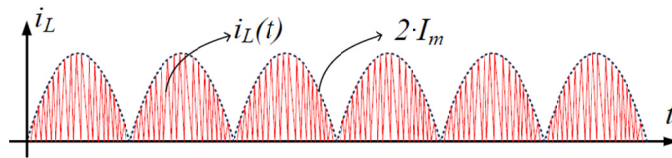


Fig 36. Input current of the PFC-boost converter.

Therefore, introducing the invariance conditions presented in [78] $s(x)=0$ and $ds(x)/dt=0$ results in the equivalent control $u_{eq}(t)$. This equivalent control is delimited by both maximum and minimum values of $u(t)$.



$$0 < u_{eq}(t) < 1 \quad (57)$$

Moreover, a switching law of the type

$$u(t) = 0 \quad \text{if} \quad s(x) > 0 \quad (58)$$

$$u(t) = 1 \quad \text{if} \quad s(x) < 0 \quad (59)$$

will induce a sliding regime on the switching surface ensuring the sliding-mode existence conditions because

$$s(x) \frac{ds(x)}{dt} < 0 \quad (60)$$

The sliding mode analysis of equations (49)-(55) will be performed in two steps. First of all, we will find the equilibrium point corresponding to a constant input voltage V_I and a constant value G of $g(t)$ in the control loop. Subsequently, we will consider the influence of the time varying components of $v_i(t)$ and $g(t)$ as low-frequency superposed signals on the corresponding constant values V_I and G . The contribution of the superposed signals will be predicted by a model derived by linearizing the ideal sliding dynamics around the equilibrium point previously obtained.

Therefore, the resulting equivalent control for $S(x)=i_L-G \cdot V_I$, and the corresponding sliding dynamics are given by the expressions (61), (62) and (63) respectively.

$$u_{eq} = 1 - \frac{V_I}{V_C} \quad (61)$$

$$i_L = G \cdot V_I \quad (62)$$

$$\frac{dv_C}{dt} = \frac{G \cdot V_I}{C} (1 - u_{eq}) - \frac{v_c}{R_o \cdot C} \quad (63)$$

Therefore, the coordinates of the equilibrium point $X^*=[I_L^* \ V_C^*]$ are given by (64)-(65)

$$I_L^* = G \cdot V_I \quad (64)$$

$$V_C^* = V_I \cdot \sqrt{R_o \cdot G} \quad (65)$$

Assuming now that $k(t)$ is time-varying, the corresponding equivalent control will be given by

$$u_{eq}(t) = 1 - \frac{v_i(t)}{v_c} + \frac{L \cdot g(t)}{v_c} \frac{dv_i}{dt} + \frac{L \cdot v_i(t)}{v_c} \frac{dg(t)}{dt} \quad (66)$$

Therefore, the ideal sliding dynamics can be expressed as (67)-(68)

$$i_L(t) \approx k(t) = g(t) \cdot v_i(t) \quad (67)$$

$$\frac{dv_C}{dt} = \frac{g(t) \cdot v_i^2(t)}{C \cdot v_c} - \frac{g^2(t) \cdot v_i(t) \cdot L}{C \cdot v_c} \frac{dv_i}{dt} - \frac{g(t) \cdot v_i^2(t) \cdot L}{C \cdot v_c} \frac{dg(t)}{dt} - \frac{v_c}{RC} = f(x) \quad (68)$$



assuming that

$$\begin{aligned} g(t) &= G + \hat{g}(t) \\ v_i(t) &= V_i + \hat{v}_i(t) \\ i_L(t) &= I_L^* + \hat{i}_L(t) \\ v_c(t) &= V_c^* + \hat{v}_c(t) \end{aligned} \quad (69)$$

and linearizing equation (68) around the equilibrium point $X^*=[I_L^* \ V_c^*]$ lead to the following expression

$$\frac{d\hat{v}_c}{dt} = a \cdot \hat{g}(t) + b \cdot \frac{d\hat{g}(t)}{dt} + c \cdot \hat{v}_i(t) + d \cdot \frac{d\hat{v}_i(t)}{dt} + e \cdot \hat{v}_c \quad (70)$$

where coefficients a , b , c , d and e are given by expressions (71),(72),(73), (74) and (75) respectively.

$$a = \left. \frac{\partial f(x)}{\partial g} \right|_{X^*} = \frac{V_i}{C \cdot \sqrt{R_o \cdot G}} \quad (71)$$

$$b = \left. \frac{\partial f(x)}{\partial \alpha} \right|_{\alpha = \frac{dg(t)}{dt}, X^*} = - \frac{G \cdot V_i \cdot L}{C \cdot \sqrt{R_o \cdot G}} \quad (72)$$

$$c = \left. \frac{\partial f(x)}{\partial v_i(t)} \right|_{X^*} = - \frac{2 \cdot G}{C \cdot \sqrt{R_o \cdot G}} \quad (73)$$

$$d = \left. \frac{\partial f(x)}{\partial \beta} \right|_{\beta = \frac{dv_i(t)}{dt}, X^*} = - \frac{G^2 \cdot L}{C \cdot \sqrt{R_o \cdot G}} \quad (74)$$

$$e = \left. \frac{\partial f(x)}{\partial v_c} \right|_{X^*} = - \frac{2}{R_o \cdot C} \quad (75)$$

Fig. 37 shows the model of the closed loop of the sliding mode controlled boost converter presented in Fig. 34, where $\hat{I}_{REF}(s)$ represents the variations of the output reference, and the expressions of $H(s)$ and $A(s)$ are derived from expression (70) by assuming $\hat{v}_i(t)=0$ and $\hat{g}(t)=0$ respectively

Hence,

$$H(s) = \frac{\hat{V}_c(s)}{\hat{G}(s)} = \frac{a+b \cdot s}{s-e} = \frac{\frac{V_i}{C \cdot \sqrt{R_o \cdot G}} \cdot (1-s \cdot G \cdot L)}{s + \frac{2}{R_o \cdot C}} \quad (76)$$

$$A(s) = \frac{\hat{V}_c(s)}{\hat{V}_i(s)} = \frac{c+d \cdot s}{s-e} = - \frac{\frac{G}{C \cdot \sqrt{R_o \cdot G}} \cdot (2+s \cdot G \cdot L)}{s + \frac{2}{R_o \cdot C}} \quad (77)$$

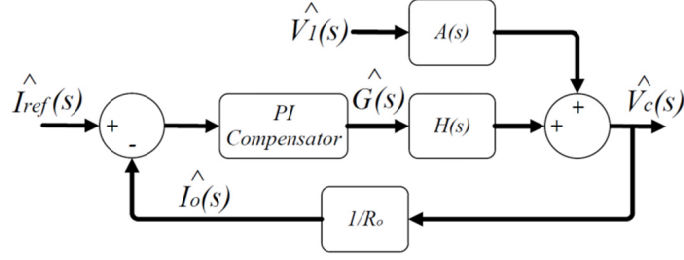


Fig 37. Dynamic model of the switched regulator depicted in Fig. 32.

The system loop gain can be expressed as

$$T(s) = H(s) \cdot \frac{1}{R_o} \cdot \left(k_p + \frac{k_i}{s} \right) = \frac{s^2 \cdot b \cdot k_p + s \cdot (b \cdot k_i + a \cdot k_p) + a \cdot k_i}{s \cdot R_o \cdot (s - e)} \quad (78)$$

and the characteristic equation of the system will be given by

$$1 + T(s) = s^2 \cdot (k_p \cdot b + R_o) + s \cdot (k_i \cdot b + k_p \cdot a - e \cdot R_o) + k_i \cdot a = 0 \quad (79)$$

which will correspond to a stable system provided that following conditions are satisfied

$$0 < k_i < \frac{1}{G \cdot L} \cdot k_p + \frac{2}{V_i \cdot G \cdot L} \sqrt{R_o \cdot G} \quad (80)$$

$$k_p < \frac{R_o \cdot C \cdot \sqrt{R_o \cdot G}}{G \cdot V_i \cdot L} \quad (81)$$

2.3.3 Normal mode vs. burst mode in the PFC-boost converter.

2.3.3.1 Normal operation.

In order to check the proposed control, the boost converter with PFC capability and output current regulation has been simulated using the PSIM program professional version 9.0 with the circuit parameters shown in Table X. It is important to notice that the output load in the simulation is of resistive type absorbing the same level of current than an equivalent load made of series connected LEDs.

Table X. Design specifications.

Input voltage	230 V/ 50 Hz
Output load R_o	60 k Ω
Output power	24 W
Output Current	20 mA
L/C	1 mH/16 μ F

Fig. 38 (a) illustrates the steady-state response of the boost converter output current. Note that the output current is almost constant and regulated at 20 mA, which corresponds to the rated current of 5 mm diameter LEDs devices. A small remaining ripple of 100 Hz produced



in the rectifying stage is superposed to the output current as it can be observed in the same figure.

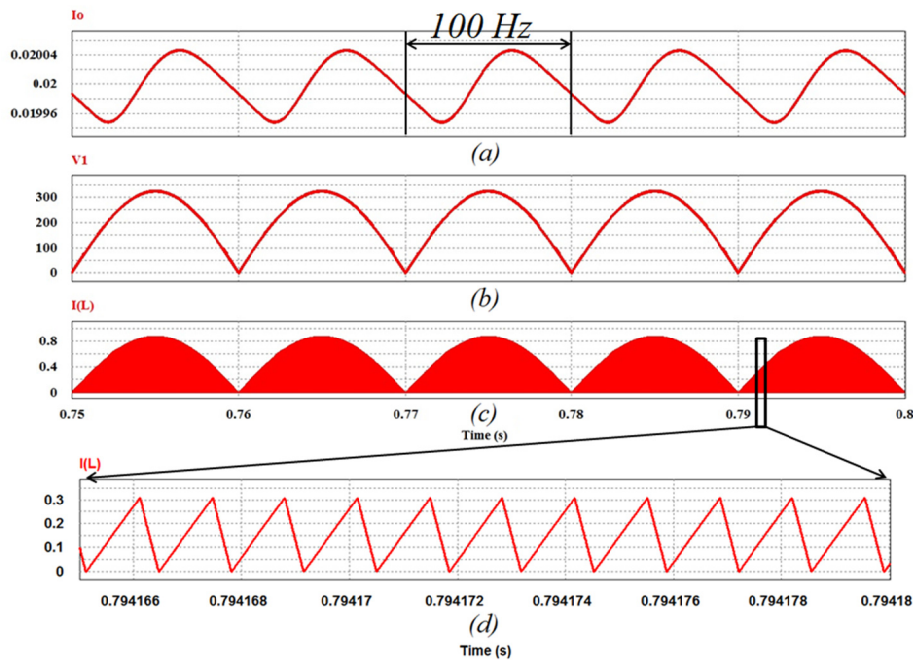


Fig 38. Steady-state response of: a) Output current $i_o(t)$. b) Rectified line voltage $v_i(t)$, c) inductor current $i_L(t)$, d) zoom of the inductor current $i_L(t)$.

Fig. 38 (b), and 38 (c), in turn, shows the steady-state behaviour of the rectified input voltage and inductor current, respectively. It can be observed, that the input voltage $v_i(t)$ is around $230 V_{rms}$, and the inductor current $i_L(t)$ is at DCM-CCM boundary as illustrated Fig 38 (d). Moreover, it is possible to see that the inductor current $i_L(t)$ is practically in phase with the rectified line voltage $v_i(t)$, so that a near unity power factor is achieved.

The limits of this operation (normal operation) are established by low values of inductor current corresponding to low values of power. For example, an output voltage of 1.2 kV with an output current of 20 mA, i.e., a delivery of 24 W to the LEDs, would imply an average value of the inductor current around several of hundreds of mili-amperes. As a consequence, the inductor current would rapidly attain the reference signal $k(t)$, this resulting in higher values of switching frequencies and therefore in larger losses.

To counteract this problem, a solution could be the increment of the input inductance L . However, this increase of inductance entails three important drawbacks. First, the size and weight of the inductor increases, which means that the power density of the converter is decreased. Second, if the inductance increases, the series inductor resistance will increase too, thus implying higher conduction losses and lower efficiency. Third, if the inductor resistance is higher, the voltage gain will be reduced as demonstrated in [128]. Hence, increasing the inductance is not a good solution to improve the efficiency of the converter.



Therefore, it is proposed in the next subsection the design of the single-stage PFC-boost converter operating in a burst mode [138] with the aim of improving the converter efficiency without changing the inductor value and using the same control technique presented in subsection 2.3.2.

2.3.3.2 Burst operation.

In the literature there are some publications about the burst mode applied in the field of LED lighting, the most relevant being reference [139], where this mode is used to obtain a light regulation.

Fig. 39 shows the block diagram of the burst mode implementation in our case. The grid voltage (V_s) is measured and processed by a pulse generator which provides a positive pulse train (V_{PULSE}) synchronized with the grid frequency. Subsequently, a flip-flop acting as a counter provides a positive pulse at the output (V_{COUNT}) for every two pulses at the input. Finally, V_{COUNT} and the signal provided by the hysteretic comparator ($Q_{SLIDING}$) are introduced in an AND gate, so the corresponding output Q_{BURST} is applied to the MOSFET only when $V_{COUNT}=1$. Hence, Q_{BURST} constitutes a grid-synchronized repetitive sequence of two states, in which the MOSFET is activated in the first state, and deactivated in the second one. In other words, $Q_{SLIDING}$ is applied to the MOSFET only one of each two cycles.

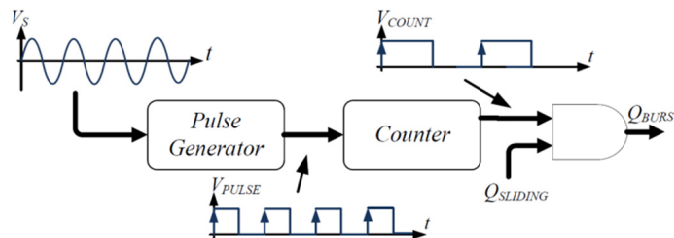


Fig 39. Burst mode control block diagram.

Fig. 40 shows the expected behaviour of the inductor current in the burst mode under sliding mode control. N_A represents the number of the input current semi-cycles employed in this operation, whereas N_T is the total number of semi-cycles. Since the MOSFET is only activated by the hysteretic control in the desired periods, the instantaneous input current $i_L(t)$ must be higher than in the normal operation mode to satisfy the load requirements. Consequently, such current will take more time to achieve the desired reference $k(t)$, and the resulting switching frequency will be reduced, thus improving the efficiency.

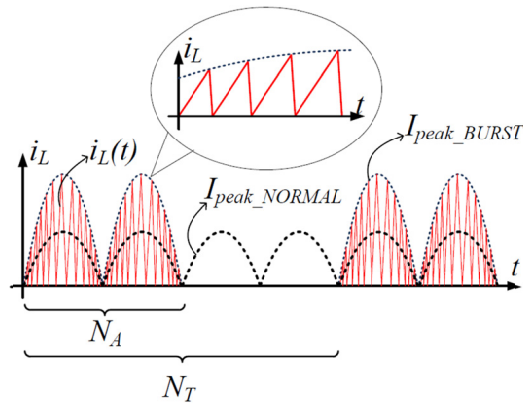


Fig 40. Input current of the PFC-boost converter under burst operation compared with input current envelope in normal mode ($N_A=2$, $N_T=4$).

Besides, considering the cycles in which the control is acting, it is possible to calculate both envelope and switching frequency of the input current as follows

$$I_{peak_BURST} = I_{peak_NORMAL} \cdot \sqrt{\frac{N_T}{N_A}} = \frac{2 \cdot V_o \cdot I_o}{220} \cdot \sqrt{\frac{N_T}{N_A}} \quad (82)$$

$$f_{sw_BURST} = f_{sw_NORMAL} \cdot \left(\frac{N_A}{N_T} \right)^{\frac{3}{2}} \quad (83)$$

It has to be pointed out that I_{peak_BURST} and I_{peak_NORMAL} are the highest current peaks inside the sinusoidal waveform in burst and normal operation modes respectively. Similarly, f_{sw_BURST} and f_{sw_NORMAL} are the corresponding switching frequencies.

However, some drawbacks associated to the use of burst mode are due to an the increase of the output voltage ripple provoked by the presence of input current semi-cycles of higher amplitude and smaller frequency, this eventually producing slight power factor degradation.

2.3.4 PFC-boost converter implementation.

2.3.4.1 Power stage

Figs. 41 and 43 illustrate the power stage circuit and the implementation of the hysteretic control respectively.

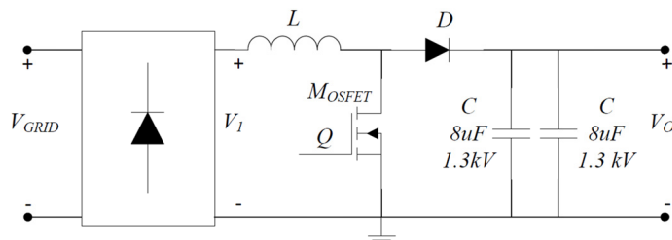


Fig 41. Power stage scheme



The prototype has been implemented with the SiC devices whose characteristics are shown in Table XI. These characteristics illustrate the blocking voltage for both transistor and diode.

Table XI. Power switches used in the PFC-boost converter.

C4D02120 CREE	SiC	1.2kV	4.5 A	V _{on} 1.4-1.9V	Q _c 11nC	
CMF20120D Semisouth	SiC	1.2kV	80mΩ (42A)	V _{th} 4V	V _g -5/+20V	Q _g 90nC

Note that the crucial element determining the final efficiency is the power transistor. Thus, a comparison among different Si MOSFETs and the SiC device CMF20120D has been first carried out in terms of losses estimation following the classical procedure described in [130]. The results of the comparison are shown in Fig. 42 for a current reference of 20 mA and four different output loads (30 kΩ, 40 kΩ, 50 kΩ, and 60 kΩ) corresponding respectively to four output voltages (600 V, 800 V, 1.0 kV, and 1.2 kV). It can be observed the predicted superior performance of the SiC device.

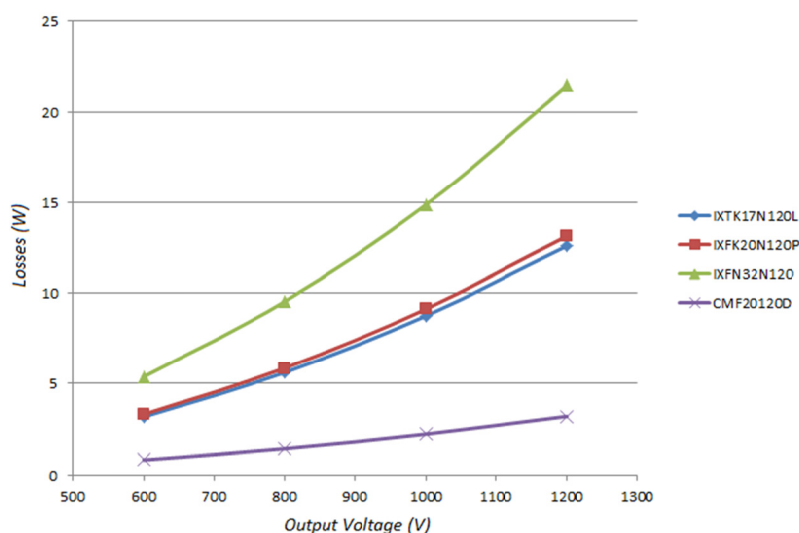


Fig 42. Losses comparison among Si and SiC devices.

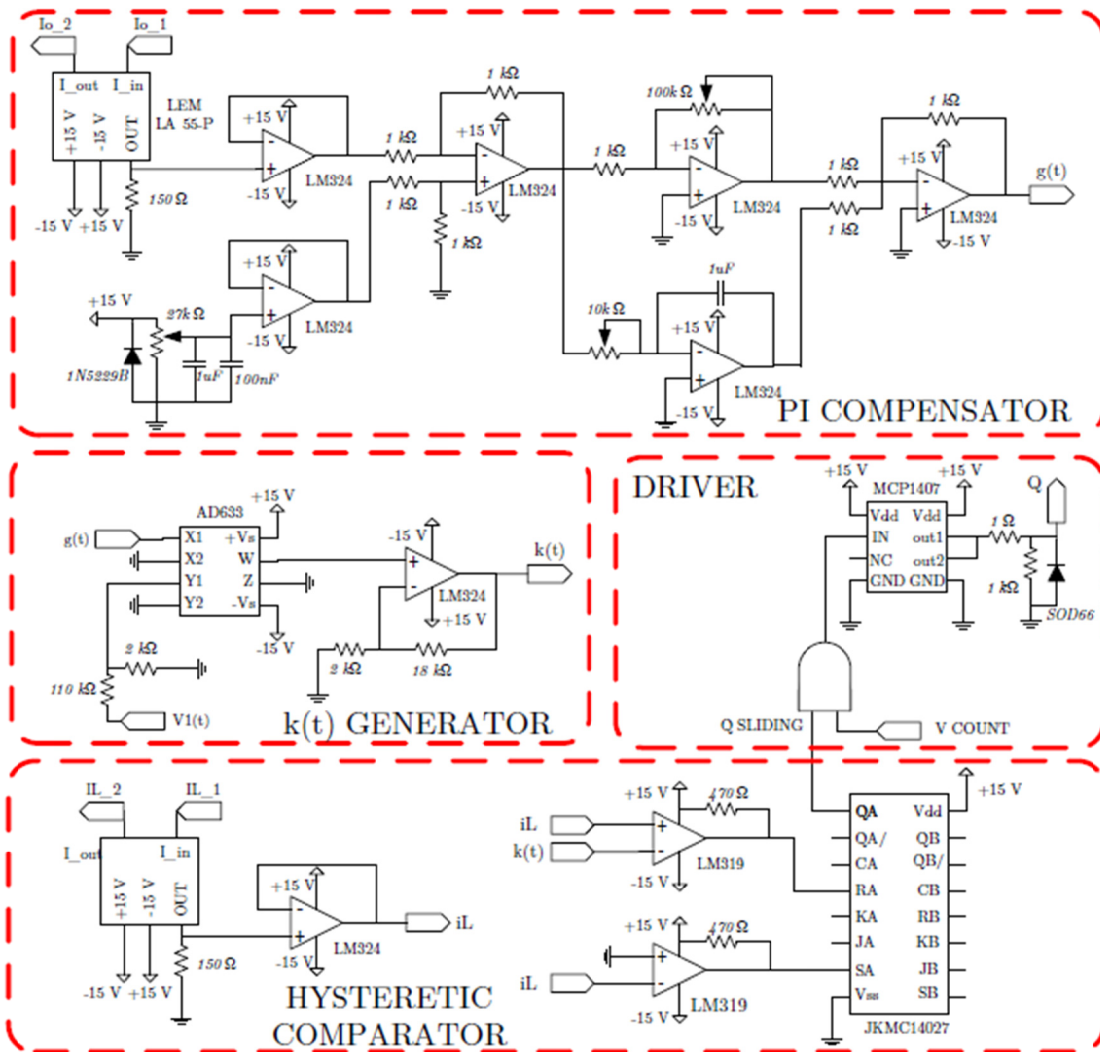


Fig 43. Detailed circuit implementation of the sliding mode control.

Also, the bridge rectifier used in this circuit is the silicon device PB3006-E3/45 from VISHAY capable to support 600 V, and 30 A respectively. The input series inductor of 1 mH has been realized with 20 wires of 0.07 mm² by making 120 turns around the ETD34/17/11-3C90 core with an air-gap of 5 μm, which has a relative permeability of 1740. Finally, at the converter output there are two capacitors in parallel of 8 μF capacitance, 8 mΩ equivalent series resistance (ESR) and 1.3 kV rated voltage each one.

2.3.4.2 Control stage.

Fig. 43 shows the practical implementation of the sliding mode controller, namely, *PI* compensator of the output current error, generation of the current reference $k(t)$, the hysteresis comparator, and finally the driver.

It is important to notice that input and output current measurements are made using two Hall-effect current sensors of the type LEM-LA-55P with a bandwidth of 200 kHz. Besides, it is important to remark that these current sensors are designed for high currents, and in this



application the currents are very low. For that reason, the wire corresponding to the input current has 27 turns to increase 27 times the measured value, and similarly the output current sensor has 44 turns.

On the one hand, the PI compensator has been implemented with a circuit based on LF347 operational amplifiers. The hysteretic circuit employs two LM319 comparators with a response time of 80 ns, and a JKMC14027 flip flop with a bandwidth of 13 MHz. On the other hand, the current reference $k(t)$ is obtained by means of an analogue multiplier AD633 with a slew rate of 20 V/ μ s. Finally, the low-side driver used to turn-on and turn-off the main switch is the IC MCP1407 capable to deliver a current peak of 6 A to the MOSFET with a maximum delay of 20 ns.

The inputs of the analogue multiplier are the signal $g(t)$, and the measured input rectified voltage $v_i(t)$, which are respectively given by the output of the PI compensator and the output of the resistor divider used to sense the input rectified voltage. The input of the hysteretic comparator are $k(t)$ and I_L , which are respectively given by the output of the analogue multiplier and the output of the input current measurement. The output of the hysteretic comparator is a digital signal ($Q_{SLIDING}$) which activates the driver through an AND gate, which is enabled by the V_{COUNT} signal. In normal operation V_{COUNT} is always activated while in burst mode is only activated during certain input current semi-cycles. The output of the AND gate provides the signal Q to turn on and turn off the power transistor in both operating modes.

2.3.4.3 Burst mode operation implementation.

The circuit implementation of the burst mode is shown in Fig. 44. This has been built using an AD629ANZ high common mode voltage differential amplifier with a bandwidth of 500 kHz, an LM319 comparator, a JKMC14027 flip-flop with a bandwidth of 13 MHz.

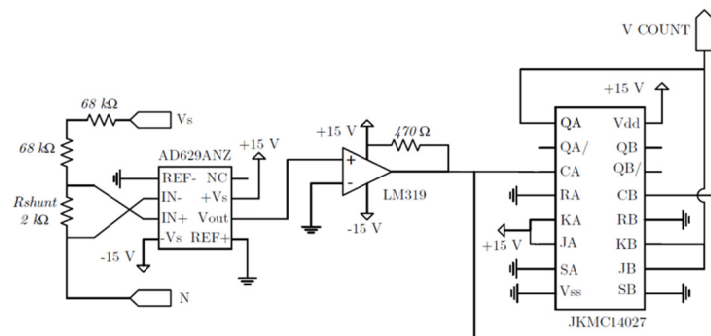


Fig 44. Detailed circuit implementation of the burst mode control.

2.3.5 Experimental results.

The power stage used in the experimental results, as well as, the implementation of the sliding mode control and the burst operation, are illustrated in Figs. 45, 46 (a) and 46 (b) respectively. Fig. 46 (c) shows both top and bottom sides of the LED array used in the tests.

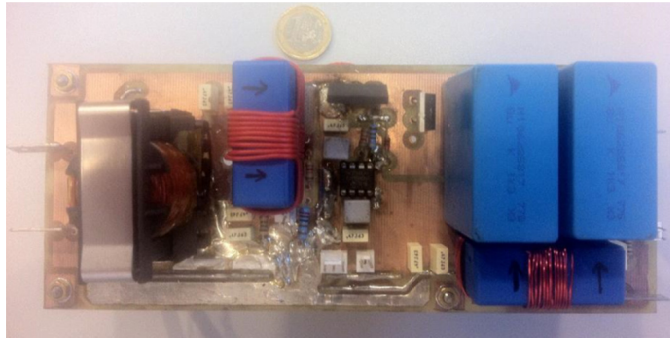
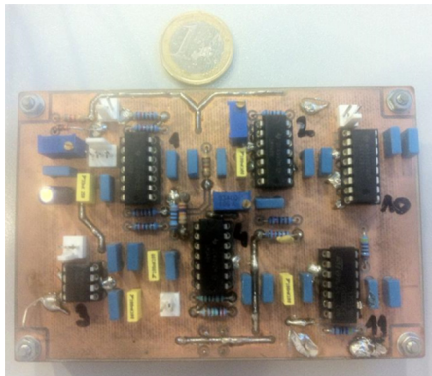


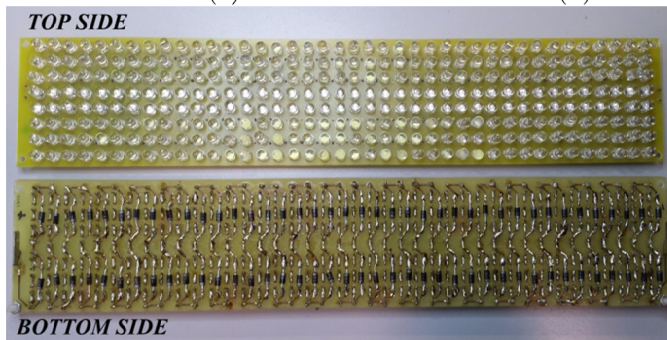
Fig 45. Single-stage PFC boost converter prototype.



(a)



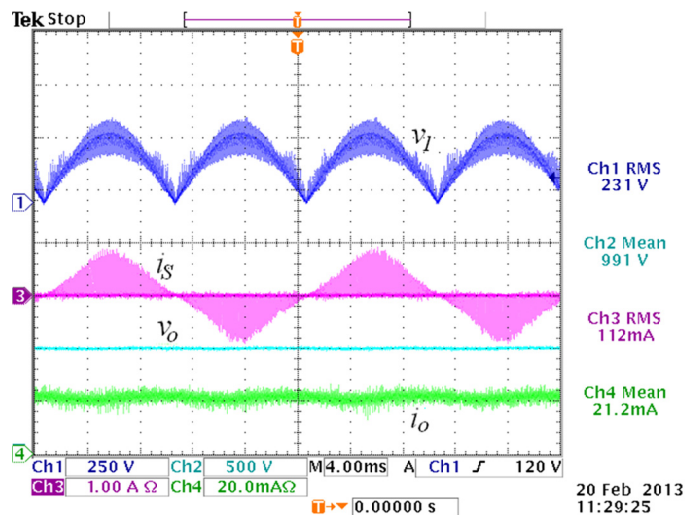
(b)



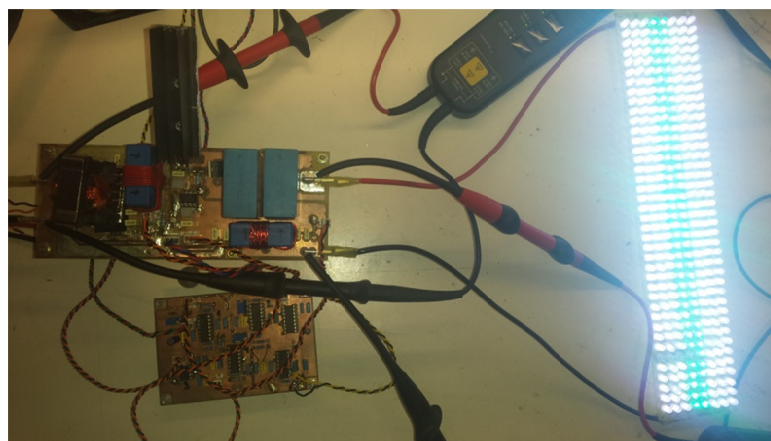
(c)

Fig 46. (a) Practical sliding mode control implementation. (b) Practical burst operation implementation
(c) LED array with bypass Zener on the bottom side.

Fig. 47 (a) shows the experimental results when a 320-LED spot based on conventional 5 mm diameter LED is connected to the output as depicted in Fig. 47 (b). In this specific case the output DC current (i_o) is controlled at 21.2 mA, and the corresponding voltage drop of the LEDs (v_o) is about 991 V. Moreover, the caption shows the rectified input voltage (v_i), and the grid current (i_s), showing that the input voltage and current are perfectly in phase working in the DCM-CCM boundary with an overall efficiency of 81%. Once the converter behaviour has been verified with the LED spot, the latter has been replaced by the a resistive load of 60 k Ω , absorbing the same current of the LEDs, in order to achieve high output voltages with the same level of current as illustrated in Fig. 48.



(a)



(b)

Fig 47. (a) Converter waveforms for a LED spot load. (b) Converter with LED spot-light

In Fig. 48 the input voltage (v_I) is the rectified grid-voltage of $230 V_{RMS}$, the input current (i_S) is again in phase with the input voltage and operates at the DCM-CCM boundary as expected. The measured output current is 19.1 mA, and the final output voltage is 1.145 kV. Observe that the MOSFET breakdown voltage is 1200 V, so that the final output current has been adjusted slightly below 20mA to avoid reaching the mentioned upper limit. In this case the output and input power of the converter are 21.85 W and 27.50 W respectively, so the overall efficiency of the converter is about 80%.

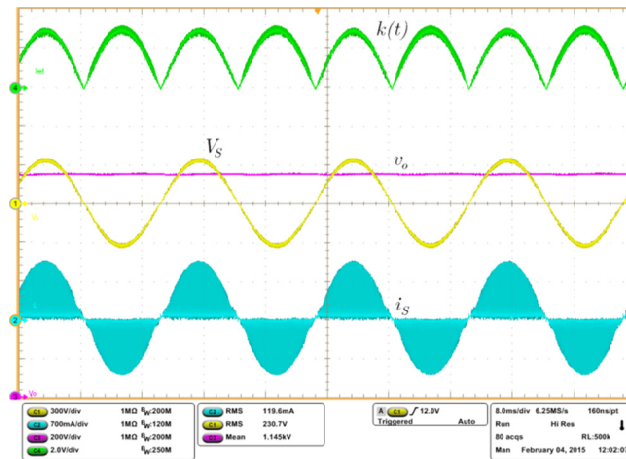


Fig 48. Converter waveforms for a 60 kΩ load.

Fig. 49 shows the harmonic content of the input current in normal mode, measured by a Tektronix MSO5204 Mixed Signal Oscilloscope with 2 GHz and 10 GS/s demonstrating the fulfilment of EMI standard IEC 61000-3-2 class C with a power factor of 0.945.

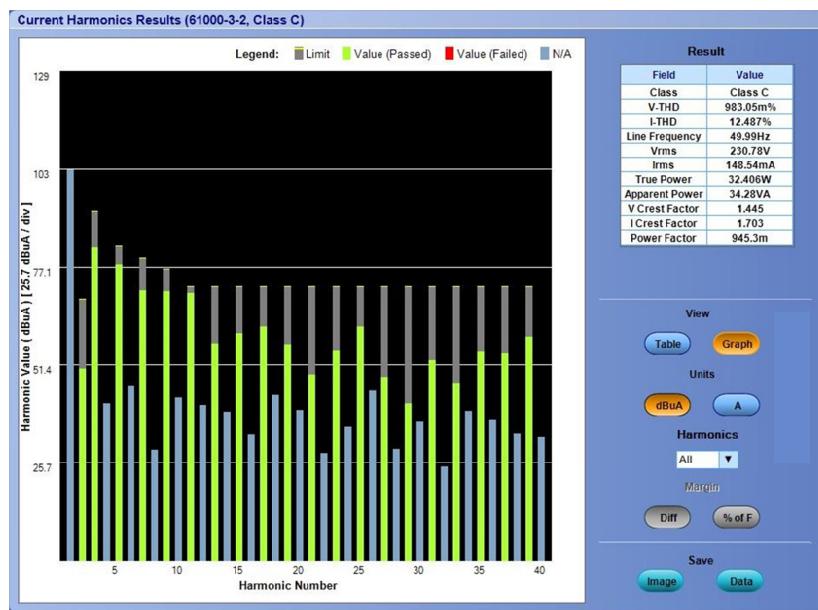


Fig 49. Input current harmonic content for a 60 kΩ resistive load in normal mode.

In order to improve the overall efficiency, Fig. 50 shows the experimental results when the burst mode is applied. As in the last experiment, the converter is loaded with a resistor of 60 kΩ, and in this particular case the output voltage (v_o) is about 1.154 kV, corresponding to an output current of 19.23 mA (i_o), and an output power of 22.19 W.

Furthermore, it is possible to see in the same figure the rectified input voltage (v_i) and the inductor current (i_L). As expected, due to the burst mode, the sliding mode control is acting only one of each two grid cycles in this case. This results in a reduction of the switching frequency in comparison with the one in Fig. 48. Hence, in this case the input current is about 101 mA, this resulting in an input power of 23.43 W, and an overall efficiency of 94%. As in the



previous case, Fig. 51, shows the harmonic content in the input current when the converter is working in burst mode. As expected, the converter is accomplishing the IEC 61000-3-2 Class C EMI standard. Notice that concerning the experimental value of the power factor depicted in Fig. 49, the measurement in burst mode does not correspond to the actual value of the power factor because the automatic measurement procedure of Tektronix MSO5204 Mixed Signal Oscilloscope is carried out without considering that there is no input current in one of each two cycles.

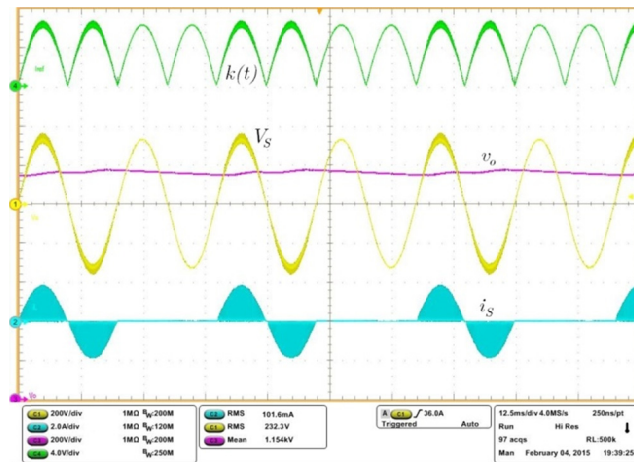


Fig 50. Converter waveforms with burst operation for a 60 kΩ load.

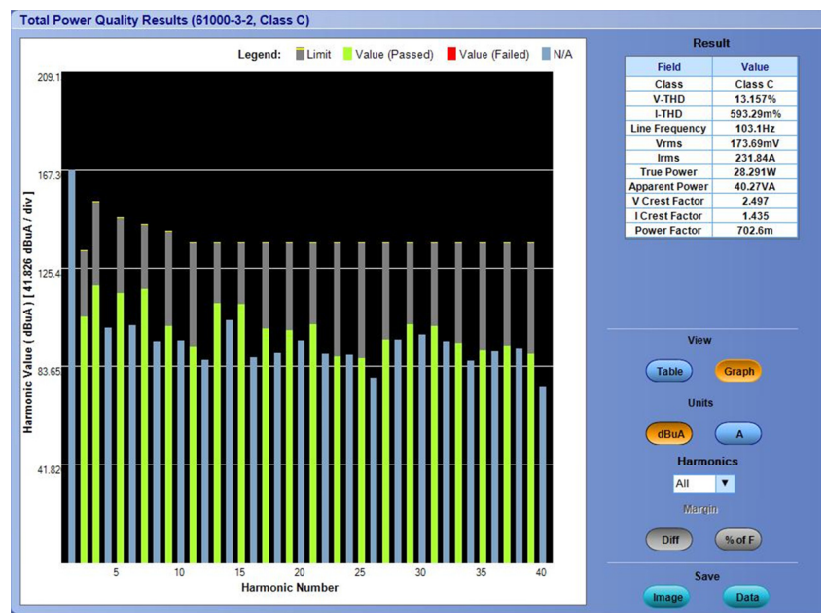


Fig 51. Input current harmonic content for a 60 kΩ resistive load in burst mode.

Finally, Figs. 52 to 55 show the converter response to input voltage variation of different nature, which had been introduced in the system by means of the UPC Pacific Smart Source model 360 AMC POWER SOURCE. It is worth noting that in all cases the output voltage remains at the expected value of 1.0 kV for a 50 kΩ output load and an output current



reference of 20 mA, in spite of the strong variations of different nature in the input voltage waveform. Also the PFC feature is preserved in all the experiments.

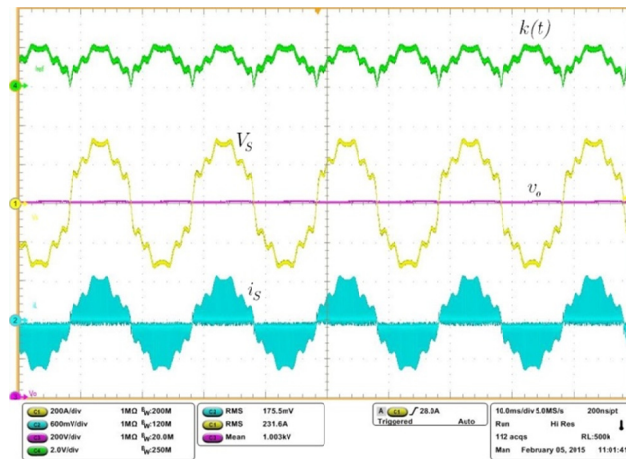


Fig 52. Converter response for input voltage variations IEC 77A Class 2.

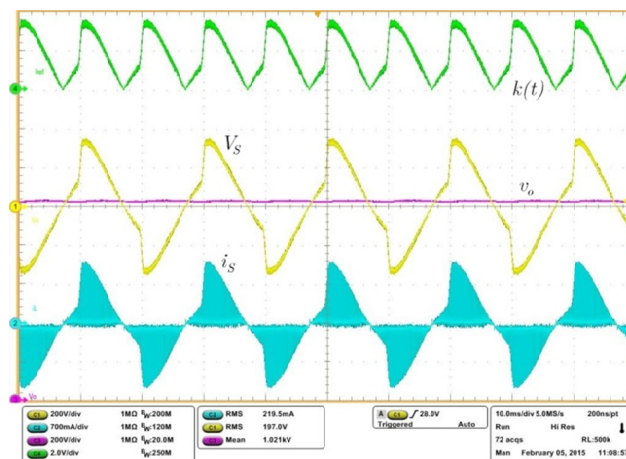


Fig 53. Converter response for input voltage variations of triangular type.

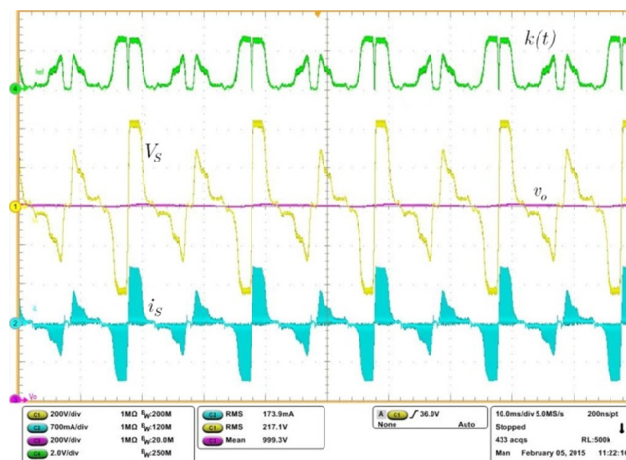
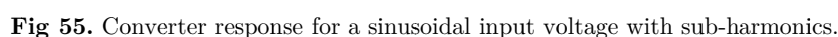


Fig 54. Converter response for a highly distorted input voltage.



A single-stage boost PFC implemented with SiC devices has been implemented and tested for on-grid LED lighting applications. The system operates at the boundary of CCM and DCM to make compatible a high output voltage load and a high duty cycle operation with minimum switching losses. The proposed solution is based on the use of sliding-mode control to impose a quasi LFR behaviour at the input port for PFC correction and to regulate at the same time the output current. The experimental results are in good agreement with the theoretical predictions. The main switch has been implemented with SiC devices, with a resulting efficiency around 85%. It has been also shown that the efficiency of the converter can be significantly improved up to 94% using a burst operation, in which the switching frequency of the converter has been reduced without changing the inductor value, and without modifying the output voltage ripple. Therefore, this kind of converter is a good solution to supply high-voltage low-power loads, like in LED lighting applications. A future work contemplates obtaining the optimal values of k_P and k_i using robust control criteria in the dynamic model presented in Fig.37 in order to derive the best trade-off between the PFC and the output current control.



3 Dimmable Electronic ballast based on Loss-Free Resistor (LFR) approach to supply High-Intensity Discharge (HID) Lamps.

Now the LFR concept is used to control the power delivered to different types of HID lamps as metal halide, vapour sodium and mercury vapour discharge lamps. This chapter is divided in two sections.

The first section presents a two stage ballast to supply an HID lamp in DC current. The first stage is a boost converter with LFR behaviour. In the second stage, a switched capacitor boost converter is used to ignite the lamp. The ballast has two operation modes, the ignition operation, where the two converters are connected in cascade with the same control signal, and the warm-up and steady-state operation where only the boost converter is working. During the ignition operation the ballast is able to reach a voltage of 6 kV from 12 V batteries. Among the ballast advantages it is worth mentioning the absence of light flickering, warm-up time reduction, no aging effects on lamp power, easy dimming control, and absence of acoustic resonances (AR). The ballast dynamics in both operation modes is analysed by means of sliding mode control showing the stability of the proposed ballast. The results with diverse HID lamps of 250 W demonstrate experimentally the feasibility of the proposed approach, where extreme voltage gains are achieved without a transformer and different HID lamps are supplied in steady- state with stable operation.

The second section reports a two-stage high-frequency electronic ballast supplied from a low DC voltage (12 V – 14 V) with Loss-Free Resistor (LFR) behaviour for High Intensity Discharge (HID) lamps. By means of a resonant ignitor, the lamp is started-up at high-frequency. To avoid the Acoustic Resonances (AR) at steady state operation, the lamp is supplied with a HFSW above the AR (~ 100 kHz). An FPGA digital controller is employed in the ballast for diverse purposes: first, to implement easily the sliding mode control law that ensures system stability and the LFR behaviour of the electronic ballast, delivering always the desired power to the lamp with dimming capability. The second task of the FPGA is to perform the high frequency ignition sequence for the full bridge resonant inverter, and after the ignition, to supply the lamp at high-frequency (~ 100 kHz) for warm-up and for steady- state operation avoiding the acoustic resonances. The lamp start-up, warm-up and steady-state operation has been verified loading the ballast with an HID lamp showing perfect agreement with the theoretical predictions.



3.1 Battery-Supplied DC-ballast for high Intensity Discharge (HID) Lamps.

As previously mentioned in the section 1.3, one solution to supply HID lamps avoiding AR is supplying the lamp with a DC current. Consequently, this work presents a LFR-based DC ballast using a double stage converter, as shown in the block diagram of Figs. 56 and 57.

The ignition circuit is performed by a boost converter with LFR behaviour connected in cascade with a switched capacitor boost converter. This second stage only works when the lamp is off and requires a high voltage switch (4 kV IGBT). Once the lamp is started, only the first converter is operating, and the second one is bypassed by a relay avoiding the losses in steady-state operation. Although the relay is an electro-mechanic device, submitted to fatigue, and therefore susceptible of both unpredictable and premature failures, there is no semiconductor-based switching device with lower losses ($r_{ON} < 150 \Omega$), and equivalent breakdown voltage (10 kV).

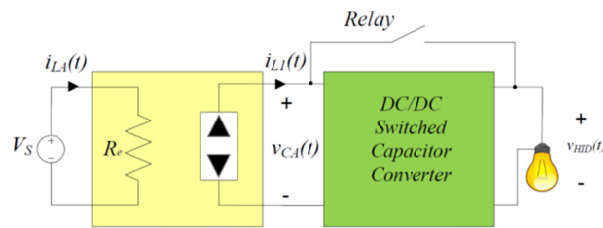


Fig 56. Block diagram of the LFR-based ballast.

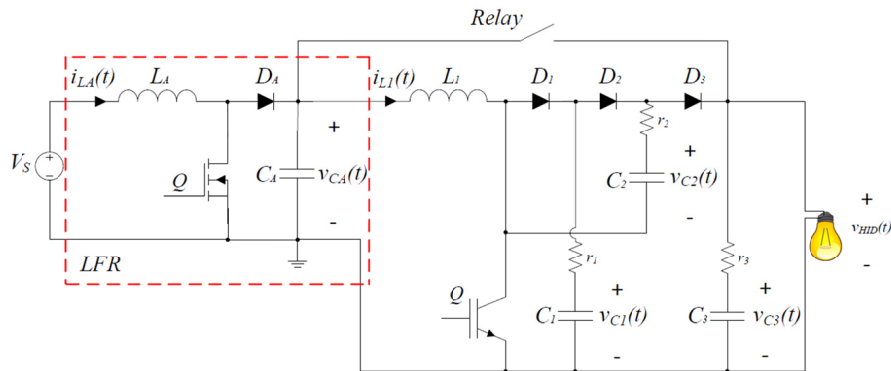


Fig 57. DC Electronic Ballast with LFR behaviour for HID Lamps.

3.1.1 DC-Electronic Ballast description and analysis.

This section presents the two operation modes of the electronic ballast, and its analysis by means of sliding mode control. The ballast dynamics including system stability are presented in both operation modes when a lamp is connected in the ballast output.

3.1.1.1 Ignition operation description and stability analysis.

During the start-up mode, both switching converters are connected in cascade, sharing the same control signal (Q) and duty ratio. The resulting connexion of the two converters has



an ideal gain given by (84). Once the converter is connected with the power supply, the lamp voltage starts to increase, until the spark is generated, and the lamp is turned ON. At this moment, the switched capacitor converter is bypassed and only the first converter is operating delivering the selected power to the lamp.

$$\frac{V_{HID}}{V_s} = \frac{2}{(1-D)^2} \quad (84)$$

If in the start-up transient the lamp voltage reaches 6 kV and no spark is produced, because the lamp is hot or malfunctioning, the converter stops and the output voltage is decreased by the parasitic elements of the ballast until a certain low voltage is reached. Then, both converters operate again trying a second start.

In this start-up operation mode the converter is controlled by means of sliding- mode control with the control surface that appears in (85), where the current through L_A is never zero, this means that no discontinuous modes appear in this inductor. Besides, as $L \gg L_A$ by design, the second inductor L also operates in CCM.

$$s(x) = i_{LA} - k(t) \quad (85)$$

where $k(t) = g(t) \cdot v_s(t)$

As the switch S_2 is an IGBT device, the converter must operate at low frequency ($f_s \approx 6$ kHz). Then, depending on the time constants determined by capacitors C_1 to C_3 and their respective ESR resistances r_1 to r_3 , two discontinuous modes appear caused by D_1 and D_2 . Thus depending on the capacitor values and the switching frequency the converter can have 2 or 4 topologies. In this specific case, as we want to minimize the energy stored in the capacitor for user safety, and reducing the capacitor size, the converter has four different topologies. The sequences of theses topologies or conduction states are shown in Fig. 58.

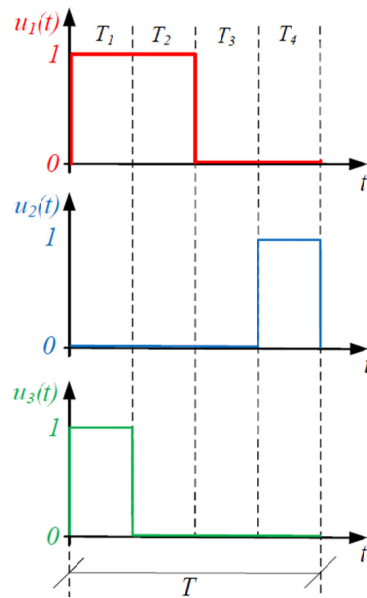


Fig 58. Sequence of ballast conduction states.



Roughly speaking, the switching of a diode is natural, unforced, so the change from one topology to another is produced only when the current through it is zero. Although these state changes are not forced, we can model them considering that the state changes generated by D_1 and D_2 are governed by the control signals $u_2(t)$ and $u_3(t)$ respectively. These control signals will take “ $u=1$ ” if the diode is conducting, and “ $u=0$ ” if the diodes are blocked. The remaining control signal $u_1(t)$ is controlled by the switching surface.

Therefore, the converter in start-up operation depicted in Fig. 59 has the four topologies shown in Fig. 60 to Fig. 63. The respective matrices A_1 to A_4 , and the corresponding excitation vectors B_1 to B_4 are given in (87)-(90), where the state vector appears in (86). Notice that we have considered that $C_3=C_2=C_1$, and $r_3=r_2=r_1$ in the switched capacitor stage for simplicity.

$$X = [i_{LA} \quad v_{CA} \quad i_L \quad v_{C1} \quad v_{C2} \quad v_{C3}]^T \quad (86)$$

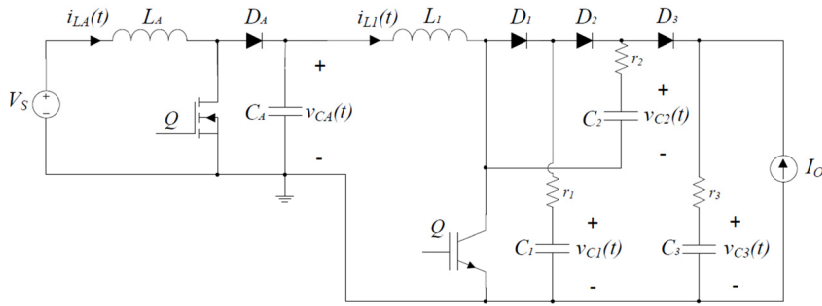


Fig 59. DC Electronic Ballast in start-up operation.

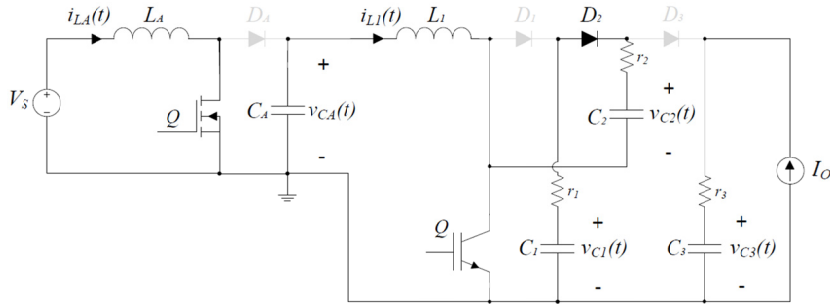


Fig 60. Topology A of the DC Electronic Ballast in start-up operation.

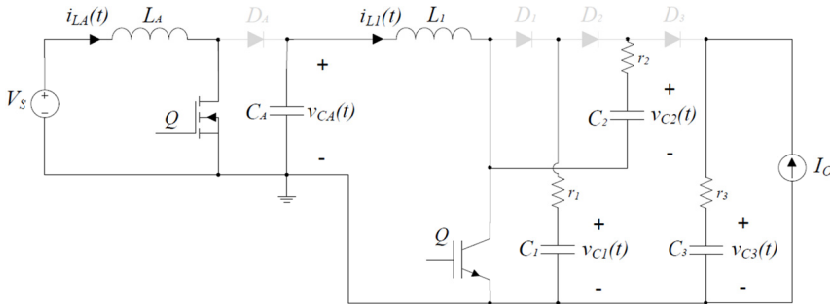


Fig 61. Topology B of the DC Electronic Ballast in start-up operation.

Dimmable Electronic ballast based on Loss-Free Resistor (LFR) approach to supply High-Intensity Discharge (HID) Lamps.

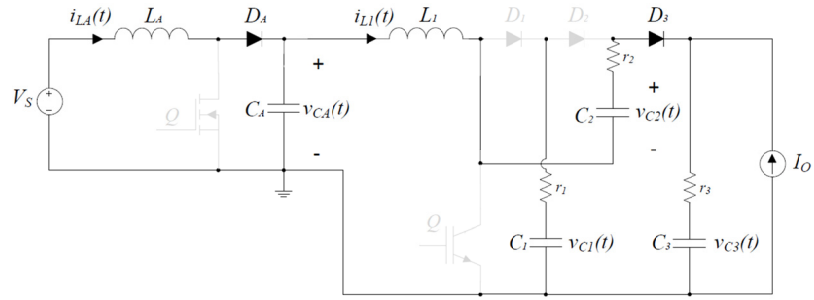


Fig 62. Topology C of the DC Electronic Ballast in start-up operation.

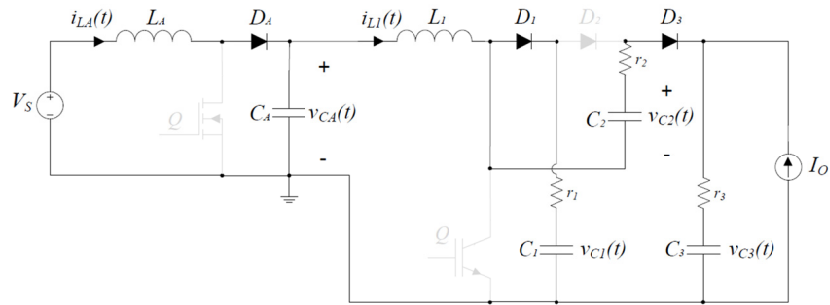


Fig 63. Topology D of the DC Electronic Ballast in start-up operation.

Observe that I_o represents the current delivered by the DC Electronic ballast to the HID lamp.

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_A} & 0 & 0 & 0 \\ 0 & \frac{1}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{2 \cdot r \cdot C} & \frac{1}{2 \cdot r \cdot C} & 0 \\ 0 & 0 & 0 & \frac{1}{2 \cdot r \cdot C} & -\frac{1}{2 \cdot r \cdot C} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{V_s}{L_A} \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{I_o}{C} \end{bmatrix} \quad (87)$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_A} & 0 & 0 & 0 \\ 0 & \frac{1}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{V_s}{L_A} \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{I_o}{C} \end{bmatrix} \quad (88)$$



$$A_3 = \begin{bmatrix} 0 & -\frac{1}{L_A} & 0 & 0 & 0 & 0 \\ \frac{1}{C_A} & 0 & -\frac{1}{C_A} & 0 & 0 & 0 \\ 0 & \frac{1}{L} & -\frac{r}{L} & 0 & \frac{1}{L} & \frac{1}{L} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \quad B_3 = \begin{bmatrix} \frac{V_s}{L_A} \\ 0 \\ -\frac{r \cdot I_o}{L} \\ 0 \\ 0 \\ \frac{I_o}{C} \end{bmatrix} \quad (89)$$

$$A_4 = \begin{bmatrix} 0 & -\frac{1}{L_A} & 0 & 0 & 0 & 0 \\ \frac{1}{C_A} & 0 & -\frac{1}{C_A} & 0 & 0 & 0 \\ 0 & \frac{1}{L} & \frac{2 \cdot r}{3 \cdot L} & \frac{2}{3 \cdot r \cdot L} & \frac{1}{3 \cdot r \cdot L} & \frac{1}{3 \cdot L} \\ 0 & 0 & \frac{2}{3 \cdot C} & -\frac{1}{3 \cdot r \cdot C} & \frac{1}{3 \cdot r \cdot C} & \frac{1}{3 \cdot r \cdot C} \\ 0 & 0 & -\frac{1}{3 \cdot C} & -\frac{1}{3 \cdot r \cdot C} & \frac{1}{3 \cdot r \cdot C} & \frac{1}{3 \cdot r \cdot C} \\ 0 & 0 & \frac{1}{3 \cdot C} & \frac{1}{3 \cdot r \cdot C} & -\frac{1}{3 \cdot r \cdot C} & -\frac{1}{3 \cdot r \cdot C} \end{bmatrix} \quad B_4 = \begin{bmatrix} \frac{V_s}{L_A} \\ 0 \\ -\frac{I_o \cdot r}{3 \cdot L} \\ \frac{I_o}{3 \cdot C} \\ \frac{I_o}{3 \cdot C} \\ \frac{2 \cdot I_o}{3 \cdot C} \end{bmatrix} \quad (90)$$

The control technique applied to the ballast implies the establishment of a sliding control surface to force the input current (85) to track a slow varying constant “ $k(t)$ ”.

The study the sliding-mode control in a converter follows the standard methodology. The presence of four topologies and three control signals yield

$$\dot{X} = F(X) + N(X)U \quad (91)$$

where

$$F(X) = A_4 \cdot X + B_4 \quad (92)$$

$$N(X) = \left[(A_1 - A_4) X + (B_1 - B_4) , (A_2 - A_4) X + (B_2 - B_4) , (A_3 - A_4) X + (B_3 - B_4) \right] \quad (93)$$

$$U = \begin{bmatrix} u_1 & u_2 & u_3 \end{bmatrix}^T \quad (94)$$

Now we define a tri-dimensional surface because we have three control components. Two of these dimensions are referred to the discontinuous modes that appears in D_2 and D_1 determining the change from the first topology to the second, and the change from the third topology to the fourth. The dimension referred to the input current allows the control of the system.

$$\sigma(x, t) = \begin{bmatrix} \underbrace{i_{LA} - k(t)}_{u_1} & \underbrace{v_{C1} - v_{C2}}_{u_2} & \underbrace{v_{C3} - v_{C2} - v_{C1}}_{u_3} \end{bmatrix} \quad (95)$$



Now, it is important to remark that the sliding mode analysis will be performed in two steps. First of all, we will find an equilibrium point corresponding to a constant input voltage V_s and a constant value G of $g(t)$ in the control loop. Subsequently, we will consider the influence of the time varying components $v_s(t)$ and $g(t)$ as low-frequency superposed signals on the corresponding constant values V_s and G . The contribution of the superposed signals will be predicted by a model derived by linearizing the ideal sliding dynamics around the equilibrium point previously obtained.

Therefore, the resulting equivalent control for $S(x)=i_{LA}-G \cdot V_s$ (96) is presented in (97)

$$\sigma(x, t) = \begin{bmatrix} \underbrace{i_{LA} - G \cdot V_s}_{u_1} & \underbrace{v_{C1} - v_{C2}}_{u_2} & \underbrace{v_{C3} - v_{C2} - v_{C1}}_{u_3} \end{bmatrix} \quad (96)$$

$$U_{eq} = -\{J[\sigma(X)] \cdot N(X)\}^{-1} \cdot \{J[\sigma(X)] \cdot F(X)\} \quad (97)$$

By means of mathematic manipulations, the equivalent control components, and the corresponding sliding dynamics are given by the expressions (98) to (104) respectively.

$$U_{eq} = \begin{bmatrix} \frac{r \cdot I_L \cdot V_s}{V_{CA} \cdot (V_{C1} - V_{C2})} \\ -\frac{V_s \cdot (I_L \cdot r + V_{C1} - V_{C2}) + V_{CA} \cdot (V_{C2} - V_{C1})}{V_{CA} \cdot (V_{C1} - V_{C2})} \\ \frac{V_s \cdot (I_O \cdot r + V_{C3} + V_{C2} - V_{C1}) - V_{CA} \cdot r \cdot I_O}{V_{CA} \cdot (r \cdot I_O + 2 \cdot I_L \cdot r - V_{C1} + V_{C2} + V_{C3})} \end{bmatrix} \quad (98)$$

$$\frac{di_{LA}}{dt} = 0 \quad (99)$$

$$\frac{dv_{CA}}{dt} = \frac{G \cdot V_s^2 - v_{CA} \cdot i_L}{v_{CA} \cdot C_A} \quad (100)$$

$$\frac{di_L}{dt} = \frac{v_{CA}^2 - v_{C1} \cdot V_s}{v_{CA} \cdot C} \quad (101)$$

$$\frac{dv_{C1}}{dt} = \frac{1}{6} \cdot \frac{2 \cdot I_O \cdot v_{CA} + i_L \cdot V_s}{v_{CA} \cdot C} \quad (102)$$

$$\frac{dv_{C2}}{dt} = \frac{1}{6} \cdot \frac{2 \cdot I_O \cdot v_{CA} + i_L \cdot V_s}{v_{CA} \cdot C} \quad (103)$$

$$\frac{dv_{C3}}{dt} = \frac{1}{3} \cdot \frac{2 \cdot I_O \cdot v_{CA} + i_L \cdot V_s}{v_{CA} \cdot C} \quad (104)$$

Therefore the coordinates of the equilibrium point $X^*=[I_{LA}^* \ V_{CA}^* \ I_L^* \ V_{C1}^* \ V_{C2}^* \ V_{C3}^*]$ are given by (105) to (110) respectively. Since the current delivered to the lamp (I_{HID}) has the opposite direction of I_O , because $I_O < 0$ we consider that $-I_O = I_{HID}$.

$$I_{LA}^* = G \cdot V_s \quad (105)$$



$$V_{CA}^* = \frac{G \cdot V_s^2}{\sqrt{2(-I_o) \cdot G \cdot V_s}} = \frac{G \cdot V_s^2}{\sqrt{2I_{HID} \cdot G \cdot V_s}} \quad (106)$$

$$I_L^* = \sqrt{2(-I_o) \cdot G \cdot V_s} = \sqrt{2I_{HID} \cdot G \cdot V_s} \quad (107)$$

$$V_{C1}^* = \frac{G \cdot V_s^2}{2(-I_o)} = \frac{G \cdot V_s^2}{2I_{HID}} \quad (108)$$

$$V_{C2}^* = \frac{G \cdot V_s^2}{2(-I_o)} = \frac{G \cdot V_s^2}{2I_{HID}} \quad (109)$$

$$V_{C3}^* = \frac{G \cdot V_s^2}{(-I_o)} = \frac{G \cdot V_s^2}{I_{HID}} \quad (110)$$

Assuming now that $k(t)$ is time varying, the corresponding equivalent control is calculated by

$$U_{eq} = -\left\{J[\sigma(X)] \cdot N(X)\right\}^{-1} \cdot \left\{J[\sigma(X)] \cdot F(X) + \frac{d\sigma(X)}{dt}\right\} \quad (111)$$

where

$$\frac{d\sigma(X)}{dt} = \begin{bmatrix} g(t) \cdot \frac{dv_s(t)}{dt} + v_s(t) \cdot \frac{dg(t)}{dt} \\ 0 \\ 0 \end{bmatrix} \quad (112)$$

Therefore, the ideal sliding dynamics can be expressed as (113)-(118)

$$\frac{di_{LA}}{dt} = g(t) \cdot \frac{dv_s(t)}{dt} + v_s(t) \cdot \frac{dg(t)}{dt} \quad (113)$$

$$\frac{dv_{CA}}{dt} = \frac{g^2(t) v_s(t) L_A \frac{dv_s(t)}{dt} + g(t) v_s^2(t) L_A \frac{dg(t)}{dt} + g(t) v_s^2(t) - v_{CA} i_L(t)}{v_{CA} C_A} \quad (114)$$

$$\begin{aligned} \frac{di_L}{dt} = & \frac{v_{CA}^2(t) v_{C3}(t) v_s(t) L_A \frac{dg(t)}{dt} + v_{C3}(t) v_s(t) - v_{C3}(t) g(t) L_A \frac{dv_s(t)}{dt}}{v_{CA} L} + \\ & + \frac{v_{C1}(t) g(t) L_A \frac{dv_s(t)}{dt} + v_{C1}(t) v_s(t) L_A \frac{dg(t)}{dt} + v_{C1}(t) v_s(t)}{v_{CA} L} \end{aligned} \quad (115)$$

$$\frac{dv_{C1}}{dt} = \frac{1}{6} \frac{i_L(t) v_s(t) + 2 i_o(t) v_{CA} + i_L(t) g(t) L_A \frac{dv_s(t)}{dt} + i_L(t) v_s(t) L_A \frac{dg(t)}{dt}}{v_{CA} C} \quad (116)$$



$$\frac{dv_{C2}}{dt} = \frac{1}{6} \frac{i_L(t)v_s(t) + 2i_o(t)v_{CA} + i_L(t)g(t)L_A \frac{dv_s(t)}{dt} + i_L(t)v_s(t)L_A \frac{dg(t)}{dt}}{v_{CA}C} \quad (117)$$

$$\frac{dv_{C3}}{dt} = \frac{1}{3} \frac{i_L(t)v_s(t) + 2i_o(t)v_{CA} + i_L(t)g(t)L_A \frac{dv_s(t)}{dt} + i_L(t)v_s(t)L_A \frac{dg(t)}{dt}}{v_{CA}C} \quad (118)$$

assuming that

$$g(t) = G + \hat{g}(t) \quad (119)$$

$$v_s(t) = V_s + \hat{v}_s(t) \quad (120)$$

$$v_{CA}(t) = V_{CA} + \hat{v}_{CA}(t) \quad (121)$$

$$i_L(t) = I_L + \hat{i}_L(t) \quad (122)$$

$$v_{C1}(t) = V_{C1} + \hat{v}_{C1}(t) \quad (123)$$

$$v_{C2}(t) = V_{C2} + \hat{v}_{C2}(t) \quad (124)$$

$$v_{C3}(t) = V_{C3} + \hat{v}_{C3}(t) \quad (125)$$

and linearizing the equations (114)(115)(116) and (118) around the equilibrium point $X^* = [I_{LA}^* \ V_{CA}^* \ I_L^* \ V_{C1}^* \ V_{C2}^* \ V_{C3}^*]$ lead to the following expressions

$$\frac{dv_{CA}}{dt} = a\hat{g}(t) + b\frac{d\hat{g}(t)}{dt} + c\hat{v}_s(t) + d\frac{d\hat{v}_s(t)}{dt} + e\hat{v}_{CA}(t) + f\hat{i}_L(t) = f_1(t) \quad (126)$$

$$\frac{di_L}{dt} = h\hat{g}(t) + i\frac{d\hat{g}(t)}{dt} + j\hat{v}_s(t) + k\frac{d\hat{v}_s(t)}{dt} + l\hat{v}_{CA}(t) + m\hat{v}_{C1}(t) + n\hat{v}_{C3}(t) = f_2(t) \quad (127)$$

$$\frac{dv_{C1}}{dt} = o\hat{g}(t) + p\frac{d\hat{g}(t)}{dt} + q\hat{v}_s(t) + r\frac{d\hat{v}_s(t)}{dt} + t\hat{i}_o(t) + v\hat{v}_{CA}(t) + w\hat{i}_L(t) = f_3(t) \quad (128)$$

$$\frac{dv_{C3}}{dt} = x\hat{g}(t) + y\frac{d\hat{g}(t)}{dt} + z\hat{v}_s(t) + \alpha\frac{d\hat{v}_s(t)}{dt} + \beta\hat{i}_o(t) + \varepsilon\hat{v}_{CA}(t) + \tau\hat{i}_L(t) = f_4(t) \quad (129)$$

where coefficients $a, b, c, d, e, f, h, i, j, k, l, m, n, o, p, q, r, t, v, w, x, y, z, \alpha, \beta, \varepsilon$, and τ are given by the expressions (130) to (156) respectively.

$$a = \left. \frac{\delta f_1(t)}{\delta g(t)} \right|_{X^*} = \frac{\sqrt{2 \cdot I_{HID} \cdot G \cdot V_s}}{G \cdot C_A} \quad (130)$$

$$b = \left. \frac{\delta f_1(t)}{\delta \frac{dg(t)}{dt}} \right|_{X^*} = \frac{L_A}{C_A} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (131)$$

$$c = \left. \frac{\delta f_1(t)}{\delta v_s(t)} \right|_{X^*} = \frac{2}{V_s \cdot C_A} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (132)$$



$$d = \left. \frac{\delta f_1(t)}{\delta \frac{dv_s(t)}{dt}} \right|_{X^*} = \frac{G \cdot L_A}{V_s \cdot C_A} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (133)$$

$$e = \left. \frac{\delta f_1(t)}{\delta v_{CA}(t)} \right|_{X^*} = -\frac{2 \cdot I_{HID}}{V_s \cdot C_A} \quad (134)$$

$$f = \left. \frac{\delta f_1(t)}{\delta i_L(t)} \right|_{X^*} = -\frac{1}{C_A} \quad (135)$$

$$h = \left. \frac{\delta f_2(t)}{\delta g(t)} \right|_{X^*} = 0 \quad (136)$$

$$i = \left. \frac{\delta f_2(t)}{\delta \frac{dg(t)}{dt}} \right|_{X^*} = -\frac{V_s \cdot L_A}{2 \cdot L \cdot I_{HID}} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (137)$$

$$j = \left. \frac{\delta f_2(t)}{\delta v_s(t)} \right|_{X^*} = -\frac{1}{2 \cdot L \cdot I_{HID}} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (138)$$

$$k = \left. \frac{\delta f_2(t)}{\delta \frac{dv_s(t)}{dt}} \right|_{X^*} = -\frac{G \cdot L_A}{2 \cdot I_{HID} \cdot L} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (139)$$

$$l = \left. \frac{\delta f_2(t)}{\delta v_{CA}(t)} \right|_{X^*} = \frac{2}{L} \quad (140)$$

$$m = \left. \frac{\delta f_2(t)}{\delta v_{C1}(t)} \right|_{X^*} = \frac{1}{V_s \cdot G \cdot L} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (141)$$

$$n = \left. \frac{\delta f_2(t)}{\delta v_{C3}(t)} \right|_{X^*} = -\frac{1}{V_s \cdot G \cdot L} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (142)$$

$$o = \left. \frac{\delta f_3(t)}{\delta g(t)} \right|_{X^*} = 0 \quad (143)$$

$$p = \left. \frac{\delta f_3(t)}{\delta \frac{dg(t)}{dt}} \right|_{X^*} = \frac{I_{HID} \cdot L_A}{3 \cdot C} \quad (144)$$

$$q = \left. \frac{\delta f_3(t)}{\delta v_s(t)} \right|_{X^*} = \frac{1}{3} \cdot \frac{I_{HID}}{V_s \cdot C} \quad (145)$$



$$r = \left. \frac{\delta f_3(t)}{\delta \frac{dv_s(t)}{dt}} \right|_{X^*} = \frac{1}{3} \cdot \frac{L_A \cdot I_{HID} \cdot G}{V_s \cdot C} \quad (146)$$

$$t = \left. \frac{\delta f_3(t)}{\delta i_o(t)} \right|_{X^*} = \frac{1}{3C} \quad (147)$$

$$v = \left. \frac{\delta f_3(t)}{\delta v_{CA}(t)} \right|_{X^*} = -\frac{1}{3 \cdot G \cdot C \cdot V_s^2} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (148)$$

$$w = \left. \frac{\delta f_3(t)}{\delta i_L(t)} \right|_{X^*} = \frac{1}{6 \cdot G \cdot C \cdot V_s} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (149)$$

$$x = \left. \frac{\delta f_4(t)}{\delta g(t)} \right|_{X^*} = 0 \quad (150)$$

$$y = \left. \frac{\delta f_4(t)}{\delta \frac{dg(t)}{dt}} \right|_{X^*} = \frac{2 \cdot I_{HID} \cdot L_A}{3 \cdot C} \quad (151)$$

$$z = \left. \frac{\delta f_3(t)}{\delta v_s(t)} \right|_{X^*} = \frac{2}{3} \cdot \frac{I_{HID}}{V_s \cdot C} \quad (152)$$

$$\alpha = \left. \frac{\delta f_3(t)}{\delta \frac{dv_s(t)}{dt}} \right|_{X^*} = \frac{2}{3} \cdot \frac{L_A \cdot I_{HID} \cdot G}{V_s \cdot C} \quad (153)$$

$$\beta = \left. \frac{\delta f_4(t)}{\delta i_o(t)} \right|_{X^*} = \frac{2}{3 \cdot C} \quad (154)$$

$$\varepsilon = \left. \frac{\delta f_4(t)}{\delta v_{CA}(t)} \right|_{X^*} = -\frac{2}{3 \cdot G \cdot C \cdot V_s^2} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (155)$$

$$\tau = \left. \frac{\delta f_4(t)}{\delta i_L(t)} \right|_{X^*} = \frac{1}{6 \cdot G \cdot C \cdot V_s} \cdot \sqrt{2 \cdot I_{HID} \cdot G \cdot V_s} \quad (156)$$

Fig. 64 shows the dynamic model of the boost converter in cascade with the switched capacitor converter presented in Fig. 59, controlled by means of sliding mode control with LFR behaviour.

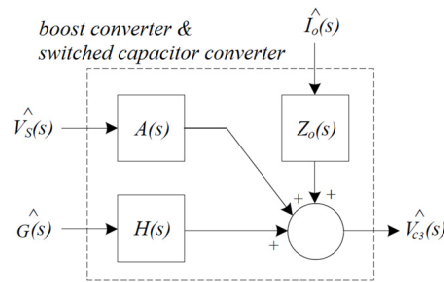


Fig 64. Dynamic model of the switched converter.

Hence,

$$H(s) = \frac{\hat{V}_{C3}(s)}{\hat{G}(s)} \bigg|_{\substack{\hat{v}_s(t)=0 \\ \hat{i}_o(t)=0}} = \frac{s^3 \cdot \left(\frac{2 \cdot I_{HID} \cdot L_A}{3 \cdot C} \right) - s^2 \cdot \left(\frac{2 \cdot V_S \cdot L_A}{C \cdot L} \right) - s \cdot \frac{8}{9} \left(\frac{I_{HID}^3 - I_{HID}^2 \cdot L_A \cdot G \cdot V_S}{C_A^2 \cdot C^2 \cdot G^2 \cdot L \cdot V_S} \right)}{s^3 + s^2 \cdot \left(\frac{2 \cdot I_{HID}}{V_S \cdot C_A} \right) + s \cdot \left(\frac{I_{HID}}{3 \cdot G \cdot V_S \cdot L \cdot C} + \frac{2}{L \cdot C_A} \right) + \frac{4 \cdot I_{HID}^2}{3 \cdot G \cdot V_S^2 \cdot L \cdot C \cdot C_A}} \quad (157)$$

$$A(s) = \frac{\hat{V}_{C3}(s)}{\hat{V}_S(s)} \bigg|_{\substack{\hat{g}(t)=0 \\ \hat{i}_o(t)=0}} = \frac{2 \cdot s^3 - 2 \cdot s^2 \cdot \left(\frac{G \cdot L_A}{6 \cdot C \cdot L} - \frac{I_{HID}}{3 \cdot V_S \cdot C} \right) - 2 \cdot s \cdot \left(\frac{-2 \cdot L_A \cdot I_{HID} \cdot G}{2 \cdot V_S \cdot C \cdot L \cdot C_A} + 2 \cdot \frac{I_{HID}^2}{V_S^2 \cdot C \cdot C_A} + \frac{1}{6 \cdot C \cdot L} \right) + \frac{2 \cdot I_{HID}}{V_S \cdot C_A \cdot C \cdot L}}{s^3 + s^2 \cdot \left(\frac{2 \cdot I_{HID}}{V_S \cdot C_A} \right) + s \cdot \left(\frac{I_{HID}}{3 \cdot G \cdot V_S \cdot L \cdot C} + \frac{2}{L \cdot C_A} \right) + \frac{4 \cdot I_{HID}^2}{3 \cdot G \cdot V_S^2 \cdot L \cdot C \cdot C_A}} \quad (158)$$

$$Z_o(s) = \frac{\hat{V}_{C3}(s)}{\hat{I}_o(s)} \bigg|_{\substack{\hat{g}(t)=0 \\ \hat{v}_s(t)=0}} = \frac{2 \cdot G \cdot V_S^2 \left[s^2 \cdot (L \cdot C_A \cdot V_S) - s \cdot (2 \cdot I_{HID} \cdot L) + 2 \cdot V_S \right]}{s^3 + s^2 \cdot \left(\frac{2 \cdot I_{HID}}{V_S \cdot C_A} \right) + s \cdot \left(\frac{I_{HID}}{3 \cdot G \cdot V_S \cdot L \cdot C} + \frac{2}{L \cdot C_A} \right) + \frac{4 \cdot I_{HID}^2}{3 \cdot G \cdot V_S^2 \cdot L \cdot C \cdot C_A}} \quad (159)$$

Now, in order to check the stability of the boost in cascade with the switched capacitor converter, we have used the Routh Hurwitz 'criterion in equation (160), as shown in (161)

$$s^3 + s^2 \cdot \left(\frac{2 \cdot I_{HID}}{V_S \cdot C_A} \right) + s \cdot \left(\frac{I_{HID}}{G \cdot V_S \cdot L \cdot C} + \frac{2}{L \cdot C_A} \right) + \frac{4 \cdot I_{HID}^2}{3 \cdot G \cdot V_S^2 \cdot L \cdot C \cdot C_A} \quad (160)$$

$$\begin{array}{c|cc} s^3 & 1 & \frac{I_{HID}}{3 \cdot G \cdot V_S \cdot L \cdot C} + \frac{2}{L \cdot C_A} \\ s^2 & \frac{2 \cdot I_{HID}}{V_S \cdot C_A} & \frac{4 \cdot I_{HID}^2}{3 \cdot G \cdot V_S^2 \cdot L \cdot C \cdot C_A} \\ s^1 & \frac{I_{HID}}{3 \cdot G \cdot V_S \cdot L \cdot C} + \frac{2}{L \cdot C_A} & 0 \\ s^0 & \frac{4 \cdot I_{HID}^2}{3 \cdot G \cdot V_S^2 \cdot L \cdot C \cdot C_A} & 0 \end{array} \quad (161)$$

Considering the converter parameters and the fact that the current supplied to the lamp I_{HID} has a very small value (tens of mA) when the lamp is off, it is possible to conclude that the converter is always stable in the start-up transient because the following condition is satisfied.

$$\frac{I_{HID}}{3 \cdot G \cdot V_S \cdot C} < \frac{2}{C_A} \quad (162)$$



3.1.1.2 Warm-up and steady-state operation description and stability analysis.

As previously mentioned, in the warm-up and steady-state operation, only the boost converter is operating, and the switched capacitor converter used to start the lamp is bypassed by a relay in order to avoid the losses. Considering that the boost converter depicted in Fig. 65 (a) is working in CCM, it only has two structural changes within a period, as shown Fig. 65 (b) and Fig. 65 (c), and therefore can be represented by means of two linear vector differential equations (167)(168), where the corresponding state vector $x(t)$ is given by expression (169). Notice that, as the value of capacitor C_A is much higher than the value of capacitor C_3 , we have only considered in the analysis the value of capacitor C_A .

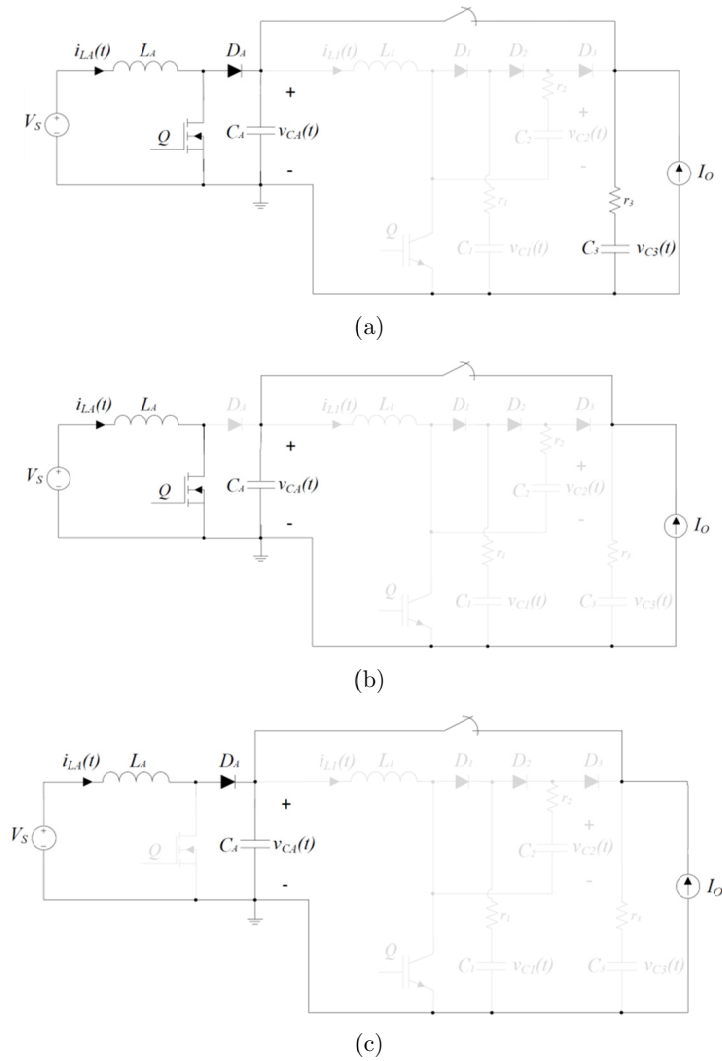


Fig 65. (a) DC Electronic ballast in warm-up and steady-state operation. (b) ON-state. (c) OFF-state.

$$\dot{x}(t) = A_1 \cdot x(t) + B_1 \quad \text{for } u = 1 \quad (\text{ON state}) \quad (163)$$

$$\dot{x}(t) = A_2 \cdot x(t) + B_2 \quad \text{for } u = 0 \quad (\text{OFF state}) \quad (164)$$



$$x(t) = \begin{bmatrix} i_{LA} & v_{CA} \end{bmatrix}^T \quad (165)$$

Matrices A_1 , A_2 , B_1 , and B_2 are given respectively by

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, A_2 = \begin{bmatrix} 0 & -\frac{1}{L_A} \\ \frac{1}{C_A} & 0 \end{bmatrix}, B_1 = B_2 = \begin{bmatrix} \frac{V_s}{L_A} \\ -\frac{I_o}{C_A} \end{bmatrix} \quad (166)$$

Where I_o represents the current delivered by the boost LFR to the lamp, as in the previous case.

The converter dynamics can be described by using a bilinear equation (167), where $A=A_2$, $B=A_1-A_2$, $\sigma=B_2$, and $\gamma=B_1-B_2$, that conveniently particularized to our converter leads to the equation set (168).

$$\dot{x}(t) = [A \cdot x(t) + \sigma] + [B \cdot x(t) + \gamma] \cdot u \quad (167)$$

$$\begin{cases} \frac{di_{LA}}{dt} = \frac{u-1}{L_A} \cdot v_{CA}(t) + \frac{V_s}{L_A} \\ \frac{dv_{CA}}{dt} = \frac{1-u}{C_A} \cdot i_{LA}(t) + \frac{I_o}{C_A} \end{cases} \quad (168)$$

As in the start-up transient, the control surface applied to the converter forces the input current (169) to track a constant reference current $k(t)$ proportional to the ballast input voltage V_s . Thus assuming ideal efficiency, the lamp active power P_{AC} , is regulated indirectly by controlling the converter input power through the adjustment of the LFR conductance “ g ”.

$$s(x) = i_{LA} - k(t), \quad \text{where } k(t) = g(t) \cdot v_s(t) \quad (169)$$

$$P_{AC} = P_{IN} = g \cdot V_s^2 \quad (170)$$

Introducing the invariance conditions [78] $s(x)=0$ and $ds(x)/dt=0$ yields the equivalent control $u_{eq}(t)$, which is bounded by both maximum and minimum values of $u(t)$.

$$0 < u_{eq}(t) < 1 \quad (171)$$

Moreover, a switching law of the type

$$u(t) = 0 \quad \text{if} \quad s(x) > 0 \quad (172)$$

$$u(t) = 1 \quad \text{if} \quad s(x) < 0 \quad (173)$$

will induce a sliding regime on the switching surface ensuring the sliding-mode existence conditions because

$$s(x) \cdot \frac{ds(x)}{dt} < 0 \quad (174)$$



The sliding mode analysis of equations (163)-(169) is performed in two steps. First, we will find the equilibrium point corresponding to a constant V_s and a constant value G of $g(t)$ in the control loop. Second, we will consider the influence of the time varying components $v_s(t)$ and $g(t)$ as low-frequency superposed signals on the corresponding values V_s and G . The contribution of the superposed signals will be predicted by a model derived by linearizing the ideal sliding dynamics around the equilibrium point previously obtained.

Therefore the resulting equivalent control for $S(X)=I_{LA}-G \cdot V_s$, the corresponding sliding dynamics, and the coordinates of the equilibrium point $X^*=[I_{LA}^*, V_{CA}^*]$ are given by the expressions (175) to (178) respectively considering as in the previous case that $I_o < 0$, so $-I_o = I_{HID}$

$$u_{eq}(t) = 1 - \frac{V_s}{V_{CA}} \quad (175)$$

$$i_{LA}(t) = G \cdot V_s \quad (176)$$

$$\frac{dv_{CA}}{dt} = \frac{G \cdot V_s}{C_A} (1 - u_{eq}) + \frac{I_o}{C_A} \quad (177)$$

$$X^* = \left[G \cdot V_s, \frac{V_s^2 \cdot G}{-I_o} \right]^T = \left[G \cdot V_s, \frac{V_s^2 \cdot G}{I_{HID}} \right]^T \quad (178)$$

Assuming now that $k(t)$ is time-varying, the corresponding equivalent control will be given by

$$u_{eq} = 1 - \frac{v_s(t)}{v_{CA}(t)} + L_A \cdot \frac{g(t)}{v_{CA}(t)} \cdot \frac{dv_s(t)}{dt} + L_A \cdot \frac{v_s(t)}{v_{CA}(t)} \cdot \frac{dg(t)}{dt} \quad (179)$$

Therefore, the ideal sliding dynamics can be expressed as

$$i_{LA}(t) = k(t) = g(t) \cdot v_s(t) \quad (180)$$

$$\frac{dv_{CA}}{dt} = \frac{g(t) \cdot v_s^2(t)}{C_A \cdot v_{CA}(t)} - \frac{g(t)^2 \cdot v_s(t) \cdot L_A}{C_A \cdot v_{CA}(t)} - \frac{L_A \cdot g(t) \cdot v_s^2(t)}{C_A \cdot v_{CA}(t)} + \frac{i_o(t)}{C_A} \quad (181)$$

assuming that

$$g(t) = G + \hat{g}(t) \quad (182)$$

$$v_s(t) = V_s + \hat{v}_s(t) \quad (183)$$

$$i_{LA}(t) = I_{LA}^* + \hat{i}_{LA}(t) \quad (184)$$

$$v_{CA}(t) = V_{CA}^* + \hat{v}_{CA}(t) \quad (185)$$

and linearizing the equation (181) around the equilibrium point $X^*=[I_{LA}^*, V_{CA}^*]$ lead to the following expression



$$\frac{dv_{CA}}{dt} = a \cdot \hat{g}(t) + b \cdot \frac{dg(t)}{dt} + c \cdot \hat{v}_s(t) + d \cdot \frac{d\hat{v}_s(t)}{dt} + e \cdot \hat{v}_{CA}(t) + f \cdot \hat{i}_o(t) \quad (186)$$

where coefficients a , b , c , d , e , and f are expressed by (187) to (192) respectively

$$a = \frac{I_{HID}}{C_A \cdot G} \quad (187)$$

$$b = -\frac{L \cdot I_{HID}}{C_A} \quad (188)$$

$$c = -\frac{2 \cdot I_{HID}}{C_A \cdot V_S} \quad (189)$$

$$d = -\frac{L \cdot I_{HID} \cdot L_A}{C_A \cdot V_S} \quad (190)$$

$$e = -\frac{I_{HID}^2}{C_A \cdot V_S^2 \cdot G} \quad (191)$$

$$f = \frac{1}{C_A} \quad (192)$$

Fig. 66 shows the corresponding model of the sliding-mode controlled boost converter, operating in the warm-up and steady state with LFR behaviour.

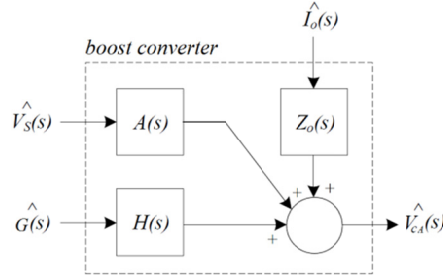


Fig 66. Dynamic model of the boost converter in warm-up and steady -state operation.

Hence,

$$H(s) = \left. \frac{\hat{V}_{CA}(s)}{\hat{G}(s)} \right|_{\substack{\hat{v}_s(t)=0 \\ \hat{i}_o(t)=0}} = \frac{a + s \cdot b}{s - e} \quad (193)$$

$$A(s) = \left. \frac{\hat{V}_{CA}(s)}{\hat{V}_S(s)} \right|_{\substack{\hat{g}(t)=0 \\ \hat{i}_o(t)=0}} = \frac{c + s \cdot d}{s - e} \quad (194)$$

$$Z_o(s) = \left. \frac{\hat{V}_{CA}(s)}{\hat{I}_o(s)} \right|_{\substack{\hat{v}_s(t)=0 \\ \hat{g}(t)=0}} = \frac{f}{s - e} \quad (195)$$



Note that the control to output transfer function $H(s)$ expressed in (196) corresponds to a stable system because the condition (197) is always satisfied.

$$H(s) = \frac{\hat{V}_{CA}(s)}{\hat{G}(s)} \bigg|_{\substack{\hat{v}_s(t)=0 \\ \hat{i}_o(t)=0}} = \frac{\frac{I_{HID}}{C_A \cdot G} - s \cdot \frac{L_A \cdot I_{HID}}{C_A}}{s + \frac{I_{HID}^2}{C_A \cdot G \cdot V_s^2}} \quad (196)$$

$$\frac{I_{HID}^2}{C_A \cdot G \cdot V_s^2} > 0 \quad (197)$$

3.1.2 DC Electronic Ballast Implementation.

This section shows the practical implementation of the power stage, control stage, and overvoltage protection of the DC Electronic ballast for HID lamps.

3.1.2.1 Power Stage Implementation.

Fig. 67 shows the circuit scheme of the power stage.

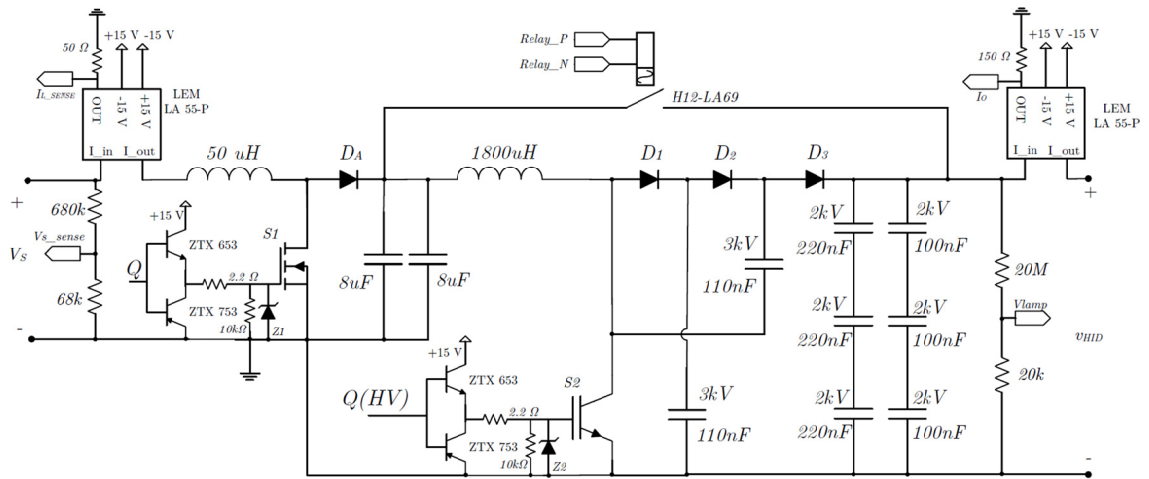


Fig 67. Power stage circuit scheme of the proposed DC Electronic ballast.

The prototype has been implemented with the switching devices whose characteristics are shown in Table XII. These characteristics illustrate the blocking voltages for transistor, diodes and for the relay used to bypass the switched capacitor converter.

It has to be pointed out that the signal Q in Fig. 67 is the output of the hysteretic comparator described later in Fig. 68. In the switched capacitor stage, the signal used to switch the IGBT (Q_{HV}) is only activated when the lamp is off. Moreover, it can be observed that the driver in both cases is realized by two bipolar transistors, a npn transistor (ZTX 653) with V_{ce} of 100 V and a collector current of 2 A, and a pnp transistor (ZTX 753) with an V_{ce} of 100 V and a current of -2 A. The MOSFET gate resistance is an E24 resistor of 2.2 Ω while the protection parallel resistance and Zener are an E24 10 k Ω and C16PH (16 V) diode Zener respectively.



Table XII. Power switches of the DC-Electronic ballast for HID lamps.

S_1	IRFP4768PbF IR	Si	250 V	14mΩ (93A)	Vth 3V	Vg ±20V	Qg 180nC
S_2	IRFP4768PbF IXYS	Si	4 kV	VCE(SAT)=4V (40A)	Vth 6V	Vg ±20V	Qg 310nC
D_A	STTH30R04 ST	Si	400 V	30 A	Von 0.8-1.1V	trr 35 ns	
D_1	DHH55-36N1F IXYS	Si	1.8 kV	60 A	Von 2.0-2.5V	trr 230 ns	
D_2	DHH55-36N1F IXYS	Si	1.8 kV	60 A	Von 2.0-2.5V	trr 230 ns	
D_3	DHH55-36N1F IXYS	Si	1.8 kV	60 A	Von 2.0-2.5V	trr 230 ns	
$Relay$	H12-LA69		10 kV	3A	150 mΩ		

The output capacitor in the boost converter stage (C_A) consists in two polypropylene type capacitors in parallel of 8 μF each one (EPCOS B32776T5855) with a 500 V rated voltage. The capacitors used in the switched capacitor stage, C_1 and C_2 are two capacitors of 110 nF of the type GenteQ 42L4102 with a 3 kV rated voltage. The output capacitor C_3 used in the switched capacitor stage consists in the combination of three capacitor in series of 2 kV rated voltage and a capacitance of 220 nF each one of the type GenteQ 42L3222, which in turn are in parallel with a combination of three capacitor in series model VISHAY MKP1845 of 2 kV rated voltage and 100 nF each one, obtaining a final capacitance C_3 of 110 nF.

The input series inductor L_A of 50 μH has been realized with 50 wires of 0.007 mm² by making 35 turns around the Kool M μ 77111-A7 core, which has a permeability of 26. Notice that the use of 50 wires instead of 1 tends to reduce the skin effect when the switching frequency increases beyond 30 kHz. The inductor L of 1800 μH has been realized with the same core, but in this case making 290 turns with 1 wire of 0.7 mm². Besides, we have used only one wire because the switching frequency is lower (around 10 kHz) when this inductor is working.

The input and output voltages are sensed by two voltage dividers of (680 k Ω -1 k Ω) and (20 M Ω -20 k Ω) respectively. These signals V_{S_sense} and V_{lamp} are proportional to the input and output voltage respectively. The input and output current sensors consist in two Hall effect transducers of the type LEM-LA-55P with a bandwidth of 200 kHz. Signals I_{L_SENSE} and I_O are proportional to the inductor current I_{LA} and lamp current I_{HID} respectively.

3.1.2.2 Control stage.

Fig. 68 shows the practical implementation of the sliding mode controller, namely hysteretic comparator of the input current, $k(t)$ generator, HID on detector, overvoltage protection, and finally hysteresis control.

On the one hand, the hysteretic comparator circuit of the input current employs two LM319 comparators with a response time of 80 ns, and a JKMC14027 flip-flop with a bandwidth of 13 MHz. The output of the hysteretic comparator is a digital signal Q which



activates the driver of the boost converter depicted in Fig. 67. On the other hand the inputs of the hysteretic comparator are the subtraction between the measured input current I_{L_SENSE} , and the reference current $k(t)$, treated by a circuit based on LM324 operational amplifiers, and the hysteretic bands H_POS and H_NEG .

Next, $k(t)$ generator is the responsible to provide signal $k(t)$ that is connected to the hysteretic comparator. This signal is obtained by means of an analogue multiplier AD633 with a slew-rate 20 V/ μ s, which multiplies the input reference conductance $g(t)$ and the measured input voltage V_{S_sense} .

Fig. 68 shows the HID on detector that is the circuit responsible to determine when the lamp is turned on. This circuit is a hysteretic comparator that employs two LM319 comparators and a JKMC14027. When the measured lamp current I_o is higher than a reference value of 700 mA, the signal QS is activated with a logic "1", and the signal QN is a logic "0". In the same scheme an AND gate provides the signal to the driver of the IGBT depicted in Fig. 67. The inputs of the AND gate are the output of the hysteretic comparator Q , and the output QN that only is activated when the lamp is Off. This results in the second converter operation only when the lamp has not started.

The overvoltage protection is performed by means of a hysteretic comparator that employs two LM319 comparators and a JKMC14027 flip-flop. In this case the inputs of the hysteretic comparator are two reference voltage values of 6 V and 0.7 V, and the measured lamp voltage V_{lamp} . When the lamp voltage is above 6 kV, the output of the hysteretic comparator Q_g is provides an "1" logic, and when this lamp voltage is decreased under 700 V output Q_g yields an "0" logic. This output Q_g is used to short-circuit the input conductance $g(t)$ to zero, when the lamp voltage is above 6 kV. When the lamp voltage is under 700 V, the conductance is activated again.

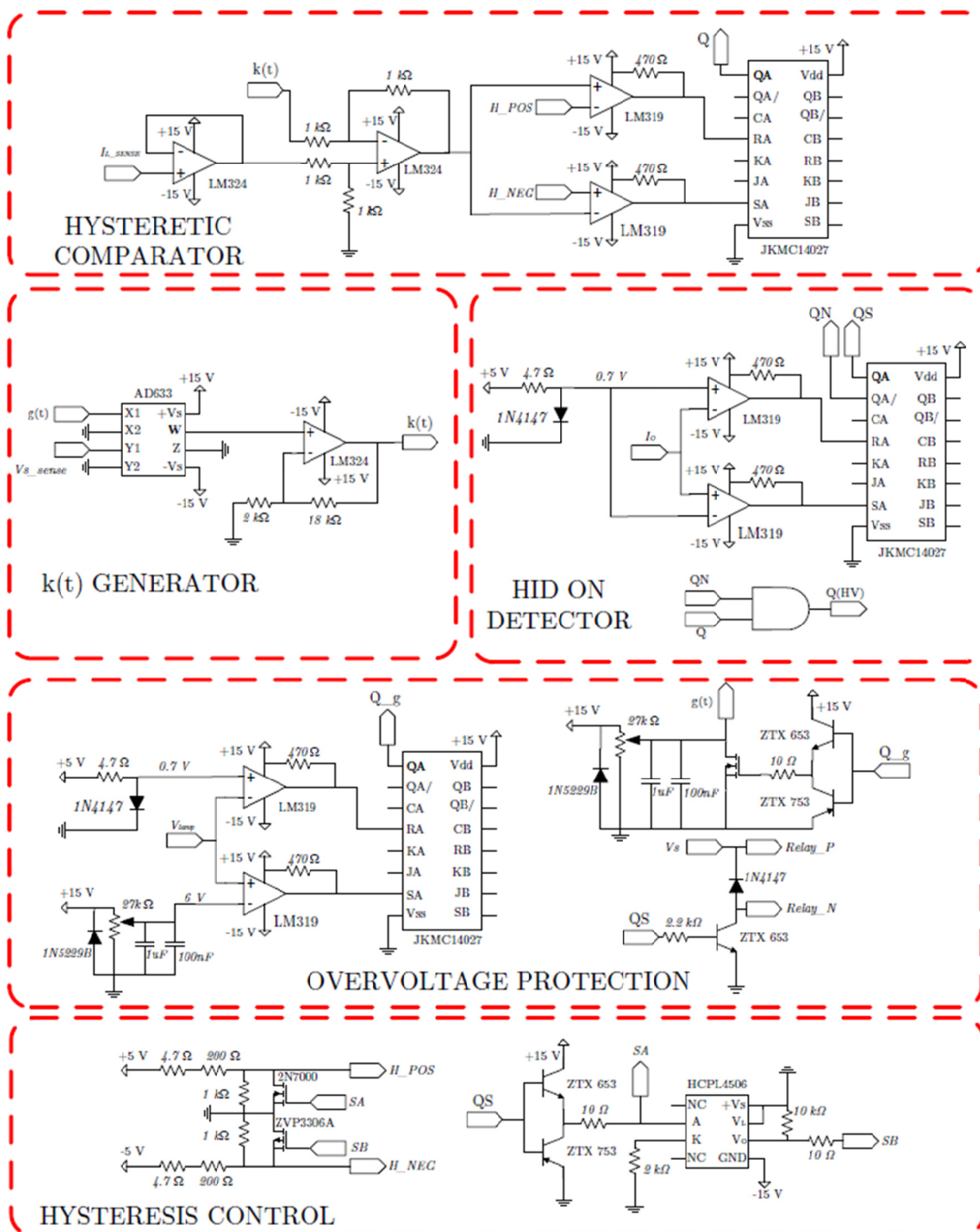


Fig 68. Power stage circuit scheme of the proposed DC Electronic ballast.

Finally, the hysteresis control bands are introduced by means of two voltage dividers, which partially short-circuited when the lamp is started in order to change the hysteretic band value and increase the switching frequency in warm-up and steady- state operation.



3.1.3 Experimental results.

The main experimental results are given in this section. The experimental prototype used in the tests with three different HID lamps is depicted in Fig. 69. Therefore, all the experimental results shown in this section have considered a power reference of 250 W.



Fig 69. Experimental set-up with three HID lamps.

3.1.3.1 Results with Metal Halide Lamp Pulse start Lamp.

First, the results with a metal halide pulse start lamp are presented. In this specific case the lamp used is HIE/C/BU/DU/4.5K from Phillips Lighting.

Fig. 70 shows the start-up transient results when a metal halide pulse start lamp is connected in the output of the electronic ballast. In this specific case it is possible to appreciate how the lamp voltage (v_{HID}) starts and increases until 3.7 kV are reached. At this moment, the lamp has started, the switched capacitor converter is stopped and bypassed, and the warm-up operation begins. It can be observed that when the lamp is started, the voltage decreases under its nominal value in steady-state operation due to the HID characteristic impedance.

Moreover, Fig. 70 illustrates the inductor current behaviour (I_{LA}). It is important to notice that when the lamp is off, and the switched capacitor converter is connected in cascade with the boost converter, the inductor ripple is higher because the switching frequency has been decreased in order to protect the IGBT S_2 . In this case, the switching frequency in the start-up transient is approximately 10 kHz. After the ignition the hysteretic band is self-adjusted in order to increase the switching frequency above the audible frequencies in the warm-up and steady-state operation, i.e. about 30 kHz approximately.



In the same figure, it is possible to see the lamp current I_{HID} starting to flow through the HID after the spark generation while the input voltage V_S is always 12 V.

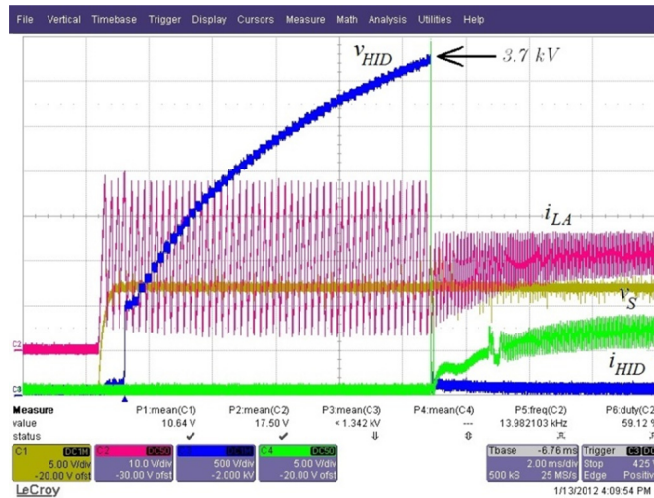


Fig 70. DC-Electronic Ballast start-up transient with Metal Halide Lamp Pulse start Lamp.

Fig. 71 shows the warm-up operation, realized after the lamp ignition. As previously mentioned, when the spark is generated the second converter is bypassed, and the lamp voltage decreases under its nominal value in steady- state operation. Similarly, the lamp current begins to flow when the lamp has started, and is above the final value in steady- state operation. A good LFR behaviour of the converter delivering always the same power during all the warm-up operation is observed due to the automatic adjustment of voltage and current independently of the HID characteristic impedance. It is important to remark that this warm-up duration is approximately 1'30" and the input voltage V_S is always 12 V.

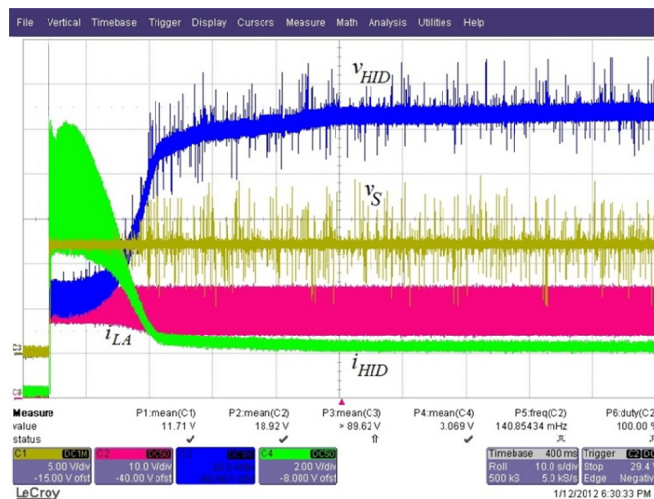


Fig 71. DC-Electronic Ballast warm-up operation with Metal Halide Pulse Start Lamp.

Finally, Fig. 72 shows the steady-state operation after the warm-up. It can be observed that the lamp voltage V_{HID} in steady-state operation is about 110 V and the lamp current I_{HID} is about 2.3 A , which means a power of 253 W approximately. The input voltage and current are

Dimmable Electronic ballast based on Loss-Free Resistor (LFR) approach to supply High-Intensity Discharge (HID) Lamps.



12 V and 22 A respectively, which implies that the converter is absorbing a power of 264 W. Hence, the efficiency of the converter in steady state is about 95%.

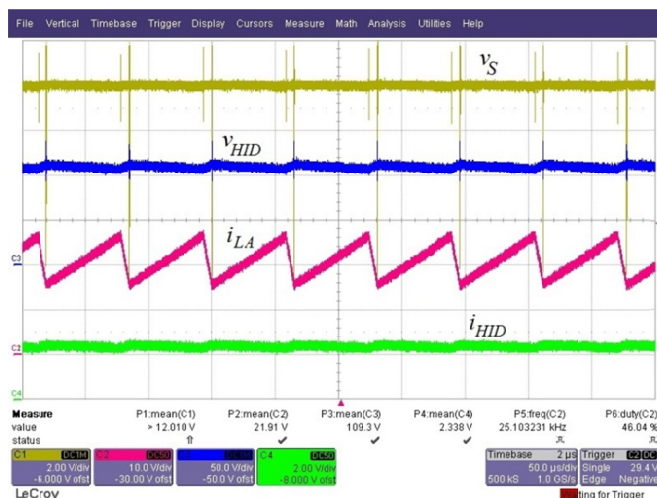


Fig 72. DC-Electronic Ballast steady-state operation with Metal Halide Pulse Start Lamp.

3.1.3.2 Results with Vapour Sodium Lamp.

Now the experimental results with a vapour sodium HID lamp model HPSE.250W/E40/HOV of 250 W from OSRAM are presented.

Fig. 73 shows the start-up transient results when the vapour sodium lamp is connected in the output of the electronic ballast. The behaviour of the converter is practically the same than the one depicted in Fig. 70. The main difference in this case is the spark, which is generated at higher voltage, i.e. 5.5 kV approximately.

Fig. 74 shows, in turn, the warm-up of the vapour sodium lamp, and as in the case depicted in Fig. 71, it is possible to appreciate the goof LFR behaviour of the ballast prototype, delivering the selected power to the lamp during all the warm-up phase.

Finally, Fig. 75 shows the steady-state operation after the warm-up. The lamp voltage V_{HID} in steady-state operation is about 106 V and the lamp current I_{HID} is about 2.4 A , which means a power of 254 W approximately. In this case the input voltage and current are 12 V and 23 A respectively, which implies that the converter is absorbing a power of 276 W. Therefore, the efficiency of the converter in steady -state is about 92%.

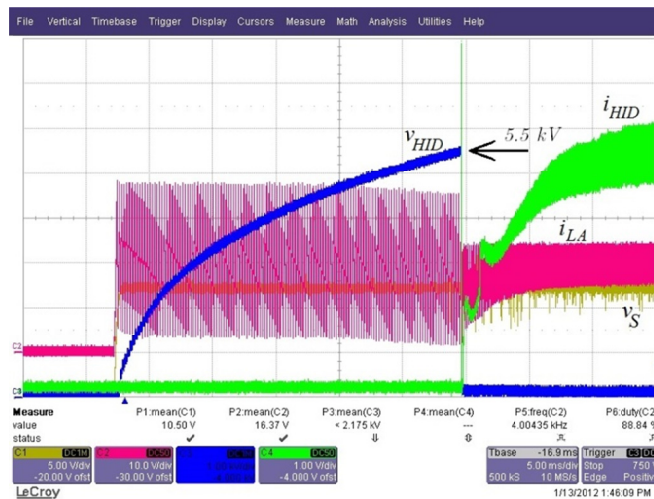


Fig 73. DC-Electronic Ballast start-up transient with Vapour Sodium Lamp.

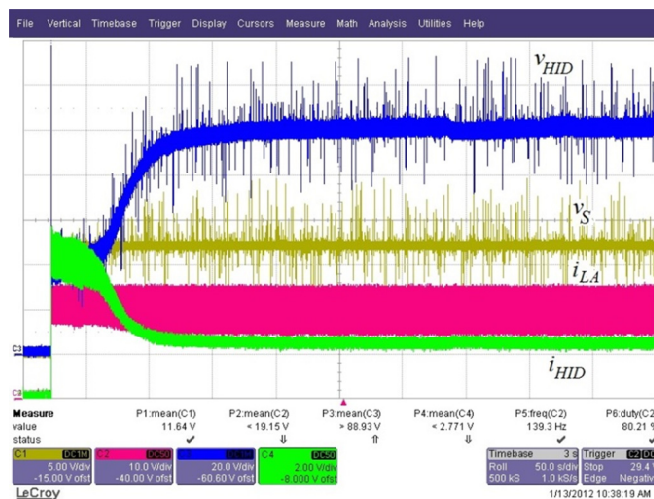


Fig 74. DC-Electronic Ballast warm-up operation with Vapour Sodium Lamp.

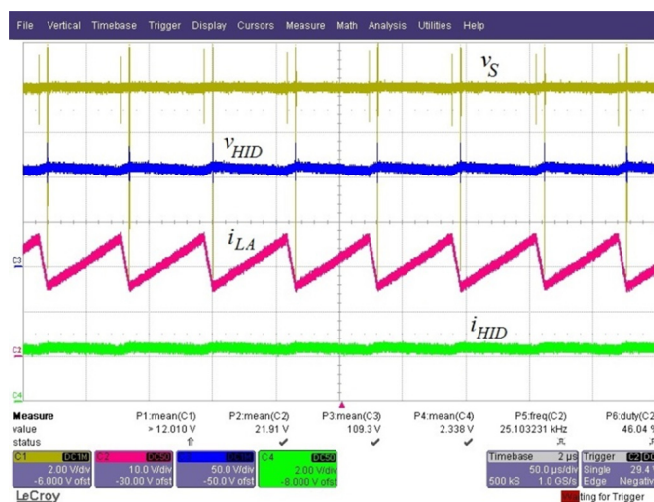


Fig 75. DC-Electronic Ballast steady-state operation with Vapour Sodium Lamp.



3.1.3.3 Results with Dual Metal Halide Lamp

The last experimental results are realized with a dual metal halide HID lamp model HIE250W/C/V/DU/4.5K of 250 W from Venture Lighting.

As in the previous cases, Fig. 76 shows the start-up transient results when the dual metal halide HID lamp is connected in the output of the electronic ballast. The behaviour of the converter is the same than the one depicted in Fig. 70, and the generated spark is of 3.5 kV approximately.

Fig. 77 shows the warm-up of the dual metal halide lamp and the good LFR behaviour of the ballast prototype delivering the selected power to the lamp during all the warm-up phase.

Fig. 78 shows the steady-state operation after the warm-up. The lamp voltage V_{HID} is about 121 V and the lamp current I_{HID} is around 2 A, which means a power of 254 W approximately. In this case the input voltage and current are 12 V and 22 A respectively, which implies that the converter is absorbing a power of 264 W. Hence, the efficiency of the converter in steady- state is around 96%.

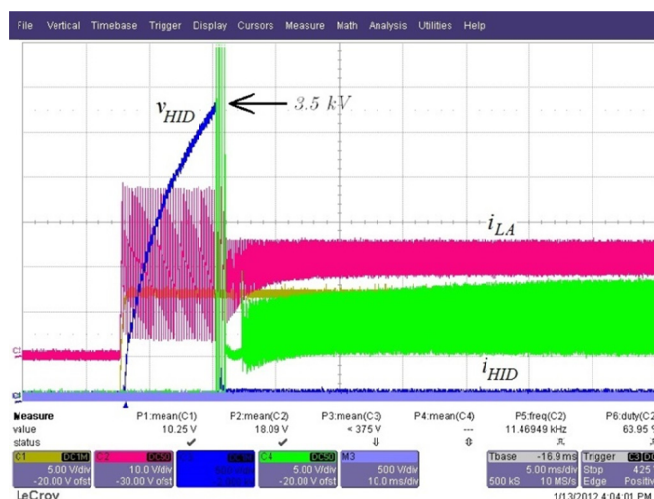


Fig 76. DC-Electronic Ballast Start-Up transient with Dual Metal Halide Lamp.

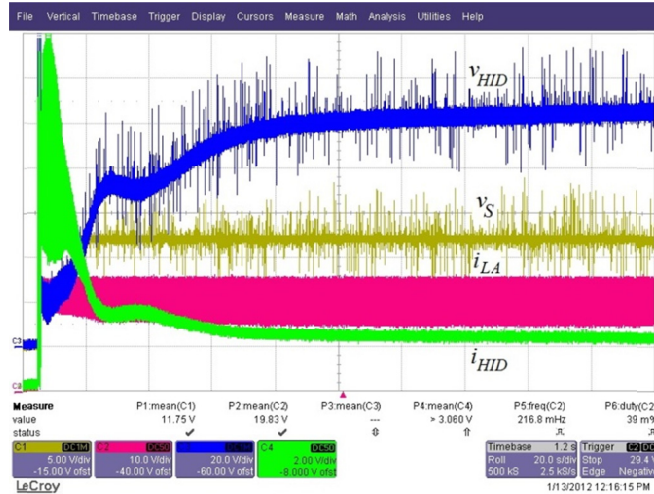


Fig 77. DC-Electronic Ballast Warm-up operation with Dual Metal Halide Lamp.

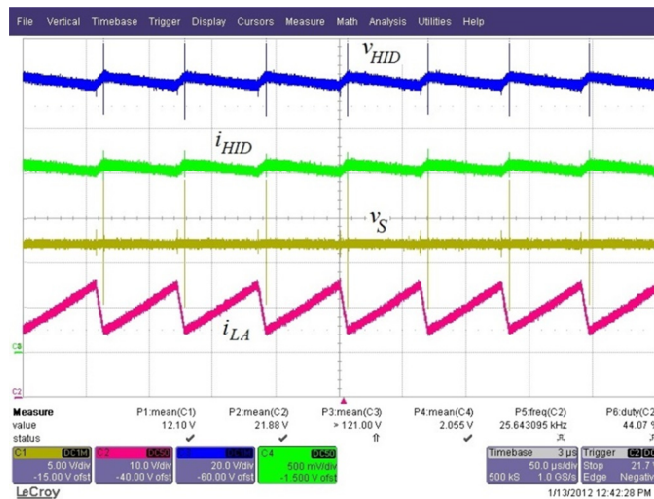


Fig 78. DC-Electronic Ballast Steady-State operation with Dual Metal Halide Lamp.

3.1.4 Conclusions of the DC Electronic Ballast with LFR behaviour.

An electronic ballast to drive different HID lamps has been presented and its dynamics for both operation modes have been analysed.

The ballast behaves like a LFR delivering always the selected power to the lamp, independently of the lamp impedance due to the action of an appropriate sliding- mode control law. This feature ensures the lamp operation at nominal power during all the lamp life and reduces the warm-up time. As the power reference can be adjusted using a potentiometer, the light intensity can be easily regulated. Besides, as the lamps are supplied in DC, the AR problems are avoided.

Another accomplished target has been designing the DC Electronic Ballast using commercial switching devices and evaluating the main technological features of this proposal. Several experimental tests with commercial HIDs have shown the feasibility of the proposed



approach, and its good efficiency demonstrating that the ballast is capable to achieve 6 kV to start the lamp from a 12 V power source.

The introduction of SiC devices can simplify the proposed ballast, reducing the number of stages and devices, and obtaining high power densities and efficiencies. Moreover, the relay could be substituted in a near future by a semiconductor device with the same characteristics.

3.2 High-Frequency Electronic Ballast for HID lamps with LFR behaviour based on sliding mode control implemented in FPGA.

The goal of this section is to design a two-stage electronic ballast, where the first-one is a boost converter with loss-free resistor (LFR) behaviour supplied by a low DC voltage. This stage is controlled by means of sliding-mode control, implemented with a field programmable gate array (FPGA). The second stage must supply the lamp with an AC voltage generated by a full bridge resonant inverter operating in open loop. Although there are two operating options: LFSW and HFSW, we have selected the second one. In this last case, the lamp is operated always at high frequency. Thus, the second stage is used to perform the ignition sequence ($215 \text{ kHz} < f_s < 350 \text{ kHz}$), and supply subsequently the lamp with a HFSW ($\sim 100 \text{ kHz}$) to avoid the acoustic resonances. The ballast circuit description and ballast block diagram is shown in Figs. 79 and 80 respectively.

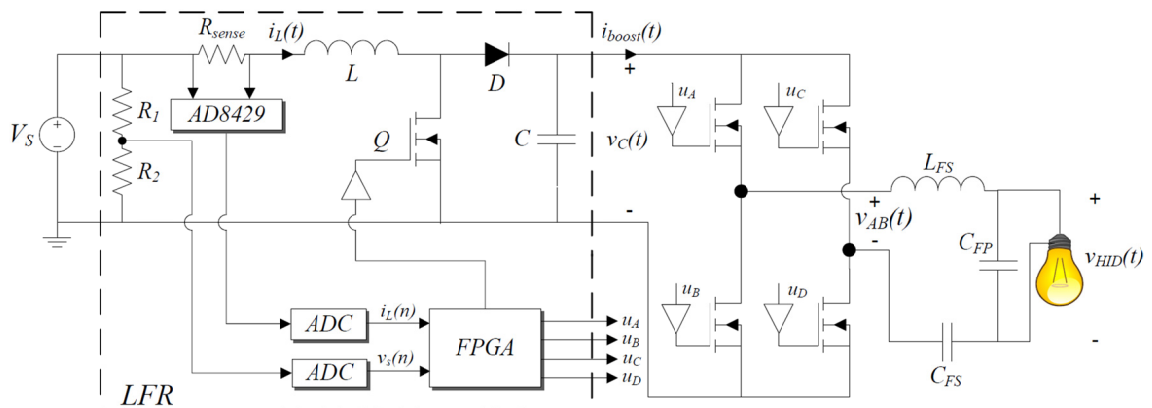


Fig 79. Boost converter-based LFR plus full bridge resonant inverter and FPGA control implementation.

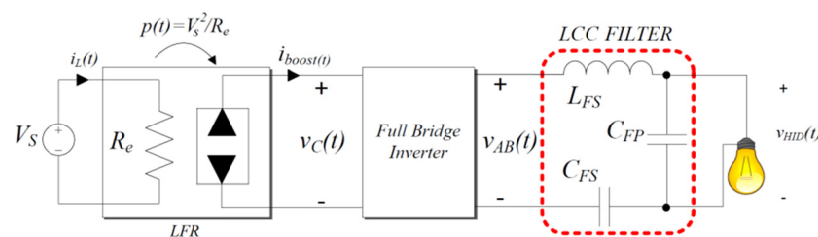


Fig 80. Electronic ballast block diagram with boost-based LFR.

3.2.1 Loss-Free Resistor approach implemented by FPGA.

As previously mentioned, a LFR can be realized if appropriate sliding motions are induced in some converters. Moreover, the sliding-mode control is a very useful tool in the



power electronics field to design controllers and analyse the variable-structure control systems [140], exhibiting a fast response and low sensibility to external perturbations at the expense of variable switching frequency [141]. Due to its robustness and fast dynamic behaviour this control has been the subject of many reports [81, 142].

Furthermore, digital control techniques are increasingly used in switched power converters due their inherent advantages compared to the analogue control techniques. Digital control techniques offer more flexibility in order to modify or change the control strategy without significant hardware changes, in comparison with analogue control techniques. Other important characteristics are the high immunity to noise and the absence of aging effects.

In terms of sliding -mode control, diverse publications are focused on its implementation by means of low cost controllers. The limitations imposed by the microcontrollers require a complex discrete-time treatment to facilitate the subsequent sliding control algorithm implementation [143-145].

However, the high frequency sampling capability of an Analogue to Digital Converter (ADC-4 MHz) connected in an FPGA (Altera-Cyclone II) implementing a hysteretic comparator results in a good approximation of the continuous-time sliding mode control. Thus, the analytical treatment of the sliding dynamics will be held in continuous time without resorting to an analytical study of the discretized sliding dynamics. Therefore, the boost converter will behave like LFR whose digital controller has the same behaviour as an analogue one, designed using the sliding equations in continuous time.

3.2.1.1 Digital LFR approach by means of sliding mode control.

The main target of this section is to control the first stage of the converter depicted in Fig. 79 by means of sliding- mode control considering the discretized variables as shown in Fig. 81. It is important to notice that the higher are the sampling frequency of the ADC (f_{sample}) and the number of quantization levels, the more close is the approximation to the analogue behaviour. Hence, considering a sampling frequency of 4 MHz, and a switching frequency in the converter below 100 kHz, it is possible to study the controller as a continuous system.

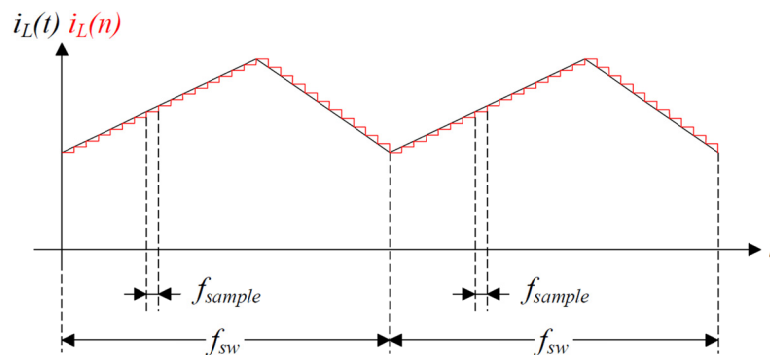


Fig 81. Inductor current $i_L(t)$, and discretized inductor current $i_L(n)$.



As in previous cases, assuming that the boost converter operates in continuous conduction mode (CCM), the converter only has two structural changes within a period, as shown in Fig 82. The main target of this section is to control the first stage of the converter depicted in Fig. 79, which can be represented by means of two linear vector differential equations (198)(199), where the corresponding state vector is shown in (200).

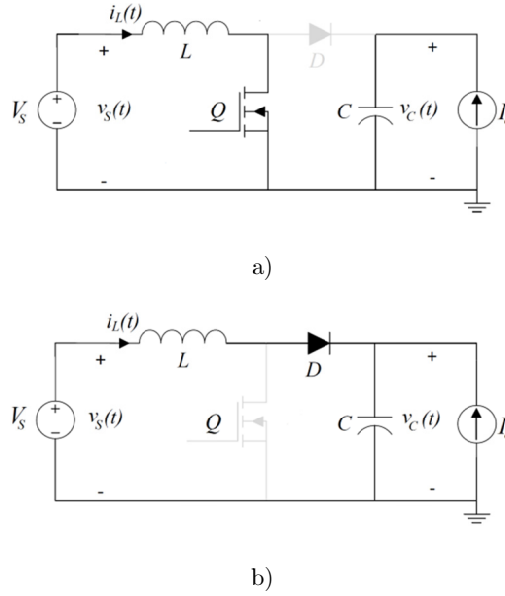


Fig 82. Boost converter states. a) ON-state; and b) OFF-state

$$\dot{x}(t) = A_1 x(t) + B_1 \quad \text{for } u = 1 \quad (ON \text{ state}) \quad (198)$$

$$\dot{x}(t) = A_2 x(t) + B_2 \quad \text{for } u = 0 \quad (OFF \text{ state}) \quad (199)$$

$$x(t) = [i_L \quad v_C]^T \quad (200)$$

Matrices A_1 , A_2 , B_1 and B_2 are given respectively by

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}; \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}; \quad B_1 = B_2 = \begin{bmatrix} \frac{v_s(t)}{L} \\ -\frac{I_o}{C} \end{bmatrix} \quad (201)$$

where I_o represents the current delivered by the boost LFR to the second stage. The converter dynamics can be described using the bilinear equation (202) where $A=A_2$, $B=A_1-A_2$, $\sigma=B_2$ and $\gamma=B_1-B_2$, which particularized to our converter leads to the equation set (203).

$$\dot{x}(t) = [A \cdot x(t) + \sigma] + [B \cdot x(t) + \gamma] \cdot u \quad (202)$$

$$\begin{cases} \frac{di_L}{dt} = \frac{u-1}{L} \cdot v_C(t) + \frac{v_s(t)}{L} \\ \frac{dv_C}{dt} = \frac{1-u}{C} \cdot i_L(t) + \frac{I_o}{C} \end{cases} \quad (203)$$

The control surface applied to the converter forces the input current to track a constant reference $k(t)$ proportional to the ballast input voltage V_s . Thus assuming ideal efficiency, the



lamp active power P_{AC} can be regulated indirectly by controlling the converter input power through the adjustment of the LFR conductance “ g ” (205).

$$s(x) = i_L - k(t) \quad \text{where} \quad k(t) = g(t) \cdot v_s(t) \quad (204)$$

$$P_{AC} = P_{IN} = g \cdot V_s^2 \quad (205)$$

Introducing the invariance conditions [78] $s(x)=0$ and $ds(x)/dt=0$ yield the equivalent control $u_{eq}(t)$, which is bounded by both maximum and minimum values of $u(t)$.

$$0 < u_{eq}(t) < 1 \quad (206)$$

Moreover, a switching law of the type

$$u(t) = 0 \quad \text{if} \quad s(x) > 0 \quad (207)$$

$$u(t) = 1 \quad \text{if} \quad s(x) < 0 \quad (208)$$

will induce a sliding regime on the switching surface ensuring the sliding-mode existence because

$$s(x) \frac{ds(x)}{dt} < 0 \quad (209)$$

The sliding analysis of equations (198)-(204) is performed in two steps. First, we will find the equilibrium point corresponding to a constant V_s and a constant value G of $g(t)$ in the control loop. Second, we will consider the influence of the time varying components $v_s(t)$ and $g(t)$ as low-frequency superposed signals on the corresponding values V_s and G . The contribution of the superposed signals will be predicted by a model derived by linearizing the ideal sliding dynamics around the equilibrium point previously obtained.

Therefore, the resulting equivalent control, the corresponding sliding dynamics, and the equilibrium point coordinates $X^*=[I_L, V_C^*]$ are given by (210) to (213) respectively, after considering as in the previous cases that $I_O < 0$, so $-I_O = I_{BOOST}$

$$u_{eq}(t) = 1 - \frac{V_s}{V_C} \quad (210)$$

$$i_L(t) = G \cdot V_s \quad (211)$$

$$\frac{dv_C}{dt} = \frac{G \cdot V_s}{C} (1 - u_{eq}) + \frac{I_O}{C} \quad (212)$$

$$X^* = \begin{bmatrix} G \cdot V_s & \frac{V_s^2 \cdot G}{-I_O} \end{bmatrix}^T = \begin{bmatrix} G \cdot V_s & \frac{V_s^2 \cdot G}{I_{BOOST}} \end{bmatrix}^T \quad (213)$$

Assuming now that $k(t)$ is time-varying, the corresponding equivalent control will be given by

$$u_{eq} = 1 - \frac{v_s(t)}{v_C} + L \cdot \frac{g(t)}{v_C} \cdot \frac{dv_s(t)}{dt} + L \cdot \frac{v_s(t)}{v_C} \cdot \frac{dg(t)}{dt} \quad (214)$$



Therefore, the ideal sliding dynamics can be expressed as

$$i_L(t) = k(t) = g(t) v_s(t) \quad (215)$$

$$\frac{dv_C}{dt} = \frac{g(t) v_s^2(t)}{C \cdot v_C} - \frac{g(t)^2 \cdot v_s(t) \cdot L \cdot dv_s(t)}{C \cdot v_C \cdot dt} - \frac{L \cdot g(t) v_s^2(t) \cdot dg(t)}{C \cdot v_C \cdot dt} + \frac{i_o(t)}{dt} \quad (216)$$

Assuming now

$$\begin{aligned} g(t) &= G + \hat{g}(t) \\ v_s(t) &= V_s + \hat{v}_s(t) \\ i_L(t) &= I_L^* + \hat{i}_L(t) \\ v_C(t) &= V_C^* + \hat{v}_C(t) \end{aligned} \quad (217)$$

and linearizing equation (216) around the equilibrium point $X^* = [I_L^*, V_C^*]$ led to the following expression

$$\frac{d\hat{v}_C}{dt} = a \cdot \hat{g}(t) + b \cdot \frac{d\hat{g}(t)}{dt} + c \cdot \hat{v}_s(t) + d \cdot \frac{d\hat{v}_s(t)}{dt} + e \cdot \hat{v}_C(t) + f \cdot \hat{i}_O(t) \quad (218)$$

where coefficients a , b , c , d , e and f are given by expressions (219)-(224) respectively

$$a = \left. \frac{\partial f(x)}{\partial g(t)} \right|_{X^*} = \frac{I_{BOOST}}{C \cdot G} \quad (219)$$

$$b = \left. \frac{\partial f(x)}{\partial a(t)} \right|_{a(t)=\frac{dg(t)}{dt}, X^*} = -\frac{L \cdot I_{BOOST}}{C} \quad (220)$$

$$c = \left. \frac{\partial f(x)}{\partial v_s(t)} \right|_{X^*} = \frac{2 \cdot I_{BOOST}}{C \cdot V_s} \quad (221)$$

$$d = \left. \frac{\partial f(x)}{\partial b(t)} \right|_{b(t)=\frac{dv_s(t)}{dt}, X^*} = -\frac{I_{BOOST} \cdot G \cdot L}{C \cdot V_s} \quad (222)$$

$$e = \left. \frac{\partial f(x)}{\partial v_C(t)} \right|_{X^*} = -\frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G} \quad (223)$$

$$f = \left. \frac{\partial f(x)}{\partial i_O(t)} \right|_{X^*} = \frac{1}{C} \quad (224)$$

Now, Fig. 83 shows the dynamical model of the boost converter with LFR behaviour controlled by means of sliding mode control.

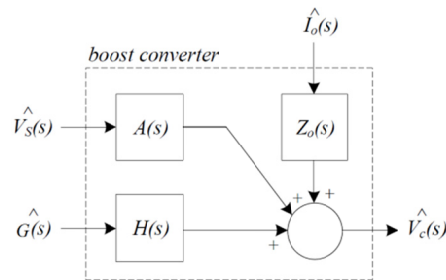


Fig 83. Switched converter dynamic model.



Hence,

$$H(s) = \frac{\hat{V}_C(s)}{\hat{G}(s)} = \frac{a + s \cdot b}{s - e} = \frac{\frac{I_{BOOST}}{C \cdot G} - s \cdot \frac{L \cdot I_{BOOST}}{C}}{s + \frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G}} \quad (225)$$

$$A(s) = \frac{\hat{V}_C(s)}{\hat{V}_s(s)} = \frac{c + s \cdot d}{s - e} = \frac{\frac{2 \cdot I_{BOOST}}{C \cdot V_s} - s \cdot \frac{I_{BOOST} \cdot G \cdot L}{C \cdot V_s}}{s + \frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G}} \quad (226)$$

$$Z_o(s) = \frac{\hat{V}_C(s)}{\hat{I}_o(s)} = \frac{f}{s - e} = \frac{\frac{1}{C}}{s + \frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G}} \quad (227)$$

The transfer function output-control $H(s)$ is expressed in (225), which corresponds to a stable system because condition (228) is always satisfied.

$$\frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G} > 0 \quad (228)$$

3.2.2 Resonant Inverter Design.

In this section the inverter stage is designed for a resonant frequency of 215 kHz approximately. The FPGA switches the inverter at this resonance frequency until the lamp is turned on. After the ignition, the inverter is operated at 100 kHz during the warm-up, and in steady-state operation (HFSW) avoiding the AR, as depicted Fig. 84. When the lamp is off, the inverter is switched at a frequency above the resonance (350 kHz) and is decreased in steps of 5 kHz, in order to obtain a soft-start, as depicted Fig. 84. If the full bridge reaches the 215 kHz frequency and the lamp has not started, the sequence is repeated until the lamp is turned on.

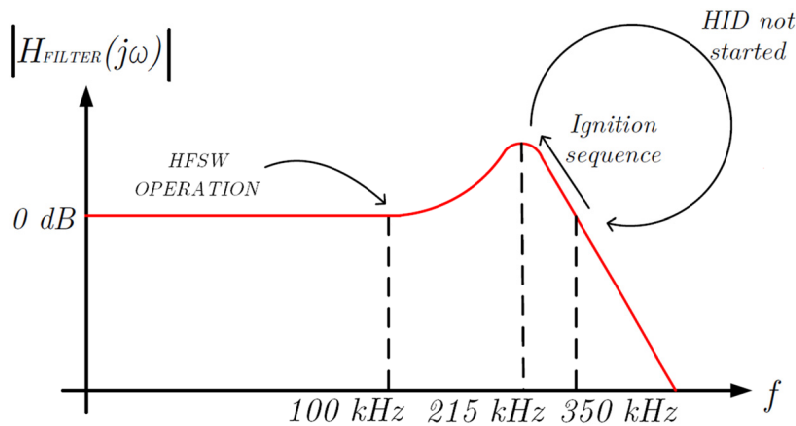


Fig 84. Start-Up transient and steady-state operation

3.2.2.1 Ignition sequence, warm-up and steady-state operation.

As depicted in Fig. 79 the inductor L_{FS} and the capacitors C_{FS} and C_{FP} act as a resonant filter before and after the lamp ignition. The resonant frequency is shown in (229). Before the



ignition, the lamp acts as an open circuit, and the resonant filter can be characterized by the transfer function shown in (231). After the ignition, in steady-state operation we take into account the HID lamp small signal impedance [38](230) in order to obtain the resonant filter transfer function in (232).

$$f_{RES} = \frac{1}{2\pi\sqrt{L_{FS} \cdot (C_{FS} \parallel C_{FP})}} \quad (229)$$

$$\hat{Z}_{LAMP}(s) = R_o \cdot \frac{\left(\frac{s}{z} + 1\right)}{\left(\frac{s}{p} + 1\right)} \quad (230)$$

$$H_{FILTER}(s) \Big|_{IGNITION}^{BEFORE} = \frac{V_{HID}(s)}{V_{AB}(s)} = \frac{1/L_{FS} \cdot C_{FP}}{s^2 + 1/L_{FS} \cdot C_{FS} + 1/L_{FS} \cdot C_{FP}} \quad (231)$$

$$\begin{aligned} H_{FILTER}(s) \Big|_{STATE}^{STEADY} &= \frac{V_{HID}(s)}{V_{AB}(s)} = \dots \\ &= \frac{\frac{s(s+z)}{L_{FS}C_{FP}}}{s^4 + s^3 \left(\frac{z + R_o C_{FP} p z}{C_{FP} R_o p} \right) + s^2 \left(\frac{L_{FS} C_{FS} z + C_{FP} R_o + C_{FS} R_o}{L_{FS} C_{FS} C_{FP} R_o} \right) + s \left(\frac{p z R_o + C_{FP} z + C_{FS} z}{L_{FS} C_{FS} C_{FP}} \right) + \frac{z}{L_{FS} C_{FS} C_{FP} R_o}} \end{aligned} \quad (232)$$

where $R_o \approx 50 \Omega$ is the steady state value of the lamp equivalent resistance, z is a positive half-plane zero (ranged from tents to hundreds of hertz) and p is a negative half-plane pole (ranged from hundreds of hertz to few kilohertz).

Assuming that the resonant frequency is 215 kHz, Fig. 85 depicts the Bode diagram of transfer function $H(s)$ after the ignition for different sets of pole and zero values for the HID lamp. Notice that after the ignition, the steady-state operation at 100 kHz is not always possible and depends on the lamp type. Nevertheless, the steady-state operation can be realized at a lower frequency, but risking to enter in the zone where AR can be excited. In addition, depending on the lamp zero or pole positions, the at steady-state frequency (100 kHz) can be less than zero dB, this implying that the lamp voltage is lower than the boost one.

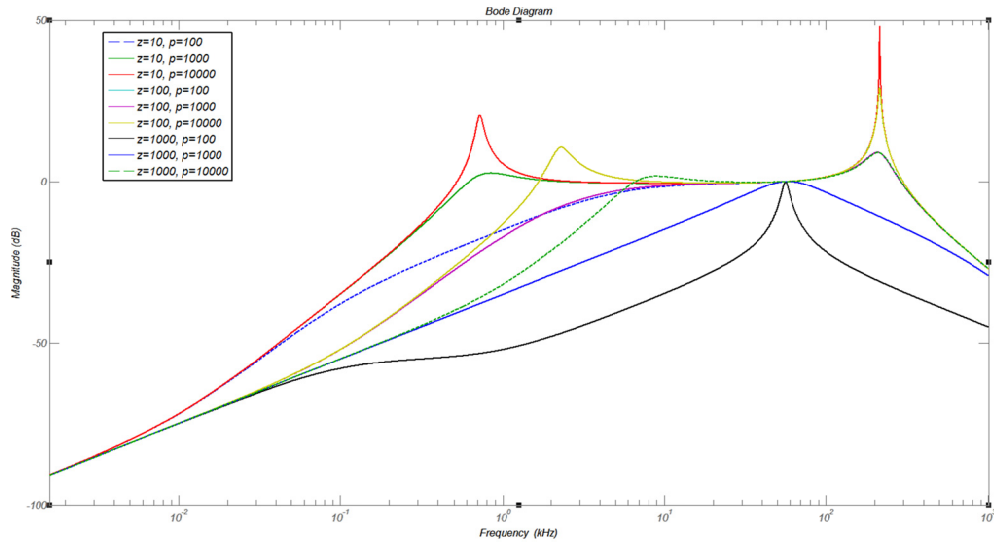


Fig 85. $H(s)_{FILTER}$ transfer function after ignition considering the lamp parameters set. $z=(1,10,100)$ Hz, and $p=(100,1000,10000)$ Hz.

3.2.3 Electronic Ballast Stability Analysis.

The interconnection of two cascaded conversion systems may provoke instability problems in some cases. To ensure the connection of the cascaded LFR with the resonant inverter we have to study the relationship between the output impedance of the first stage, and the input impedance of the second one following the classical procedure proposed by Middlebrook [146].

Assuming no input voltage perturbations in the control loop in the system presented in Fig. 83, this one can be modelled as appears in Fig. 86, where it has been added the input impedance of the second stage $Z_i(s)$ characterized by the expression (233). The output impedance of the boost converter $Z_o(s)$ is given by (234). This impedance has been calculated in the preceding section 3.2.1.1.

$$Z_i(s) = \frac{s^4 (L_{FS} C_{FS} C_{FP} R_o p) + s^3 (L_{FS} C_{FS} C_{FP} R_o p z + L_{FS} C_{FS} z) + s^2 (L_{FS} C_{FS} z p + C_{FS} R_o p + C_{FP} R_o p)}{s^3 (C_{FP} C_{FS} R_o p) + s^2 (C_{FS} z + C_{FS} C_{FP} R_o p z) + s (C_{FS} z p)} + \frac{s (C_{FS} R_o p z + C_{FP} R_o p z + z) + z p}{s^3 (C_{FP} C_{FS} R_o p) + s^2 (C_{FS} z + C_{FS} C_{FP} R_o p z) + s (C_{FS} z p)} \quad (233)$$

$$Z_o(s) = \frac{\hat{V}_c(s)}{\hat{I}_o(s)} = \frac{f}{s - e} = \frac{1/C}{s + \frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G}} \quad (234)$$

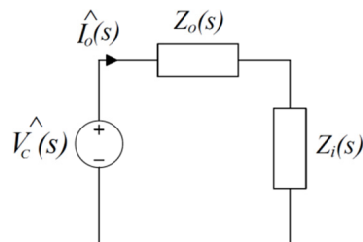


Fig 86. Electronic ballast small-signal circuit to stability analysis.



Since the first stage is stable, and considering that the second-one is a passive system (HID lamp with resonant tank), and therefore stable, the interconnection stability can be ensured by applying the Nyquist criteria to the transfer function $Z_o(s)/Z_i(s)$. Hence, it is possible to ensure the stability of the system if the following inequality is satisfied

$$\frac{|Z_o(j\omega)|}{|Z_i(j\omega)|} < 1 \quad \forall \omega \quad (235)$$

Both impedances are represented in Fig. 87 and therefore it is possible to conclude that the boost converter in cascade with the resonant inverter is always stable because the module of the impedance $|Z_i(j\omega)|$ is always above to $|Z_o(j\omega)|$, independently of the locations of zeros and poles of the lamp.

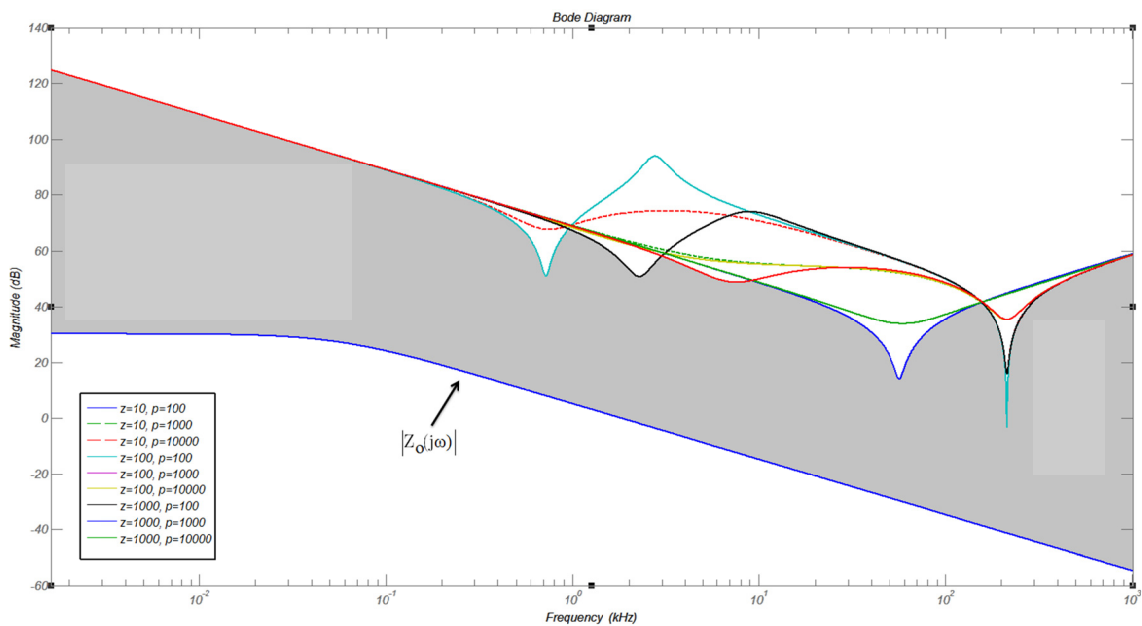


Fig 87. Modules of boost $Z_o(s)$ and resonant tank $Z_i(s)$ impedances considering $R_o=50$, and different values of lamp poles and zeros.

The preceding discussion concerns the ballast stability at steady-state operation. During the start-up, as the resonant tank is an open circuit, the lamp voltage is expected to increase until the spark level is reached. To improve the start-up, it is recommended to minimize the boost output impedance by increasing the boost output capacitor. At the resonant frequency, significantly above the boost switching frequency, the boost output impedance is determined practically by the output capacitor. As a consequence, the higher is this capacitor and lower is its equivalent impedance, the easier the ignition will be.

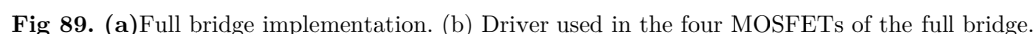
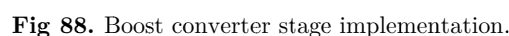
3.2.4 Electronic Ballast Implementation.

The electronic ballast implementation is composed by five different parts. The first part is an FPGA designed and developed by the Faculty of Electrical Engineering and Computer Science, in the University of Maribor (Slovenia). This FPGA has diverse devices, in order to

Besides, three power stages are developed independently, i.e. the boost converter with LFR behaviour, the full bridge inverter, and the resonant tank.

This design allows obtaining a modular electronic ballast that makes possible to change all the power stages easily.

The four different stages implemented in the prototype namely boost converter, full bridge, resonant filter and interface PCB are depicted in Fig. 88 to Fig. 91 respectively.



Dimmable Electronic ballast based on Loss-Free Resistor (LFR) approach to supply High-Intensity Discharge (HID) Lamps.

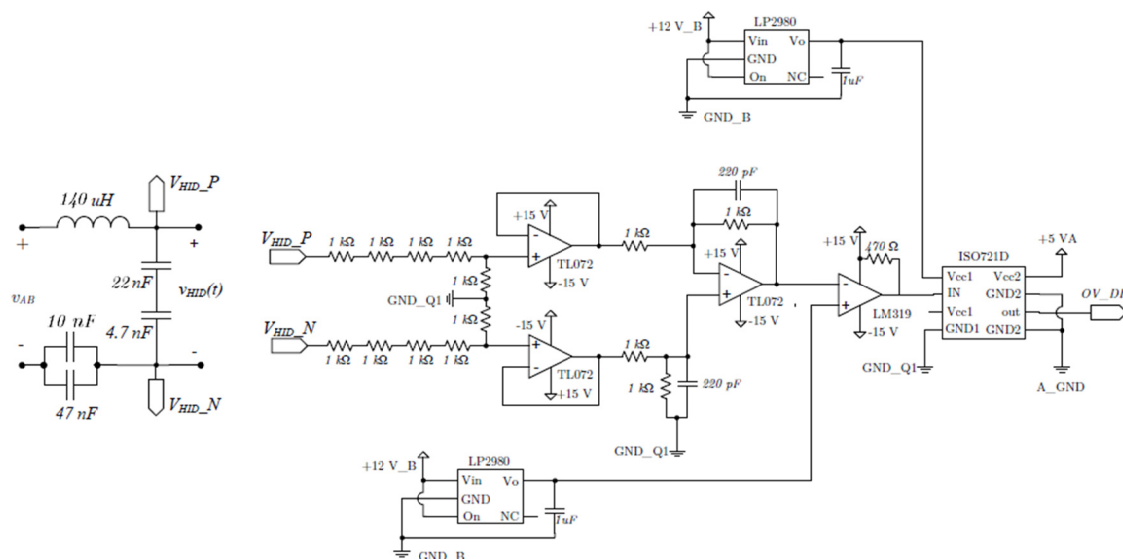


Fig 90. Resonant filter implementation and output voltage protection.

The prototype has been implemented with Si and SiC devices whose characteristics are shown in Table XIII. These characteristics illustrate the blocking voltage for the transistors and the used diode.

Table XIII. Power switches used in the boost converter.

D	C4D15120A CREE	SiC	1200 V	20 A	V_F 1.6-1.0V	C_T 1200 pF	
S_I	IRFP4768PbF International Rect.	Si	250 V	14.5mΩ (93A)	V_{th} 3V	V_g ±20V	Q_G 180nC
S_A, S_B, S_C, S_D	CMF20120D CREE	SiC	1200 V	80mΩ (42A)	V_{th} 2.65V	V_g -5/+25V	Q_G 90.8nC

The input series inductor L of 30 μ H has been realized with 40 wires of 0.07 mm² by making 11 turns around the Kool M μ 55106A2, which has a permeability of 200.

The output capacitor shown in Fig. 88, consists in a parallel connection of: one electrolytic capacitor of 47 μ F and a rated voltage of 250 V. The capacitor of 11 μ F is made by the connection of five ceramic capacitors in parallel, each one of 2.2 μ F and rated voltage of 250 V. The capacitor of 19 μ F is made by the connection of five polypropylene capacitors in parallel, each one of 4.75 μ F and rated voltage of 275 V. The capacitor of 16 μ F is made by the connection of two film capacitors in parallel, each one of 8 μ F and rated voltage of 1.2 kV. The capacitor of 10 μ F is made by the one film ceramic capacitor with a rated voltage of 250 V. Finally the capacitor of 28.5 μ F is made by the connection of six polypropylene capacitors in parallel, each one of 4.75 μ F and rated voltage of 250 V.

The input current sensor is made of an SMD resistance of 50 mΩ and 5 W, while the subtraction between the signals I_{LP} and I_{LN} are proportional to inductor current i_L .



The MOSFET driver is made up of three different elements, namely a voltage regulator, an isolator and the own driver. The voltage regulator LP2980 supplies each isolator ISO721D with its own voltage. Each regulator, in turn, is supplied by an individual voltage of 12 V and ground. On the one hand, the input of the isolator is supplied with 5V provided by the FPGA, and on the other hand is also supplied by means of the regulator, in order to isolate the FPGA signals of the power signals. The other input of the driver is the PWM1 that provides the control signal to the boost converter. The corresponding output of the isolator sends the signal to the driver (LM5112), which has in its output an on resistance of 10Ω to charge the gate, and other resistance of the same value to discharge the gate.

The MOSFET drivers used in the full bridge are the same than in the boost converter as shown in Fig. 89 (b). As these drivers are isolated, it is not necessary to use a specific high-side and low-side drivers.

The resonant tank is depicted in Fig. 90 where the series inductor (L_{FS}) of $140 \mu\text{H}$ has been realized with 15 wires of 0.07 mm^2 by making 17 turns around the Molypermalloy 55868-A2, which has a permeability of 26. The parallel capacitor (C_{FP}) consists in two polypropylene capacitors in series of 4.7 nF and 22 nF respectively with a rated voltage of 2 kV each one. The series capacitor (C_{FS}) consists in two polypropylene capacitors in parallel of 47 nF and 10 nF respectively with a rated voltage of 1 kV each one.

Moreover, it can be observed in Fig. 90 the signal sent to the FPGA if the lamp voltage is higher than 3.3 kV . The lamp voltage is measured by means of a differential amplifier made by three TL072 AOs with a bandwidth of 3 MHz and slew rate of $13 \text{ V}/\mu\text{s}$. Subsequently, this voltage is compared by means a LM319, so that if this voltage is higher than a reference signal provided by an LP2980 (3.3 V), the LM319 will send a signal to the ISOLATOR and the latter to the FPGA. Like in the MOSFETs drivers, the ISOLATOR ISO721D separates the FPGA signals from the power signals.

3.2.4.2 Control Stage.

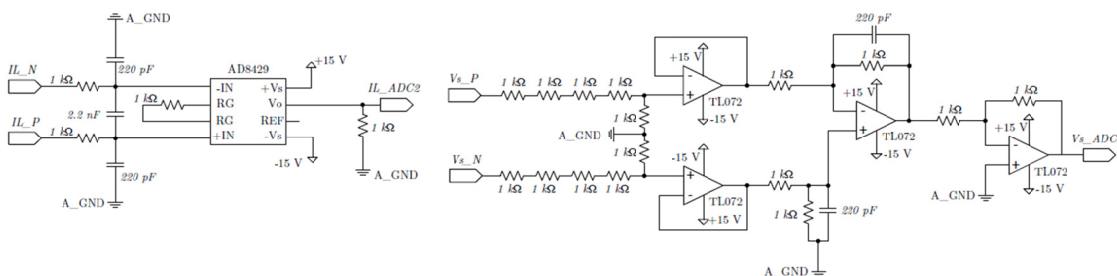


Fig 91. Input current and voltage measurements implementation.

The measured signals IL_N and IL_P in the power stage are amplified by a differential amplifier model A8429 with a bandwidth of 15 MHz , and a slew rate of $22 \mu\text{s}$. The output of the AD8429 is proportional to inductor current i_L . Moreover the input voltage is measured by



means a connection of 4 TL072 AO. This two measured signals are connected to the ADC2 and ADC1 converters respectively.

3.2.4.3 FPGA Controller.

This subsection presents how the FPGA controls the boost converter and the full bridge inverter. Both flowcharts appear in Figs. 92 and 93 respectively.

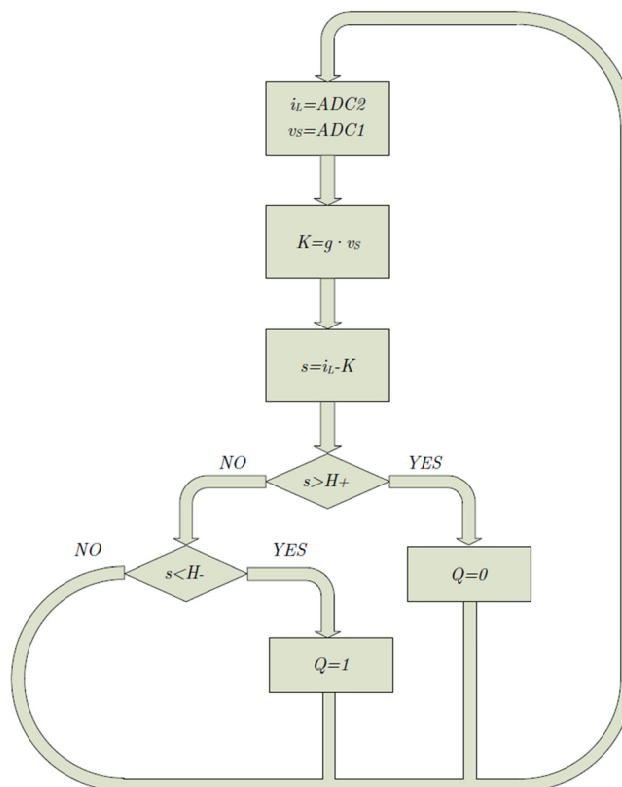


Fig 92. Flowchart of the switching algorithm implemented in the FPGA for the boost converter with LFR behaviour.

Fig. 92 shows the flowchart of the hysteretic control implemented in the FPGA. Each 250 ns the ADC2 and ADC1 obtain a new value of i_L and v_S respectively. Then, the input voltage v_S is multiplied by a reference conductance G in order to obtain the input current level reference K . Then the measured sliding surface S is i_L subtracted to K . Finally, a comparison is made, i.e. if the surface S is higher than a hysteretic positive band $H+$ the output signal Q that activates the MOSFET will be set to zero; if the resulting sliding surface S is lower than a hysteretic negative band $H-$ the output signal Q will be set to one.

Fig. 93 shows the flowchart of the full bridge inverter. First, the control checks if the lamp is ON. If the lamp has not started, the soft start transient will begin loading a counter with the necessary value to switch the full bridge at 350 kHz. Then, it is checked again if the lamp is turned ON. Then, if the lamp has not started, the soft start counter will be increased in order to reduce the switching frequency in steps of 5 kHz each time, until the lamp starts or the counter reaches its maximum value (corresponding to 215 kHz). Then, it is checked again if the



lamp has started. If the counter achieves its maximum value and the lamp has not started, the soft start sequence is repeated loading the ignition counter with the value corresponding to the 350 kHz. If in some check, the lamp has started, the counter is loaded with the corresponding value to switch the full bridge at HFSW.

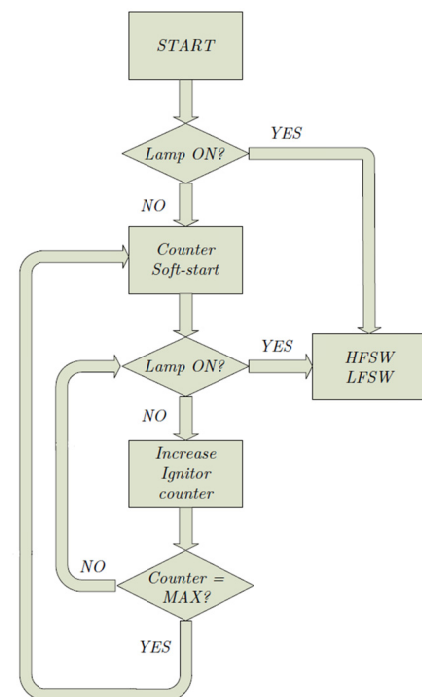


Fig 93. Flowchart of the full bridge soft-start and steady-state operation.

3.2.5 Experimental Results.

The designed electronic ballast and the FPGA used to obtain the experimental results are shown in Fig. 94, in which the HID lamp (SYLVANIA SHP-T 150W Basic Plus) is working at the nominal power of 150 W.

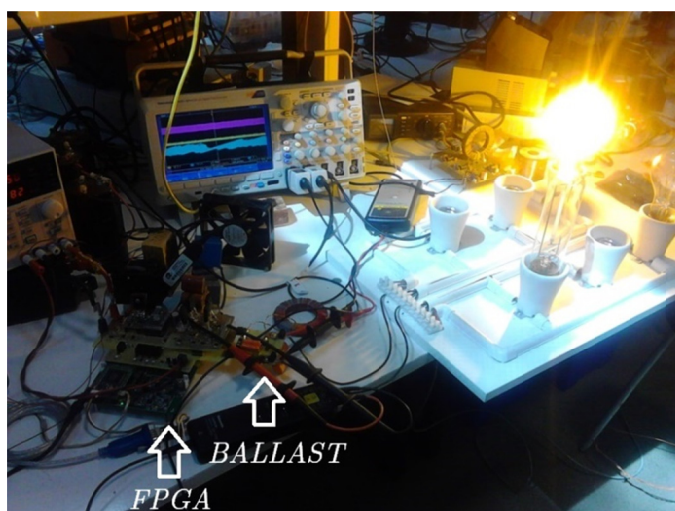


Fig 94. Electronic Ballast with LFR to supply HID lamps experimental prototype.



3.2.5.1 High-Frequency sinusoidal waveform operation results.

The first experimental results correspond to the start-up transient when the HID lamp is connected at the output of the electronic ballast. In this case it is possible to appreciate how the lamp voltage (v_{HID}) is increasing until a peak of 1.7 kV is reached, switching at 230 kHz approximately. At this moment the lamp is started and the warm-up operation starts. It can be observed that when the lamp is started, the voltage decrease below its nominal value in steady-state operation due to the HID characteristic impedance. Moreover, after the ignition, it is possible to appreciate how the current (i_{HID}) starts to flow through the HID.

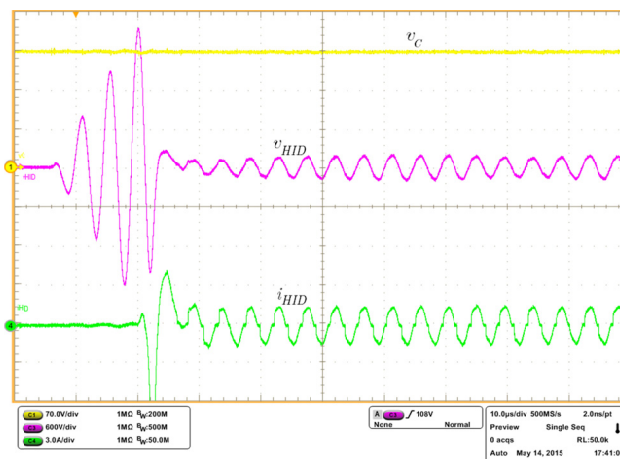


Fig 95. Start-up transient.

Fig. 96 shows the warm-up operation, occurred after the lamp ignition. As previously mentioned, after the spark is generated the lamp voltage decreases under its nominal value in steady-state operation. Similarly, the lamp current begins to flow when the lamp has started, and is above the final value in steady-state operation. A good LFR behaviour of the converter (delivering always the same power during all the warm-up operation) is observed due to the automatic adjustment of voltage and current independently of the HID impedance, showing how the lamp voltage and current reach its nominal value in steady state.

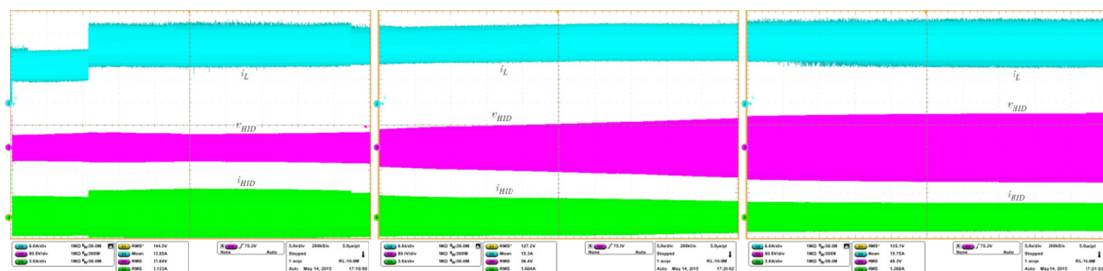


Fig 96. Warm-up operation of the electronic ballast in HFSW.

Finally, Fig. 97 shows the steady-state operation after the warm-up. It is possible to appreciate that the lamp voltage v_{HID} is about 100 V and the lamp current i_{HID} about 1.89 A, which means a power of 190 W approximately. We have supplied the lamp at 190 W instead of



4 Dimmable electronic ballast with LFR behaviour to supply Induction Electrode-less Lamps (IEFL).

4.1 Introduction

This section presents the analysis and design of an electronic ballast for induction electrode-less fluorescent lamps (IEFLs). The ballast is planned to supply a 150 W IEFL at 234 kHz with dimming capability. The proposed topology consists in a single stage boost converter powered from a low DC voltage (12 V- 14 V), employed as control power stage, with a resonant inverter in cascade. The inverter will supply the lamp at a high frequency AC voltage, and deliver the high voltage gain necessary to start the lamp. Sliding-mode control theory is applied to analyze the dynamic behaviour of the boost switching regulator and to establish the system stability. The control technique allows the converter to behave as a Loss-Free Resistor (LFR) delivering the desired power to the lamp with dimming capability. The experimental results demonstrate the feasibility of the proposed ballast achieving a 50% lamp-power dimming (60 W), with a global efficiency about 93% at nominal power lamp.

The block diagram of the proposed electronic ballast is shown in Fig.98. A boost converter with LFR behaviour controlled with sliding- mode control is connected to an $L_S C_S C_P$ full bridge resonant inverter with a switching frequency of 234 kHz. The boost converter is supplied by a low DC voltage between 12 -14 V, but the inclusion of the $L_S C_S C_P$ resonant inverter allows the ballast to start and deliver the desired power to the IEFL regardless of the lamp impedance. The ballast analysis is performed in detail to assure the ballast stability, and the lamp operation at diverse power ratings.

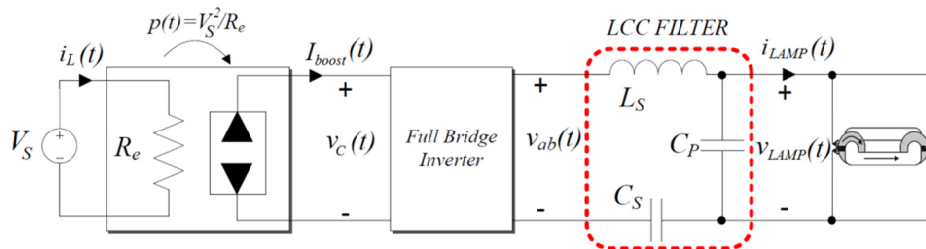


Fig 98. Electronic Ballast block diagram with boost LFR.

4.2 IEFL Electrical Equivalent Model.

The IEFL model used in this design is an ENDURA lamp (150 W) from OSRAM. First of all, diverse tests have been made with a commercial ballast to see the lamp operation at full power (150 W), which has shown that the commercial ballast switches around 234 kHz. Then, the stage responsible to supply the AC voltage to the IEFL will switch at this frequency.

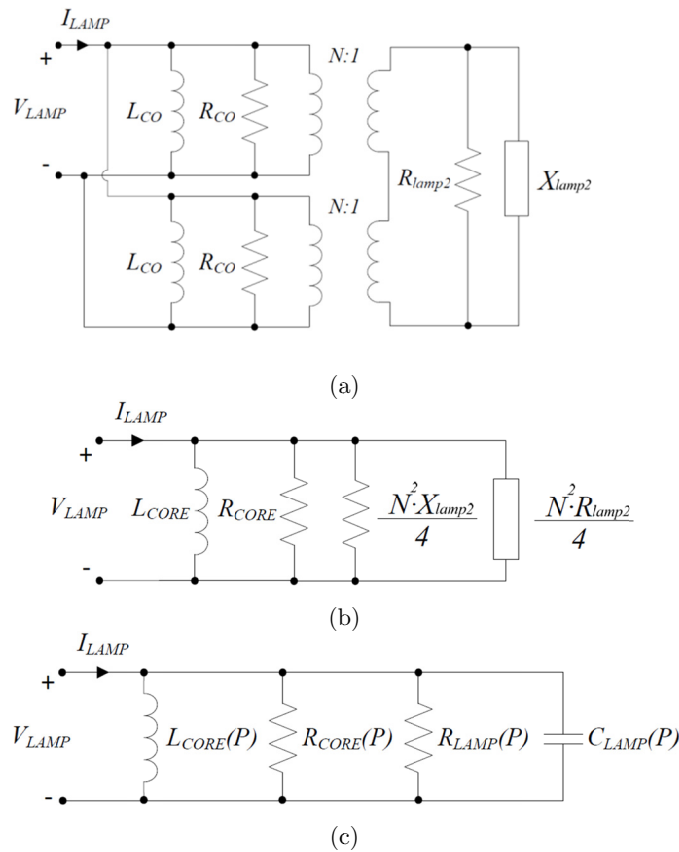


Fig 99. (a) IEFL Electrical Equivalent Model. (b) Model with the lamp parameters referred to the primary. (c) IEFL simplified model considering the lamp core parameters [59].

The electrical equivalent model of the IEFL has been the subject of several papers [49, 148], although a more detailed model has been reported in [59]. In this section, we will try to achieve a light regulation considering the latter model. The external lamp coils behave as a primary winding of a transformer and the load of the secondary winding coincides with the inner plasma of the discharge bulb. Hence, as depicted in Fig. 99(a), the secondary winding can be represented as a plasma resistance (R_{LAMP2}) in parallel with an equivalent reactance (X_{LAMP2}). These values are reflected in the primary side of the transformer with a coupling factor close to unity [149], as shown Fig. 99 (b).

In [59] the IEFL capacitive behaviour was introduced in the electrical equivalent model, in which this type of behaviour was explained by the lamp geometry and coil capacitance [150, 151]. This electrical model is the accurate model that appears in the current literature, because it clearly distinguishes the physical phenomena that occur in the lamp in terms of capacitive, inductive and resistive effects. Fig. 99 (c) shows this model referred to the primary side of the transformer, where the plasma resistance (R_{LAMP}), the lamp capacitance (C_{LAMP}), the core inductance (L_{CORE}) and finally the core resistance (R_{CORE}) are represented.

As a consequence, considering the procedure presented in [59], diverse polynomial regression functions have been employed to determine the equations that represent the IEFL parameters variation as a function of its real power. In a clear-cut contrast, all the parameters here are considered as a function of the power. Equation (236) shows the polynomial function



for $R_{LAMP}(P)$, equation (237) for $R_{CORE}(P)$, equation (238) for $C_{LAMP}(P)$, and equation (239) for the $L_{CORE}(P)$.

$$R_{LAMP}(P) = \sum_{j=0}^m A_j \cdot P^j \quad (236)$$

$$R_{CORE}(P) = \sum_{j=0}^m B_j \cdot P^j \quad (237)$$

$$C_{LAMP}(P) = \sum_{j=0}^m C_j \cdot P^j \quad (238)$$

$$L_{CORE}(P) = \sum_{j=0}^m D_j \cdot P^j \quad (239)$$

The values of the different coefficients are presented in Tables XIV, XV, XVI, and XVII respectively.

Table XIV. $R_{LAMP}(P)$ Calculated Data.

Coefficients	Values
A_0	14117.233215013 Ω
A_1	-443.950488282 Ω/W^1
A_2	5.493256119 Ω/W^2
A_3	-0.030667550 Ω/W^3
A_4	64.361976873 $\mu\Omega/W^4$

Table XV. $R_{CORE}(P)$ Calculated Data.

Coefficients	Values
B_0	8804.849133877 Ω
B_1	1088.916103851 Ω/W^1
B_2	-16.900193211 Ω/W^2
B_3	110.405406941 $m\Omega/W^3$
B_4	-264.550606589 $\mu\Omega/W^4$

Table XVI. $C_{LAMP}(P)$ Calculated Data.

Coefficients	Values
C_0	494.002399899 pF
C_1	-7.686979613 pF/W ¹
C_2	196.722252662 fF/W ²
C_3	-2.372495175 fF/W ³
C_4	8.392864473 aF/W ⁴

Table XVII. $L_{CORE}(P)$ Calculated Data.

Coefficients	Values
D_0	972.131645679 μH
D_1	-17.681495843 $\mu H/W^1$
D_2	307.799162275 nH/W ²
D_3	-2.359976783 nH/W ³
D_4	6.167635098 pH/W^4

Besides, Figs. 100, 101, 102 and 103 show respectively the variation of the plasma resistance, core resistance, capacitance and core inductance as a function of the lamp active power.

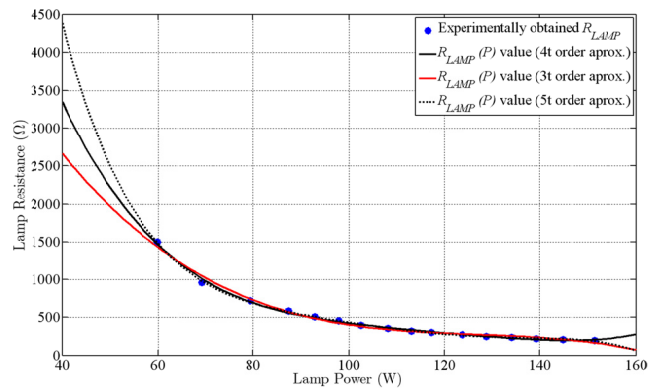


Fig 100. R_{LAMP} as function of the lamp active power.

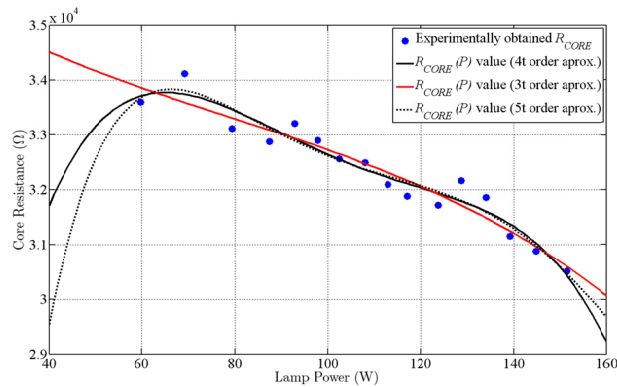


Fig 101. R_{CORE} as function of the lamp active power.

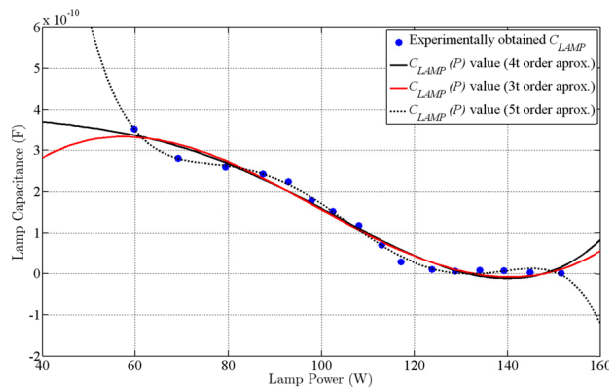


Fig 102. C_{LAMP} as function of the lamp active power.

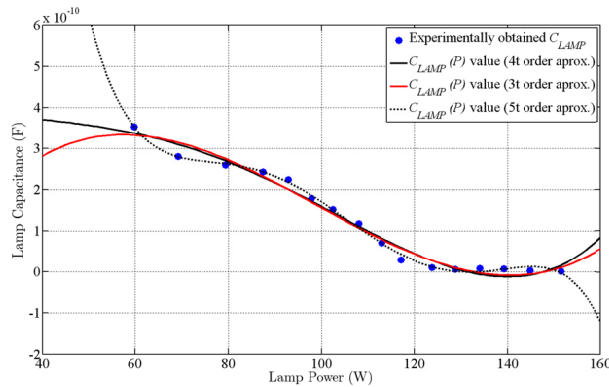


Fig 103. L_{CORE} as function of the lamp active power.

4.3 LFR Based Dimming Methodology

As mentioned in the first chapter, the IEFL light regulation can be achieved by diverse methods as frequency modulation [152], PWM modulation [18], changing the output filter parameters [153], or controlling the bus voltage [55]. As in the other cases reported in the previous chapters, we will take advantage of the LFR characteristics in order to supply an IEFL with dimming capability and deliver the desired power to the lamp independently of the lamp impedance.



Therefore, a LFR is proposed to supply an IEFL from a low voltage DC battery (12 – 14 V) as depicted in Fig. 104, where $I_{BOOST}(t)$ is the current that the boost converter delivers to the resonant inverter.

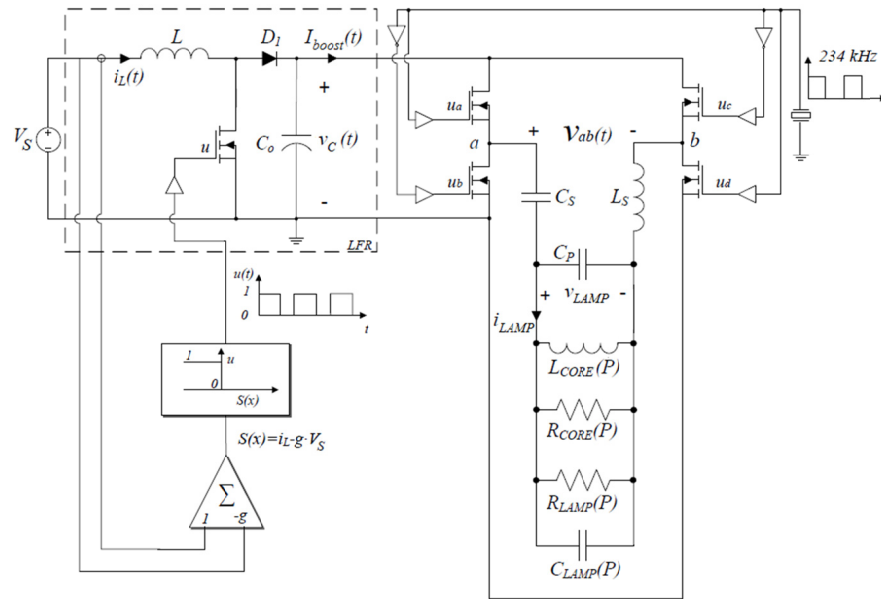


Fig 104. Total ballast block diagram. Boost converter with $L_s C_s C_p$ full bridge inverter and IEFL Electrical Equivalent Model.

As the ballast is supplied at a given constant DC power, lamp dimming can be easily made by adjusting the LFR input equivalent resistor R_e showed in Fig. 98. Neglecting converter efficiency issues, the lamp voltage and current are automatically self-adjusted to ensure that the lamp active power equals to the input DC power.

In this case, as depicted in Fig. 104, introducing the corresponding sliding surface (240) in the converter, and modifying the converter conductance “g” (241), allow determining the maximum and minimum (242) DC power absorbed by the converter, or equivalently the power delivered to the lamp.

$$s(x) = i_L - g \cdot V_S \quad (240)$$

$$g = 1/R_e \quad (241)$$

$$g_{MAX} = P_{MAX} (150W) / V_S^2, \quad g_{MIN} = P_{MAX} (60W) / V_S^2 \quad (242)$$

4.3.1 Sliding Mode converter Analysis.

Note that the boost converter with LFR behaviour controlled by means of sliding mode control presented in this section is the same converter presented in subsection 3.2.1. Therefore, the control to output transfer function $H(S)$ will be expressed as in (243), which corresponds to a stable system because condition (244) is always satisfied.



$$H(s) = \frac{\hat{V}_C(s)}{\hat{G}(s)} = \frac{a + s \cdot b}{s - e} = \frac{\frac{I_{BOOST}}{C \cdot G} \cdot s \cdot \frac{L \cdot I_{BOOST}}{C}}{s + \frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G}} \quad (243)$$

$$\frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G} > 0 \quad (244)$$

4.4 $L_s C_s C_P$ Resonant Inverter Analysis

In the technical literature there are some works analysing the role of $L_s C_s C_P$ resonant filters of an electronic ballast for an IEFL [54] considering the dimming operation, but these studies don't take into account the complete IEFL model reported in [59].

For this reason, in this section an analysis of the $L_s C_s C_P$ resonant inverter is carried out considering the complete model of [59]. The analysis takes into account the full bridge inverter with the resonant filter and the IEFL accurate electrical model as shown in Fig. 104, where the full bridge is working at 234 kHz and

$$C_P(P) = \frac{R_C + R_L}{\omega \cdot R_C \cdot R_L} \cdot \sqrt{\frac{P \cdot R_C \cdot R_L}{V_{AB} \cdot (R_C + R_L)}} \cdot (1 + \tan^2(\phi)) - 1 + \frac{1}{L_C \cdot \omega^2} - C_L \quad (245)$$

$$L_s(P) = \frac{\tan(\phi) \cdot R \cdot L_C - R \cdot \omega \left(C_P - C_P - C_C + \frac{1}{\omega^2 \cdot L_C} \right)}{\omega^3 \cdot R^2 \cdot L_C \cdot [(C_P + C_C)^2] - 2\omega R^2 \cdot (C_P + C_C)} + \frac{1}{C_s \cdot \omega^2} \quad (246)$$

where

$$R = \frac{R_C \cdot R_L}{R_C + R_L} \quad (247)$$

and $R_L = R_{LAMP}(P)$, $R_C = R_{CORE}(P)$, $C_L = C_{LAMP}(P)$, $L_C = L_{CORE}(P)$, ϕ is the phase shift between voltage and current for a given power, V_{AB} is the applied voltage in the half-bridge output, and ω is the angular frequency determined by $2 \cdot \pi \cdot f$, where f is the lamp switching frequency, 234 kHz in this particular case.

As usually the series capacitor C_s value is selected to be around 10-20 times the value of the parallel capacitor C_P .

Hence, the aim of the study presented in this section is to show the influence of the lamp parameter variation in the $L_s C_s C_P$ response.

4.4.1 $L_s C_s C_P$ response under dimming operation.

The ballast allows a light intensity regulation, so the electrical lamp parameters will change as a function of the lamp power. Now, the main idea of this section is to evaluate how the parameters variation affects the electronic ballast.

From the obtained values of the electrical equivalent model and the rest of the components of the resonant filter, the total impedance of the resonant filter $Z_T(s, P)$ can be obtained as function of the lamp power.



$$Z_T(s, P) = Z_s(s) + Z_p(s, P) \quad (248)$$

Where $Z_p(s, P)$ is the parallel impedance, and $Z_s(P)$ is the series impedance, as shown the Fig. 105, and represented by (249) and (250) respectively.

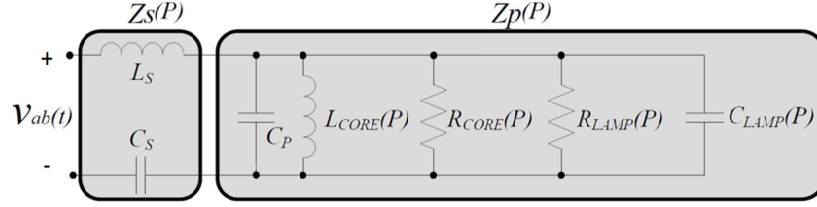


Fig 105. Filter and IEFL Electrical equivalent model impedances.

$$Z_s(s) = \frac{s^2 \cdot L_s \cdot C_s + 1}{s \cdot C_s} \quad (249)$$

$$Z_p(s, P) = \frac{s \cdot R_L \cdot R_C \cdot L_C}{s^2 \cdot R_C \cdot R_L \cdot L_C \cdot (C_P + C_L) + s \cdot L_C \cdot (R_C + R_L) + R_C \cdot R_L} \quad (250)$$

Now, the resonant inverter transfer function can be represented as follows

$$H(s) = \frac{V_{LAMP}(s)}{V_{AB}(s)} = \frac{Z_p(s, P)}{Z_p(s, P) + Z_s(s)} \quad (251)$$

The resonant tank values C_s , C_p , and L_s , are calculated taking into account the nominal lamp power (150 W), and the phase angle of the load for this power level. Therefore, the final transfer function with all the lamp and resonant tank parameters is expressed in (252), whose module and phase representation are illustrated in Fig. 106.

$$H(s) = \frac{s^2}{L_s(C_L + C_P) \left[s^4 + s^3 \left(\frac{R_L + R_C}{(R_L R_C)(C_L + C_P)} \right) + s^2 \left(\frac{1}{L_C(C_P + C_L)} + \frac{1}{C_s L_s} + \frac{1}{L_s(C_P + C_L)} \right) \right]} + \frac{s^2}{L_s(C_L + C_P) \left[s \left(\frac{R_L + R_C}{R_L R_C C_s L_s (C_P + C_L)} \right) + \frac{1}{L_C C_s L_s (C_P + C_L)} \right]} \quad (252)$$

Diverse conclusions can be extracted from Fig.106. First, it is possible to see that the lower is the power delivered to the lamp, the higher is the resonant tank gain. This fact comes from the incremental negative impedance lamp behaviour depicted in Fig. 107, which shows that the lamp voltage V_{LAMP} is higher when the lamp is supplied at lower powers than the nominal one. As previously advanced in other publications [148], this phenomenon corroborates the fact that the resonant tank gain is ideally infinite when the lamp is off, which allows to achieve the necessary high voltage to start the lamp (approximately 1 kV, as shown in the next section).

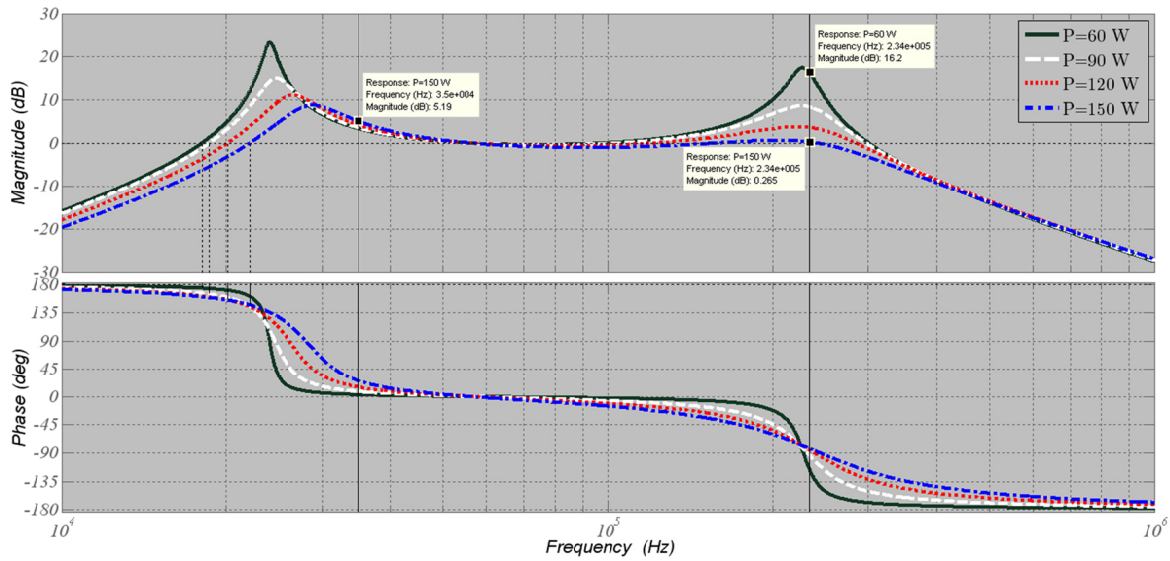


Fig 106. $L_S C_S C_P$ Resonant inverter Bode diagram for different lamp power levels.

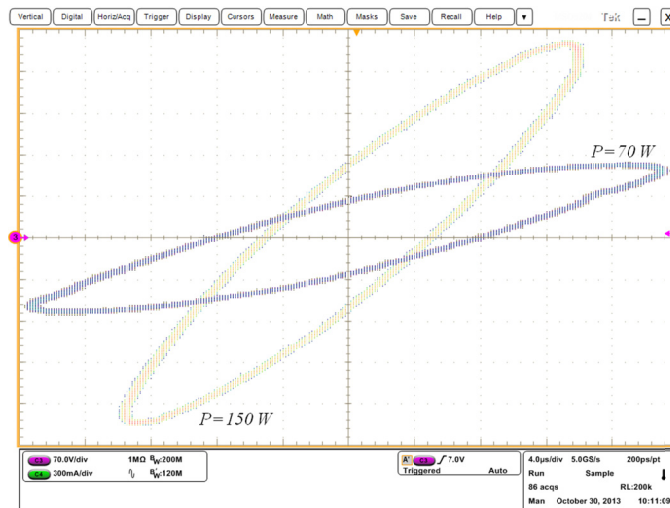


Fig 107. Measured I-V curve of the IEFL Endura 150 W.

Secondly, notice that analysing the transfer function reveals two resonant frequencies that can be considered as separable poles (253)(254) depending on L_S, C_S , and L_S, C_P, C_L respectively.

$$f_{RL} = \frac{1}{2 \cdot \pi \sqrt{L_C(P) \cdot C_S}} \quad (253)$$

$$f_{RP} = \frac{1}{2 \cdot \pi \sqrt{(C_P + C_L(P)) \cdot L_S}} \quad (254)$$

As shown Fig. 106, the peak of both resonant frequencies varies as a function of the lamp power, because this power variation causes changes in the electrical lamp parameters. In addition, the resonant inverter behaviour can be modified by replacing the filter parameters to obtain a desired response and gain for a given power.



Thirdly, it is important to remark that the peak resonance that appears at low frequency (≈ 20 kHz) imposes that the boost converter with LFR behaviour must be designed to switch beyond 35 kHz at 150 W to avoid some resonances

Finally, the theoretical gain achieved by the resonant inverter as a function of the power delivered to the lamp at it appropriate switching frequency (234 kHz) is presented in Table XVII and calculated by means of (255)

$$G = 10^{\frac{|H(j\omega)|_{dB}}{20}} \quad (255)$$

Table XVIII. Resonant Inverter Gain as a Lamp Power Function.

Lamp Power	60 W	90 W	120 W	150 W
$ H(j\omega) _{dB}$	0.265	8.45	3.62	16.2
Gain G	1.03	2.64	1.51	6.45

4.5 Electronic Ballast Stability Analysis

As in the case presented in subsection 3.2.3, it is necessary to corroborate that the two cascaded conversion systems presented are not producing instability problems in the interconnection. Hence, the classical procedure presented by Middlebrook is used as in the previous chapter to corroborate the electronic ballast stability.

Therefore, assuming that the boost converter with LFR is the same, it is possible to consider that without input voltage perturbations in the control loop in the system presented in Fig. 83, this one can be modelled as illustrated in Fig. 108. In this figure, $Z_i(s)$ represents the input impedance of the second stage $Z_i(s)$ characterized by expression (256) and $Z_o(s)$ is the output impedance of the boost converter given by (257)

$$Z_i(s) = \frac{s^4 L_s C_s R_C R_L L_C (C_P + C_L) + s^3 C_s L_s L_C (R_C + R_L) + s^2 R_C R_L L_C (C_P + C_L) + s L_C (R_C + R_L) + R_C R_L}{s C_s (s^2 R_C R_L L_C (C_P + C_L) + s L_C (R_C + R_L) + R_C R_L)} + \frac{s^2 R_C R_L (C_s L_s + L_C (C_L + C_P + C_s)) + s L_C (R_C + R_L) + R_C R_L}{s C_s (s^2 R_C R_L L_C (C_P + C_L) + s L_C (R_C + R_L) + R_C R_L)} \quad (256)$$

$$Z_o(s) = \frac{\hat{V}_c(s)}{\hat{I}_o(s)} = \frac{f}{s - e} = \frac{1/C}{s + \frac{I_{BOOST}^2}{C \cdot V_s^2 \cdot G}} \quad (257)$$

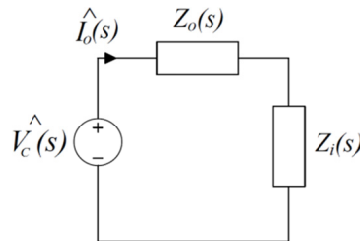


Fig 108. Electronic ballast small-signal circuit to stability analysis.



Assuming now that the first stage is stable, and considering that the second-one is a passive system (IEFL lamp with resonant tank) and therefore stable, the interconnection stability can be ensured by applying the Nyquist criteria to the transfer function $Z_o(s)/Z_i(s)$. It is possible to ensure the stability of the system if the following inequality is satisfied

$$\frac{|Z_o(j\omega)|}{|Z_i(j\omega)|} < 1 \quad \forall \omega \quad (258)$$

Both impedances are represented in Fig. 109, where it is possible to conclude that the boost converter in cascade with the resonant inverter is always stable because the module of the impedance $|Z_i(j\omega)|$ is always above to $|Z_o(j\omega)|$, independently of the power supplied to the lamp. Here it is considered that the lamp is supplied by four different powers (60, 90, 120 and 150 W), so that in all the cases the interconnection of the two stages is stable.

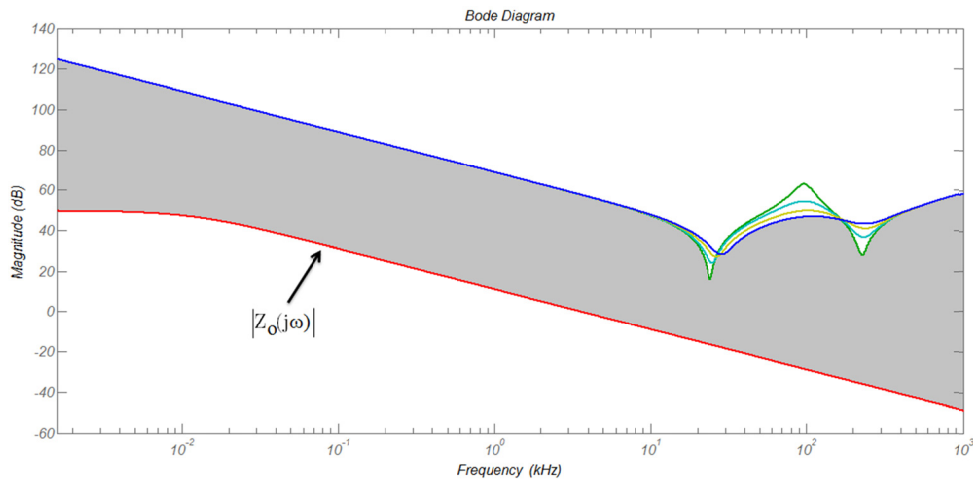


Fig 109. Electronic ballast impedance stability analysis.

4.6 Electronic Ballast Implementation.

4.6.1 Boost converter design.

Figs. 110 and 111 show the circuit scheme of the power stage and sliding-mode controller respectively.

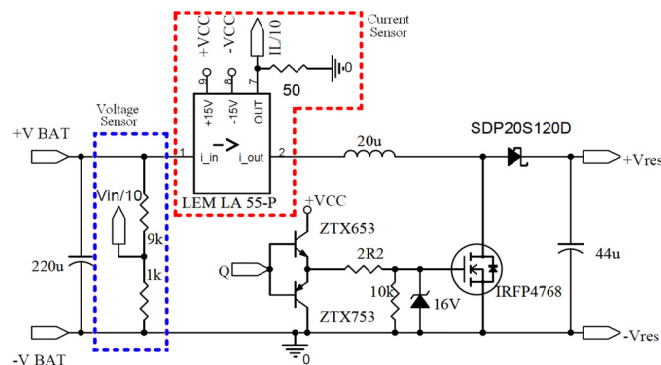


Fig 110. Power stage circuit scheme of the proposed boost-based LFR.

Dimmable electronic ballast with LFR behaviour to supply Induction Electrode-less Lamps (IEFL).



The main switch is based on the complementary action of diode D1 (SDP20S120D), and MOSFET Q1 (IRFP4768PBF), which is activated by a driver. It has to be pointed out that signal Q in Fig. 110 is the output of the hysteretic comparator represented in Fig. 111. It can be observed that the driver is realized by two bipolar transistors, a npn transistor (ZTX 653) with a V_{ce} of 100 V and a collector current of 2 A, and a pnp transistor (ZTX 753) with an V_{ce} of 100 V and a current of -2 A. The MOSFET gate resistance is realized by an E24 resistor of $2.2\ \Omega$ and the protection parallel resistance and zener are an E24 $10\ \text{k}\Omega$ and C16PH (16 V) diode respectively.

The input series inductor of $20\ \mu\text{H}$ has been realized with 50 wires of $0.07\ \text{mm}^2$ by making 17 turns around the Kool M μ 77109-A7, which has a permeability of 125. It is necessary to remark that the use of 50 wires instead of 1 intends to reduce the skin effect when the switching frequency of the converter increases beyond 40 kHz.

The output capacitor is made by two polypropylene capacitors of $20\ \mu\text{F}$, each one (EPCOS B32926E3206M) with a breaking voltage of 500 V in parallel with four SMD ceramic capacitors of $1\ \mu\text{F}$ (AVX 1825PC105AT1A) with a rated voltage of 300 V.

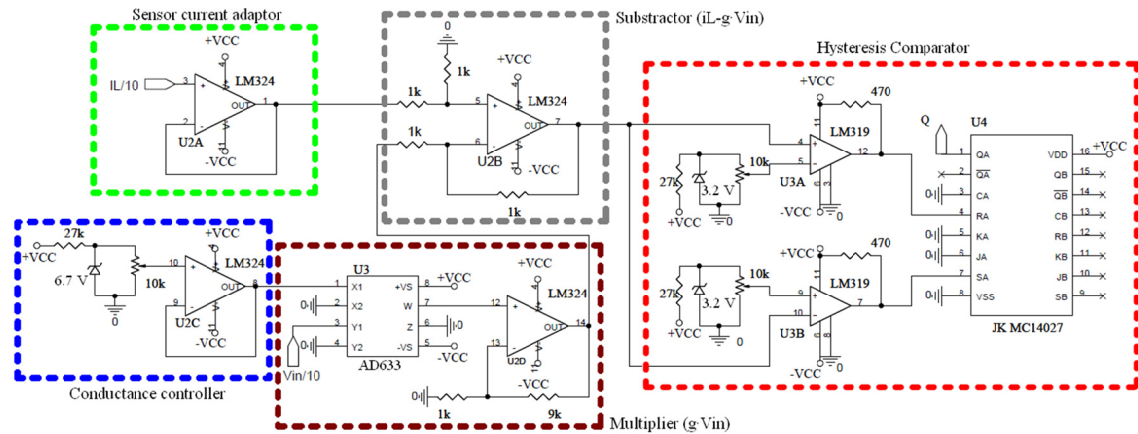


Fig 111. Sliding-mode controller circuit scheme.

The input voltage is sensed by a voltage divider ($9\ \text{k}\Omega$ - $1\ \text{k}\Omega$) and the input current sensor is made up with a Hall Effect transducer model (LEM-LA-55P) with a bandwidth of 200 kHz. Signals $V_{in}/10$ and $I_L/10$ are proportional to the input voltage V_s and inductor current i_L respectively.

Fig. 111 shows the main blocks of the sliding-mode controller, namely conductance controller, sensor current adaptor, multiplier block, subtracting block, and hysteretic comparator. The conductance controller has been implemented by a potentiometer to adjust the conductance “ g ”.

The hysteretic circuit employs two LM319 comparators with a response time of 80 ns, and a JKMC14027 flip flop with a bandwidth of 13 MHz. The input of the hysteretic comparator is $s(x) = i_L \cdot g \cdot V_s$, which is given by the output of the subtracting block based on



LM324. The inputs in this block are given by the output of the sensor current adaptor, and by the output of the multiplier block, based on a multiplier AD633 with a slew rate of 20 V/ μ s and with a non-inverting amplifier realized with a LM324.

The output of the hysteretic comparator is a digital signal Q which activates the driver to turn on or turn off the power transistor. The transistor turn on corresponds to the high level of Q, and the transistor turn off corresponds to the Q low level.

4.6.2 $L_S C_S C_P$ Resonant Inverter Design.

Fig. 112 shows the circuit scheme of the $L_S C_S C_P$ resonant inverter power stage, and the necessary logical circuitry to activate both high- and low-side MOSFETS introducing delays to avoid short circuits in the half-bridge.

The full bridge employs four MOSFETs (IRFP4768PBF) that are represented by M2 to M5. The four switches have an E24 gate resistance of 5 Ω . Moreover, every switch has the protection parallel resistance and Zener, namely an E24 1 k Ω resistor and a C16PH (16 V) diode. Each bridge branch is activated by driver IR2110. It has to be pointed that the input digital signals for IR2110 (Hin, Lin, Hin2, and Lin2) are given by the logical circuitry represented in the same figure. For each branch the logical circuitry is composed by 4 NOR gates (4001), and two delay blocks realized by means of a RC filter of 1k Ω resistance in parallel with a 1N418 diode and with a 1 nF capacitor. The delay block guarantees that the MOSFETs of the same branch are never activated at same time, thus provoking a short circuit. The first NOR gate (U7A) receive the signal of 234Hz generated by an oscillator (High), and the high and low signal (Hin/Lin) supplied by the logical circuitry are connected at the input of the IR2110 driver.

In the $L_S C_S C_P$ resonant tank, the series inductor (L_S) of 140 μ H is realized with 15 wires of 0.07 mm² by making 17 turns around the Molypermalloy 55868-A2, which has a permeability of 26. The series capacitor (C_S) consists in two polypropylene capacitors in parallel of 47 nF and 10 nF (VYSHAY) with a rated voltage of 2 kV each one. Finally, the parallel capacitor (C_P) is realized by connecting two polypropylene capacitors in series of 47 and 4.7 nF with a rated voltage of 2kV each one.

Dimmable electronic ballast with LFR behaviour to supply Induction Electrode-less Lamps (IEFL).

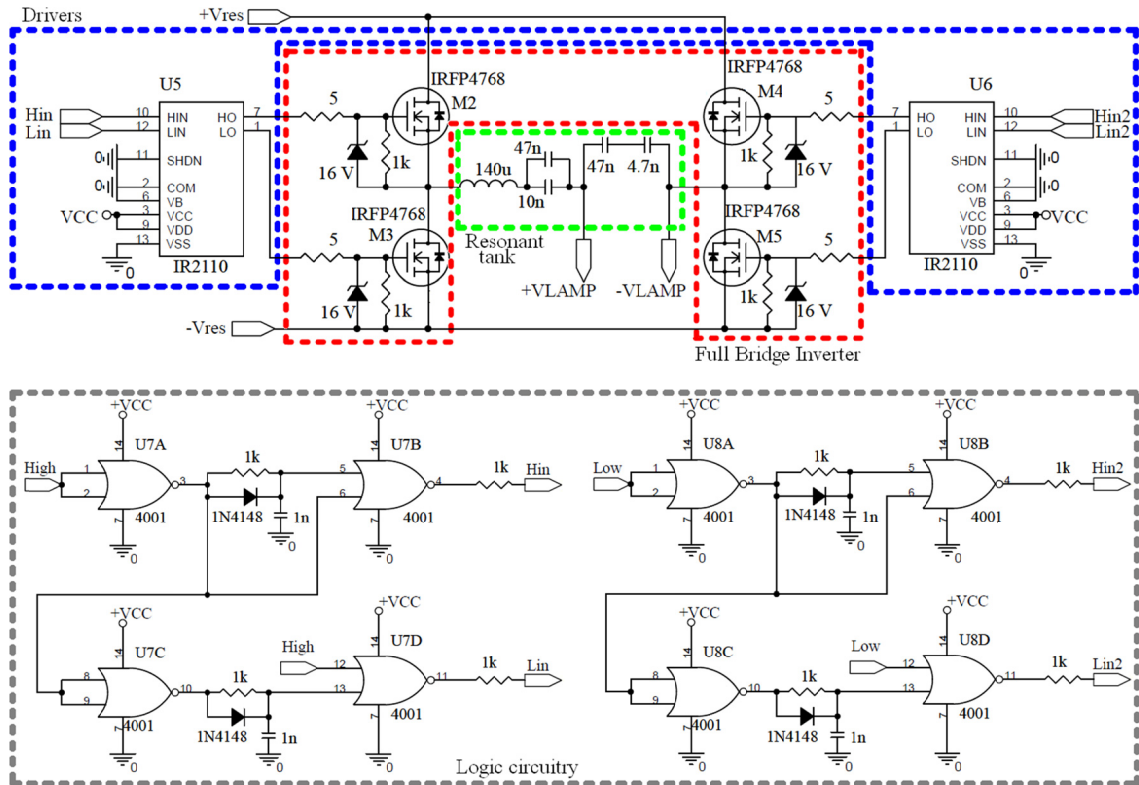


Fig 112. Power stage circuit and logic circuitry scheme of the proposed $L_s C_s C_P$ resonant inverter.

4.7 Experimental results

The main experimental results are given in this section. The experimental set-up appears in Fig. 113, in which the external coil IEFL is working at the nominal power of 150 W.

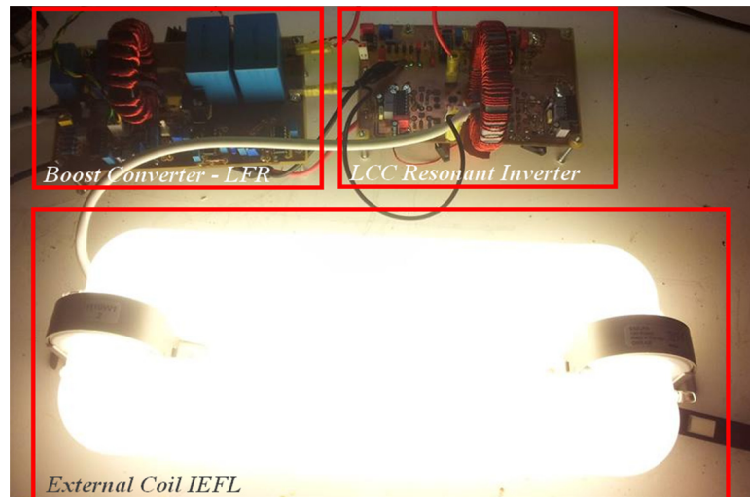


Fig 113. Picture of the electronic ballast experimental prototype.

The first caption depicted in Fig. 114 is the start-up transient. During the start-up, the lamp coils reach 1 kV (V_{LAMP}), whereas the resonant inverter input voltage (V_C) is around 250 V. Once the lamp is ignited, the coil voltage decreases until 100 V to be finally stabilized (see Fig. 116) around 185 V, while the current flowing through the coils increases. The input



voltage V_s is always the same, i.e. 13 V approximately. The warm-up transient appears in Fig.115, where the lamp voltage and current achieve the steady-state values. It is important to remark that the evolution of the coil current is just the opposite of the coil voltage, as expected from a power source ballast delivering always the same power to the lamp regardless the IEFL impedance.

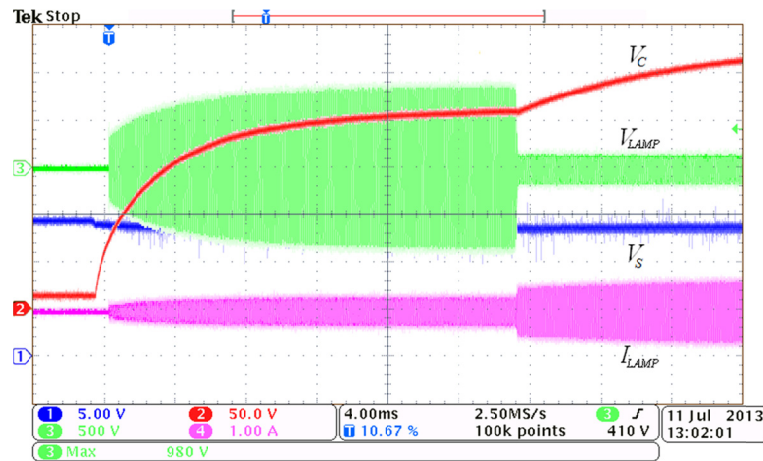


Fig 114. Start-up transient.

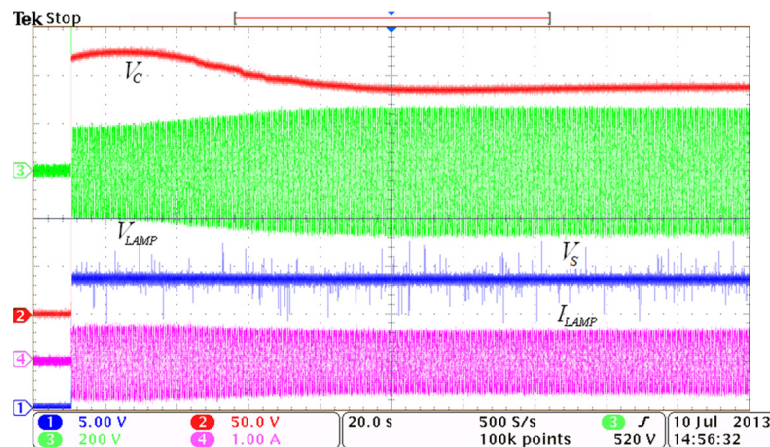


Fig 115. Warm-up transient.

According to Fig. 116, the lamp voltage and current are $184 V_{RMS}$ and $0.434 A_{RMS}$ respectively, and the phase-shift between both is 18.73° approximately. Considering both coils, the lamp apparent power is $S_{LAMP}=2 \cdot 0.434 \cdot 184=159.712 \text{ VA}$, whereas the active lamp power is $P_{LAMP}=S_{LAMP} \cdot \cos(18.73)=151.25 \text{ W}$, and the reactive power is $Q_{LAMP}=S_{LAMP} \cdot \sin(18.73)=51.28 \text{ Var}$. Furthermore, the input voltage and current are 13.4 V and 13 A respectively. Thus the total input power P_{IN} is about 174.2 W. Comparing the lamp active power P_{LAMP} , and the input power P_{IN} , the prototype has an efficiency of 87 %. It has to be pointed out that this conclusion is very sensitive in terms of the lamp coil voltage and current phase shift. It is important to comment, that when the lamp works at full power (150 W), the boost switching frequency is the lower, which in this case is about 36 kHz. As previously



explained in subsection 4.4.1, this switching frequency will be always higher than 35 kHz. Moreover, it is very easily to increase this switching frequency by modifying the control hysteresis, but this fact directly affects the ballast efficiency and degrades it. Another characteristic to remark is that in all the measurements, the frequency of lamp voltage and current is 234 kHz.

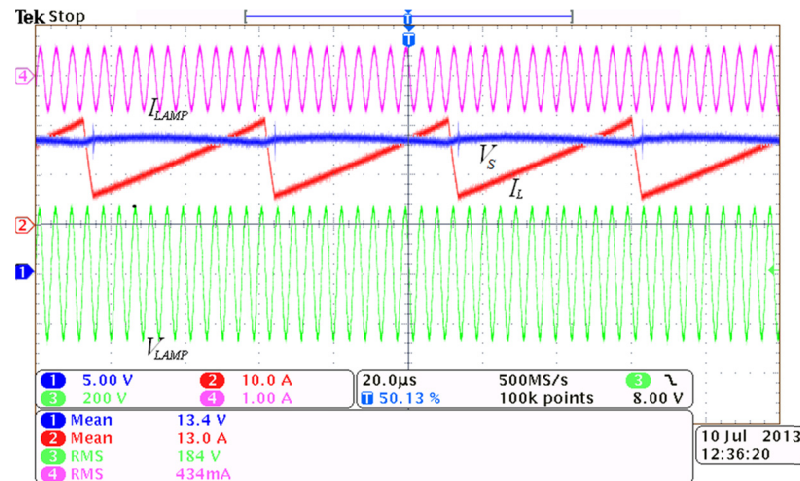


Fig 116. Lamp coil and boost input variables.

Fig.117 shows a detail of the resonant inverter waveforms, where lamp voltage and current values are 185 V_{RMS} and 0.433 A_{RMS} respectively with a phase shift of 18.84°. Also, the resonant inverter input DC voltage (V_C) and DC current (I_{BOOST}) are 235 V and 0.695 A respectively, so that the inverter efficiency when the lamp is supplied at full power is about 92.8 %.

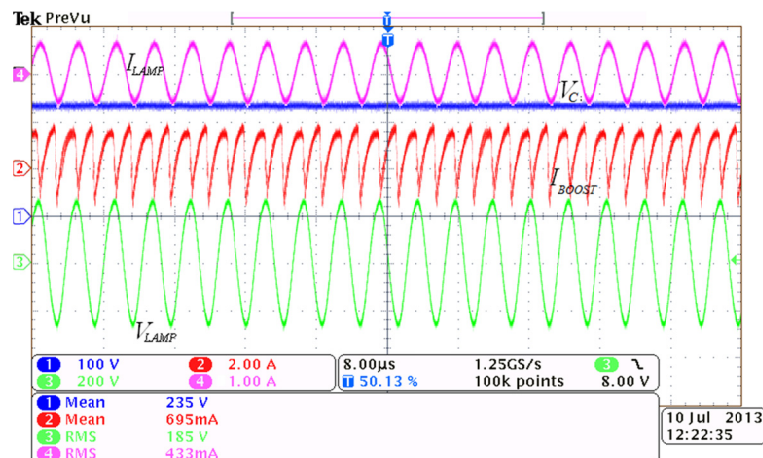


Fig 117. Resonant inverter detail.

Fig.118 illustrates, in turn, the boost converter waveforms, in which input voltage and current values are 13.3 V and 13.3 A respectively. Besides, output voltage and current are 233 V and 0.699 A respectively, which results in a converter efficiency of 92%.

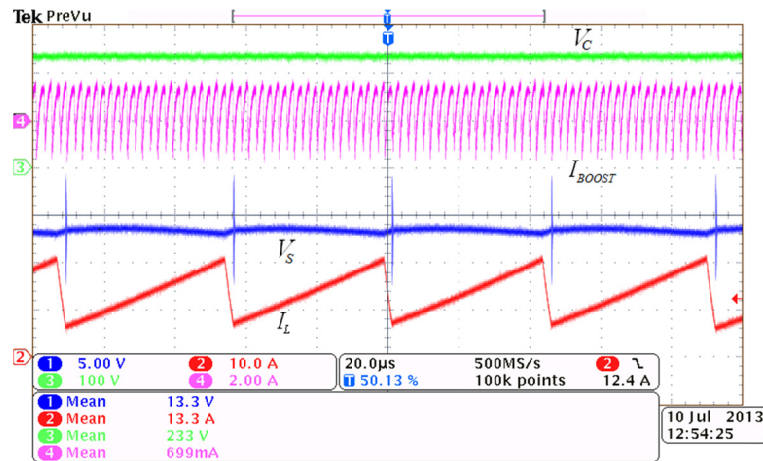


Fig 118. Boost converter detail.

Finally, Fig. 119 illustrates the light regulation capability. In this case, by decreasing the ballast conductance “g” it is possible to deliver to the lamp only 61 W. The waveforms correspond to a lamp voltage of 293 V_{RMS} , a lamp current of 0.138 A_{RMS} and a phase-shift between both about 41.05° , so the active power supplied to the lamp is 61 W, and the voltage supplied to the resonant inverter is 104 V. Moreover, the lamp nonlinear behaviour can be observed in Figs. 116 and 119, where it can be asserted that lamp voltage, current, and phase-shift are power dependent, and it is possible to conclude that the ballast is delivering the desired power to the IEFL regardless of its impedance.

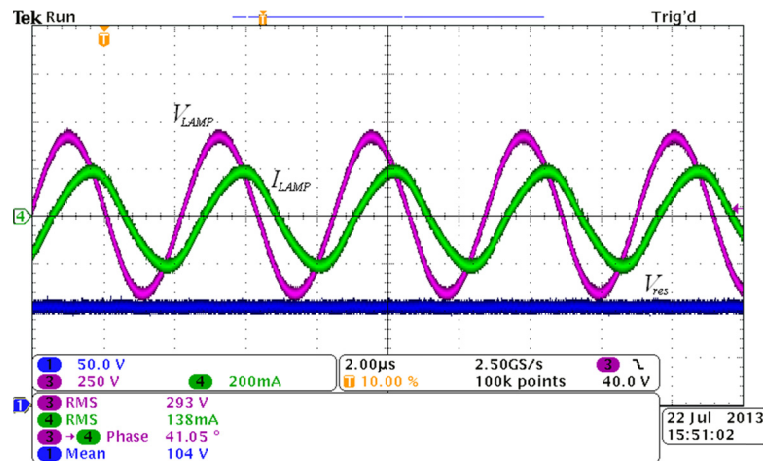


Fig 119. Low power experimental waveforms (61 W).

4.8 Conclusions of the LFR ballast to supply IEFLs

A two-stage electronic ballast to drive IEFL lamps based on the Loss-Free resistor (LFR) concept has been described in this chapter. Its design key issues have been discussed and an experimental prototype has been realized and tested with a 150 W IEFL lamp proving the feasibility of the proposed approach and the design robustness.



Several experimental results, including start-up, warm-up transients as well as steady-state oscilloscope measurements have verified the theoretical predictions. Performance measurements at diverse operating points have exhibited a global efficiency in the range of 86%-91%. Future works contemplate the improvement of the global efficiency by introducing Silicon Carbide (SiC) or Gallium Nitride (GaN) devices.

The use of an appropriate sliding-mode control has imposed to the ballast an LFR behaviour, so that it has always delivered to the lamp the desired power irrespectively of the lamp impedance.. This feature ensures the lamp operation at nominal power during all the lamp lifetime and allows an easy light dimming. The desired lamp power is adjusted changing the input conductance “ g ”, so the light intensity can be easily regulated.



5 Conclusions and future works

5.1 General Conclusions

In this thesis, it has been shown that LFR approach in the design of power converters for efficient lighting is the core of a reliable and efficient supply at constant power for three large classes of lamps, namely LEDs, HIDs and IEFLs. In all cases, both output voltage and current of each regulator are automatically adjusted by the lamp impedance.

In chapter 2, a very high voltage-gain single stage boost converter operating at the boundary of CCM and DCM has been proved to be a good candidate for LED supplying. A voltage gain around 100 has been obtained with duty cycles near 1 without risk of saturation due to the use of a hysteretic modulator. The converter has been controlled through the inductor current whose reference is given by the integral of the output current error. The dynamic behaviour of the system has been studied by means of the sliding-mode control theory to establish the stability conditions. The converter has been implemented by means of a normally-OFF JFET and a Schottky diode, which has been specifically fabricated for the application. The use of SiC devices has allowed yielding 1200 V from an input voltage of 12 V with an efficiency of 83% operating at 24 kHz.

In the same chapter, the previous converter with the same control has been used for on-grid LED lighting applications with PFC. It has been also shown that the efficiency of the converter can be significantly improved up to 94% using a burst operation, in which the switching frequency of the converter has been reduced without changing the inductor value, and without modifying the output voltage ripple.

An electronic ballast to drive different HID lamps has been presented in chapter 3, and its dynamics for its operation modes have been analysed. The ballast behaves like a LFR delivering always the selected power to the lamp, independently of the lamp impedance due to the action of an appropriate sliding-mode control law. This feature ensures the lamp operation at nominal power during all the lamp life and reduces the warm-up time. As the power reference can be adjusted using a potentiometer, the light intensity can be easily regulated. Besides, as the lamps are supplied in DC, the AR problems are avoided. Several experimental tests with commercial HIDs have shown the feasibility of the proposed approach, and its good efficiency demonstrating that the ballast is capable to achieve 6 kV to start the lamp from a 12 V power source.

Also in the same chapter, with the aim of supplying the HID lamp in AC, an electronic ballast with LFR behaviour imposed by means of sliding-mode control implemented with an FPGA has been presented. Experimental results have verified the good performance of the ballast working with the HID lamp in the start-up, warm-up and steady-state operation. It has also been shown that the electronic ballast is capable to supply the lamp in HFSW.



A two-stage electronic ballast to drive IEFL lamps has been described in chapter 4, where an experimental prototype has been realized and tested with a 150 W IEFL lamp proving the feasibility of the proposed approach and the design robustness. Several experimental results, including start-up, warm-up transients as well as steady-state oscilloscope measurements have verified the theoretical predictions. Performance measurements at diverse operating points have exhibited a global efficiency in the range of 86%-91%.

5.2 Future works

In addition to the work in this thesis, the research that should be continued in this area are as follows: 1) reducing the ballast size, 2) increasing the switching frequency in IEFL operation, 3) designing a general electronic ballast.

The power density of the current ballasts could be improved by increasing the switching frequency or introducing new switching devices, as Gallium Nitride (GaN) devices. As a consequence, a significant reduction of the present size of the prototypes could be expected.

Similarly, the introduction of GaN devices could extend the application range of the IEFL ballast from 250 kHz up to 2.5 MHz and even 13 MHz, the latter being the highest frequency for commercial products.

A general electronic ballast could operate indistinctly with AC or DC input voltage and should be able to supply LEDs, HID, and IEFLs. The problem is open.

5.3 Patents and publications

The main contributions of this PhD has been patented and published in diverse journals and conferences

5.3.1.1 Patents.

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; L.Martínez-Salamero, “Up converter and light provided with the same” Patent Number : PCT/ES2011/070603.

5.3.1.2 Journal Publications.

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; F. Flores-Bahamonde; L.Martínez-Salamero, “High Voltage LED Supply Using a Hysteretic Controlled Single Stage Boost Converter”, *Przegląd Elektrotechniczny*, vol. 1, pp. 26-30, 2012.

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; J.Maixé-Altés; L.Martínez-Salamero, “Sliding-Mode-Control-Based Boost Converter for High-Voltage-Low-Power Applications”, *Industrial Electronics, IEEE Transactions on*, vol. 62, pp. 229-237, 2015.

A.Leon-Masich; H. Valderrama-Blavi; J.M.Bosque-Moncusí; L. Martínez-Salamero, “Efficiency comparison between Si and SiC-based implementations in a high gain DC-DC boost converter” *IET Power Electronics*, DOI 10.1049/iet-pel.2014.0591.



A.Leon-Masich; H. Valderrama-Blavi; J.M.Bosque-Moncusí; L. Martínez-Salamero, “A High Voltage SiC-based Boost PFC for LED Applications” *Power Electronics, IEEE Transactions on*, DOI 10.1109/TPEL.2015.2418212.

5.3.1.3 Conference Publications.

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; A. Cid-Pastor; L. Martínez-Salamero, “High-Voltage LED-based efficient lighting using a hysteretic controlled boost converter”, *7th International Conference-Workshop Compatibility and Power Electronics CPE 2011*, Tallin, Estonia, 2011.

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; A. Cid-Pastor; L. Martínez-Salamero, “Convertidor con alta ganancia de tensión para iluminación eficiente”, *XVIII Seminario Anual de Automática, Electrónica Industrial e Instrumentación, SAAEI*, Badajoz, España, Julio 2011 (In Spanish).

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; F. Flores-Bahamonde; J.A Barrado; L. Martínez-Salamero, “Battery Supplied Transformerless Ballast for DC high Intensity Discharge (HID) Lamps”, *IECON 2012 - Annual International Conference of the IEEE Industrial Electronics Society*, Montreal, Canada, 2012.

A.Leon-Masich; H. Valderrama-Blavi; J.M. Bosque-Moncusí; F. Flores-Bahamonde; J.A Barrado; L. Martínez-Salamero, “Balasto para alimentación de lámparas HID en DC basado en resistor libre de pérdidas (LFR)”, *XIX Seminario Anual de Automática, Electrónica Industrial e Instrumentación, SAAEI*, Guimaraes, Portugal, Julio 2012 (In Spanish).

A. Leon-Masich; H. Valderrama-Blavi; L. Albiol-Tendillo; J.M. Bosque-Moncusí; L. Martínez-Salamero, “A Dimmable Electronic Ballast for Induction Electrodeless Lamps Based on Loss-Free Resistor”, *International Conference on Electrical Drives and Power Electronics, EDPE*, Dubrovnik, Croatia, 2013.

A. Leon-Masich; H. Valderrama-Blavi; L. Albiol-Tendillo; J.M. Bosque-Moncusí; J.A Barrado; L. Martínez-Salamero; “A Loss Free Resistor Based Approach to Regulate Electrodeless Induction Lamps” *International Journal on Advanced electrical engineering, ICPEA*, Djelfa, Algeria, 2013.

A.Leon-Masich; H. Valderrama-Blavi; J.M.Bosque-Moncusí; L. Martínez-Salamero, “Balastro Electrónico basado en control por deslizamiento con comportamiento de LFR para Lámparas de Inducción sin Electrodo”, *XX Seminario Anual de Automática, Electrónica Industrial e Instrumentación, SAAEI*, Tanger, Morroco, Junio 2014 (In Spanish).

A.Leon-Masich; H. Valderrama-Blavi; J.M.Bosque-Moncusí; L. Martínez-Salamero, “A high voltage SiC-based boost PFC for LED Applications”, *Ninth International Conference on Ecological Vehicles and Renewable Energies, EVER*, Monaco, 2014.





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