Architectures and Control of Submodule Integrated DC-DC Converters for Photovoltaic Applications

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***Abstract*—This paper describes photovoltaic (PV) module architectures with parallel-connected submodule integrated DC-DC converters (subMICs) that improve efficiency of energy capture in the presence of partial shading or other mismatch conditions. The subMICs are bidirectional isolated dc-dc converters capable of injecting or subtracting currents to balance the module substring voltages. When no mismatches are present, the subMICs are simply shut down, resulting in zero insertion losses. It is shown that the objective of minimum subMIC power processing can be solved as a linear programming problem. A simple close-to-optimal distributed control approach is presented that allows autonomous subMIC control without the need for a central controller or any communication among the subMICs. Furthermore, the proposed control approach is well suited for an isolated-port architecture, which yields additional practical advantages including reduced subMIC power and voltage ratings. The architectures and the control approach are validated by simulations and experimental results using three bidirectional flyback subMICs attached to a standard 180 W, 72-cell PV module, yielding greater than 98 % module-level power processing efficiency for a mismatch less than 25 %.**

***Index Terms*—Photovoltaic Modules, Sub-Module Integrated Converters, SubMICs, DC-DC Converters, Modeling and Control of Power Electronics, Renewable Energy Systems.**

I. Introduction

PHOTOVOLTAIC (PV) systems are usually composed of series-parallel arrangements of PV modules, each module consisting of a string of series-connected PV cells, as shown in Fig. 1(a). It is well known that mismatches due to manufacturing tolerances, partial shading, dirt, thermal gradients, or aging result in losses in energy captured by a PV system. The mismatches have disproportional effects on the overall available power due to the reduction in current through the series-connected cells. Typically, bypass diodes are connected in parallel with groups (substrings) of cells, as shown in Fig. 1(b), to prevent cell failures due to hot spots induced by power losses on reverse-biased cells operating in breakdown [1]. However, the efficiency losses with the bypass diodes are still significant, as reported in [2]–[7]. Furthermore, mismatched PV modules or systems exhibit non-convex output power versus output voltage characteristics with multiple maxima that hinder operation of maximum power point (MPP) tracking algorithms and result in the need to operate PV system power electronics over a wider range of MPP voltages.

Many PV architectures based on distributed power electronics capable of module-level MPP tracking (MPPT) have been investigated, including dc-ac microinverters, e.g. [8]–[12], or dc-dc module-integrated converters (MICs), e.g. [13]–[15]. In these approaches, the impact of mismatches is reduced by performing module-level MPPT, at the expense of insertion losses and increased cost associated with the distributed power optimizers that are required to process full PV power even in the case when no mismatches are present. Furthermore, since it has been found that efficiency and energy capture can be improved further by performing finer-granularity MPPT in PV modules or systems [6], it is of interest to examine alternatives to full power processing module-level solutions.

This paper focuses on PV architectures, such as the example shown in Fig. 1(c), where submodule integrated converters (subMICs) are configured to process only a mismatch fraction of power, present no insertion losses, and are capable of performing finer-granularity MPPT [16]–[21]. It should be noted that various partial power processing approaches applied to active cell balancing in battery systems [22]–[25] can also be applied to PV modules and systems. For example, versions of the "shuffling" cell-balancing architecture [22] have been applied to PV systems [16], [18], [19]. Similarly, the architecture of Fig. 1(c) has been applied to battery cell balancing [24], [25] and PV systems [17]. A more detailed review of PV architectures based on distributed full or partial power processing converters can be found in [21].

This paper generalizes the architecture proposed in [17], [21], showing that the objective of minimum power processed by subMICs can be solved as a linear programming problem, and achieved using bidirectional subMICs and a central controller. A much simpler, close-to-optimal distributed control approach is then introduced that allows autonomous subMIC control without the need for a central controller or any com-

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000216. The information, data, or work presented herein was funded in part by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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munication of control or sensing signals among the subMICs. This simple control approach leads to the introduction of an isolated-port subMIC-enhanced PV module architecture, which offers a number of additional practical implementation advantages.

The paper is organized as follows. Section II examines power processing in the subMIC-enhanced PV module architecture shown in Fig. 1(c), and introduces a simple distributed control method that balances the substrings and is well suited for the isolated-port subMIC-enhanced architecture. Section III describes an example subMIC implementation based on a bidirectional flyback converter, and presents system modeling and subMIC controller design. Simulation and experimental results validating the architectures and the control approach are presented in Section IV for three bidirectional flyback subMICs attached to a standard 180 W, 72-cell PV module. Conclusions are presented in Section V.

II. Power Processing and Control in SubMIC-Enhanced PV Modules

Figure 1(a) shows a block diagram of a PV module consisting of N_c PV cells connected in series, divided in n_s substrings by the corresponding bypass diodes, as shown in Fig. 1(b). In order to illustrate the considered architectures, a typical 72-cell module ($N_c = 72$) with $n_s = 3$ substrings is considered as an example, where each substring contains the same number of $n_c = 24$ cells. Under normal operation, substring currents i_{g_i} are nearly identical and substrings are forward biased by nearly identical substring voltages v_{sub_i}, which results in a maximum power point (MPP) voltage v_{mpp} close to the module nominal value. In cases of solar irradiation mismatches (i.e. partial shading), or other mismatches among the cells, the series connection limits the output current to the minimum cell current. As a result, even small mismatches have a disproportionate effect in the available power [5]. Besides, since substring voltages are different, in the absence of bypass diodes, reverse-biasing of those substrings producing less current leads to the appearance of hot-spots [1]. Bypass diodes (Fig. 1(b)) prevent the appearance of those hot-spots and protect the PV module from potentially destructive effects. However, in doing so, mismatched substrings become shorted and produce no output power. As a consequence, mismatched PV modules exhibit non-convex characteristics with multiple maxima that hinder operation of MPP algorithms and result in the need to operate PV system power electronics over a wide range of MPP voltages. In addition, when the bypass diodes are not forward biased, mismatches have the same disproportionate effect on the available power as in Fig. 1(a).

As an example of bypass diodes operation, consider the PV module of Fig. 2(a), where two substrings operate at the nominal MPP ($G_2 = G_3 = 60$ W), while the third substring is mismatched and only generates half of its nominal power ($G_1 = 30$ W). As shown in Fig. 3, a local MPP exists in this case, when bypass diodes do not conduct and the three substrings deliver approximately the same power, so that $P_{mod} \approx 90$ W. However, the global MPP occurs when substring 1 is shorted by its bypass diode and substrings 2 and 3 are able to supply all their generated power $P_{mod} \approx 120$ W. It should be noted that ideal available power is $G = G_1 + G_2 + G_3 = 150$ W, while the maximum output power that can be seen at the output is only $P_{mod} \approx 120$ W. As a result, the module-level power processing efficiency in this case is only 80 %. Furthermore, the global MPP is achieved at an output voltage far from the nominal MPP voltage.

Figure 1(c) shows the PV module architecture of Fig. 1(b), where the bypass diodes have been replaced by subMICs. The primary side of each subMIC is connected in parallel to each substring, in direct replacement of the corresponding bypass diode. The secondary side is connected in parallel across the output of the module, which is why the subMICs are implemented as dc-dc converters with isolation.

In the case of perfectly matched conditions, the subMICs are simply shut-down, resulting in 100 % module-level power processing efficiency. In the case of mismatches, subMICs only need to handle the portion of power necessary to balance the substrings. In such a case, forcing current balance of substrings with subMICs allows extraction of all the available power in the module, except for the small amount of power lost in each subMIC. As a result, module-level power processing efficiency can be very high.

The same example case of Fig. 2(a) is depicted in the subMIC-enhanced PV module in Figs. 2(b) and 2(c). In Fig. 2(b), for example, subMICs 2 and 3 extract the necessary current to achieve power balance between the substrings. Neglecting subMIC losses, the output power is $P_{mod} \approx G_1 + G_2 + G_3 = 150$ W and the power processed by the subMICs is equal to $P = P_2 + P_3 = 60$ W. Similarly, Fig. 2(c), shows another solution to the same mismatch case, in which subMIC 1 only needs to inject a certain amount of current in parallel with substring 1 to achieve the same balancing effect. Note that in this case only one subMIC processes power, and the total processed power is $P = P_1 = 30$ W.

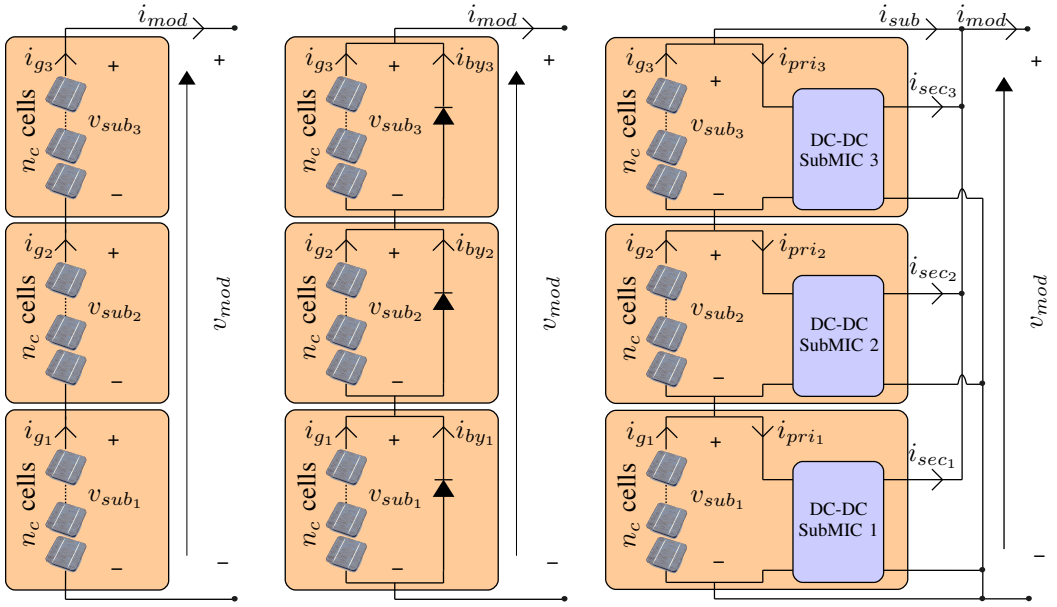
Two important facts arise from this example: (i) multiple solutions to the same mismatch case can exist, where the optimal solution with the least processed power yields the maximum module-level efficiency; (ii) since optimal solutions can require injecting or extracting currents from substrings, the subMICs should be implemented as bidirectional dc-dc converters.

The results of subMIC processing, if power processing losses are neglected, can be seen in Fig. 3. Note that, compared to the case where bypass diodes are used, the subMICs not only yield significantly higher output power but also result in a convex power-voltage characteristic for the subMIC-enhanced module, as well as an MPP voltage that remains close to the nominal value.

The next section addresses the problem of multiple balancing solutions and describes an optimal approach that can be implemented with a central module-level controller. Then, an alternative suboptimal strategy that can be carried out with simple distributed subMIC controllers is introduced and analyzed in Section II-B.

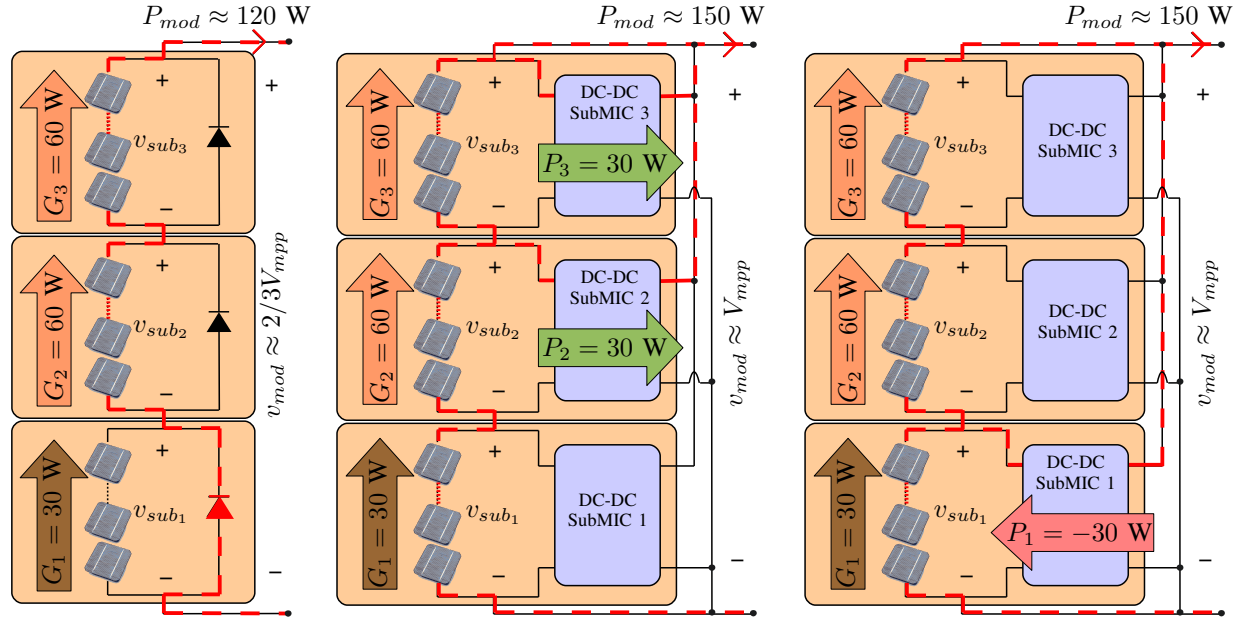
A. Optimal Power Processing

In a general case of a PV module with n_s substrings, following the same notation as in the considered example,



(a) Series-connected PV cells in a PV module. (b) PV module with bypass diodes. (c) PV module with submodule integrated dc-dc converters (subMICs).

Figure 1. Standard and subMIC-enhanced PV module architectures.



(a) PV module with bypass diodes. (b) PV module with subMICs extracting current from substrings #2,3. (c) PV module with subMICs injecting current to substring #1.

Figure 2. Examples of PV module operation with substring #1 mismatched to 50 % of nominal power.

the power generated by the substrings can be written as $G_1, \ldots, G_{n_s}$ and the power processed by the subMICs is denoted as $P_1, \ldots, P_{n_s}$. The optimal power flow can be posed as a linear programming problem as follows.

$$\begin{aligned} \min\ & P = |P_1| \ + \ \ldots \ + \ |P_{n_s}| \\ \text{subject to}\ & G_1 - P_1 \ = \ G_2 - P_2 \\ & \vdots \\ & G_{n_s-1} - P_{n_s-1} \ = \ G_{n_s} - P_{n_s} \end{aligned} \tag{1}$$

where P is the total power processed by subMICs. That is, this program finds the minimum value of P such that power balance in all substrings is achieved. Again, note that since subMICs are bidirectional, processed power P_i can be either positive or negative. Consequently, in general, more than one solution with the same optimal objective value P^* can be achieved.

An optimal control approach could be implemented with a central controller. Various simplifications are possible, depending on how the subMICs are implemented. For example,

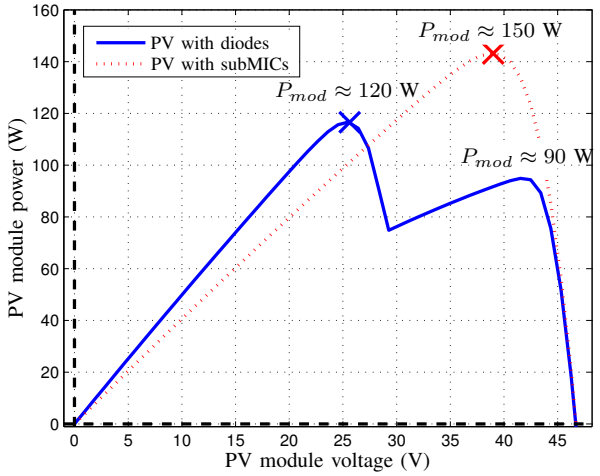
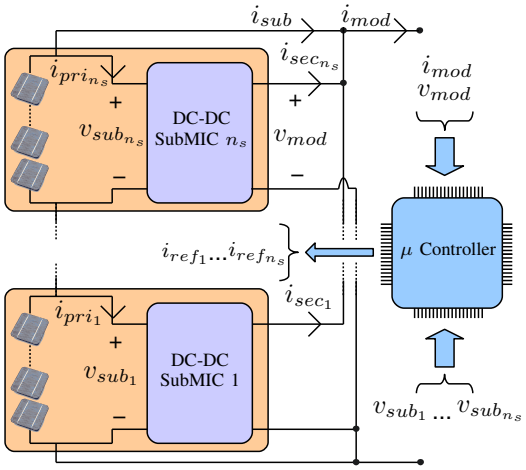
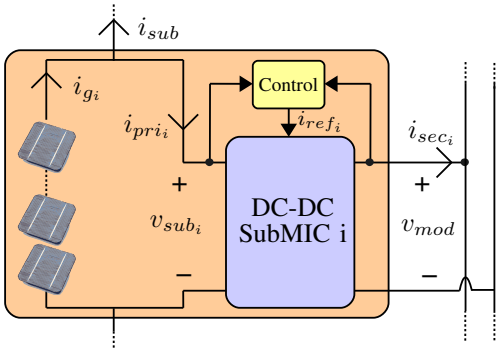


Figure 3. Power-voltage characteristic of a mismatched PV module with bypass diodes and with subMICs.



(a) Optimal power processing with a centralized controller.



(b) Sub-optimal power processing with a local controller.

Figure 4. SubMIC control block diagrams.

with subMICs implemented as dc-dc converters operating in discontinuous conduction mode (DCM), there is no need to sense substring currents. This means that current commands i_{ref_i} can be executed as duty-cycle commands, as explained further in Section III. In such a case, the knowledge of the substring voltages and subMIC duty cycles can be employed to estimate the power generated by the substrings and then the linear programming problem (1) can be solved for each sampling time, yielding the new current commands (or references) for the different subMICs. A possible implementation diagram of this approach is shown in Fig. 4(a), using a central controller and only one module-level current sensor, which could be the same current sensor used for MPP tracking by downstream power electronics (e.g. a micro-inverter supplied by the module). A flowchart of the control algorithm is shown in Fig. 5. A disadvantage of the approach shown in Fig. 4(a) is that the central controller must sense multiple voltages and issue multiple reference signals to the subMICs. An alternative, simpler control approach is introduced in the next section.

B. Distributed SubMIC Control

An alternative control approach that does not require a central controller is proposed in this subsection. This approach allows each subMIC to be controlled independently from the others. In the discussion that follows, it is assumed that the subMIC-enhanced PV module is attached to a converter (e.g. a microinverter) that performs traditional MPP tracking using one of many available methods [26]–[28]. The module output voltage is set to the MPP value $v_{mod} = V_{mod}$.

Assuming that substrings have identical number of cells, power balance can be achieved by balancing substring voltages [19]. Although the substring MPP voltage may change with operating conditions (such as irradiance and temperature), it is assumed that such changes can be considered relatively small. This limitation is discussed further in Section IV-D. Figure 4(b) shows a substring and its corresponding subMIC that regulates the substring voltage to a reference,

$$V_{ref} = \frac{v_{mod}}{n_s} \tag{2}$$

To do so, the current injected or taken by the subMIC i_{pri_i} can be set to follow a current reference i_{ref_i}, which is a function of the voltage error:

$$i_{pri_i} = i_{ref_i} = K(s)(V_{ref} - v_{sub_i}), \tag{3}$$

where $K(s)$ is a controller whose transfer function has a finite DC gain K. It should be noted that such a subMIC controller would operate autonomously, without the need for a central controller, or any communication of sensing or control signals among the subMICs. Besides, if $K(s)$ is of low order, it could be implemented easily using standard low-cost analog or digital realizations.

In order to examine the effect of the control strategy (3) in steady-state, note that I_{sub_i} is now a function of K, I_{g_i}, and the voltage error,

$$I_{sub_i} = I_{g_i} - I_{pri_i} = I_{g_i} - K(V_{ref} - V_{sub_i}). \tag{4}$$

From (4) it follows that the sum of substring voltages can be expressed as

$$\sum_{i=1}^{n_s} V_{sub_i} = n_s V_{ref} + \frac{1}{K}\left(I_{sub_i} n_s - \sum_{i=1}^{n_s} I_{g_i}\right) \tag{5}$$

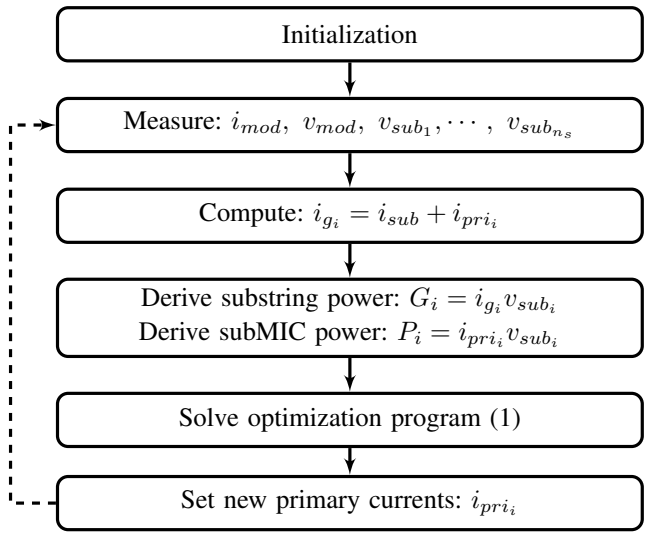


Figure 5. Flowchart of a possible implementation of the optimal power processing controller.

Since substrings are all connected in series, the currents are all the same, $I_{sub_i} = I_{sub}\ \forall i$. Furthermore, since $v_{mod} = \sum_{i=1}^{n_s} V_{sub_i} = n_s V_{ref}$, and since the controller DC gain K is finite, (5) implies that

$$I_{sub} = \frac{\sum_{i=1}^{n_s} I_{g_i}}{n_s}, \tag{6}$$

It is important to note that the key result (6) is enabled by the fact that the substring voltage controller (3) in each subMIC has a finite DC gain K, so that the subMIC steady-state primary current I_{pri_i} is proportional to the steady-state voltage error $V_{ref} - V_{sub_i}$. Otherwise, the equilibrium point of each subMIC would not be unique and would depend on initial conditions.

The power processed by each subMIC is equal to $P_i = V_{ref} I_{pri_i}$. The currents processed by each subMIC and the total processed power can be computed as follows

$$I_{pri_i} = I_{sub} - I_{g_i}, \quad \text{and} \quad P = V_{ref} \sum_{i=1}^{n_s} I_{pri_i} \tag{7}$$

It should be noted that with the distributed subMIC controller (3) the total processed power can be larger than the optimal found by solving the linear programming problem (1). The next section compares the proposed control approach with the optimal case.

C. Comparison Between Optimal and Distributed SubMIC Control

In a module with n_s substrings, assume that a substrings produce the same amount of current $I_{g_i}|_{i=1,\cdots,a} = I_g$, while b substrings produce zero current $I_{g_i}|_{i=a+1,\cdots,n_s} = 0$. Employing the sub-optimal approach of Section II-B, the steady-state substring current I_{sub} is equal to

$$I_{sub} = \frac{\sum_{i=1}^{n_s} I_g}{n_s} = \frac{a I_g}{n_s}. \tag{8}$$

Consequently, the current injected or extracted by subMICs is:

$$\text{Primary current} \begin{cases} \text{Injected: } I_{pri_i}|_{i=a+1,\cdots,n_s} = -\dfrac{a I_g}{n_s} \\ \text{Extracted: } I_{pri_i}|_{i=1,\cdots,a} = \dfrac{b I_g}{n_s} \end{cases} \tag{9}$$

and the corresponding processed power is

$$P_{\text{subopt}} = V_{ref} \left(\frac{ab}{n_s} + \frac{ab}{n_s} \right) I_g = 2 V_{ref} \left(\frac{ab}{a+b} \right) I_g \tag{10}$$

On the other hand, assuming that $a \geq b$, the optimal solution to this problem can be easily derived as follows. SubMICs process zero energy for substrings $i = 1, \cdots, a$, and inject a current equal to I_g in substrings $i = a+1, \cdots, n_s$. Thus, the processed power is $P_{\text{opt}} = b V_{ref} I_g$.

The ratio between the sub-optimal solution P_{subopt} and the optimal P_{opt}, demonstrates that the proposed sup-optimal distributed control approach results, in the worst case, in 2 times larger processed power compared to the optimal solution:

$$\frac{P_{\text{subopt}}}{P_{\text{opt}}} = 2 \frac{a}{a+b}, \quad \text{Worst case: } \lim_{\substack{a \to \infty \\ b \to 1}} 2 \frac{a}{a+b} = 2. \tag{11}$$

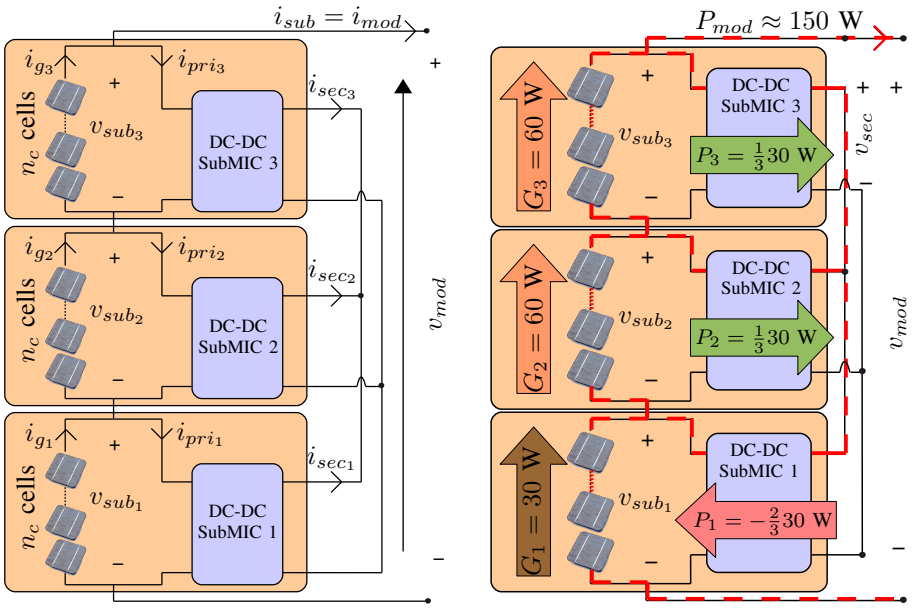
In practice, PV modules have a relatively small number of substrings and worst-case solutions for the proposed control approach are much closer to the optimal. For the considered typical module with 3 substrings, in the worst case the optimal solution corresponds to $P_{\text{opt}} = V_{ref} I_g$ while the proposed distributed control approach yields $P_{\text{subopt}} = \frac{4}{3} V_{ref} I_g$. In other words, the worst-case power processed by the subMICs using the simple, distributed control approach is 33 % higher than the optimum.

In addition to the very simple distributed implementation, the proposed suboptimal control approach has another important advantage in that it allows subMICs with lower power rating, since power is distributed following equations (6) and (7), so that subMIC power rating can be reduced to $\frac{n_s - 1}{n_s}$ of subMIC power rating with the optimal approach. In the considered typical PV module example with 3 substrings, the subMIC power rating is equal to 67 % of the subMIC power rating required to implement the optimal solution.

The steady-state solution of the sub-optimal control approach yields an important conclusion about its behavior. Since substring currents are balanced to an average value, the sum of primary/secondary subMIC currents is zero. This means that all power transferred to the secondary port of subMICs is absorbed by the remaining subMICs, and therefore the secondary port average power is zero. This implies that the secondary port of the subMICs can be disconnected from the module output, leading to the isolated-port architecture discussed in the next section.

D. Isolated-Port SubMIC PV Architecture

In the isolated-port subMIC architecture shown in Fig. 6(a), the secondary ports of all subMICs are connected in parallel, but disconnected from the module output. This architecture has several advantages, both from the theoretical and the practical point of view. First, the architecture is well suited for the sub-optimal control approach proposed in Section II-B, which can



(a) Connection diagram.

(b) Example of operation with substring #1 mismatched to 50 % of nominal power.

Figure 6. Isolated-port subMIC-enhanced PV module architecture and operation.

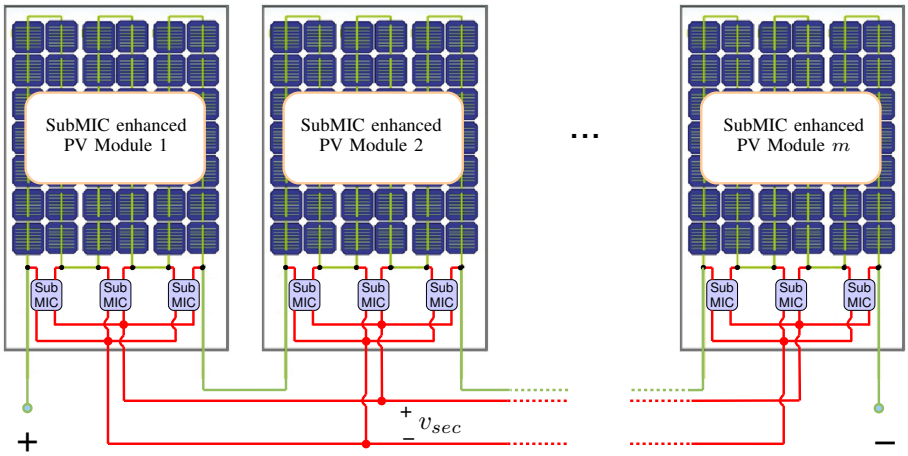


Figure 7. Array of isolated-port subMIC-enhanced PV modules connected in series, with built-in balancing.

be implemented easily and with no need for additional sensing. In addition, the subMIC power rating can be reduced to $\frac{n_s-1}{n_s}$ of the subMIC power rating for the optimal case. Since the secondary port voltage can be selected independently from the PV module voltage, the subMIC conversion ratio can also be selected independently from the number of substrings in the module. For example, a 1:1 conversion is feasible, allowing symmetrical implementation with low-voltage devices on both primary and secondary sides of a subMIC. The flexibility in selecting the voltage conversion ratio is also beneficial with respect to the magnetics size and efficiency optimization.

It should also be noted that the subMIC secondary port of a module can be connected in parallel with the subMIC secondary port of another module. In turn, such subMIC-enhanced modules with shared secondary ports can be connected in series to form larger PV arrays in much the same way traditional PV systems are realized, but with the advantage of built-in balancing (Fig. 7). The extension of the isolated-port architecture to arbitrarily long chains of series-connected substrings or modules and to arbitrarily high DC voltages does not impact subMIC power or voltage rating, with an exception of the transformer DC isolation voltage rating. Note, however, that the interconnection of secondary ports requires additional wiring.

Finally, it is worth noting that active filtering can be implemented with an energy storage capacitor on the subMIC isolated port, with potentials to reduce the cost and improve efficiency of downstream power electronics connected to the subMIC-enhanced module or a string of subMIC-enhanced modules.

Figure 6(b) shows an example of power processing in the isolated-port subMIC-enhanced PV module architecture under

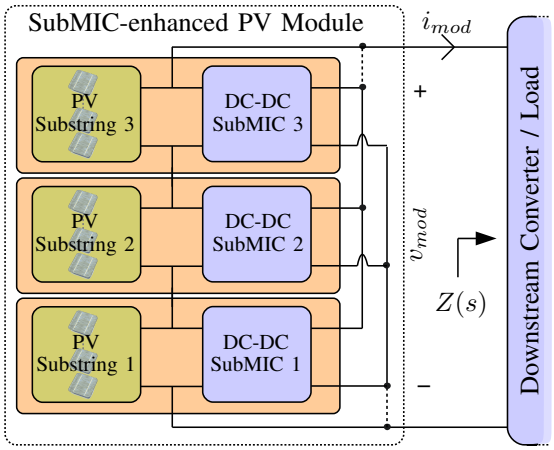


Figure 8. Simplified block diagram of a subMIC-enhanced PV module.

the same conditions as in Fig. 2. It can be observed that the total subMIC power equals $P_1+P_2+P_3 = 0$, and that the total power processed by subMICs equals $|P_1|+|P_2|+|P_3| = 40$ W or 33 % more than in the optimal cases illustrated in Fig. 2(c). On the other hand, the subMIC power rating in the isolated-port architecture can be reduced to 67 % of the subMIC power rating with optimal power processing.

III. System Modeling and SubMIC Controller Design

Figure 8 shows a simplified block diagram of the subMIC-enhanced PV module example connected to a downstream converter or load having incremental impedance $Z(s)$. The optional interconnection of the secondary subMIC port has been drawn with dashed lines.

This block diagram is used to introduce modeling and control techniques in this section. To facilitate the discussion, an example subMIC implementation, based on a bidirectional flyback dc-dc converter, is described in Section III-A. Assuming this subMIC implementation, averaged and small-signal linearized models of the PV module with subMICs are presented in Section III-B. Section III-C proposes a linear control approach for the synthesis of the corresponding distributed subMIC controllers, and addresses system and subMIC stability conditions and dynamic performance.

A. SubMIC Implementation Example

Figure 9 shows a possible implementation of each subMIC as a bidirectional flyback converter. This topology provides the required isolation and bidirectional power transfer capabilities. Operation in Discontinuous Conduction Mode (DCM) is preferred due to the elimination of diode reverse recovery losses, thus allowing high efficiency. Furthermore, when the converter is operated in DCM it exhibits simpler dynamic behavior, allowing a simpler controller design, as well as faster changes in the direction of power transfer.

In order to transfer power from primary to secondary side, Q_{pri} is controlled using conventional, constant-frequency pulse-width modulation with a duty cycle $D = \frac{T_{on}}{T_s}$, T_{on} being the switch on time and T_s the switching period. The

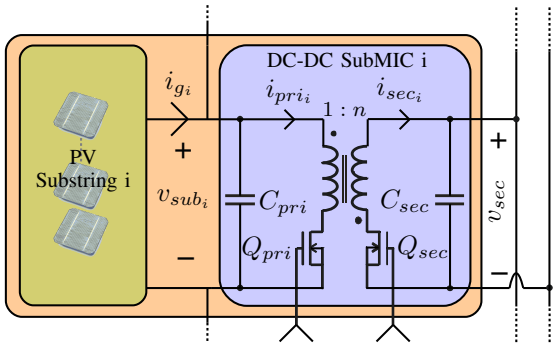


Figure 9. SubMIC implementation using a bidirectional flyback converter.

Table I
Bidirectional Flyback Example Design

Parameter	Value	Nominal Value
V_{sec}	[24,48] V	36 V
$V_{\text{sub,i}}$	[8,16] V	12 V
D	[0 , 0.4]	–
C_{pri}	188 μF	–
C_{sec}	40 μF	–
L_{pri}	2.3 μH	–
T_s	10 μs	–

secondary side switch, Q_{sec}, remains off at all times, and its body diode acts as the flyback diode. To reverse the power transfer direction, the converter is operated in a completely symmetrical manner: Q_{pri} remains off during the complete switching period, its body diode acts as the flyback diode, and Q_{sec} is now controlled in the manner described above. Although synchronous rectification could improve the efficiency of the converter, it is not considered here in order to simplify the controller implementation. Instead, a Schottky diode is placed in parallel with each switch to reduce body diode conduction and improve efficiency.

The flyback implementation of each subMIC includes capacitances both in the primary, C_{pri} and secondary side, C_{sec}. Given that all subMICs are ideally identical, the total secondary capacitance in the proposed architecture is $C_{seq} = C_{sec} \cdot n_s$. The primary side magnetizing inductance, L_{pri}, needs to be chosen to maintain DCM under all operating conditions. Table I shows an example design for a nominal $v_{sub_i} = 12$ V and a voltage conversion ratio $\frac{v_{sec}}{v_{sub_i}} = 3$, which is achieved with a transformer turns ratio of $1:3$.

B. Averaged and Linearized Dynamic Model

In this section, linear averaged models of the subMIC and the PV substring are introduced. States, inputs and outputs are represented as quiescent operating point values with small-signal ac variations, e.g.: $x(t) = X + \hat{x}(t)$ [29]. The time dependence of the variables may be omitted to simplify the notation. The models are first presented at the substring level, assuming n_s substrings. Then, a complete model of the subMIC-enhanced PV module, as shown in Figure 8, is derived.

1) Linearized Model of a PV Substring: Figure 10 shows an small-signal equivalent circuit diagram of a PV substring, which consists of a current source $\hat{i}_{g0_i}(t)$ and a resistance

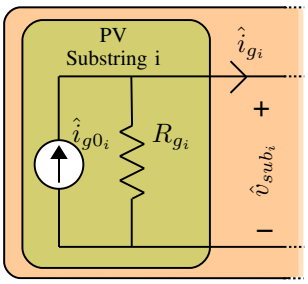


Figure 10. Linear small-signal model of a PV module substring.

R_{g_i} obtained by linearization of the nonlinear current-voltage characteristic of the PV substring at a certain operating point.

2) DCM Flyback SubMIC Current Reference to Duty-Cycle Command Response: Given that the flyback subMIC is operating in DCM, it can be modeled by a large-signal equivalent averaged circuit comprising a controllable loss-free resistance and a power source [29]. Note that the converter presents no averaged dynamics except for the input and output capacitors. The controllable resistance in the flyback DCM model is a nonlinear function of duty-cycle:

$$R_e(d_{pri_i})(t) = \frac{2L_{pri}}{d^2_{pri_i}(t)T_s}, \tag{12}$$

which implies that the primary-side current follows the substring voltage

$$i_{pri_i}(t) = \frac{v_{sub_i}(t)}{2L_{pri}} d^2_{pri_i}(t)T_s \tag{13}$$

As explained in Section II, a subMICs primary current $i_{pri_i}(t)$ should follow the current reference $i_{ref_i}(t)$ in order to achieve substring balancing. Setting $i_{pri_i}(t) = i_{ref_i}(t)$ in (13), the duty-cycle required to produce the requested $i_{ref_i}(t)$ can be found as:

$$d_{pri_i}(t) = \sqrt{\frac{i_{ref_i}(t)2L_{pri}}{v_{sub_i}(t)T_s}} \tag{14}$$

In a digital controller, given $i_{ref_i}(t)$ and sensed primary voltage $v_{sub_i}(t)$ as inputs, this duty-cycle can be computed using a lookup table. Assuming the sampling rate is high enough, $v_{sub_i}(t)$ can be considered constant over a sampling period, so that the corresponding update of $d_{pri_i}(t)$ based on (14) results in accurate matching between primary current $i_{pri_i}(t)$ and the references $i_{ref_i}(t)$.

Since subMICs must be able to transfer power in either direction, the same approach can be taken to compute the appropriate duty-cycle command for the secondary-side transistor when the primary-side current reference is negative, $i_{ref_i}(t) < 0$,

$$d_{sec_i}(t) = \sqrt{\frac{i_{ref_i^*}(t)2L_{sec}}{v_{sec}(t)T_s}}. \tag{15}$$

where, neglecting losses, the secondary current command $i_{ref_i^*}(t)$ is obtained from the primary current command

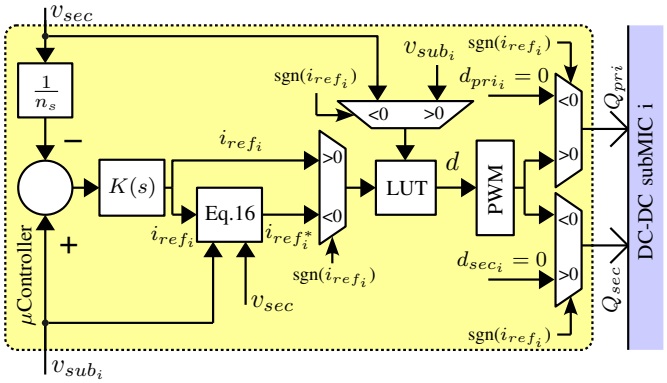


Figure 11. Block diagram of the sensorless current control of the DCM flyback converter.

$i_{ref_i}(t)$, primary voltage $v_{sub_i}(t)$ and secondary voltage $v_{sec}(t)$,

$$i_{ref_i^*}(t) = \frac{i_{ref_i}(t)v_{sub_i}(t)}{v_{sec}(t)}. \tag{16}$$

Figure 11 shows a block diagram of the subMIC current controller implemented in a micro-controller. The inputs are the sensed primary-side and secondary-side voltages. The outputs are the gate control signals for the primary-side switch Q_{pri} and the secondary-side switch Q_{sec}. Depending on the sign of the current command i_{ref_i}, only the primary or the secondary switch is active. One may note that the same look-up table is used to implement (14) or (15).

3) Linear Small-Signal Averaged Model of the SubMIC: Given the primary-port current control described above, the same large-signal averaged model of the subMIC in Fig. 9 applies, independent of the direction of power flow. The model consists of a voltage-controlled current source on the primary port, and a power source/sink on the secondary port, as shown in Fig. 12(a).

The secondary-port power source (or power sink) current can be expressed as

$$i_{sec_i}(t) = f(i_{pri_i}(t), v_{sub_i}(t), v_{sec}(t)) = \frac{i_{pri_i}(t)v_{sub_i}(t)}{v_{sec}(t)}, \tag{17}$$

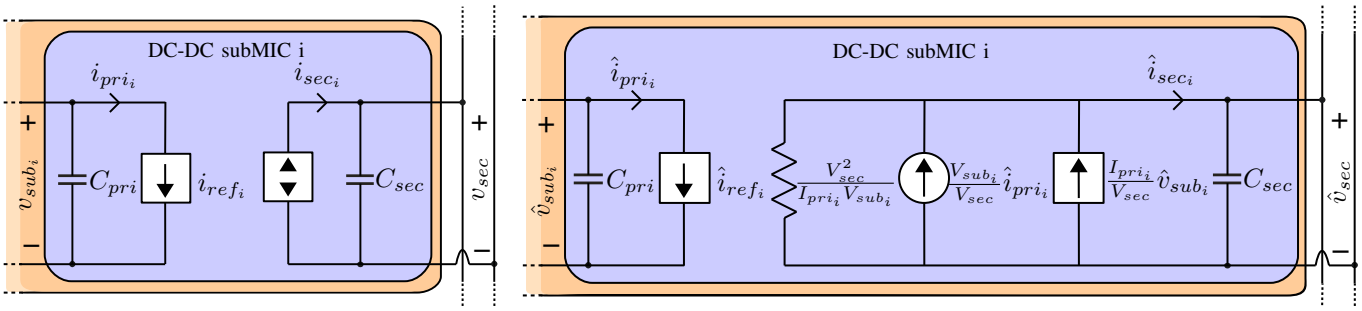
which can be linearized as follows:

$$I_{sec_i} + \hat{i}_{sec_i}(t) = f(I_{pri_i}, V_{sub_i}, V_{sec}) + \ldots \\ \frac{V_{sub_i}}{V_{sec}}\hat{i}_{pri_i}(t) + \frac{I_{pri_i}}{V_{sec}}\hat{v}_{sub_i}(t) - \frac{V_{sub_i}I_{pri_i}}{V^2_{sec}}\hat{v}_{sec}(t) \tag{18}$$

The result is the subMIC small-signal model shown in Fig. 12(b).

4) Complete Small-Signal Model of a SubMIC-Enhanced PV Module: A complete model of the subMIC-enhanced PV module example is described here, employing the linear small-signal models of the PV substring shown in Fig. 10 and the corresponding subMIC model shown in Fig. 12(b). Derivations below, which are shown for the isolated-port architecture, can be extended easily to the non-isolated architecture.

For the sake of generality, the influence of the load impedance $Z(s)$, as shown in Fig. 8, in the subMIC-enhanced



(a) Equivalent nonlinear averaged model with sensorless current control of the primary current $i_{pri_i}(t) = i_{ref_i}(t)$.

(b) Small-signal linearization at operating point V_{sub_i}, V_{sec}, I_{pri_i}.

Figure 12. SubMIC Model.

module is derived by applying Middlebrook's extra element theorem (EET) [29]. Fig. 13 illustrates application of the Middlebrook's EET theorem for the system in Fig. 8, to finding the closed-loop transfer function from PV current disturbance $\hat{i}_{g0_1}$ to module voltage $\hat{v}_{mod}$, in order to evaluate the effect of the load impedance $Z(s)$:

$$\frac{\hat{v}_{mod}(s)}{\hat{i}_{g0_1}(s)} := \left(G_{\frac{\hat{v}_{mod}}{\hat{i}_{g0_1}}}(s) \Big|_{Z(s)\to\infty} \right) \left(\frac{1+\frac{Z_N(s)}{Z(s)}}{1+\frac{Z_D(s)}{Z(s)}} \right) \tag{19}$$

by solving $G_{\frac{\hat{v}_{mod}}{\hat{i}_{g0_1}}}(s)$ when the output of the module is an open circuit ($Z(s) \to \infty$), and by extracting the port impedances $Z_D(s)$ and $Z_N(s)$, as described in [29].

Considering the open-circuit load impedance $Z(s) \to \infty$, the differential equations of the PV module with subMICs, as shown in Fig. 13, can be derived as follows:

$$\begin{cases} \dfrac{d\hat{v}_{sub_1}(t)}{dt} = \dfrac{\hat{i}_{g0_1}(t) - \frac{\hat{v}_{sub_1}(t)}{R_{g_1}} - \hat{i}_{mod}(t) - \hat{i}_{ref_1}(t)}{C_{pri}} \\ \dfrac{d\hat{v}_{sub_2}(t)}{dt} = \dfrac{\hat{i}_{g0_2}(t) - \frac{\hat{v}_{sub_2}(t)}{R_{g_2}} - \hat{i}_{mod}(t) - \hat{i}_{ref_2}(t)}{C_{pri}} \\ \dfrac{d\hat{v}_{sub_3}(t)}{dt} = \dfrac{\hat{i}_{g0_3}(t) - \frac{\hat{v}_{sub_3}(t)}{R_{g_3}} - \hat{i}_{mod}(t) - \hat{i}_{ref_3}(t)}{C_{pri}} \\ \dfrac{d\hat{v}_{sec}(t)}{dt} = \dfrac{1}{C_{seq}} \Big(K_{11}\hat{i}_{ref_1}(t) + K_{12}\hat{i}_{ref_2}(t) + \cdots \\ K_{13}\hat{i}_{ref_3}(t) + K_{21}\hat{v}_{sub_1}(t) + K_{22}\hat{v}_{sub_2}(t) + \cdots \\ K_{23}\hat{v}_{sub_3}(t) - (K_{31}+K_{32}+K_{33})\hat{v}_{sec} \Big) \end{cases} \tag{20}$$

where

$$\begin{aligned} K_{11} &= \frac{V_{sub_1}}{V_{sec}}, \quad K_{21} = \frac{I_{ref_1}}{V_{sec}}, \quad K_{31} = -\frac{I_{ref_1}V_{sub_1}}{V_{sec}^2}. \\ K_{12} &= \frac{V_{sub_2}}{V_{sec}}, \quad K_{22} = \frac{I_{ref_2}}{V_{sec}}, \quad K_{32} = -\frac{I_{ref_2}V_{sub_3}}{V_{sec}^2}. \\ K_{13} &= \frac{V_{sub_3}}{V_{sec}}, \quad K_{23} = \frac{I_{ref_3}}{V_{sec}}, \quad K_{33} = -\frac{I_{ref_3}V_{sub_3}}{V_{sec}^2}. \end{aligned} \tag{21}$$

The equations can be written in state-space form, in order to easily extract the transfer functions of interest:

$$\begin{cases} \dot{\hat{x}}(t) = A\hat{x}(t) + B_u\hat{i}_{ref}(t) + B_w\hat{w}(t) \\ \hat{y}(t) = C\hat{x}(t) \end{cases} \tag{22}$$

From (20), state vector $\hat{x}(t)$, control input vector $\hat{i}_{ref}(t)$, disturbance input vector $\hat{w}(t)$ and outputs $\hat{y}(t)$ are defined as follows:

$$\begin{aligned} \hat{x}(t) &= \begin{bmatrix} \hat{v}_{sub_1}(t) \\ \hat{v}_{sub_2}(t) \\ \hat{v}_{sub_3}(t) \\ \hat{v}_{sec}(t) \end{bmatrix}, \quad \hat{i}_{ref}(t) = \begin{bmatrix} \hat{i}_{ref_1}(t) \\ \hat{i}_{ref_2}(t) \\ \hat{i}_{ref_3}(t) \end{bmatrix}, \\ \hat{w}(t) &= \begin{bmatrix} \hat{i}_{g0_1}(t) \\ \hat{i}_{g0_2}(t) \\ \hat{i}_{g0_3}(t) \\ \hat{i}_{mod}(t) \end{bmatrix}, \quad \hat{y}(t) = \begin{bmatrix} \hat{v}_{sub_1}(t) \\ \hat{v}_{sub_2}(t) \\ \hat{v}_{sub_3}(t) \\ \hat{v}_{mod}(t) \end{bmatrix}, \end{aligned} \tag{23}$$

while the state-space matrices are:

$$A = \begin{bmatrix} -\frac{1}{C_{pri}R_{g_1}} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_{pri}R_{g_2}} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_{pri}R_{g_3}} & 0 \\ \frac{K_{21}}{C_{seq}} & \frac{K_{22}}{C_{seq}} & \frac{K_{23}}{C_{seq}} & -\frac{K_{31}+K_{32}+K_{33}}{C_{seq}} \end{bmatrix},$$

$$B_u = \begin{bmatrix} -\frac{1}{C_{pri}} & 0 & 0 \\ 0 & -\frac{1}{C_{pri}} & 0 \\ 0 & 0 & -\frac{1}{C_{pri}} \\ \frac{K_{11}}{C_{seq}} & \frac{K_{12}}{C_{seq}} & \frac{K_{13}}{C_{seq}} \end{bmatrix}, \; C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 \end{bmatrix},$$

$$B_w = \begin{bmatrix} \frac{1}{C_{pri}} & 0 & 0 & -\frac{1}{C_{pri}} \\ 0 & \frac{1}{C_{pri}} & 0 & -\frac{1}{C_{pri}} \\ 0 & 0 & \frac{1}{C_{pri}} & -\frac{1}{C_{pri}} \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{24}$$

The control-to-substring voltage transfer function, which models the effect of subMIC control on its corresponding substring voltage is:

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}}(s) := \frac{\hat{v}_{sub_i}(s)}{\hat{i}_{ref_i}(s)} \Bigg|_{\substack{\hat{i}_{ref_j}=0,\ \forall j=1,\ldots,n_s,\ j\neq i \\ \hat{i}_{g0_k}=0,\ \forall k=1,\ldots,n_s}}, \tag{25}$$

In the presence of incremental load impedance $Z(s)$, applying

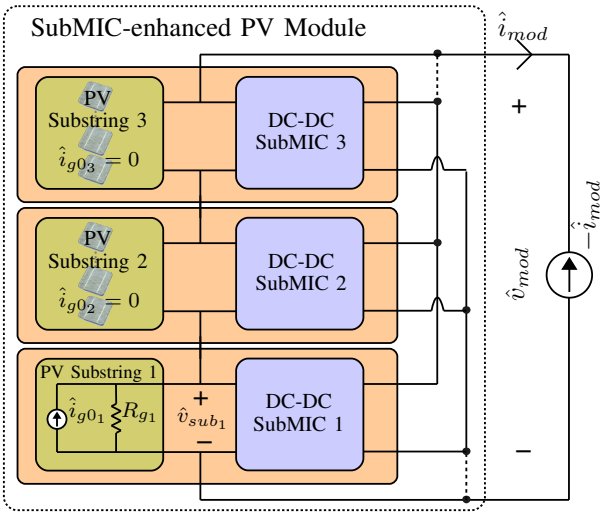


Figure 13. Application of Middlebrook's extra element theorem to the subMIC-enhanced PV module.

the EET gives

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}Z(s)}(s) = \left(G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}}(s)\right)\left(\frac{1+\frac{Z_{N_1}(s)}{Z(s)}}{1+\frac{Z_{D_1}(s)}{Z(s)}}\right) \tag{26}$$

where the disturbance input $\hat{i}_{mod}$ can be employed to derive $Z_{D_1}(s)$ and $Z_{N_1}(s)$,

$$Z_{D_1}(s) := \left.\frac{\hat{v}_{mod}(s)}{-\hat{i}_{mod}(s)}\right|_{\substack{\hat{i}_{ref_i}=0,\ \forall i=1,\dots,n_s,\\ \hat{i}_{g0_k}=0,\ \forall k=1,\dots,n_s}}, \tag{27}$$

$$Z_{N_1}(s) := \left.\frac{\hat{v}_{mod}(s)}{-\hat{i}_{mod}(s)}\right|_{\substack{\hat{v}_{sub_i}(s)\to 0,\\ \hat{i}_{ref_j}=0,\ \forall j=1,\dots,n_s,\ j\neq i\\ \hat{i}_{g0_k}=0,\ \forall k=1,\dots,n_s}}, \tag{28}$$

Another transfer function of interest is the PV current disturbance-to-substring voltage, which predicts the effect of a mismatch current on the module voltage:

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{g0_i}}}(s) := \left.\frac{\hat{v}_{sub_i}(s)}{\hat{i}_{g0_i}(s)}\right|_{\substack{\hat{i}_{g0_j}=0,\ \forall j=1,\dots,n_s,\ j\neq i\\ \hat{i}_{ref_k}=0,\ \forall k=1,\dots,n_s}}. \tag{29}$$

which in closed loop, considering the proposed subMIC control $\hat{i}_{ref_i} = K(s)(\frac{\hat{v}_{mod}(s)}{n_s} - \hat{v}_{sub_i})$, is:

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{g0_i}}CL}(s) := \left.\frac{\hat{v}_{sub_i}(s)}{\hat{i}_{g0_i}(s)}\right|_{\hat{i}_{g0_j}=0,\ \forall j=1,\dots,n_s,\ j\neq i}. \tag{30}$$

Also in this case, in order to consider the effect of possible influence of the load impedance $Z(s)$ in this transfer function, the extra element theorem can be applied as follows:

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{g0_i}}CL_{Z(s)}}(s) = \left(G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{g0_i}}CL}(s)\right)\left(\frac{1+\frac{Z_{N_2}(s)}{Z(s)}}{1+\frac{Z_{D_2}(s)}{Z(s)}}\right) \tag{31}$$

where $Z_{D_2}(s)$ and $Z_{N_2}(s)$ are:

$$Z_{D_2}(s) := \left.\frac{\hat{v}_{mod}(s)}{-\hat{i}_{mod}(s)}\right|_{\hat{i}_{g0_i}=0,\ \forall i=1,\dots,n_s} \tag{32}$$

$$Z_{N_2}(s) := \left.\frac{\hat{v}_{mod}(s)}{-\hat{i}_{mod}(s)}\right|_{\substack{\hat{v}_{sub_i}(s)\to 0,\\ \hat{i}_{g0_j}=0,\ \forall j=1,\dots,n_s,\ j\neq i}} \tag{33}$$

C. Voltage Loop Controller Design

The primary current-to-primary voltage transfer function derived previously stands for the control-to-output transfer function for each subMIC. In other words, this transfer function models the effect of each substring controller, which sets $\hat{i}_{ref_i}$ in every subMIC, on the primary voltages.

For the isolated architecture, when $Z(s) \to \infty$, this transfer function becomes:

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}}(s) = -\frac{R_{g_i}}{1+C_{pri}R_{g_i}s}, \tag{34}$$

When the PV module is working at an operating point (V_{mod}, I_{mod}), $Z(s)$ can be considered a linear resistance $Z(s) = R_{mod}$, and the control-to-output transfer function becomes:

$$G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}Z(s)}(s) = -\frac{R_g(1+R_g(\frac{2}{R_{mod}}+C_{pri}s))}{(1+C_{pri}R_gs)(1+R_g(\frac{3}{R_{mod}}+C_{pri}s))}, \tag{35}$$

In this last expression, all resistances R_{g_i} are considered equal to R_g.

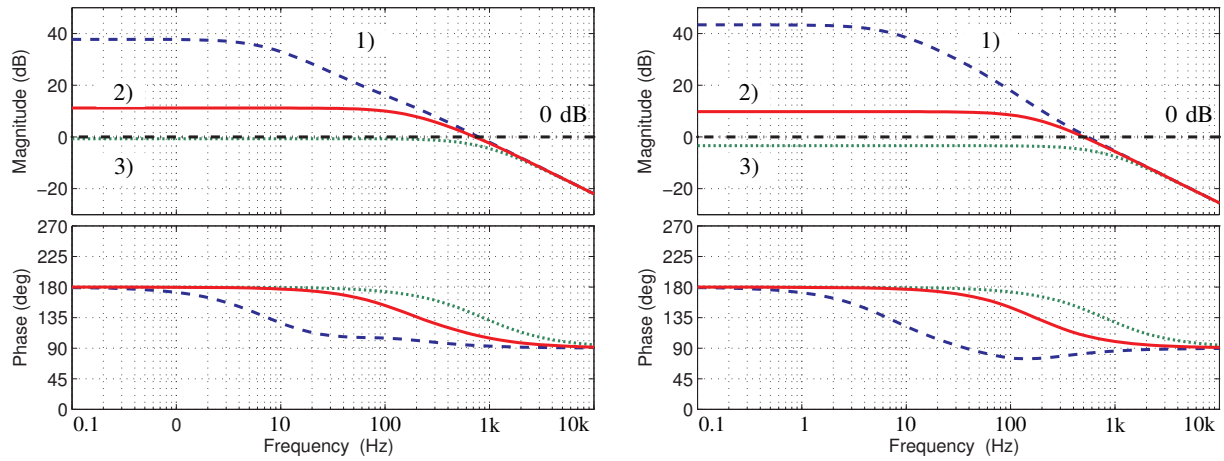
Bode plots of $G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}Z(s)}(s)$, for the isolated and the nonisolated architectures, are shown in Fig. 14 for three cases corresponding to (1) approximately constant current, (2) MPP, and (3) approximately constant voltage regions of the voltage-current characteristic of the PV module. The values of parameters used to plot the Bode diagrams are given in Table II.

While the frequency response of the non-isolated architecture is affected by the steady-state values of I_{ref_i}, V_{sub_i} and V_{sec}, the response of the isolated-port architecture is only affected by the values of R_{g_i} and R_{mod}, given that the operating point parameters from the linearization of the secondary ports only affect the isolated secondary voltage. Nevertheless, both systems are minimum-phase and consequently, phase margin can be assured to be positive for all cases.

Figure 15 depicts a block diagram of the proposed control loop for each subMIC. It is worth noting that this block diagram is valid both for the isolated-port and the non-isolated architectures. To see this, recall the control expression derived in Section II-B:

$$\hat{i}_{ref_i}(s) = K(s)(\frac{\hat{v}_{mod}(s)}{n_s} - \hat{v}_{sub_i}), \tag{36}$$

where, in the case of the non-isolated architecture, $v_{mod} = v_{sec}$. In the case of the isolated-port architecture, v_{sec} can be chosen arbitrarily, since setting the secondary voltage as reference results in the same power balance of the non-isolated version. In order to clarify this point, note that regardless of the initial condition of the secondary voltage, its steady-state value approximately equals the substring voltage, and given that the secondary port is shared, all substring voltages are equal. Also, it should be noted that given the sign of the error between v_{sub_i} and v_{mod}/n_s, and the sign of the DC gain in



(a) Non-isolated architecture.

(b) Isolated-port architecture.

Figure 14. Magnitude and phase responses of $G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}Z(s)}(s)$ for the parameters in Table II. 1) Dashed line: Constant current region, $R_{g_{1,2,3}}$ = 113 Ω, $V_{sub_{1,2,3}}$ = 10 V, R_{mod} = 18 Ω, $I_{ref_1} = -\frac{2}{3}$ 5 A, $I_{ref_{2,3}} = \frac{1}{3}$ 5 A. 2) Solid line: MPP region, $R_{g_{1,2,3}}$ = 4.6 Ω, $V_{sub_{1,2,3}}$ = 12.5 V, R_{mod} = 7.5 Ω, $I_{ref_{1,2,3}}$ = 0 A. 3) Dotted line: Constant voltage region, $R_{g_{1,2,3}}$ = 1.02 Ω, $V_{sub_{1,2,3}}$ = 13.5 V, R_{mod} = 8.1 Ω, $I_{ref_{1,2,3}}$ = 0 A.

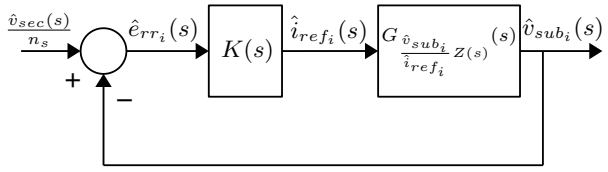


Figure 15. Small-signal block diagram of a PV substring with the proposed subMIC controller.

Table II
LINEAR MODEL PARAMETERS

Parameter	Constant Current Region	MPP Region	Constant Voltage Region
R_{g_i}	[37.7, 113] Ω	[4.6, 13.9] Ω	[1.02, 3] Ω
V_{sub_i}	10 V	12.5 V	13.5 V
I_{ref_i}	[-$\frac{2}{3}$ 5, $\frac{2}{3}$ 5] A	[-$\frac{2}{3}$ 5, $\frac{2}{3}$ 5] A	[-$\frac{2}{3}$ 5, $\frac{2}{3}$ 5] A

the transfer function $G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{ref_i}}}(s)$, the DC gain of the controller must be negative to satisfy closed-loop stability.

From Fig. 15, the loop gain $T_{sub_i}(s)$ can be employed to synthesize an appropriate controller $K(s)$:

$$T_{sub_i}(s) := K(s)G_{\frac{\hat{v}_{sub_i}}{\hat{i}_{pri_i}}Z(s)}(s) \tag{37}$$

Figure 16 shows the Bode plots of the loop gain $T_{sub_i}(s)$, with a controller consisting of a pole at $-\omega_p$ and a zero at $-\omega_z$. Since the controller transfer function is proper, positive phase margin is guaranteed:

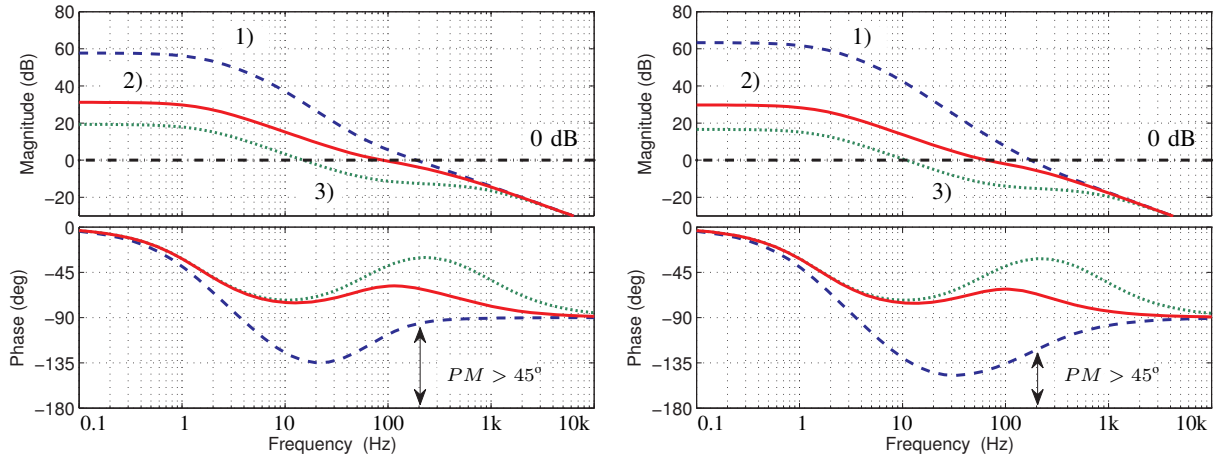
$$K(s) = K\frac{s/\omega_z + 1}{s/\omega_p + 1} = -10\frac{s/400 + 1}{s/10 + 1}. \tag{38}$$

This controller is appropriate both for the isolated-port and the non-isolated architecture. The phase margin is always approximately equal to or larger than 45 degrees for the operating points shown. Regulation bandwidth is approximately 200 Hz in the highest gain case, which is the constant current region. Note that the target controller bandwidth was set relatively low for practical reasons detailed in Section IV.

The dynamic response of the closed-loop subMIC-enhanced PV module with controller (38) has been examined with the aid of the extra element theorem, in order to explore cross-coupling effects between subMICs and interactions with the load impedance $Z(s)$.

Figure 17 shows the Bode plots of the current $\hat{i}_{g0_1}$ disturbance to substring voltages $\hat{v}_{sub_1}$ and $\hat{v}_{sub_2}$, that is, the closed-loop response to a disturbance in the corresponding substring voltage and in the remaining substrings. The figure shows the analytical linearized model matched against numerical simulations of the nonlinear averaged circuit. The responses have been derived in the MPP region for two cases: when $Z(s)$ is a resistance R_{mpp} that sets the module voltage to $V_{mod} \approx 37.5\ V$, and when $Z(s)$ is approximately zero, i.e. when the load is a downstream converter that regulates the voltage to $V_{mod} \approx 37.5\ V$. Only the frequency response of the isolated architecture is shown. The frequency response for the non-isolated architecture closely resembles the response in Fig. 17. It can be observed that, if subMICs are turned off, a perturbation in the substring current affects the substring voltage and, in turn, affects the voltage in the remaining substrings. With a resistive load, when subMICs are turned on, this effect is minimized due to the controlled voltage balancing, but the overall voltage is still affected by the disturbance, since a change in irradiance implies a change in the operating point. When the load regulates the module voltage together with subMICs, substring voltage regulation is improved, which results in approximately constant substring and module voltages, even during transients.

A numerical simulation of the 3 substrings nonlinear PV module with the nonlinear averaged model of subMICs controlled with the proposed $K(s)$ has been carried out using MATLAB. The subMIC model considers an efficiency of 90 %. The results can be observed in Fig. 18. In the simulation,



(a) Non-isolated architecture. (b) Isolated-port architecture.

Figure 16. Magnitude and phase responses of $T_{sub_1}(s)$ with controller $K(s)$ for the parameters in Table II. Phase margin (PM) is ensured to be greater than 45°. 1) Dashed line: Constant current region, $R_{g_{1,2,3}}$ = 113 Ω, $V_{sub_{1,2,3}}$ = 10 V, R_{mod} = 18 Ω, $I_{ref_1} = -\frac{2}{3}$ 5 A, $I_{ref_{2,3}} = \frac{1}{3}$ 5 A. 2) Solid line: MPP region, $R_{g_{1,2,3}}$ = 4.6 Ω, $V_{sub_{1,2,3}}$ = 12.5 V, R_{mod} = 7.5 Ω, $I_{ref_{1,2,3}}$ = 0 A. 3) Dotted line: Constant voltage region, $R_{g_{1,2,3}}$ = 1.02 Ω, $V_{sub_{1,2,3}}$ = 13.5 V, R_{mod} = 8.1 Ω, $I_{ref_{1,2,3}}$ = 0 A.

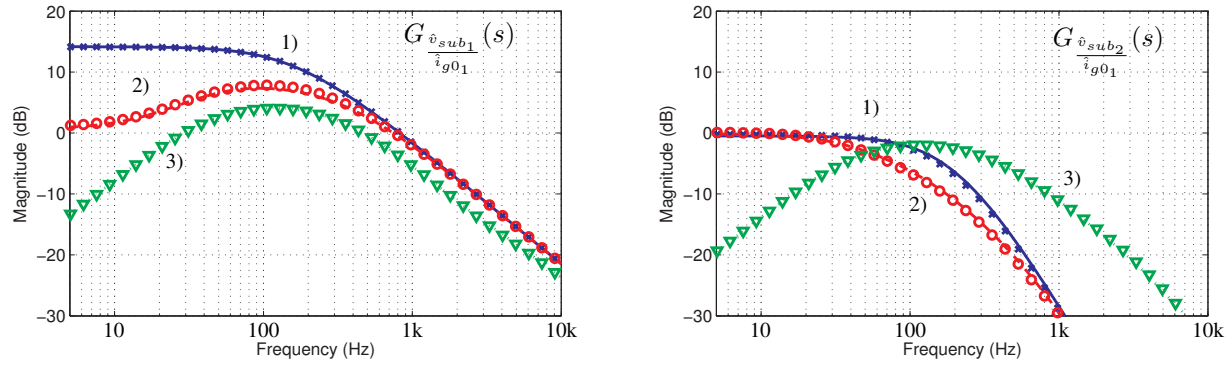
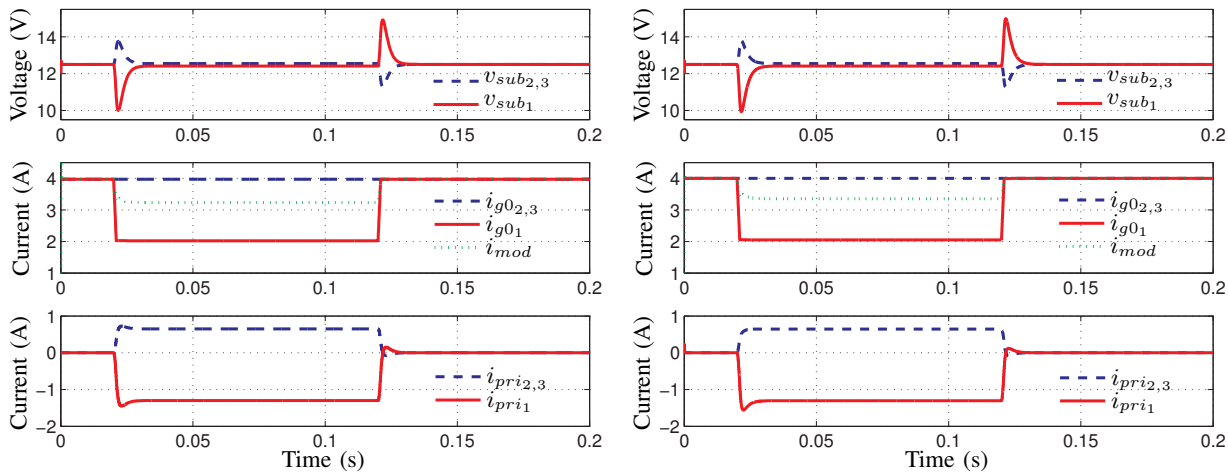


Figure 17. Bode plots of $G_{\frac{\hat{v}_{sub_1}}{\hat{i}_{g0_1}}}(s)$ and $G_{\frac{\hat{v}_{sub_2}}{\hat{i}_{g0_1}}}(s)$. 1) With subMICs turned off and $Z(s) = R_{mpp}$: analytical linear model (solid line) and simulation results (x); 2) with subMICs turned on and $Z(s) = R_{mpp}$: analytical linear model (dashed line) and simulation results (o); 3) with subMICs turned on and $Z(s)$ being a voltage regulator at $v_{mod} \approx v_{mpp}$: analytical linear model (dotted line) and simulation results (v).



(a) Non-isolated architecture. (b) Isolated-port architecture.

Figure 18. Transient simulation of a PV module with 3 substrings and 3 subMICs for a step mismatch disturbance of ± 2 A.

at $t = 0$ all substrings supply the same current, 4 A. Then, at $t = 20$ ms substring #1 becomes mismatched and supplies 2 A. SubMICs inject and extract currents so that the averaged module current is $\frac{\sum_{i=1}^{ns} i_{g_i}}{ns}$. It should be noted that $\sum_{i=1}^{ns} i_{pri_i} \approx 0$. At $t = 120$ ms, substring #1 recovers its power delivery and, as expected, the subMICs stop injecting and extracting currents.

Regarding the system stability of the nonlinear PV module, the flyback subMICs and the corresponding regulation loops, it is worth to point out that the complete system can be formally analyzed by employing Lyapunov stability concepts and linear matrix inequalities (LMIs). This framework could be employed to verify the stability of the system despite its nonlinear time-variant nature, as in [30], [31].

IV. Experimental Results

This section presents the experimental realization and results obtained for the subMIC realization, subMIC-enhanced PV module architectures, and the proposed control methods.

A. Experimental Setup

In order to demonstrate the proposed architectures, control methods and dynamic models, three flyback converter prototypes are attached as subMICs to the corresponding substrings in a 72-cell, 180 W PV module with a nominal MPP voltage of 37 V. The experimental setup can be seen in Fig. 19. For flexibility, converter power rating was chosen to be as large as a substring power rating, i.e. 60 W. For the proposed sub-optimal control approach, the maximum required power processing, corresponding to 100 % mismatch is:

$$\frac{n_s - 1}{n_s} G_i = \frac{2}{3} 60 \text{ W} = 40 \text{ W}. \tag{39}$$

In practice, given that the worst-case mismatch is typically much smaller than 100 %, the subMICs would be rated at a fraction of the substring nominal power.

Each flyback subMIC is designed for a nominal conversion ratio $\frac{v_{\text{sec}}}{v_{\text{pri}}} = 3$, employing a transformer turns ratio of $1 : 3$. Consequently, the subMIC prototypes could be used in both the isolated-port and the non-isolated architectures, keeping the same voltage reference $v_{ref} = v_{sec}/n_s$. The remaining design parameters are given in Table I. Experimental results for conversion efficiencies for primary-to-secondary power processing and for secondary-to-primary power processing, together with the waveforms of the converter for a duty-cycle of $D = 0.2$, are shown in Fig. 20. As mentioned above, the switching period is $T_s = 10$ μs. Note that the prototypes present efficiencies close to 90 % for a wide range of output powers.

Three separate low-cost microcontrollers TMS320F28027 implement the control algorithm for each subMIC. Each microcontroller includes a $\mathcal{Z}$-domain version of the compensator $K(s)$ in (38), obtained using a first order transformation, as well as the mapping between the current reference and the duty cycle command (14) using look-up tables. A sampling time equal to $T_{sm} = 0.2$ ms was used due to the limited computation capabilities of the TMS320 microcontroller; the controller

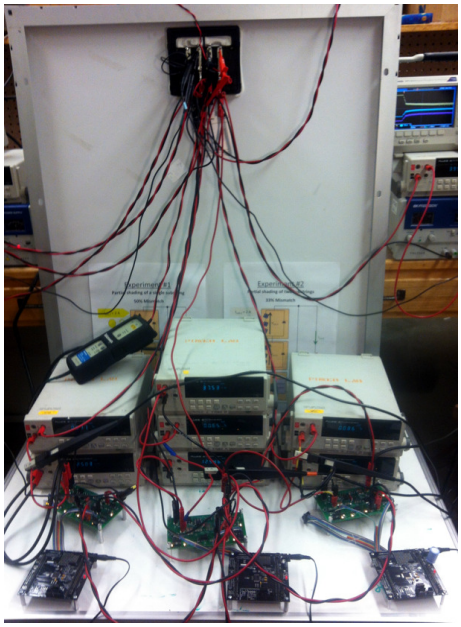
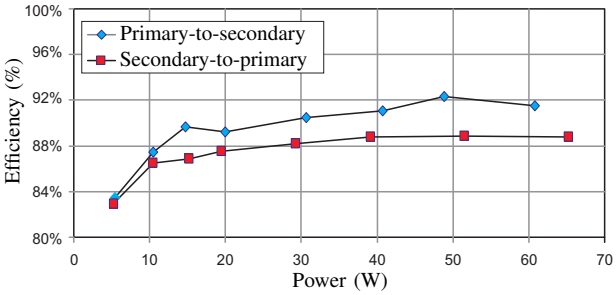
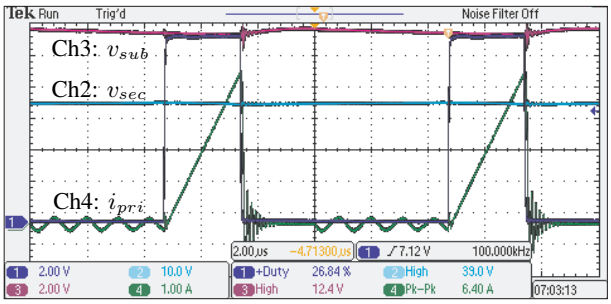


Figure 19. Experimental setup: back: PV module; middle: flyback subMICs; front: microcontroller development boards.



(a) Flyback subMIC efficiency.



(b) Experimental waveforms in a flyback subMIC prototype injecting current at a duty cycle of $D = 0.2$, i.e. $P \approx 12$ W.

Figure 20. Experimental flyback subMIC efficiency and converter operating waveforms.

$K(s)$ is designed taking into account this relatively large sampling time. Finally, note that the three microcontrollers operate autonomously with no need for any data interchange or synchronization.

The experiments were carried out indoors, biasing the PV substrings individually with a current limited voltage source to emulate various solar irradiation levels. Mismatching of each substring was forced by adjusting the current limit in the corresponding voltage source. The output of the module

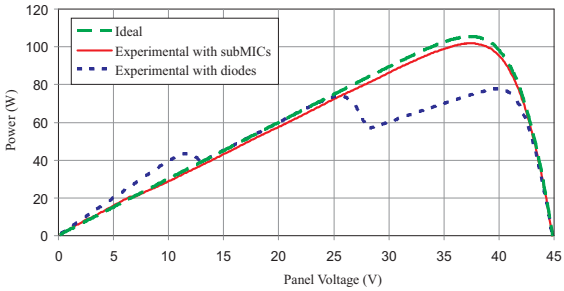


Figure 21. Experimental power-voltage characteristics of a mismatched PV module with bypass diodes and with subMICs.

was connected to an electronic load that regulated the module voltage.

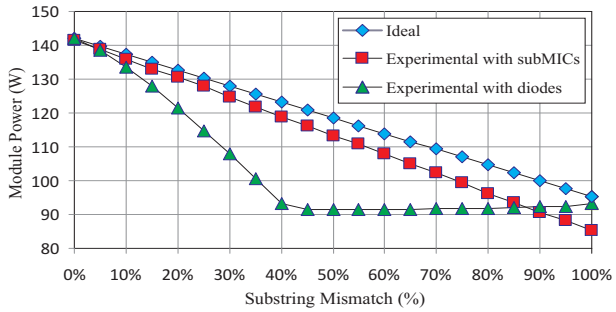
B. Steady-state Results

In order to verify the main features of the proposed system, the electronic load attached to the module was programmed to perform a voltage sweep while measuring the power output of the PV module. Two sets of measurements were carried out, one using conventional bypass diodes, and a second one with the diodes replaced by flyback subMICs controlled using the proposed distributed method. Both the non-isolated and the isolated-port architectures were tested.

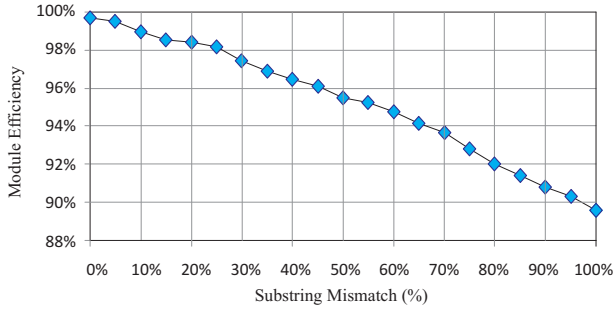
Figure 21 shows the results in the case of the non-isolated architecture, with the three substrings biased with 2 A, 3 A and 4 A, respectively. A typical non-convex power-voltage curve is obtained when using the bypass diodes, the MPP being at 40 V, 77 W. The curve obtained with the subMICs yields a single MPP at around 37 V, very close to the nominal module MPP voltage, and an output power of 102 W, which yields 32 % higher output power. The results obtained with the isolated-port architecture are identical to those shown in Fig. 21.

Steady-state measurements showing the PV module efficiency with respect to [0-100] % mismatch in one of the substrings are shown in Fig. 22. Figure 22(a) shows a comparison between the available power (ideal) and the measured output power obtained using the flyback subMICs, as well as bypass diodes. The same data is shown in normalized form in Fig. 22(b) for the subMIC-enhanced module. The module-level efficiency of the subMIC-enhanced module is close to 90 % for a 100 % mismatch in one of the substrings, whereas it remains above 98 % for mismatch less than about 25 %.

Figure 23 shows measured steady-state substring voltages, as well as the reference voltage for the non-isolated subMIC architecture. In the absence of any power processed by the subMICs (no mismatch), there is an offset between the substring voltages, which is mainly due to ADC calibration errors. According to the proposed control method (3), the primary current of each subMIC is proportional to the controller DC gain and to the steady-state voltage error between the reference and the substring voltage. When subMICs process no power they process zero primary current and thus the voltage error is very small. As the mismatch in substring #1 increases, subMIC #1 injects more current; Fig. 23 shows the steady-state voltage error increasing accordingly. SubMICs #2 and #3 also increase



(a) Comparison between ideal and experimental power output with bypass diodes and with subMICs.



(b) Experimental module-level efficiency with subMICs: ratio of the actual output power to the ideal output power.

Figure 22. Experimental efficiency of a PV module with subMICs, for [0, 100] % mismatch of one of the substrings.

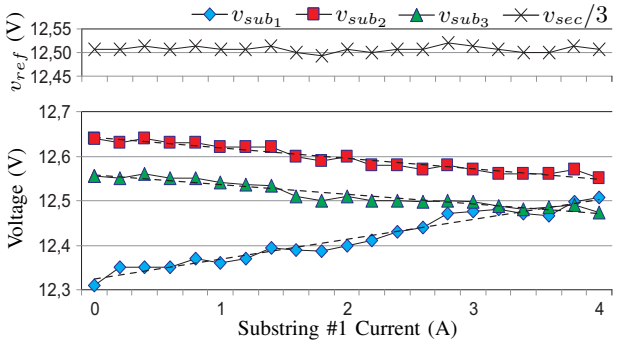


Figure 23. Experimental substring and reference voltages for [0, 4] A in substring #1, while substrings #2 and #3 deliver 4 A.

their voltage error, but with half the slope as they always handle half of the current of subMIC #1. Moreover, the voltage error has opposite sign in subMIC #1 with respect to subMICs #2 and #3, which corresponds to power (current) circulating in opposite directions. For example, for a mismatch of 4 A in substring #1, the primary current in subMIC #1 is $I_{pri_1} = -\frac{2}{3}4A$, and the steady-state error between reference and substring voltage equals $V_{ref} - V_{sub_1} = \frac{1}{K} I_{pri_1} \approx 250\ mV$, which is in good agreement with the results in Fig. 23.

C. Dynamic Responses

The dynamics of the system were verified under the same conditions of the simulations shown in Fig. 17. A resistive load R_{mpp} was set up to operate approximately at the MPP and a current disturbance was injected in substring #1 in order to evaluate the transfer function $G_{\frac{\hat{v}_{sub_1}}{\hat{i}_{g0_1}}}(s)$. The top diagram

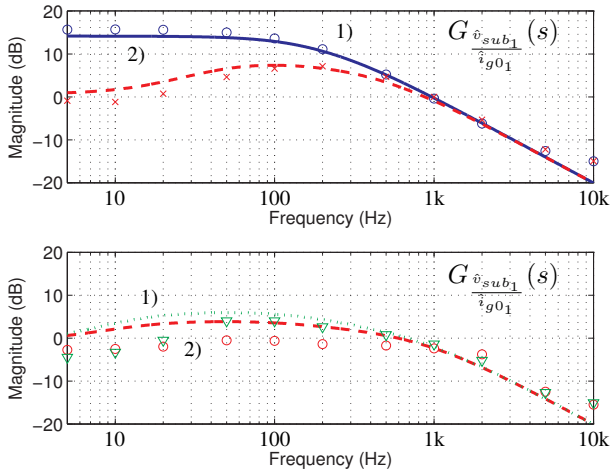


Figure 24. Experimental frequency response of the subMIC-enhanced PV module, $G_{\frac{\hat{v}_{sub_1}}{\hat{i}_{g0_1}}}(s)$, at MPP ($V_{mod} \approx 37.5\ V$), against analytical linear model. Top Diagram: 1) With subMICs turned off and $Z(s) = R_{mpp}$: analytical linear model (solid line) and experimental results (o); 2) with subMICs turned on and $Z(s) = R_{mpp}$: analytical linear model (dashed line) and experimental results (x). Bottom Diagram: 1) with subMICs turned on at $I_{ref_1} = 1A$, $I_{ref_{2,3}} = -0.5A$, and $Z(s) = R_{mpp}$: analytical linear model (dashed line) and experimental results (o), 2) with subMICs turned on at $I_{ref_1} = -1A$, $I_{ref_{2,3}} = 0.5A$, and $Z(s) = R_{mpp}$: analytical linear model (dotted line) and experimental results (v).

shows the frequency response in absence of mismatch, while the bottom bode plot shows the frequency response when subMICs are correcting a mismatch of approximately ± 1.5 A between substring #1 and substrings #2 and #3.

The transient simulations of Fig. 18 were experimentally verified with an electronic load placed in parallel with substring #1, and programmed to step down the substring bias current by 2 A, emulating a sudden change in solar irradiation. The results of this experiment are depicted in Fig. 25, both for the non-isolated and the isolated-port architectures.

In the figure, substring current i_{g_1} decreases abruptly at $t = 20$ ms. This disturbance produces a mismatch and perturbs substrings voltages, which are regulated back to the reference voltage by subMICs, which process the required power to do so. It can be observed how the steady-state values of the primary currents, during the disturbance, are $i_{pri_1} = -\frac{2}{3}2A$ and $i_{pri_{2,3}} = \frac{1}{3}2A$. Also, it is worth noting that the sum of perturbed substring voltages remains approximately zero and that the secondary voltage stays approximately constant. Nevertheless, the secondary voltage in the isolated-port version changes slightly during the disturbance, due to the possible mismatches in subMICs operation. Finally, it should be noted that neither the capacitance of the PV module nor the capacitance introduced by the electronic load were taken into account in the model. While these capacitances do not modify the steady-state characteristics of the system, they may reduce bandwidth and therefore, increase settling time.

D. Effects of Temperature Gradients and Substring Shading Conditions

It is understood that the PV characteristic and the location of the MPP voltage may change with temperature gradients across substrings, different values of irradiance, and the distribution of shading. Although a complete analysis of these effects is beyond the scope of this paper, this section presents experimental results examples of experimentally measured system efficiency under various conditions.

a) Irradiance:
In the experimental tests performed an uniform change in irradiance of 75 % decreased the affected substring MPP voltage by 10 %. Compared to the ideal maximum available power of approximately 107 W the output power of the subMIC-enhanced PV module was approximately 106 W, corresponding to approximately 0.93 % of loss in output power.

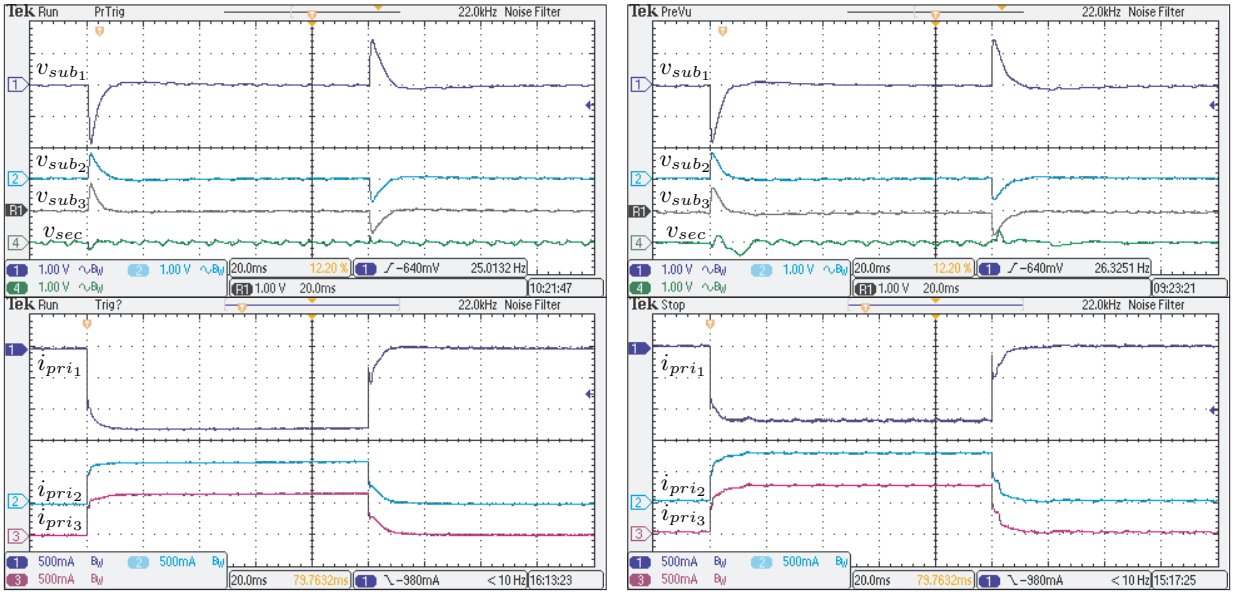
b) Temperature:
Another experimental test was set up by artificially cooling one of the substrings to about 30^oC while the other two substrings where at about 55^oC. The PV module was uniformly irradiated. Experimental data with subMICs indicated an output power of 121.9 W, compared to a maximum ideal power of 123.1 W, representing a power loss of about 1.7 % attributed to the significant difference in temperature.

c) Non-uniform shading:
A non-uniform shading of the PV module was reproduced experimentally by shading one cell in one of the substrings of the module. While the voltage-power shape increased the MPP voltage by 25 %, the subMIC-enhanced PV module was able to output a total power of 104.9 W, which corresponds to a power loss of 0.9 % of the maximum available power (105.9 W).

The experimental results presented in this section indicate that the subMIC-enhanced module is capable of recovering most of the ideally available output power even under significant temperature and shading variations.

V. Conclusions

In photovoltaic (PV) power modules or systems based on series-connected PV cells, mismatches due to manufacturing tolerances, partial shading, dirt, thermal gradients, or aging can result in significant losses in efficiency and energy captured by the PV system. This paper is focuses on PV module architectures where submodule integrated dc-dc converters (subMICs) are configured to process only a mismatch fraction of power, present no insertion losses, and are capable of performing fine-granularity MPPT. A basic, non-isolated subMIC-enhanced PV module architecture consists of the subMIC primary port connected in parallel with a PV cell substring, while the secondary ports are all connected in parallel across the module output. The subMICs are implemented as bidirectional dc-dc converters with isolation. It is shown that optimal power processing, corresponding to the minimum total power processed by the subMICs, can be solved as a linear programming problem and implemented using a central module-level controller. A much simpler, close-to-optimal distributed control approach is introduced that allows autonomous subMIC control without the need for a central controller or any communication of control or sensing signals among the subMICs. Furthermore, the subMICs can be rated at reduced power level compared to the optimal power processing case.



(a) Non-isolated architecture.

(b) Isolated-port architecture.

Figure 25. Experimental transient response of a 72-cell PV module with 3 substrings and 3 flyback subMICs for a step mismatch disturbance of $\pm$ 2 A.

The proposed subMIC control approach is well suited for an isolated-port architecture, where the subMIC secondary ports are connected in parallel, but disconnected from the module output. As opposed to the non-isolated architecture, where the subMICs must provide a conversion ratio equal to the number of substrings in the module, and switching devices must then be rated to cope with these voltage levels, the conversion ratio and the isolated-port voltage can be selected arbitrarily in the isolated-port architecture. This leads to practical advantages in terms of the size of magnetics, use of low-voltage components, efficiency optimization, as well as opportunities for scaling to arbitrarily large PV arrays. In practice, the subMICs can be implemented at a fraction of the PV module power rating, thus significantly reducing the cost of fine-granularity MPPT. Furthermore, the isolated-port architecture can enable an effective integration of active filtering, which leads to the potentials to reduce the cost and improve reliability of downstream grid-tied PV power electronics.

The isolated-port architecture can be controlled using a simple and effective approach based on distributed linear voltage regulators having finite dc gain. The regulators take the secondary voltage as a reference and balance the substrings, injecting or extracting power as required. The implementation of such a controller strategy can be done by means of standard analog or digital techniques without the need for current sensing. In addition, all subMICs operate autonomously, requiring no interconnections or synchronization between the converters.

The subMIC-enhanced PV module architectures and the control approach are validated by static and dynamic simulations and experimental results using three bidirectional flyback subMICs effectively replacing bypass diodes in a standard 72-cell, 180 W PV module, yielding greater than 98 % module-level power processing efficiency for a mismatch less than 25 %.

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