An Efficiency Comparison of Fuel-Cell Hybrid Systems Based on the Versatile Buck-Boost Converter

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***Abstract*—This paper extends the use of the versatile buck-boost converter to power manage a parallel hybrid system topology as an alternative to the well-known serial hybrid (SH) topology and the most recent series-parallel hybrid (SPH) topology. These systems utilize a proton exchange membrane fuel cell (PEMFC) as the primary source in combination with an auxiliary storage device (ASD), and the selected converter is in charge of the power management between the sources (FC or ASD) and the load. Therefore, the converter has a very important role in the system since it is responsible of ensuring a dc bus voltage regulation with a safe and reliable operation of the entire system while also guarantee a high power conversion efficiency. Hence, this is the third topology where the coupled-inductor dc-dc buck-boost converter is studied to demonstrate and exploit its advantages such as noninverting voltage step–up and step–down, high efficiency, regulation of input and output currents and low ripple values, and the ability to change from input to output current regulation loop, suddenly and smoothly, and vice versa. In order to determine which topology (SH, PH, or SPH) exhibits the highest power conversion efficiency under a certain load profile it is important to ensure a fair efficiency comparison that will only reflect the properties of the topology and not its individual components. Therefore, the same design criteria, the same control and the same components were used for all the studied topologies. Simulation and experimental results have been validated on a 48-V 1200-W dc bus.**

***Index Terms*—Energy management, dc-dc power conversion, current control, efficiency comparison, PEM fuel cell, hybrid topologies.**

I. Introduction

The energy sharing between the fuel cell, the ASD and the load can be successfully managed by means of switching power converters [1]–[3]. However, designing the hybrid power system architectures and their energy management algorithms is a complex task which directly affects the elements' sizing, costs and efficiency of the whole system [4]–[6]. Furthermore, the design of a hybrid system is closely related to the specific application and the load profile [7]. In this context, the fuel cell hybrid system architectures and algorithms are designed to support a specific load power consumption profile with minimum required production costs, system size, and hydrogen consumption, as well as a maximum achievable efficiency of the whole system [8].

A mathematical analysis of efficiency of the commonly used serial hybrid (SH) and parallel hybrid (PH) topologies, shown in Fig. 1(a) and (b), has been presented in [9]. In addition, a novel series-parallel hybrid (SPH) topology, shown in Fig. 1(c), has also been proposed in [9]. This new topology exhibits a higher efficiency than the SH or PH topologies in non-regenerative operation, independent of the load profile. However, the results presented in [9] are based only on a complex mathematical analysis and supported with numerical simulation, without any experimental verification.

For designing the three different hybrid topologies depicted in Fig. 1, the same kind of a switching power converter will be used for all the required dc-dc converters in the system. The use of identical converters at all the locations within the three studied topologies reduces the costs and development time, as well as simplifies the control strategy [10]. The selected dc-dc converter topology is the non-inverting buck-boost converter proposed in [11] shown in Fig. 2. Its advantageous features include a non-inverting step-up/step-down dc-dc characteristic that allows interfacing between unregulated voltage sources, high power conversion efficiency, the possibility of controlling either the input and output voltages or currents [12], and achieving fast and smooth transitions when changing the control objective from controlling the input current to controlling the output current and vice-versa [13].

In addition, the selected converter is capable of avoiding the operational dead zone at the transition between buck and boost operating modes, as presented in [14]. Further, the utilization of the same converter and the same number of converters in all the topologies shown in Fig. 1 allows a fairer efficiency comparison between the different topologies. The chosen non-inverting buck-boost converter has been previously employed with success in the SH topology [15] and the SPH topology [10]. The information about the control and protection loops design, the elements' sizing criteria, the converters' models,

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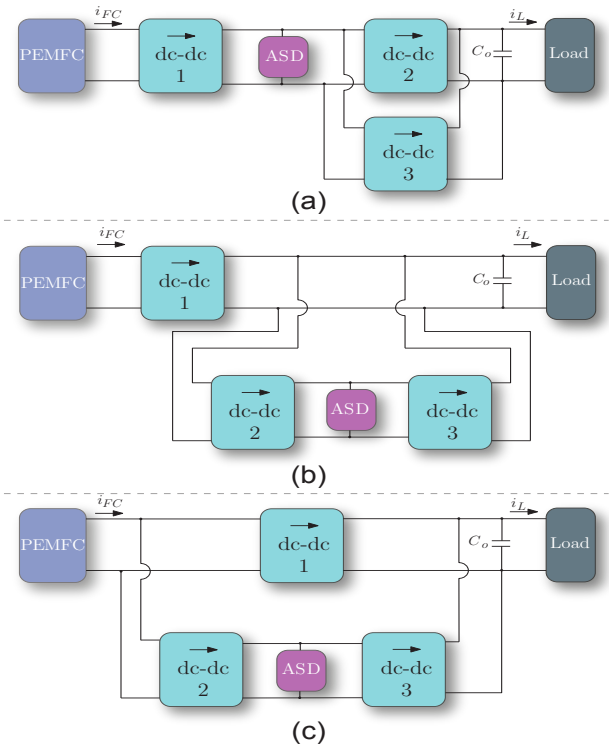


Fig. 1. FC-based hybrid power system topologies: (a) SH topology, (b) PH topology, and (c) SPH topology.

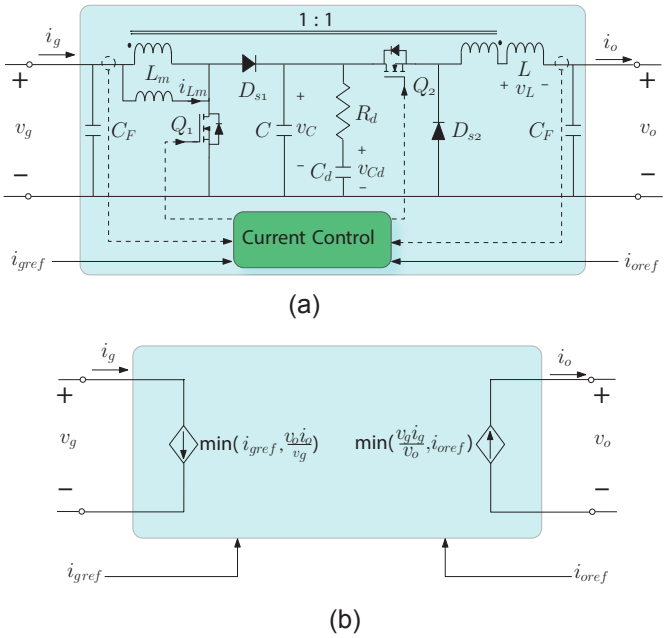


Fig. 2. Proposed modular buck-boost converter and its respective current control: (a) switching model to study short-time simulations ($L_m = 35\ \mu$H, $C = 13.2\ \mu$F, $R_d = 1.5\ \Omega$, $C_d = 66\ \mu$F, $L = 35\ \mu$H and a switching frequency of 100 kHz) and (b) block diagram to study long-time simulations.

and the digital master control block diagrams is given in [15], while the main operating states, which occur in the three discussed hybrid systems, are presented in [10].

A parallel hybrid topology (PH) consisting of a power source, an auxiliary storage device (ASD), and a load requires three unidirectional dc-dc converters for its practical realization, as demonstrated by the block diagram in Fig. 3. The five different operating states that can occur in the discussed PH topology are presented in Fig. 4, while the individual states and transitions between them are comprehensively described in [10]. Like in [15] and [10], where serial hybrid (SH) and series-parallel hybrid (SPH) topologies were discussed, the same kind of a dc-dc converter will be used to perform the tasks of the three converters within the system shown in Fig. 3.

The most notable FC-based PH systems described in the literature are listed in Table I. On the basis of this state-of-the-art review, the main contributions of this paper are following:

- A simulation and experimental validation of energy management by a PH topology utilizing three identical non-inverting buck-boost converters. The performed validation tests are the same of the two hybrid topologies previously published [10], [15]. In addition, the PH topology is much more complex to manage compared to the SH and SPH topologies. This is because the dc-bus voltage v_o is Is controlled by one of the three converters of the system in the PH topology (see Fig. 4) while in the other SH and SPH topologies it is only performed by one of only two converters connected to the bus.
- The usage of the same module for all the dc-dc converter's within each topology reduces the manufacturing times and costs, while simplifies modeling and control design tasks. It is evident that the converters 2 and 3 from Fig. 3 can be replaced by a bidirectional module, however, the bidirectional current-controlled coupled-inductor dc-dc buck-boost converter is under study. In addition, to ensure a fair efficiency comparison between the topologies is necessary to use the same number of converters in each of them as shown in Fig. 1.
- An fair experimental efficiency comparison of three different PEM fuel cell power systems topologies.

This paper is organized as follows: Section II presents a detailed description of the energy management algorithm design for the PH topology. Simulations and experimental results of the PH topology are presented and discussed in Section III. Their aim is to validate the performance of the PH topology under the same testing conditions as presented in [10], [15] for SH and SPH topologies, and thus obtain a fair efficiency comparison between the three hybrid topologies. Section IV provides an experimental efficiency comparison of the three discussed FC-based hybrid topologies. Finally, the main conclusions and the remaining challenges for the future are summarized in Section V.

II. PH TOPOLOGY ENERGY MANAGEMENT DESCRIPTION

The main goal of this subsection is to describe the energy management for the PH topology shown in Fig. 3. The capacitors' voltage ranges and capacitances, dc-bus voltage reference, the maximum and minimum fuel cell slew rates (SRs), the converters' maximum currents, the control loops'

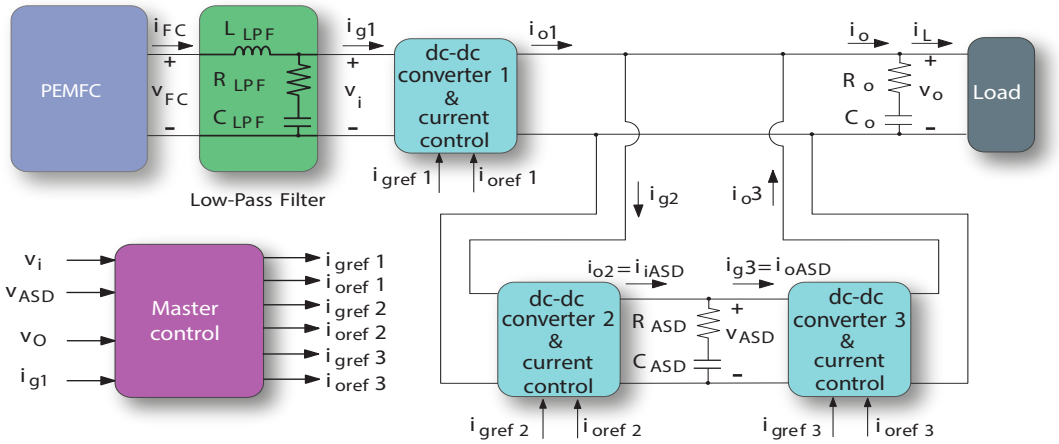


Fig. 3. Block diagram of the FC-based PH topology. The system consists of a PEMFC, second order low-pass filter, noninverting buck-boost converter 1, 2, and 3, ASD capacitor C_{ASD}, dc bus capacitor C_o and the load. The master control regulates all the system voltages and protects the components by providing the reference values for current controllers of the dc-dc converters in the system.

TABLE I
SUMMARY OF THE MAIN FC PARALLEL HYBRID SYSTEMS.

Presented in	ASD type	FC Converter type	ASD Converter type	FC SR limitation	Observations
[16]	Supercapacitors	Boost	Bidirectional buck-boost	✓	The boost converter has startup problems and there is not experimental load transients results.
[17]	Supercapacitors	Boost	Bidirectional buck-boost	×	The boost converter has startup problems and there is not experimental results.
[18]	Supercapacitors	Boost	Bidirectional buck-boost	×	The boost converter has startup problems and there is a complex control design.
[19]	Supercapacitors and/or Batteries	Buck-boost	Bidirectional buck-boost	×	There is not a description about the operational dead-zone that exists at the transition between buck and boost operating modes in the buck-boost converter connected to the FC. In additon, there is a complex control design.
[20]	Supercapacitors	Boost	Bidirectional buck-boost	×	The boost converter has startup problems and there is a complex control design.
In this work	Supercapacitors	Buck-boost	Buck-boost	✓	The use the same module for all the positions of the system simplifies the design and construction tasks.

bandwidths, and the maximum peak power are listed in Table I of [15]. As has been previously described, the presented PH topology utilizes the same components and provides the same features. Thus, a fair and realistic efficiency comparison with the other two topologies in references [10], [15] can be obtained. In order to match the values in [10], V_{FCmin}, V_{FCmax} and P_{omax} were set to 26.0 V, 42.0 V, and 1.2 kW, respectively. Such values correspond with the characteristics of the PEMFC used in the experimental testing phase.

The master control shown in Fig. 3 has the following aims:

- the FC's minimum voltage V_{FCmin} limitation and the ASD voltage reference V_{ASDref} regulation by means of i_{gref1}, as shown in Fig. 5 (a) and (b);
- the maximum ASD voltage V_{ASDmax} limitation by means of i_{oref2}, as shown in Fig. 5 (c);
- the dc bus voltage v_o regulation at 48 V by means of i_{gref2}, i_{oref3}, and i_{oref1}, as shown in Fig. 5 (d);
- the minimum ASD voltage V_{ASDmin} limitation by means of i_{gref3}, as shown in Fig. 5 (e);
- the maximum current limitation in each converter;
- ensuring a safe start-up and shutdown of the system.

This master control sends the current references to the analog current control loops of each converter with the aim of regulating the different voltages of the system. The master control parameters are listed in Table II of [15], [21]. For the purpose of this work, it was implemented within a Texas Instruments' TMS320F28335 digital signal controller (DSC). The dc-bus voltage v_o is controlled at 48 V by one of only two converters in the SH topology (converter 2 or 3 in Fig. 1(a)), and SPH topology (converter 1 or 3 in Fig. 1(c)). In case of PH topology this control is in charge of all the converters depicted in Fig. 1(b). Due to the interaction between these converters, the dc-bus voltage control is more complex in the PH topology than in the case of the other two topologies.

Particularly critical for stability of the system is the interaction between the anti-parallel converters 2 and 3 in Fig. 3. It should be noted that the anti-parallel connection is required because of the unidirectional power flow characteristics of the selected converter structure. Due to the nonlinearities and tolerances of the analog current controller's components in both converters, it is impossible to have a current of zero amperes in the non-active converter while the other is operating. Such reference winds up the average current-mode control's PI-controller of the converter that is not active and causes a delay in the instant of re-activation. In order to prevent this issue, a minimum current of $I_{min} = 1.8$ A has been

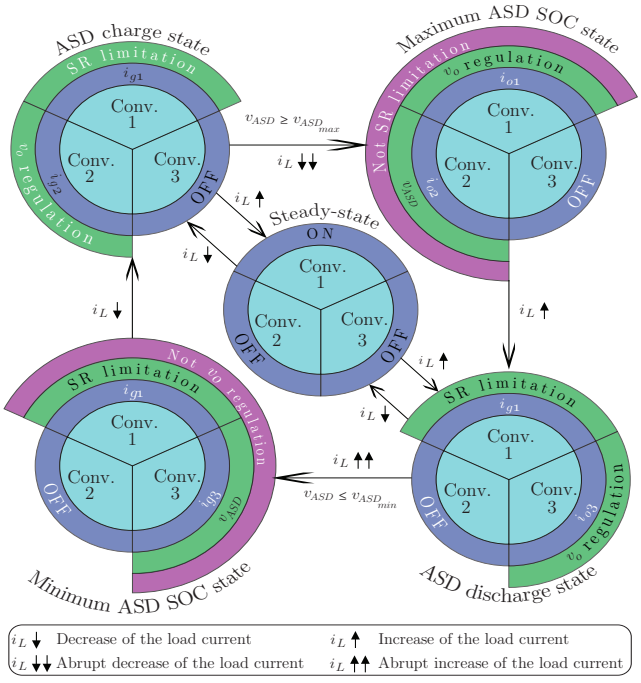


Fig. 4. Main states of the fuel Cell parallel hybrid topology.

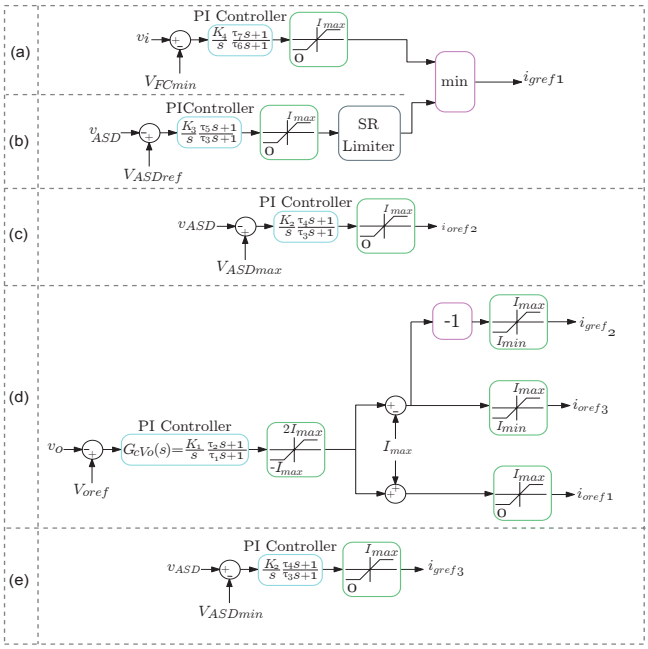
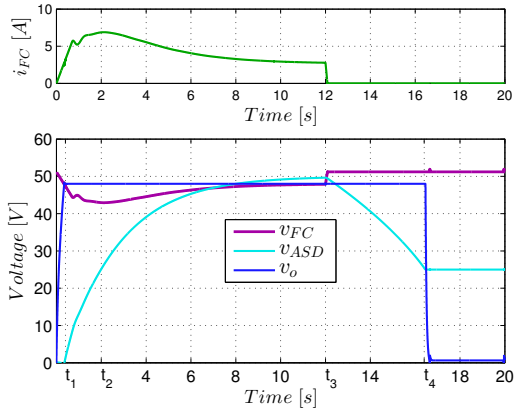


Fig. 5. Control and protection block diagrams for a PEMFC-based PH power system topology: (a) The FC minimum voltage V_{FCmin} is limited and regulated by means of i_{gref1}. (b) The ASD voltage reference V_{ASD} is limited and regulated by means of i_{gref1}. (c) ASD maximum voltage protection loop is limited by means of i_{oref2}. (d) Output voltage v_o is regulated by means of i_{gref2}, i_{oref3}, and i_{oref1}. (e) ASD minimum voltage protection loop is limited by means of i_{gref3}.

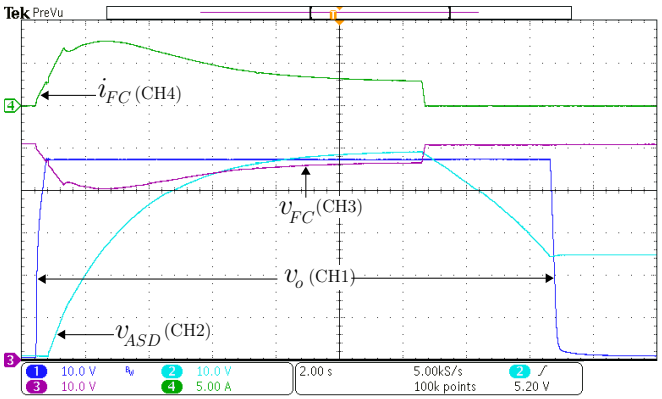
experimentally adjusted for the converters 2 and 3, which are responsible for the dc bus voltage v_o regulation (see Fig. 5 (d)). With this minimum current value the dc bus voltage v_o control stability is ensured at the expense of the whole system's efficiency.

III. Simulation and Experimental Results of the PH Topology

This section will focus on validation of the PH topology with the same experiments as presented in [10], [15]. For verifying a proper performance of the PH topology, several specific experiments are required. The latter were carried out on an FC emulator based on the Thévenin's equivalent circuit [22], which has been successfully validated in [15]. The simulation results of the FC system's start-up and shutdown are presented in Fig. 6(a).



(a)

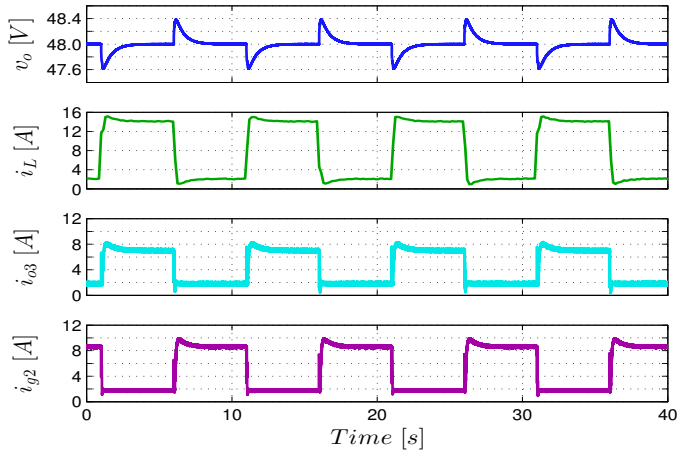


(b)

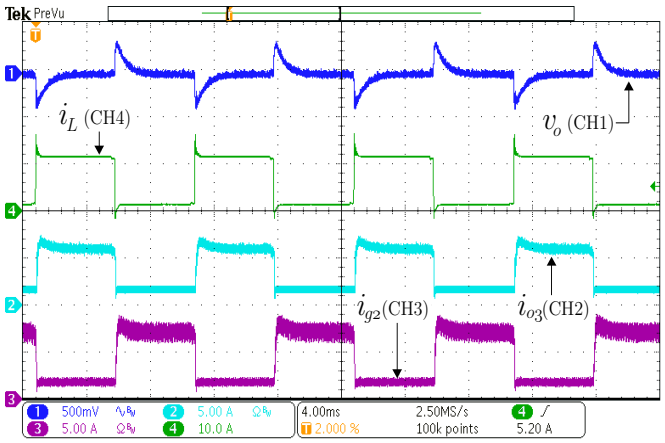
Fig. 6. FC-based PH system startup and shutdown with a constant resistive load of 20 Ω (a) PSIM simulation. (b) Experimental measurement. CH1: DC bus voltage v_o (10 V/div), CH2: ASD voltage v_{ASD} (10 V/div), CH3: FC voltage v_{FC} (10 V/div), CH4: FC current i_{FC} (5 A/div) and time base of 2 s.

The simplified noninverting buck-boost converter described in [15] and [10] has been used in this simulation. Initially, it can be observed in Fig. 6(a) how the capacitor is discharged to the time instant t_1, where the FC starts up and the capacitor begins to charge. The figure shows how the FC current i_{FC} has an appropriate slew-rate SR_{FCu} and the output voltage v_o is not regulated because the capacitor voltage has not reached its minimum value V_{ASDmin} of 25 V. Therefore, the active control loops within the interval $0 - t_1$ correspond to those illustrated in Figs. 5(b) and (e). At the instant t_2, the capacitor voltage reaches V_{ASDmin}. From this point on, v_o is regulated at $V_{oref} = 48$ V by means of the control loop shown in Fig. 5(d) and the FC current i_{FC} SR is maintained within the allowed range. Within the interval $t_2 - t_3$ the capacitor voltage continues to increase as governed by the control loop

in Fig. 5(b), until it reaches its reference value V_{ASDref} of 50 V. At the time instant t_3, the FC shuts down with a suitable current slew-rate SR_{FCd}. The output voltage v_o continues to be regulated until the capacitor voltage decreases to V_{ASDmin}, which occurs at t_4. Finally, the master control continues its minimum capacitor voltage regulation from t_4 onwards by means of the control loop presented in Fig. 5(e). The corresponding experimental result is shown in Fig. 6(b), which is in a good agreement with the simulation. Both figures, the experimental and the simulated, demonstrate a correct limitation of the FC current slew-rates SR_{FCu} and SR_{FCd}, along with the well regulated output and capacitor voltages.



(a)



(b)

Fig. 7. PH topology under a pulsating load power profile with a frequency of 100 Hz, 50% duty cycle, and $v_{FC} = 36.0$ V, $I_{FC} = 12.6$ A, $V_{ASD} = 50$ V, $V_o = 48$ V as mean values. Subfigure (a) presents the results obtained by PSIM simulation, while experimental results are shown in subfigure (b). CH1: dc-bus output voltage v_o (500 mV/div, AC coupling), CH2: input current i_{g2} (5 A/div), CH3: output current i_{o3} (5 A/div), CH4: load current i_L (10 A/div), and time base of 4 ms.

The second experiment was conducted with the load resistance varying from 24 Ω to 3.42 Ω with a frequency of 100 Hz and a duty cycle of 50%, as shown in Fig. 7. The capacitor voltage V_{ASD} is regulated at 50 V and the dc-bus output voltage v_o at 48 V. The buck-boost converter's switching model described in [10], [15] was used in the simulation. It is evident from Fig. 7(b) that the experimental results are in a good agreement with the simulation results. Initially, the system is in a steady-state and the energy is continuously transferred from the FC to the load. The dc-bus voltage v_o is regulated at V_{oref} indirectly through i_{oref1}, as depicted in Fig. 5 (d). When the load current i_L increases, the system goes into ASD discharging state, which means that the FC's maximum current SR and dc-bus voltage v_o are limited and regulated by means i_{gref1} and i_{oref3}, respectively. Therefore, the active control loops during this state correspond to those illustrated in Figs. 5(b) and (d). When i_L is decreasing, the system operates in the ASD charging state. In this state, the FC's minimum current SR and the dc-bus voltage v_o are limited and regulated by means of i_{gref1} and i_{gref2}, respectively. The same as in the ASD discharging state, the active control loops in the ASD charging state correspond with those illustrated in Figs. 5(b) and (d). Between the ASD charging and discharging states, the FC-based PH system operates in the steady-state as soon as dc-bus voltage v_o settles at 48 V. Fig. 7 shows that the dc bus voltage v_o was adequately regulated under large load current variations.

The third experiment tested the FC-based PH system's response to large periodic load variations that produced repetitive capacitor charging and discharging cycles. A step-like load variations between 24 Ω and 3.2 Ω with a frequency of 0.5 Hz and a duty cycle of 10% were applied for obtaining the simulation and experimental results, shown in Fig. 8. The same simplified buck-boost converter model as in previously described test was used in the simulation. All the subfigures in Fig. 8 represent the results of the same kind of test. However, due to a limited number of oscilloscope channels the results are split in two parts. In order to demonstrate that the waveforms correspond to the same experiment, the dc-bus output voltage v_o and fuel cell current i_{FC} are shown in all the subfigures. The maximum power drawn from the FC during the experiment was 512 W, which can be confirmed by multiplying V_{FCmin} and I_{max}, as described in [15], [21]. However, the large load variations required a peak power of 700 W, which resulted in charging and discharging the ASD. Fig. 8 shows that the bus voltage and the fuel cell current were well regulated and limited during this demanding experiment. The figure also demonstrates a good agreement between the experimental and simulation results.

IV. An Experimental Efficiency Comparison of Three Different PEMFC-Based Power Systems Topologies

In order to compare the efficiency of the different FC-based hybrid topologies, a generic load power cycle profile P_o, shown in Fig. 9, was used in this analysis. The load profile was composed of k cyclic periods of high and low power demand with a period T and a duty cycle D. The main goal of any hybrid system energy management (SH, PH, SPH or other) under such load profile is supplying a constant average power P_{oavg} from the FC, while the ASD covers the peak power demand. Therefore, the ASD is discharged when the load power demand is above the average load power P_{oavg} and recharged in the opposite case, as evident in Fig. 9.

The load profile proposed in this article is widely used in distributed generation systems for studying the system's

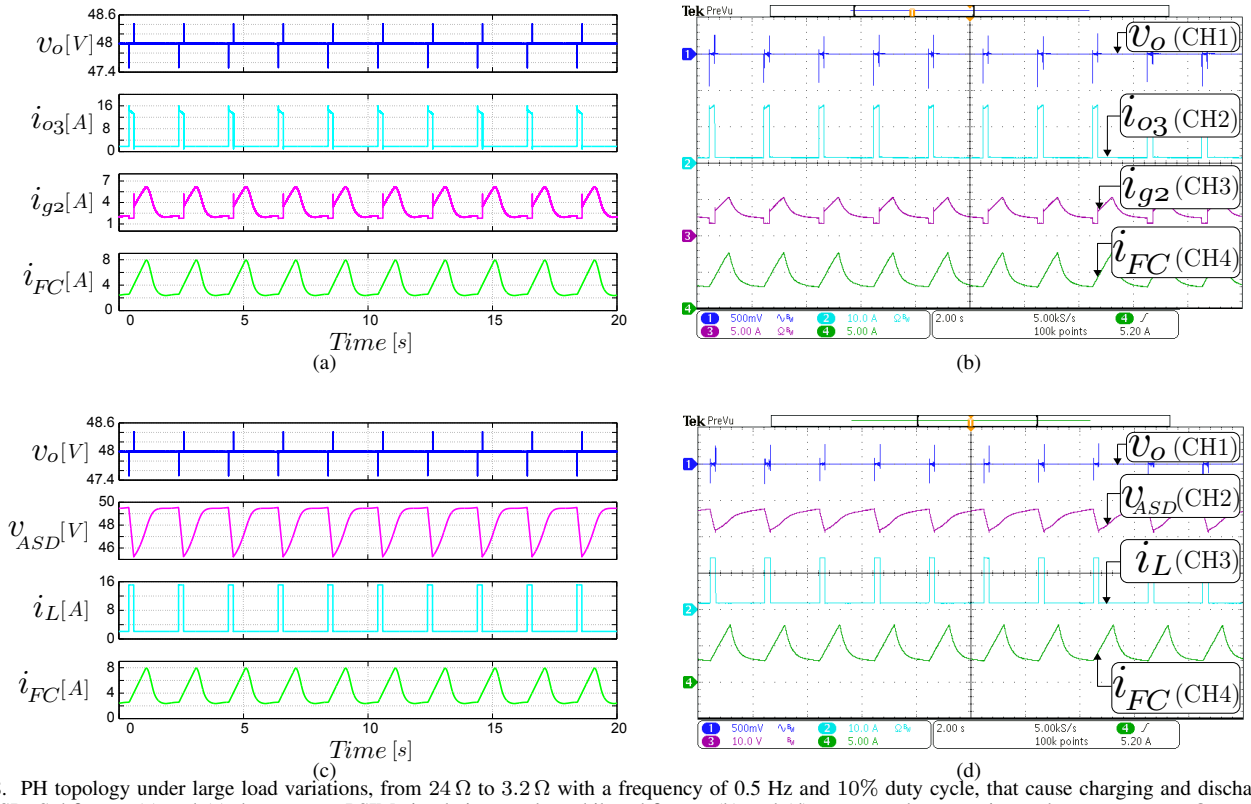


Fig. 8. PH topology under large load variations, from 24 Ω to 3.2 Ω with a frequency of 0.5 Hz and 10% duty cycle, that cause charging and discharging of the ASD. Subfigures (a) and (c) demonstrate PSIM simulation results, while subfigures (b) and (d) correspond to experimental measurements. Output voltage v_o (500 mV/div, AC coupling), load current i_L (10 A/div), input current i_{g2} (5 A/div), output current i_{o3} (10 A/div), fuel cell current i_{FC} (5 A/div), ASD voltage v_{ASD} (10 V/div) and the same time base of 2 s.

behavior under load transients in residential, industrial, and mobile applications [23]–[27]. By assuming a much higher load profile's dynamics than the FC's and a periodic steady-state operation of the hybrid system with a zero net change in the ASD's energy over one cycle, the average power values can be expressed as

$$\overline{P}_o = P_{oavg} = \frac{1}{T}\int_{t_{k-1}}^{t_k} P_o\, dt = P_{omax}\, D, \quad (1a)$$

$$\overline{P}_{FC} = \frac{1}{T}\int_{t_{k-1}}^{t_k} P_{FC}\, dt = P_{FCavg}, \quad (1b)$$

$$\overline{P}_{ASD} = \frac{1}{T}\int_{t_{k-1}}^{t_k} P_{ASD}\, dt = P^{+}_{ASD} D - P^{-}_{ASD}\,(1-D) = 0, \quad (1c)$$

where D is the steady-state duty cycle of the load profile.

On the basis of the load power profile shown in Fig. 9, it is possible to obtain a simple analytical expression for the efficiency of all the discussed FC-based hybrid topologies. The efficiency of the SH topology (η_S), the SPH topology (η_{SP}), and the PH topology (η_P) can be expressed in the same way, as the ratio of the average output power P_{oavg} to the average input power P_{FCavg} as follows:

$$\eta_S = \eta_P = \eta_{SP} = \frac{\overline{P}_o}{\overline{P}_{FC}} = \frac{P_{oavg}}{P_{FCavg}}. \quad (2)$$

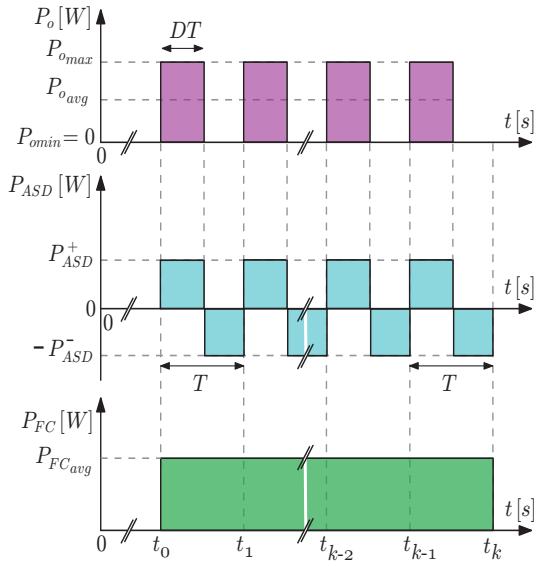


Fig. 9. Instantaneous power profiles of the load P_o, the ASD P_{ASD}, and the fuel cell P_{FC}, used for testing the efficiency of the three FC-based hybrid topologies studied in this article.

A numerical simulation of efficiency of the SH, PH and SPH topologies has been presented in [9]. These results may serve as a basis for the experimental efficiency analysis in this section. However, several differences between the numerical and experimental results are expected due to the following facts:

- The experimental converter's efficiency η varies depending on its operating point [11], [12].
- As explained in Section II, a minimum current I_{min} has been used in the dc-bus voltage v_o control loop for ensuring the stability of the system in case of PH topology. For this reason, the whole PH system's efficiency was reduced.
- In order to avoid instability and saturation in the dc-bus voltage v_o control loop a minimum load power value greater than zero ($P_{omin} > 0$, see Fig. 9) has been considered.
- The experimental converter's connectors and conduction paths as well as connections between different component in the realized system have non-ideal conductive properties. In addition, the practical ESRs of the dc-bus capacitor R_o and the ASD capacitor R_{ASD} are different from zero. A mismatch between the experimental and numerical results may arise due to neglecting all the parasitic resistances during theoretical analysis.

The following subsections provide an experimental efficiency comparison of the SH, PH, and SPH power system topologies as defined by (2). All the efficiency measurements were performed with the Voltech PM6000 Power Analyzer. It must be noted that the presented results include the power consumption of the drivers and control stages. In addition, the ASD voltage v_{ASD} has been controlled at 50 V in all the performed measurements.

A. A constant load profile

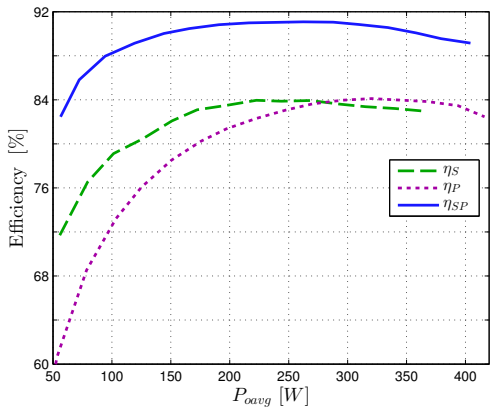


Fig. 10. Experimentally measured efficiencies for the SH, PH, and SPH topologies tested under a constant load profile ($D = 1$ or $P_o = P_{oavg}$).

The first experiment focuses on the efficiency of each power system topology under a constant load profile with a steady-state duty cycle $D = 1$ as shown Fig. 10. As it is evident from Fig. 10, the PH topology's experimental efficiency is lower with respect to the one of the SPH topology for 20.44%, 7.11%, and 6.04% for the average load powers of 50 W, 225 W, and 400 W, respectively. This results in an 11.20% average decrease of the constant load power efficiency of the PH topology in respect to the SPH topology. While the PH topology's theoretical efficiency is greater than the SH topology's efficiency at $D = 1$, this only holds true for the load powers greater than 280 W in the carried out experiments. The reason for that lies in the minimum current I_{min} that was used in the dc-bus voltage v_o control loop for ensuring the system's stability, as explained in Section II. However, the experimental tests under constant load conditions have confirmed superior performance of the SPH topology. The latter achieves higher efficiency than the other two studied topologies in both numerical and practice.

B. A load profile with a constant duty cycle

This subsection explains the experimental validation of the numerical efficiency (see Fig. 9 (d) of [9]) for duty-cycles within the range of $0 < D < 0.5$. A cyclic load profile with a duty cycle of $D = 0.3$ and a frequency of $f = 1/T = 100$ Hz was generated for obtaining the experimental results shown in Fig. 11. According to the numerical results, the SH topology's efficiency is approximately in the middle between the PH and SPH topologies at the load duty cycle of $D = 0.3$. However, the PH topology's experimental efficiency shown in Fig. 11 exhibits a drop of 1.50%, 2.66%, 3.06%, and 2.52% for the average load powers of 100 W, 150 W, 200 W, and 250 W, respectively. This results in an average efficiency decrease of 2.44% for the PH topology in respect to the numerical estimation. Again, this difference is mainly due to the inclusion of a minimum current I_{min} into the dc-bus voltage v_o control loop for ensuring the whole system's stability. Fig. 11 clearly demonstrates the relation $\eta_P < \eta_S < \eta_{SP}$ for the entire load power range. Such relation is in agreement with the numerical efficiencies for the load duty cycle range of $0 < D < 0.5$.

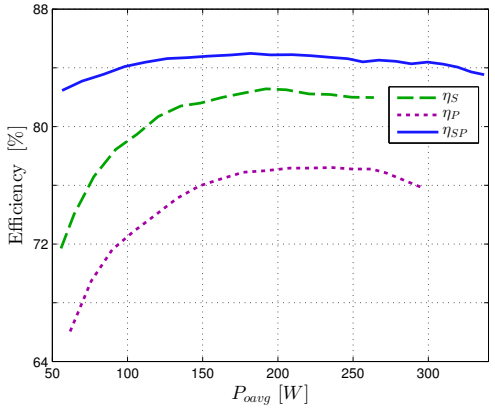


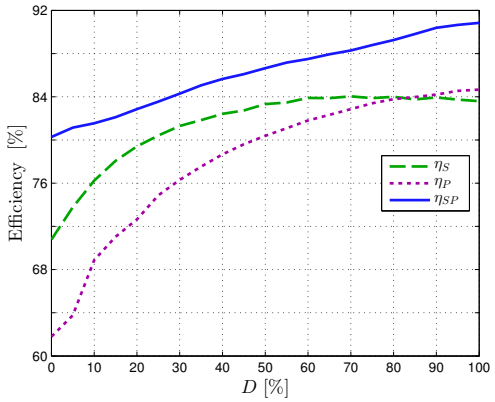
Fig. 11. Experimentally measured efficiencies for the SH, PH, and SPH topologies tested under a cyclic load variations with a duty-cycle of $D = 0.3$ and a frequency of $f = 100$ Hz.

The experimentally measured efficiencies in Figs. 10 and 11 exhibit lower than numerical estimated efficiencies at lower load powers. This is mainly due to the constant power consumption of the drivers and control stages, which have a stronger influence on the whole system's efficiency when operating under light load conditions.

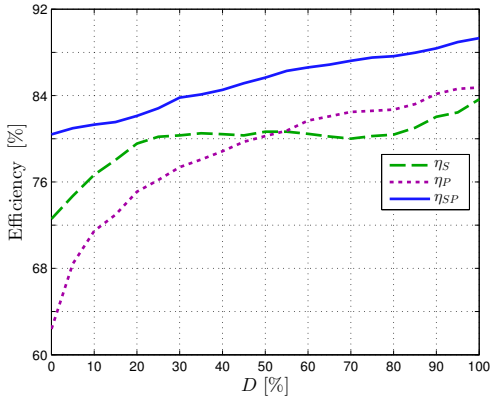
C. Load profiles that cause different voltage ripples in the ASD voltage v_{ASD}

This subsection extends the efficiency study to load profiles that cause different voltage variations in the ASD voltage v_{ASD}. Fig. 12 shows the experimentally measured efficiencies of the SH, PH, and SPH topologies as functions of the steady-state load duty cycle D for a constant load variation frequencies of 100 Hz and 0.5 Hz, respectively. The SPH topology achieves a higher efficiency than the SH and PH topologies within the entire the load duty cycle range and for both load variation frequencies, as shown in Fig. 12. In addition, $\eta_S > \eta_P$ for duty-cycles within the range of $0 < D < 80\%$ with a load variation frequency of 100 Hz and duty-cycles within the range of $0 < D < 50\%$ with a load variation frequency of 0.5 Hz.

It is important to note that the reference ASD voltage V_{ASDref} is equal to 50 V and the reference dc-bus output voltage V_{oref} equals 48 V for all performed experiments. Therefore, the ASD voltage v_{ASD} remains close to the dc-bus voltage v_o when the load variation frequency is 100 Hz, since the ASD cannot be discharged considerably in such short interval. As a consequence, the converter or converters between the ASD and the dc-bus in each topology operate close to the buck-boost mode which is the most efficient operating range of the utilized converters [11]. On the other hand, with a load variation frequency of 0.5 Hz, discharging and charging of the ASD causes different voltage variations which distance the converters between the ASD and the dc-bus from their most efficient operating range. This is clearly evident from the efficiency curves for the SH topology shown in Fig. 12, which has more converters connected between the ASD and the dc-bus than other two topologies. Additionally, if the ASD's voltage ripple increases, the losses also increase due to the ASD's ESR (R_{ASD}). It has been experimentally verified that the efficiency of each topology depends on the load variation frequency. Hence, there are slight differences between the numerical efficiency analysis presented in [9] and the experimental results illustrated in Fig. 12.



(a)



(b)

Fig. 12. Experimentally measured efficiencies for the SH, PH, and SPH topologies presented as a function of the steady-state load duty cycle D for a load variation frequency of: (a) f = 100 Hz, (b) f = 0.5 Hz. All the experiments were performed with load variations between $P_{omin} \approx 50$ W and $P_{omax} \approx 350$ W.

V. Conclusion

A PEMFC-based PH power system with an ASD and three current controlled dc-dc converters has been simulated and experimentally tested. The system's design criteria, components, and features are similar to the ones of the recently published SH and SPH power system topologies. The efficiency comparison between the three different hybrid power system topologies was obtained by testing them with a generic cyclic profile of the load power, which commonly appears in the distributed generation systems. The same versatile non-inverting buck-boost modules performed the tasks of dc-dc converters in the three investigated topologies. The voltages of these dc-dc converters were controlled indirectly by controlling the converters' input and output currents. The usage of the same converter modules reduces the costs and development time, as well as simplifies the control design. Another benefit is a fairer efficiency comparison between the studied topologies, since the losses in each power converter in all systems can be assumed as equal. Thus the effects of components are eliminated and an exclusively topology dependent power conversion efficiency comparison of the three studied hybrid topologies is achieved. In addition, the usage of the same power converter modules simplifies the mathematical analysis and derivation of the analytical efficiency functions. The simulation and experimental results have demonstrated that the proposed PH topology exhibits the same features and functionality as SH and SPH topologies. However, the efficiency analysis supported by experiments under pulsating load profiles showed a superior performance of the SPH topology in respect to the other two. For this reason SPH is the preferred option for applications with an unknown load profile. The experimental tests have also shown that the efficiency of the different topologies depends on the pulsating load profile parameters, such as the duty cycle, the switching frequency, and the maximum and minimum power levels. Although fully functional, the PH topology suffers from potential instability of the dc bus regulation due to the antiparallel connection of two converters in the system. In the scope of this work, this issue was solved at the expense of decreased total power conversion efficiency. However, a solution for the dc-bus instability issue that would preserve a close-to-theoretical efficiency of the PH topology remains a challenge for the future.

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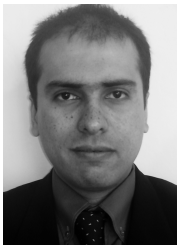

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