HM/PWM Seamless Control of a Bidirectional Buck-Boost Converter for a Photovoltaic Application

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***Abstract*— The versatile buck-boost dc/dc converter is found suitable for a particular photovoltaic application that requires either a voltage step-up or a voltage step-down operation injecting the maximum available current into an intermediate-voltage battery. It is proposed to implement the converter control stage providing seamless changes between the step-up (boost) and step-down (buck) operating modes. Based on the sliding-mode control technique, a hysteretic-modulation-based (HM) controller is designed allowing the tuning of the switching frequency around either of the two possible operating points. The introduction of minor modifications into the HM implementation results in a pulse-width modulation (PWM) controller that preserves the seamless changing features between buck and boost working modes while providing a fixed switching frequency. Experimental results demonstrate that both solutions allow the converter input voltage control by showing a perfect tracking of 1-kHz square-type references, similar to those provided by a classical perturb-and-observe (P&O) MPPT algorithm but much faster.**

***Index Terms*— Boost-Buck, Buck-Boost Converter, MPPT, Seamless Hysteretic Modulation, Sliding Mode Control, Photovoltaic Power System, PWM.**

I. Introduction

SWITCHING power converters are today presenting important technological advances fostered by their increasing use in areas as diverse as industrial equipment, computers, telecommunication devices, renewable electrical production, etc. Improving converter characteristics such as efficiency, cost, size and weight is therefore the focus of investigation in many research centers and universities that are also studying the converters' dynamic performance and promoting their use in new applications. In the field of clean power generation, switching converters have particular impact in wind and photovoltaic sectors because they allow an efficient processing of the generated power. The converters also decouple the characteristics of the generating systems from the loads by regulating the operational voltages and currents of the different systems, which are thus more easily protected in cases of perturbations, overvoltages, overcurrents, etc.

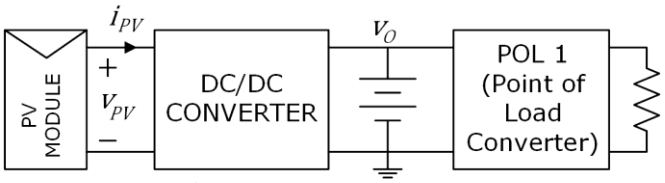

Fig. 1. Architecture of a photovoltaic system with a series type DC voltage bus.

Figure 1 shows a simplified diagram of an electrical architecture very often used in stand-alone photovoltaic systems [1]. It represents a series type DC voltage bus where the electric power produced in the photovoltaic modules is stored in a battery from which one or more point of load (PoL) converters supply the different loads of the system. In order to adapt the non-linear current-voltage (I-V) characteristic of the photovoltaic modules to that of the battery, a DC-DC switched step-up converter like those mentioned in [2], [3] are normally used. Some PV applications dealing with very low output converter voltages benefit from using step-down [4], [5] or step-up/down [6], [7] converter structures. The use of converters that provide step-up/down conversion ratios have been also reported in the literature [8], [9], [10], [11] in partially shaded PV systems like the one considered in this work.

In comparison with one-switch buck or boost topologies, well-known non-isolated step-up/step-down structures, such as the elementary buck-boost, Ćuk, or SEPIC converters, have high component stresses that result in lower overall efficiencies [12], [13]. According to reference [13], there are three two-switch topologies, unidirectional in current, that have less

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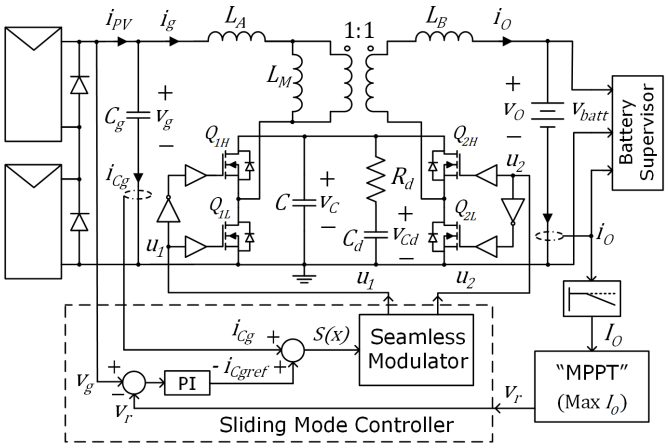

Fig. 2. Proposed photovoltaic system.

component stresses and are more efficient than the classical single-switch buck-boost unidirectional converter. To operate more efficiently, only one switch of these two-switch structures is switching at high frequency while the other is at a fixed ON or OFF state, depending on the topology. For the universal-input PFC applications considered in [13], a two-switch topology, denominated boost-interleaved buck-boost (BoIBB) converter, is compared with the two cascaded connection of buck and boost elementary stages, that are named buck-cascaded buck-boost (BuCBB) converter, and boost-cascaded buck-boost (BoCBB) converter. Because of component stress considerations, all three two-switch topologies will be also more efficient than the single-switch buck-boost topology in low-voltage PV applications such as the wide input voltage range considered here, even if the efficiency of all the topologies is improved by using synchronous rectification.

The complexity of the drivers required to substitute the diodes by MOSFETs and implement synchronous rectification will be smaller in BuCBB and BoCBB structures because of the availability of half-bridge bootstrap-based commercial drivers, such as the HIP4081A. Half-bridge drivers are not directly applicable to BoIBB because of a floating capacitor between one of the MOSFETs and its complementary diode. Adapting the BoIBB and BuCBB structures to our PV application would also require more additional filtering than the BoCBB due to the discontinuous nature of the input and output currents in the BuCBB and the output current of the BoIBB. These three main aspects, improved efficiency in comparison with one-switch converters, continuous input and output currents and availability of half-bridge commercial drivers suitable for the synchronous implementations, make a PWM-controlled coupled-inductor wide-bandwidth version of the BoCBB [14], [15], [16], [17] a suitable choice for the intended application.

Figure 2 illustrates the system here proposed, whose preliminary theoretical and simulation results were already presented in [8]. It consists of a noninverting bidirectional buck-boost structure [14] adapted in a series hybrid DC bus, which also includes a BP585 PV module and a 12.8-V lithium-ion battery. In the expected nominal operation mode, the converter steps down its input voltage because the maximum power point of the PV module is found at 18 V.

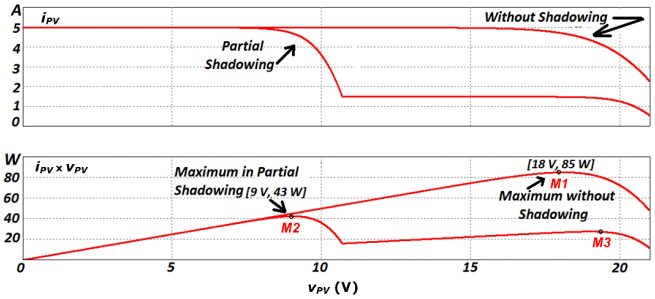

Fig. 3. Examples of I-V and P-V characteristics of the BP585 PV module. Without shadowing and a single maximum at nominal MPPT point M1 (18 V, 85 W). With partial shadowing and two maxima: M2 (9 V, 43 W) and M3 (19.5 V, 28 W).

The BP585 PV module consists of 36 solar cells in series, grouped into two sub-sets, each of them protected by an antiparallel bypass diode. In the case of shadowing or mismatch, the bypass diodes turn on in order to avoid the appearance of hot spots that can permanently damage the module. If one of the two bypass diodes is turned on, the power-voltage (P-V) curve of the module will present two maxima. Fig. 3 shows examples of I-V and P-V module curves in both a non-shadowing and a partial shadowing case. Nominal conditions of temperature and irradiation, i.e. 25 ℃ and 1 kW/m^2, are assumed in the non-shadowed cells. In the partial-shadowing case, the irradiation of 300 W/m^2 considered for one of the sub-modules causes the activation of its bypass diode. While the non-shadowing P-V curve exhibits a unique maximum M1 (85 W @ 18 V), the partial shadowing curve has two maxima: M2 (43 W @ 9 V) and M3 (28 W @ 19.5 V). In the partial-shadowing example, the power generated if the system operates around the maximum of minor voltage M2 is higher than that obtained at M3. If maximum power is to be generated even in partial-shadowing conditions, the system must be able to operate at M1 as well as at M2. Therefore, since the battery voltage lies in an intermediate range between the maximum power point voltages of 9 V and 18 V, the converter has to be able to step up voltage if required. Designing the control so that the system is able to evolve as seamlessly [18] as possible from the vicinity of 9 V to around 18 V and vice versa is also an important requirement for the proposed system. As it is shown later, this behavior is achieved by the combination of a single control law and the seamless modulator indicated in Fig. 2.

On the other hand, switched converters are non-linear variable-structure systems that can be modelled by a set of first-order differential equations, some of whose right-hand sides are discontinuous because they depend on control inputs that can only take two discrete values (usually {0, 1}). A natural way to control switching converters is the sliding-mode control technique [19], which is employed here in the current and voltage control loops of the versatile buck-boost converter (Fig. 2). The dynamics of a system controlled in sliding mode is attracted toward a surface in the state-space known as the sliding surface. When certain conditions are satisfied, the closed-loop system's dynamics become constrained around this

surface, insensitive to variations in plant parameters and the occurrence of external perturbations.

It has to be pointed out that sliding-mode control theory assumes an infinite switching frequency in the theoretical approach of the problem but its practical implementation is performed by a hysteresis comparator yielding a finite switching frequency that can be efficiently handled by the converter power devices. The resulting switching regulator is fast and robust but exhibits a variable switching frequency that can complicate the design of additional filters and limit certain ways of converter interconnection such as interleaving or other forms of synchronization [20]. Hysteresis implementation of converter control yielding constant switching frequency is a well-known problem that can be solved by the inclusion of an additional PI control loop that regulates the switching period by acting on the comparator hysteresis width [21], [22]. Another solution of the problem is the sliding mode- based pulse width modulation (PWM) approach which can be implemented analogically [20], [23] or digitally [24] by equating the equivalent control to the duty cycle.

In the system depicted in Fig. 2, the outer conventional MPPT loop has been replaced by one that maximizes the current delivered to the battery [25]. It has been assumed that a battery supervision system uses a low bandwidth current sensor for implementing protections, which together with voltage measurements could be used to determine the battery's state of charge (SoC) and state of health (SoH) by means of hardware in the loop (HIL) impedance spectroscopy techniques. As mentioned in [26], sensing the capacitor current using a low side resistive approach is preferable to measuring the input inductor current with a high side resistive configuration whose DC component and conduction losses are much higher.

It is shown in this paper that the implementation of the control circuit presents a significant improvement with respect to the solution in [8] that allows independent adjustments of the switching frequency for each of the two modes of operation: step-down (18 V) and step-up (9 V). This improvement takes into account the fact that the PV module considered has only two maximum power points. In the case of PV modules with more bypass diodes, having similar switching frequencies at many more different operation points would rely on more sophisticated HM implementation techniques, such as those that dynamically adjust hysteresis width. Instead, it is proposed in this paper the use of PWM as a complementary alternative.

The present article is divided into 5 sections. This first introductory section is followed by a section of theoretical analysis in which the converter's characteristics, its two operation modes and the corresponding simplified converter models are explained. The stability analysis of the system in closed loop at the end of Section II is the entry point of Section III, in which an implementation example of the converter power stage and the two previously mentioned control implementation proposals are detailed. Section IV shows the results obtained in the laboratory, and finally Section V provides the final conclusions and some proposals for future work.

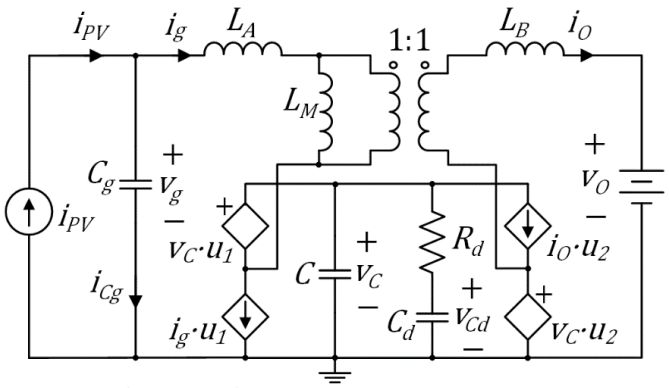

Fig. 4. Simplified model of the system (PV module-converter-battery) where MOSFETs have been substituted by equivalent controlled sources [28].

II. Theoretical Analysis

The versatile buck-boost converter presents a wide set of interesting characteristics such as high efficiency, easy regulation with a large bandwidth of input and output currents and voltages, and simple implementation of protections, all of which complement its step-up/step-down voltage transfer ratio that makes it suitable for our application [14], [15], [16]. In order to have high efficiency, only one of the converter half-bridges switches at high frequency while the other remains in a fixed conduction state. Depending on the input-to-output voltage ratio, the versatile buck-boost converter operates like a buck converter with an inherent input filter or a boost converter with an also inherent output filter [27]. In buck mode, the input filter is composed of input inductor L_A, intermediate capacitor C, and damping network R_dC_d. In boost mode, the output filter contains again the intermediate capacitor with its associated damping network, and output inductor L_B.

As mentioned in [14], the combination of the magnetic coupling between the two converter inductors and the series R_dC_d damping network avoids the usual resonances exhibited by high-order converter structures and also provides minimum-phase dynamics even in boost mode. This facilitates the design of the wide bandwidth control loops that may be necessary in applications involving fast irradiation variations, such as those caused by shadows of buildings, vegetation or other elements in PV modules installed in vehicles. In our case, even if there were no fast irradiation changes, the use of a P&O MPPT algorithm would require the tracking of reference voltages with fast step-type changes driving the system from around 9 V to the vicinity of 18 V and vice versa. The faster these changes can be tracked, the faster the sweeping between the two P-V local maxima takes place, which results in significantly improved transient efficiencies [11].

A. Converter Modeling.

The main drawback of the converter is its complex high-order structure, which in general makes it difficult to analyze. Nevertheless, if we model the photovoltaic module in a simplified form as a current source and assume that the transitions between step-up and step-down modes are slow, it is possible to analyze the system's input voltage control using the

sliding mode control technique for each of the two operating modes without considering the effect of the outer MPPT loop. Figure 4 shows a simplified model of the system, in which voltage- and current-controlled sources represent the bidirectional converter switches in order to make the analysis independent of their exact activation and deactivation sequences [28]. The converter scheme depicts the way in which the coupled inductors have been implemented in the experimental prototype: two non-coupled inductors (L_A, L_B) and a 1:1 tightly coupled inductors of magnetizing inductance L_M. Unlike the most general analysis in [8], all the theoretical expressions in this section take into account that the coupled inductors implementation implies that $L_M = M > 0$, $L_1 = L_A + M > 0$, $L_2 = L_B + M > 0$, and $L_M(L_A + L_B) > 0$. Note that L_1 and L_2 are the self-inductances of port 1 and 2 of the coupled inductors, and M is the mutual inductance.

The system in Fig. 4 could be described using six differential equations in the form of $\frac{dx}{dt} = f(x, u_1, u_2, w)$ [14], with $x = \left[i_g, i_o, v_C, v_{Cd}, v_g, int\_err\right]^T$ and $w = \left[i_{pv}, v_o, v_r\right]^T$ being the transposed state and input vectors respectively.

$$
\begin{aligned}
f_1(x) &= \frac{di_g}{dt} = \frac{(L_B + L_M)\left[v_g - v_c(1-u_1)\right] - L_M[v_o - v_c u_2]}{L_A L_B + L_M(L_A + L_B)} \\
f_2(x) &= \frac{di_o}{dt} = \frac{L_M\left[v_g - v_c(1-u_1)\right] - (L_A + L_M)[v_o - v_c u_2]}{L_A L_B + L_M(L_A + L_B)} \\
f_3(x) &= \frac{dv_C}{dt} = \frac{i_g(1-u_1) - i_o u_2}{C} - \frac{v_C - v_{Cd}}{R_d C} \\
f_4(x) &= \frac{dv_{Cd}}{dt} = \frac{v_C - v_{Cd}}{R_d C_d} \\
f_5(x) &= \frac{dv_g}{dt} = \frac{i_{Cg}}{C_g} = \frac{i_{pv} - i_g}{C_g} \\
f_6(x) &= \frac{dint\_err}{dt} = v_g - v_r
\end{aligned} \tag{1}
$$

The fifth equation corresponds to the dynamics of C_g, a capacitor connected in parallel at the converter input in order to adapt its structure to a current source-like input generator. Assuming that the control objective is to regulate input capacitor voltage v_g so that it will track external reference voltage v_r without steady-state error, an additional sixth equation corresponding to the time derivative of *int_err* has also been introduced. This *int_err* variable is the voltage error integral term that appears in the proposed switching surface (see the PI block in Fig. 2):

$$
\begin{aligned}
S(x) &= i_{pv} - i_g + G \cdot \left(v_g - v_r\right) + k \cdot int_{err} = \\
&= C_g \frac{dv_g}{dt} + G \cdot \left(v_g - v_r\right) + k \cdot int\_err = 0
\end{aligned} \tag{2}
$$

The reference-to-input voltage transfer function corresponding to (2) is

$$
H(s) = \frac{V_g(s)}{V_r(s)} = \frac{Gs + k}{C_g s^2 + Gs + k}, \tag{3}
$$

the two poles of which will be placed in the left half-plane if $G > 0$, $C_g > 0$, and $k > 0$.

B. Buck Mode Analysis: $u_1 = 0,\ f(x, 0, u_2) = f_{buck}(x, u_2)$

The equivalent control in buck mode (5) corresponding to the switching surface (1) is obtained from

$$
\begin{aligned}
&\frac{dS(x)}{dt} = \frac{di_{pv}}{dt} - f_{buck1}(x, u_2) \\
&+ G\left(f_{buck5}(x, u_2) - \frac{dv_r}{dt}\right) = 0
\end{aligned} \tag{4}
$$

$$
\begin{aligned}
u_{2eq} = \frac{v_o}{v_c} + \frac{L_B + L_M}{L_M}\left(1 - \frac{v_g}{v_c}\right) + \frac{L_A L_B + L_M(L_A + L_B)}{L_M v_c}\left[\frac{G}{C_g}\left(i_{pv} - i_g\right) + \right. \\
\left. k(v_g - v_r) + \frac{di_{pv}}{dt} - G\frac{dv_r}{dt}\right]
\end{aligned} \tag{5}
$$

In sliding regime, the equivalent control should fulfill

$$
0 < u_{2eq} < 1. \tag{6}
$$

In the absence of magnetic coupling ($L_M = 0$), the equivalent control in buck mode u_{2eq} tends toward infinity, which in practice is the equivalent of a saturated control ($u_{2eq} \geq 1$). Having positive magnetic coupling guarantees that the system relative degree is 1 because control variable u_2 appears explicitly in the derivate of the surface (7) when $L_M > 0$. Note again that positive magnetic coupling has been assumed in the coupled inductors implementation depicted in Figs. 2 and 4.

$$
\frac{\partial}{\partial u_2}\left(\frac{dS(x)}{dt}\right) = \frac{-L_M v_c}{L_A L_B + L_M(L_A + L_B)} < 0 \tag{7}
$$

Another important control-related design consideration results from the expression of the equivalent control (5). Since it contains the term $-G\frac{dv_r}{dt}$, we conclude that limiting the derivative of the reference voltage is required in order to fulfill (6). If a non-filtered step-type reference typical in many MPPT algorithms is applied, the control will saturate and the sliding regime be lost. This does not always mean that the system is performing incorrectly, but, as it is shown later, it is preferred to avoid this problem by inserting a low-pass pre-filter at the sliding controller reference input.

The equilibrium point of the ideal system in closed loop $X = \left[I_{pv}, \frac{V_r I_{pv}}{V_o}, V_r, V_r, V_r, 0\right]^T$ is as expected in a buck converter with input filter being the static values of the input vector $W = \left[I_{pv}, V_o, V_r\right]^T$. The ideal sliding dynamics in closed loop around the previous working point are obtained by substituting the equivalent control u_{2eq} in $f_{buck}(x, u_2)$ and imposing that $S(x)$ must be equal to zero. We have omitted the resulting non-linear expression because of its length. It is worth noting that the expression of the equivalent control in equilibrium point $U_{2eq} = \frac{V_o}{V_r}$ is coincident with the voltage conversion ratio of a buck converter in open loop switching at constant duty cycle D.

By linearizing the ideal sliding dynamics around the equilibrium point, the following fifth order expression of the characteristic polynomial is obtained:

$$\left(s^2+\frac{G}{C_g}s+\frac{k}{C_g}\right)(s^3+a_2s^2+a_1s+a_0) \quad (8)$$

$$a_2=\frac{1}{R_d}\left(\frac{1}{C_d}+\frac{1}{C}\right)+\frac{I_{pv}}{V_OC}\left(1-\frac{V_O}{V_r}+\frac{L_B}{L_M}\right)$$

$$a_1=\frac{V_O}{V_rL_MC}+\frac{I_{pv}}{R_dC_dV_OC}\left(1-\frac{V_O}{V_r}+\frac{L_B}{L_M}\right)$$

$$a_0=\frac{V_O}{R_dC_dV_rL_MC}$$

$$a_2\,a_1-a_0=\frac{V_O}{V_rR_dC^2L_M}+\frac{1}{R_dC_d}\left(\frac{I_{pv}}{V_OC}\left(1-\frac{V_O}{V_r}+\frac{L_B}{L_M}\right)\right)^2.$$

Two of the poles of the characteristic polynomial are imposed by the sliding dynamics (3), which simplifies the stability analysis through Routh's criterion. Given that $\infty > \frac{L_B}{L_M} > 0$, $a_0 > 0$, and $a_2\,a_1 - a_0 > 0$, the system will be stable in buck mode since $\left(1-\frac{V_O}{V_r}\right) \geq 0$ and therefore $a_2 > 0$, $a_1 > 0$.

C. *Boost Mode Analysis:* $u_2 = 1$, $f(x,u_1,1) = f_{boost}(x,u_1)$

In boost mode the input voltage derivative term in the switching surface provided by the input capacitor current ensures that there is transversality (11) even in the absence of magnetic coupling

$$\frac{dS(x)}{dt}=\frac{di_{pv}}{dt}-f_{boost1}(x,u_1)+G\left(f_{boost5}(x,u_1)-\frac{dv_r}{dt}\right)=0 \quad (9)$$

$$u_{1eq}=1-\frac{v_g}{v_c}+\frac{L_M}{(L_B+L_M)}\left(\frac{v_o}{v_c}-1\right)+\frac{L_AL_B+L_M(L_A+L_B)}{(L_B+L_M)v_c}\left[\frac{G}{C_g}(i_{pv}-i_g)+\frac{di_{pv}}{dt}-G\frac{dv_r}{dt}\right] \quad (10)$$

$$\frac{\partial}{\partial u_1}\left(\frac{dS(x)}{dt}\right)=\frac{-(L_B+L_M)v_c}{L_AL_B+L_M(L_A+L_B)}<0 \quad (11)$$

In this case, even with $L_M = 0$, only the reference derivative in (10) could endanger the constraint

$$0 < u_{1eq} < 1 \quad (12)$$

As in buck mode, it is necessary to impose that $S(x) = 0$, $f_{boost}(x,u_{1eq}) = 0$ and $\frac{dw}{dt} = 0$ ($W = [I_{pv}, V_o, V_r]^T$) in order to obtain the ideal sliding dynamics around closed loop equilibrium point $X = \left[I_{pv}, \frac{V_rI_{pv}}{V_o}, V_o, V_o, V_r, 0\right]^T$. The equivalent control at equilibrium point $U_{1eq} = 1 - \frac{V_r}{V_O}$ is also the one expected for a boost converter.

Now, the characteristic polynomial is:

$$\left(s^2+\frac{G}{C_g}s+\frac{k}{C_g}\right)(s^3+b_2s^2+b_1s+b_0) \quad (13)$$

$$b_2=\frac{1}{R_d}\left(\frac{1}{C_d}+\frac{1}{C}\right)+\frac{I_{pv}}{V_OC}\left(\frac{V_r}{V_O}-\frac{L_M}{L_B+L_M}\right)$$

$$b_1=\frac{1}{(L_B+L_M)C}+\frac{I_{pv}}{V_OR_dC_dC}\left(\frac{V_r}{V_O}-\frac{L_M}{L_B+L_M}\right)$$

$$b_0=\frac{1}{R_dC_dC(L_B+L_M)}$$

$$b_2b_1-b_0=\frac{1}{R_dC^2(L_B+L_M)}+\frac{1}{R_dC_d}\left(\frac{I_{pv}}{V_OC}\left(\frac{V_r}{V_O}-\frac{L_M}{L_B+L_M}\right)\right)^2.$$

Given that in boost mode $\left(1-\frac{V_r}{V_O}\right) \geq 0$ the fulfilment of stability conditions $b_2 > 0$ and $b_1 > 0$ is not always guaranteed, both conditions should be checked numerically when selecting the converter parameters.

III. System Implementation

The selection of the converter and controller parameters is carried out by studying several root locus of internal dynamics' characteristic polynomials. Since neither the controller parameters G and k nor capacitance C_g appear at polynomials $s^3+a_2s^2+a_1s+a_0$ and $s^3+b_2s^2+b_1s+b_0$ corresponding to the internal system dynamics, the first goal is to determine a reasonable set of values for L_A, L_B, L_M, C, C_d and R_d that guarantee sufficiently damped complex poles ($\xi > 0.5$) for voltages and currents in the ranges of the selected battery and PV module. For a given battery voltage V_O a root locus plot is generated by seeping current I_{pv} in 200 mA steps in the $(0\,\text{A}, 8\,\text{A})$ range and considering twenty uniformly distributed points for the input voltage V_r in both buck and boost regions. In the buck case, the twenty different voltage coordinates are in the $(0, V_O)$ range, while in the boost case the voltage goes from V_O to a maximum voltage of 24 V. This maximum voltage is slightly above the 22-V at 25 ºC nominal open circuit voltage of the considered PV module, thus taking into account cold weather operation. To determine the worst case scenario, a multidimensional set of the previous root locus plots has to be generated. One of the dimensions is the battery voltage for which three discrete V_O values $\{10\text{ V}, 12.8\text{ V}, 15\text{ V}\}$, two extremes and the nominal value, have been considered. The other dimensions concern the converter parameters C_d, R_d, L_A, L_B, L_M and C. To avoid generating too many plots, the normalizations and values reported in [14] have been taken into account. Accordingly, the damped network parameters are expressed as $C_d = C_{dn} \cdot C$ and $R_d = R_{dn} \cdot Z_n$, where Z_n is the characteristic impedance $Z_n = \sqrt{\frac{L_M}{C}}$, $C_{dn} \geq 8$ and $R_{dn} \approx 0.65$. Two characteristic impedances have been tested, $Z_n = 2.3$ as in [14], and $Z_n = 1.5$ that implies $R_d \approx 1\,\Omega$. Also, the plots have been normalized with respect to the natural frequency $\omega_n = \sqrt{\frac{1}{L_MC}}$. Further reduction in the parameter space is achieved by choosing a symmetric design of the coupled inductors in which $L_A = L_B = L$ [29] and the resulting magnetic coupling coefficient is $k = \frac{L_M}{L+L_M}$. Two magnetic coupling coefficients $k \approx 0.8$ [29] and $k = 0.5$ [15] have been considered. Selecting $k = 0.5$ and $Z_n = 1.5$ fulfills the damping requirements and yield equal inductances, $L = L_M$, and $R_d \approx 1\,\Omega$, which are interesting choices from the point of view of simplifying the implementation. Instead of a minimum value of $C_{dn} = 8$, a value of $C_{dn} = 10$ closer to the selection in [15] has been chosen. Considering that, according to table I, C_{dn} is an

electrolytic capacitor with a 20% tolerance and C is ceramic with a nonlinear X7R dielectric, increasing the C_{dn} capacitance over the minimum value in a 25% is sensible from the point of view of taking into account the practical deviations from the nominal values. Placing the natural frequency at one tenth of the nominal switching frequency $\omega_n = \frac{2\pi}{10} f_S$ results in reasonable ripples in the inductor currents and the intermediate capacitor voltage. In addition, it has been determined that an input voltage ripple $\Delta v_g = \frac{V_r(V_O - V_r)}{12 V_O C_g L f_S^2} < 30$ mV $(< 0.5\%)$ at the nominal boost operating point requires an input capacitor C_g larger than 39.5 µF.

Finally, the converter parameters are selected as $L_M = L_A = L_B = 22$ µH, $C_g = 44$ µF, $C = 10$ µF, $C_d = 100$ µF and $R_d = 1\ \Omega$. The desired switching frequency at the nominal operating points, $V_o = 12.8$ V, buck mode: $V_g = 18$ V, boost mode: $V_g = 9$ V, is 100 kHz. Steady-state ripples of inductor L_A current at the nominal operating points are about 820 mA in boost mode and 530 mA in buck mode. The corresponding ripples of inductor L_B currents are 410 mA and 1060 mA, while the respective intermediate capacitor voltage ripples are 1 V and 1.3 V. The steady-state power losses at R_d at the two nominal operating points are less than 200 mW, about 0.25% of the nominal PV module power of 85 W. Experimental data on the converter efficiency is provided in Fig. 18, at the end of Section IV.

The selection of the remaining control surface parameters in (2), G and k, has been carried out after considering that the small signal block diagram of the system is the one represented in Fig. 5, in which the closed loop converter plant is approximated by the input capacitor impedance [26]. In essence, the sliding surface equation in (14) implies that the reference i_{Cgref} for the controlled variable, which is capacitor current i_{Cg}, is provided by a PI regulator of the capacitor voltage (see Fig. 5).

$$S(x) = 0 \rightarrow i_{Cg} = i_{Cgref} = C_g \frac{dv_g}{dt} = G \cdot (v_g - v_r) + k \cdot int_{err} \qquad (14)$$

According to Fig. 5 and (14), the voltage closed loop gain is

$$T(s) = \left(G + \frac{k}{s}\right) \cdot \frac{1}{C_g s} \qquad (15)$$

The main criteria to select the control parameters is to obtain a wide bandwidth closed loop so that the converter input voltage, which is the PV module voltage, can track the references provided by a demanding MPPT algorithm and reject high frequency perturbations in i_{PV} and v_o. In the particular application of this paper it is very advantageous to have a PV system able to fast-sweep between the 9-V and 18-V nominal operating points (see Fig. 17) because faster tracking of the MPP operating points results in smaller power loss during transients [11]. It is worth noting that high frequency perturbations in v_o can be caused by the interaction of pulsating

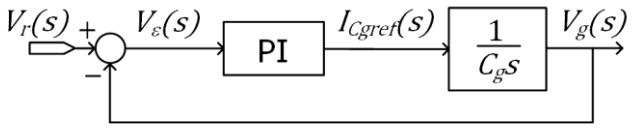

Fig. 5. Ideal block diagram of the system voltage loop in the Laplace domain.

loads and the battery impedance (omitted in the modelling for the sake of simplicity). To achieve the wide bandwidth goal, the loop gain crossover frequency has been placed at about one fifth of the nominal switching frequency, $\omega_{0dB} = \frac{G}{C_g} = \frac{\omega_s}{5}$. In addition, to obtain a phase margin close to 90º, the PI zero corner frequency $\omega_z = \frac{k}{G}$ has to be at least one decade left of the crossover frequency. Therefore, $G = C_g \frac{\omega_s}{5} = C_g \frac{2\pi}{5T_s} \approx 5.53$ and $\frac{k}{G} < \frac{\omega_s}{50} = \frac{2\pi}{50T_s} \approx 12600$. The PI implementation in Fig. 6 includes a 1/10 voltage divider factor and takes into account that the i_{Cg} sensing path has a 500 mV/A gain. The denormalized PI block transfer function is

$$\frac{-I_{gref}(s)}{V_g(s)} = G + \frac{k}{s} = 2\frac{R_G}{90\ \text{k}\Omega}\left(1 + \frac{1}{R_G \cdot C_k s}\right) \qquad (16)$$

which requires a resistor R_G of 249 kΩ to provide a high frequency gain of $\frac{R_G}{45\ \text{k}\Omega} = 5.53$. The closest normalized (E12) resistor value is 270 kΩ, which corresponds to a proportional gain of 6. Capacitor C_k in series with $R_G = 270$ kΩ in the PI block has to be $C_k > \frac{1}{12600 \cdot R_G} \approx 300$ pF. The final value selected for capacitor C_k is 1 nF, approximately 3.5 times larger than the minimum required value, which improves the phase margin from $atan(10) \approx 84°$ to $atan(35) \approx 88°$.

The final surface parameters are $G = 6\ \frac{\text{A}}{\text{V}}$, $k = 22000\ \frac{\text{A}}{\text{Vs}}$, which according to (3) correspond to the transfer function

$$H(s) \approx 136400 \frac{s+3670}{(s+3770)(s+132600)} \approx \frac{132600}{s+132600}. \qquad (17)$$

At the buck mode nominal operation point, the other poles in (8) are the roots of $(s^3 + a_2 s^2 + a_1 s + a_0) \approx (s + 86300) \cdot ((s + 17200)^2 + 8900^2)$. The damping factor of the complex poles is $\xi \approx 0.89$, with $\omega_0 \approx 19.4$ krad/s. At the nominal operating point in boost mode, the poles not directly placed by the control coefficients are the roots of the polynomial $(s^3 + b_2 s^2 + b_1 s + b_0) \approx (s + 14000) \cdot ((s + 42500)^2 + 37900^2)$, with $\omega_0 \approx 56.9$ krad/s and $\xi \approx 0.75$ for the complex poles.

Since it is out of scope of this work to design the MPTT algorithm, the amplitudes $\pm\Delta v_r^*$ of the step-like reference changes have been arbitrarily fixed to ±1 V, so that there are 9 voltage steps between M1 and M2, to illustrate the experimental reference-tracking performance of the proposed control. As it has been previously mentioned, it is sensible to place a prefiltrer to limit the term $-G\frac{dv_r}{dt}$ in the equivalent control expressions (5) and (10). Some useful considerations on the design of the reference prefilter have been provided in [26] but, since the

TABLE I
CIRCUIT COMPONENTS

ELEMENT	DESCRIPTION	TYPE
Q1, Q2, Q3, Q4	Power MOSFETs	IRFP4110PbF Case TO-247AC
LA, LB	Power Inductors	COILCRAFT VER2923-223K, 22 µH, 26 A, 12.2 MHz
LM	Custom-made 1:1 Tightly-Coupled Inductors	MAGNETICS Core 77076-A7, 2 windings 22 Turns, Multifilar AWG 15
C	X7R Ceramic Capacitor (x3 in parallel)[a]	MURATA GRM31CR71H475KA12L 4.7 µF, 50 V
Rd	Damping Resistor (x4)	VISHAY DALE CRCW25121R00FKEG In H configuration with Cd
Cd	Electrolytic Capacitor (x4)	Panasonic EEUFR1V101 35 V, 100 µF
Cg	MKT Polyester Capacitor (x2 in parallel)	KEMET R60DR52205040J 22 µF, 63 V

[a] Because on the nonlinear dielectric, at 18 V the capacitance is about 10 µF..

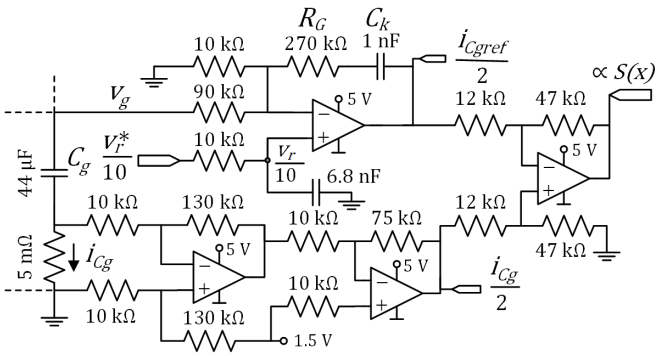

Fig. 6. Detail of the circuital implementation at OpAmp level of the current and voltage controllers in Fig. 2.

experimental results obtained using a simple first order RC implementation were satisfactory, no further investigation has been made to improve the prefilter. As a basic guideline to select the prefilter time-constant τ it has to be taken into account that the maximum slope absolute value is $\left|\frac{dv_r}{dt}\right|_{max} = \frac{\Delta v_r^*}{\tau}$. From (5), the steady-state equivalent control at the buck nominal operation point is $U_{2eq} = \frac{12.8}{18} \approx 0.71$. To guarantee that $u_{2eq} < 1$, the contribution in (5) of a negative step reference transient should not exceed $(1 - 0.71) \approx \frac{1}{4}$. Thus, a necessary condition is $\tau > 44$ µs.

$$-G\frac{dv_r}{dt}\cdot\frac{L_A L_B + L_M(L_A+L_B)}{(L_B+L_M)v_c} = G\frac{\Delta v_r^*}{\tau}\frac{3L}{2V_r} < \frac{1}{4} \qquad (18)$$

Following a similar reasoning for the boost nominal operating point, the equivalent control (10) in steady-state is $U_{1eq} = 1 + \frac{9}{12.8} \approx \frac{1}{4}$ and, since $V_c = V_o$ in boost mode, $\tau > 62$ µs. According to Fig. 6, the value selected is $\tau = 10$ kΩ × 6.8 nF = 68 µs.

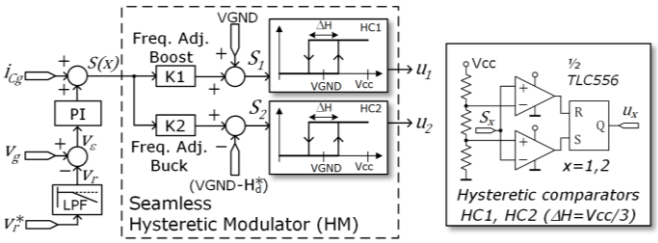

Fig. 7. Block diagram of the control circuit, detailing the implementation based on an IC556 of the two hysteretic comparators. Unlike in [8], gains K1 and K2 enable two independent adjustments of the switching frequency.

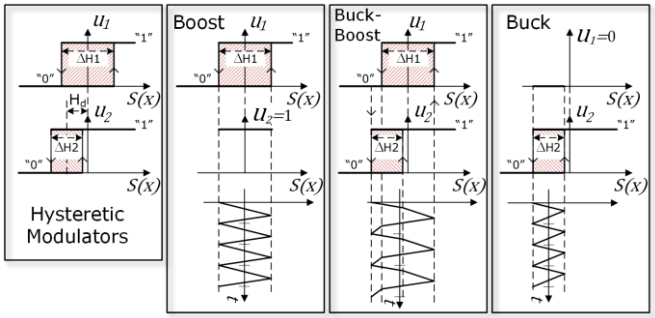

Fig. 8. Displacement (H_d) of the input-output characteristics of the hysteretic comparators in Fig. 7 to achieve automatic seamless transitions between Buck and Boost modes through a narrow Buck-Boost region. Idealized steady-state closed-loop waveforms of $S(x)$ are also depicted assuming adjustment of equal switching frequencies f_S for the Boost and Buck modes and lower f_S for the Buck-Boost operation.

A. Hysteretic-Modulation (HM) Analog Implementation

Fig. 7 shows a block diagram of the sliding controller analog implementation, in which the voltage error is fed to a PI block with the previously mentioned proportional gain $G = 6\ \frac{\text{A}}{\text{V}}$ and integral gain $k = 22000\ \frac{\text{A}}{\text{Vs}}$. The output of the PI block is added to the measurement of the input capacitor current to obtain $S(x)$. The implementation of this part of the controller (Fig. 6) uses well-known operational amplifier structures. For the sake of simplicity, the same high-bandwidth rail-to-rail OPA2350 ICs used in the capacitor current resistive sensor are also used in the inverting voltage PI and subtractor stages. The input voltage and current sensor gains have been scaled by 10:1 to adapt them to the [0 V, 5 V] dynamic range imposed by the 5-V unipolar supply voltage, and a 2.5-V virtual ground (VGND) has been also implemented.

The same OpAmp ICs are used to amplify signal $S(x)$ prior to its injection into a first hysteretic comparator (window comparator with three equal voltage divider resistors) implemented with a high-frequency version of the well-known 555 analog timer (TLC556). Since the hysteresis width is fixed (Vcc/3), the adjustment of the switching frequency in the nominal operating point is done by modifying the gain of the previous amplifier, whose input is $S(x)$ and whose output is S_1. This first comparator generates boost half-bridge control signal u_1. Control signal u_2 of the buck half-bridge is generated by another identical hysteretic comparator, for which input signal S_2 is obtained by subtracting from $\text{K2} \cdot S(x)$ a voltage $\text{VGND} - \text{H}_\text{d}^*$ corresponding to the width of the superposed

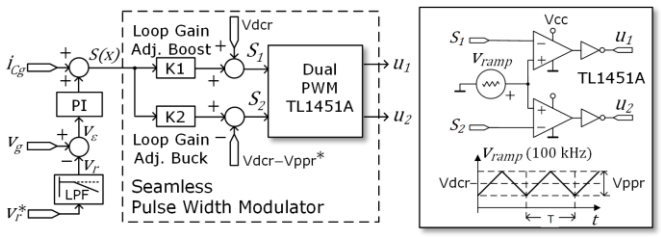

Fig. 9. Modification of the Fig. 7 block diagram for obtaining a fixed switching frequency. The two hysteretic comparators have been substituted by the dual PWM IC TL1451A already used in [15].

hysteresis bands, $0 < \mathrm{H_d} < \Delta\mathrm{H}$. The displacement of the hysteresis band (Fig. 8) provides the desired automatic seamless transition between boost and buck modes [18] by enabling a crossing through a narrow buck-boost region, limiting in this way the excessive switching frequency decrease of other types of transitions such as the "pass-through" proposed in [7]. To achieve the same switching frequency around the two nominal operating points, frequency adjustment gain K2 in the buck path must be approximately twice that of the boost path K1, thereby compensating for the $\sim 1{:}\,2$ ratio between expressions (7) and (11). Therefore, the equivalent hysteresis width of the boost path, ΔH1, is also about two times wider than ΔH2, the equivalent hysteresis width of the buck path. In the experimental prototype, $\mathrm{H_d}$ has been adjusted so that the two hysteretic bands can be clearly distinguished (see Fig.16 top).

B. PWM Analog Implementation

In the example considered in this work, the solar panel has two possible points of operation, one above and one below the battery voltage. The independent gain adjustments of Fig. 7 allow the switching frequency to be regulated to about 100 kHz around the two theoretical operating points but the frequency will be smaller for the intermediate voltages because, whenever input and output voltages are close, the slopes in the current waveforms decrease. See factors $(L_B + L_M)v_g - L_M v_o$ and $L_M v_g - (L_A + L_M)v_o$ in the numerators of $f_1(x)$ and $f_2(x)$ in (1).

If a fixed switching frequency is required in all operation points, we can opt for an implementation of the sliding mode control using PWM. In our case, the instructions given in [20], [30] to implement the sliding mode control by PWM and an indirect approximation are very difficult to follow because of the two operation modes of our system and the two different expressions of equivalent control (5) and (10). Generating analog signals proportional to both expressions has no simple solution because it is important to add integral terms of the voltage error, the saturations should be carefully considered if analog dividers are used, and it is important to avoid the high-frequency components provided by the derivatives of the inputs. We have decided to leave these possibilities of indirect implementation for future investigations and have instead chosen one solution that complies with the block diagram in Fig. 2. It uses the same signal *S(x)* in the PWM generation of the control signals to provide the seamless automatic transition between operation modes in the same way as in the voltage controller of [14], and in the average current control of [15] and [16]. As in the HM implementation, instead of a switching-free "pass-through" region, a narrow buck-boost intermediate region has been preferred, thus prioritizing the seamless of the transition (better control) at the expense of slightly increased switching losses. According to the experimental efficiency data provided at the end of section IV, these additional losses represent an efficiency reduction of about 1% (92.1%) at 13.5 V in comparison with the closer neighbors of (93,2% at 13 V and 92,8% at 14 V).

The diagram in Fig. 9 represents the modifications that need to be made to the diagram in Fig. 7 for implementation at constant switching frequency using a dual-PWM TL1451A controller instead of the two hysteretic comparators. The dual-PWM enables two control signals to be generated with independent duty cycles but with the same switching frequency, using only one 100-kHz triangular ramp [14]. Signals S_1 and S_2 are generated in the same way as shown in the top half of Fig. 7, though the frequency adjustments are transformed into independent adjustments of the two loop gains in order to fulfill the stability conditions. The H_d offset subtracted in Fig. 7 to obtain S_2 now becomes slightly smaller than the amplitude of the triangular ramp (Vppr) to provide seamless transition between buck and boost modes and has to be adjusted accordingly (Vppr^* is slightly smaller than 700 mV). As well as eliminating steady-state error, the integral term in the voltage loop compensates for the 1.4-V offset of the TL1451A triangular ramp (Vdcr). The main problem of this implementation is that multiple pulses can be produced in a switching period [31]. To prevent this unwanted high-frequency switching it is necessary to significantly reduce the loop gains and as a consequence the closed loop poles do not reach the open loop zeroes position. There is no reduction in order because none of the poles is moved toward infinity, and also the closed loop dynamics are modified in comparison with the ones obtained using the HM implementation.

IV. Experimental Results

Next the results of the laboratory tests are shown starting with the boost mode in combination with HM, and then using PWM in the same mode. After that, following the same sequence the converter performance operating in buck mode is presented.

A. Boost Mode, HM.

Figure 10 illustrates the experimental results for the bidirectional versatile buck-boost converter in step-up mode using the sliding mode control implemented with hysteretic comparators. The step-type input voltage reference v_r^* has been low-pass filtered through a first order RC passive stage with a cut-off frequency of about 800 Hz whose output is v_r.

As mentioned in Section II, the reference is varying periodically between 8 V and 9 V each 500 μs (CH1: top; scaling factor 10:1). We can clearly observe that the input voltage v_g (CH2: top) perfectly follows the variable reference voltage v_r without steady-state error.

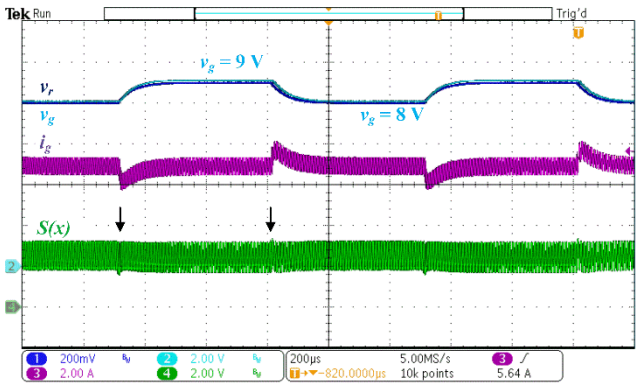

Fig. 10. Significant signals of the system operating in boost mode, using Hysteretic Modulation. CH1: scaled input voltage reference v_r (top); CH2: input capacitor voltage v_g (top); CH3: input inductor current i_g (middle trace); CH4: scaled $S(x)$ (bottom trace).

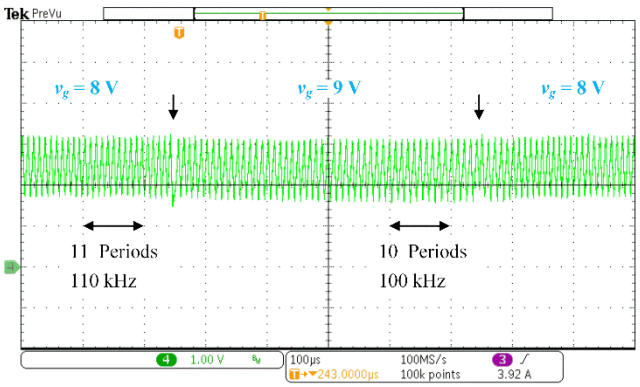

Fig. 11. Magnification of signal $S(x)$ from Fig. 10.

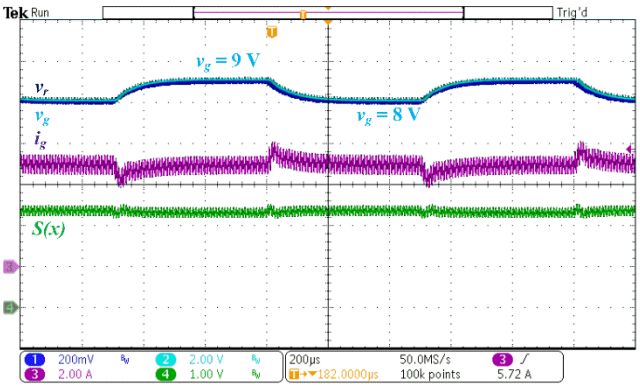

Fig. 12. Significant signals of the system operating in boost mode using PWM. CH1: scaled input voltage reference v_r (top); CH2: input capacitor voltage v_g (top); CH3: input inductor current i_g (middle trace); CH4: scaled $S(x)$ (bottom trace).

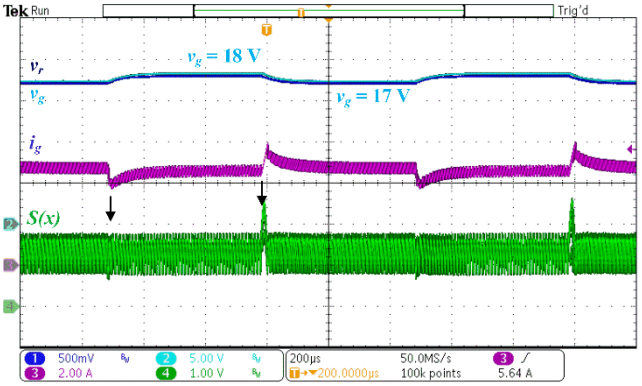

Fig. 13. Significant signals of the system operating in buck mode using HM. CH1: scaled input voltage reference v_r (top); CH2: input capacitor voltage v_g (top); CH3: input inductor current i_g (middle trace); CH4: scaled $S(x)$ (bottom trace).

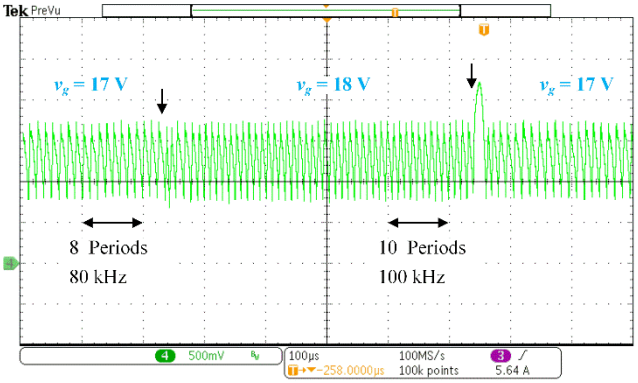

Fig. 14. Magnification of signal $S(x)$ from Fig. 13.

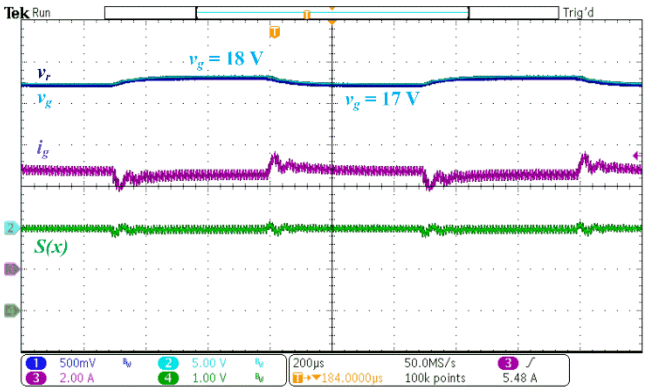

Fig. 15. Significant signals of the system operating in buck mode using PWM. CH1: scaled input voltage reference v_r (top); CH2: input capacitor voltage v_g (top); CH3: input inductor current i_g (middle trace); CH4: scaled S(x) (bottom trace).

The same oscillogram shows the current of the input capacitor (CH3: middle), which exhibits a stable dynamic behavior compatible with the poles of (16) and the 800-Hz prefilter bandwidth. Finally, we can also observe signal $S(x)$ (CH4: bottom), which shows no significant loss of the sliding regime, as can be seen in the enlargement in Fig. 11. Though difficult to perceive due to the proximity of the operating voltages, the switching frequency increases slightly from about 100 kHz (10 periods in 100 µs) to about 110 kHz (11 periods in 100 µs) when the nominal input voltage changes from 9 V to 8 V. This way of operating at variable switching frequency in combination with a P&O-type MPPT algorithm naturally provides a spreading of the frequency spectrum in the circuit signals, which can facilitate the fulfilment of the EMC norms [32] in some applications.

The main problem arises when the desired input voltage nears the output voltage (battery), because the switching frequency drops below 40 kHz. If the switching frequency is too close to the control bandwidth, its two half-bridge MOSFETS can switch at high frequency in the so-called buck-boost mode, and this presents some specific drawbacks such as larger losses and increased risk of sub-harmonics or chaotic

operation regimes. If the system has to operate frequently at these conditions, it would be preferable the fixed switching frequency alternative in order to better avoid the appearance of sub-harmonic and chaotic behaviors [17].

B. *Boost Mode*, PWM.

The experimental results obtained when the control uses the PWM implementation are shown in Fig. 12. There are no significant differences when the voltage response is compared with the result depicted in Fig. 10. Apart from the constant switching frequency, the main differences are in the transient responses of signals *S(x)* and input capacitor current, which display slightly more oscillating behaviors.

As expected [8], the smaller loop gain of the PWM implementation causes some differences in the high-frequency response, which are perfectly acceptable for the application considered here.

C. *Buck Mode*, HM.

The converter operation in buck mode at a variable switching frequency is shown in Fig. 13. Similarly to the experiments shown in Figs. 10 and 12, the capacitor voltage correctly tracks a reference voltage, which in this step-down mode varies between 17 V and 18 V and vice versa every 500 µs. The other variables in the oscillogram also exhibit fast dynamic behavior similar to the results obtained for the step-up mode using HM. Although not included in this paper, the results are also in good agreement with the PSIM simulations in [8].

Apart from the different operating point, the main difference between the step-up and step-down results is a slight loss of the sliding regime that takes place at the 18-V to 17 V transition. This can be more clearly appreciated in the magnification of the *S(x)* signal shown in Fig. 14. Given the asynchronous nature of the reference changes with respect to the switching instants, the loss of sliding regime is not always of the same duration. The magnification corresponds to an intermediate case. The switching frequency experimental values are superimposed at the bottom part of the oscillogram to point out that it has been adjusted to about 100 kHz for an input voltage of 18 V. The switching frequency corresponding to a steady state input voltage of 17 V is approximately 80 kHz, an expected smaller value since the current slopes depend on the difference between input and output voltages.

D. *Buck Mode*, PWM.

Figure 15 shows the same signals as in the previous oscillograms obtained in buck mode using the PWM implementation described previously. In this case the underdamped behavior in current i_{LA} and the *S(x)* signals is more pronounced. Nevertheless, the input capacitor voltage correctly tracks the 1-kHz reference, which qualifies it to the intended PV applications that use P&O-type MPPTs.

E. *Seamless Mode Transitions.*

To conclude the experimental results, Fig. 16 shows two oscillograms depicting the same signals as in previous figures. The signals were obtained using a triangular 200-Hz reference signal that makes the input voltage range from 7 V to 19 V and vice versa. The positive (I) and negative (II) slopes of the voltages are similar to the average ones in the zones marked also as (I) and (II) in Fig.17, in which the voltage reference changes in 1-V steps provided by a P&O MPPT basic algorithm. The upper oscillogram corresponds to the HM implementation while the PWM results are in the lower one. It can be seen that the input voltage seamlessly tracks its reference without significant dynamic problems when crossing between buck and boost modes.

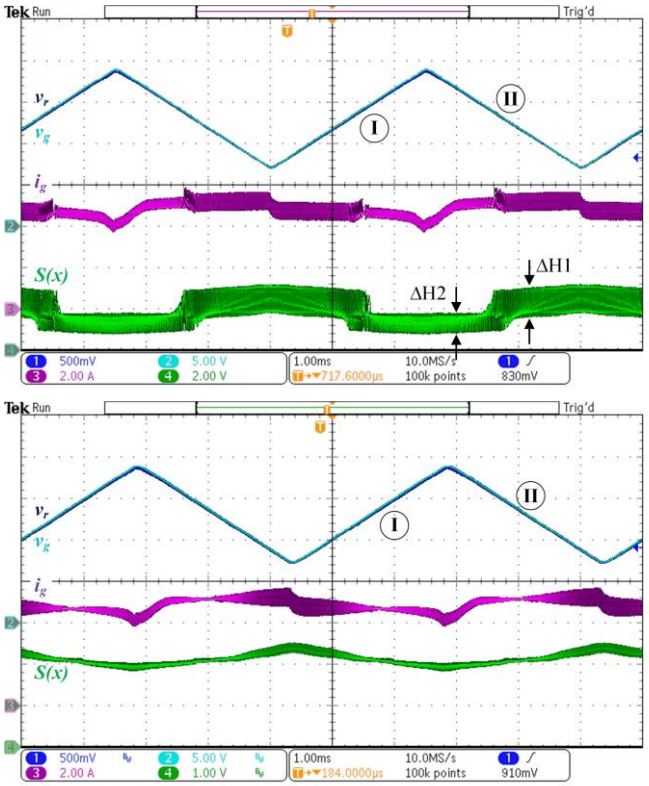

Fig. 16. System seamless transitions between buck and boost modes using HM *(top oscillogram)* and PWM (*bottom oscillogram*). Top traces: 200-Hz triangular input voltage at CH2 and its reference at CH1; CH3: input inductor current i_g (middle trace); CH4: scaled *S(x)* (bottom trace).

Finally, Fig. 17 shows a simulation of a representative example of the response of the system in Fig 2. After start-up the system operates around MPP *M1*, then a sudden partial shadowing at $t = 25$ ms causes the appearance of the two local power maxima *M2* and *M3*. A conventional P&O-type MPPT algorithm [33] has been adapted to detect the two local maxima through voltage sweeping and setting the system operation around the highest one, which in the example is *M2*. No efforts have been made to improve the MPP apart from selecting the low-pass filtered output current of the converter (the current charging the battery) as the index to be maximized [25] instead of the power generated by the PV module. Therefore the converter losses are taken into account and a multiplication operation is saved (see Fig. 2). The seamless transition from *M1* to *M2* observed in the simulation is very important to avoid confusing the MPPT algorithm, whose future versions would benefit from the improvements reported in [34]. It is also worth noting that, despite the bandwidth limitation imposed by the reference prefilter, the fast tracking capability available makes

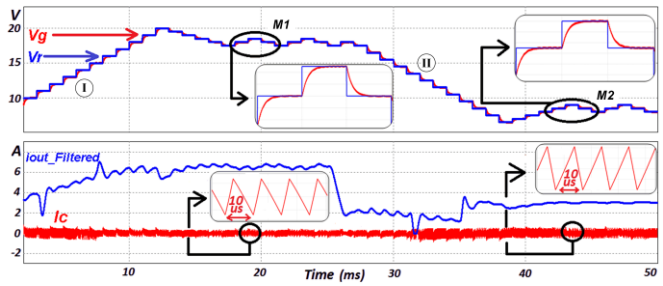

Fig. 17. PSIM simulation of the system's behavior in Fig. 2. A partial shadowing appears at t=25 ms. Top: PV module voltage (*Vg*) and its reference (*Vr*). Bottom: filtered battery current (*Iout*) and input capacitor current (*Ic*).

possible an MPP transition of only 15 ms. As a baseline, some comparable 10-step sweeps reported in [11], in which a one-switch buck-boost converter with an input capacitor of 470 µF is used, take about 200 ms. This performance makes the proposed system a strong candidate to validate researches focused on proposing and improving fast MPPT algorithms.

In the simulation, the converter uses the sliding-mode control scheme implemented with hysteretic comparators, which has been improved so that the switching frequency is similar around the two operating points: *M1* without shadowing and *M2* with partial shadowing. Since the switching frequency has been precisely adjusted to 100 kHz for input capacitor voltages of 18 V and 9 V, the two 40 µs enlarged portions of capacitor current *Ic* in Fig. 17 correspond to four periods of ripple waveforms, the differences being in their amplitudes and duty cycles. Note that there is undersampling distortion in the ripple of the 50-ms full simulation because of the different time-scales of MPPT and switching frequency. The enlarged waveforms depict the actual regular triangular shape of the current ripple.

To conclude the experimental results, Fig.18 shows the power stage and overall efficiencies of the proof-of-concept prototype together with the input and output power curves obtained by sweeping the input voltage from 5 V to 21.5 V in steps of 500 mV. As in the previous experiments, to obtain consistent and repetitive results, an Agilent's E4360A solar array simulator has been used to emulate the PV module at the converter input. A 13-V output battery has been emulated by using a KEPCO BOP72-14MG four quadrant power source. The efficiencies have been measured with a Yokogawa's WT330 digital power meter. It is worth noting that the proof-of-concept power stage prototype, whose photograph can be seen in Fig. 19, has been built with experimental robustness and easiness of repairing in mind, without any concrete efficiency goal. This is why there are so much difference in efficiencies between the power converter stage and the overall system efficiency that takes into account the consumption of the driver, current sensor, control board and other ancillary electronics such as 12-V and 5-V linear regulators. At the nominal 18-V M1 operating point the measured input and output currents were 4.72 A and 5.99 A. The measured output voltage was 13.1 V, while the ancillary electronics consumption was 2.04 W. Since the measured input and output powers and overall efficiency were 85.2 W, 78.5 W, and 92.1%, respectively, the power stage efficiency was roughly estimated as $\frac{78.5}{85.2-2.04} \approx 94.4\%$. At the

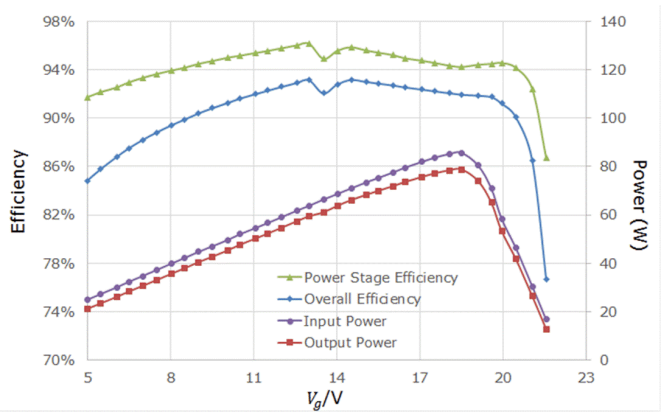

Fig. 18. Power stage and overall efficiencies of the experimental proof-of-concept prototype.

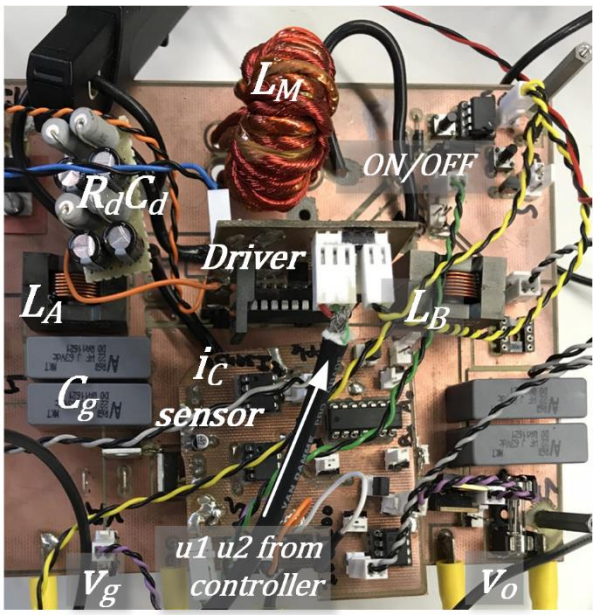

Fig. 19. Photograph of the proof-of-concept experimental power stage.

nominal M2 operating point the measured input power was about 44.7 W (9.02 V, 4.952 A) and the output power was 40.4 W (13.05 V, 3.097 A). Taking into account a measured 1.94-W consumed by the ancillary systems, the power stage and overall efficiencies were 90.4% and 94.5%, respectively.

The main visible elements of the experimental power stage have been identified in Fig.19. The view of the intermediate capacitor is blocked by the vertical driver board. The four MOSFETs are also not visible because they are placed on the other side of the main board. No effort have been done to optimize the power-stage size, giving priority instead to facilitate repairs and connections of current and voltage probes.

V. Conclusion

The step-up/down characteristics of the versatile buck-boost converter make it an appropriate choice in an application where a battery is charged from a photovoltaic panel with two internal subsections defined by two bypass diodes. The converter in the application has been modified by adding a capacitor at its input. The voltage of this input capacitor has been regulated to make

it possible maximizing the current charging the system battery in the two operating modes considered (buck and boost). The controller for the input capacitor voltage has been designed using a sliding mode approach so that its bandwidth enables a 1-kHz varying reference to be tracked, assumed to be provided by a P&O-type very fast MPPT algorithm.

The control has been implemented in two ways. The first one provides a variable switching frequency and uses a Hysteretic Modulation technique that has been modified so that, by using two hysteretic comparators with displaced hysteresis windows, it will provide an automatic seamless transition between the buck and boost modes. The implementation allows the switching frequency to be adjusted so that it is the same at both nominal buck (18-V) and nominal boost (9-V) maximum power point operating points.

An alternative constant switching frequency implementation of the control that also provides seamless transition between the two modes of operation has been derived from the hysteretic modulation implementation.

The experimental results confirm that both techniques provide satisfying results regarding the regulation of the input capacitor voltage for the PV application considered. Completing the experimental set-up of the system in Fig. 2 by digitally implementing the MPPT(Io) block is a work in progress.

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