Thermal Resistance Characterization for Multi-Finger SOI-MOSFETs

Journal:	*Transactions on Electron Devices*
Manuscript ID	TED-2018-04-0603-R.R1
Manuscript Type:	Regular
Date Submitted by the Author:	n/a
Complete List of Authors:	Gonzalez Perez, Benito; Universidad de Las Palmas de Gran Canaria, IUMA Rodríguez, Raúl; Universidad de Las Palmas de Gran Canaria - Campus de Tafira Lazaro, Antonio; Universitat Rovira i Virgili, DEEEA
Area of Expertise:	MOSFETs, Electrothermal effects

SCHOLARONE™
Manuscripts

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

Thermal Resistance Characterization for Multi-Finger SOI-MOSFETs

Benito González, Raúl Rodríguez, Antonio Lázaro, *Senior Member, IEEE*

***Abstract*— Thermal conductance in multi-finger SOI-MOSFETs is usually modeled at room temperature with a linear dependence on the total gate width, which is valid only when thermal coupling saturates. This paper presents a physically based model for calculating the thermal resistance of SOI-MOSFETs that accounts for progressive thermal coupling as the number of fingers increases and the substrate temperature. The model, extracted from a variety of gate geometries using the AC conductance method, correctly predicts the temperature rise in the device channel up to a substrate temperature of 150 ºC. Finally, this simple thermal resistance model, which is applicable to nanometer-scale transistors, can easily be added to circuit simulators.**

Index Terms—**SOI-MOSFET, thermal resistance, electrothermal characterization, substrate temperature, multi-finger model.**

I. Introduction

Miniaturization of metal oxide semiconductor field effect transistors (MOSFETs) has led to massive integration levels, where heat generation causes chip temperatures that can prevent the circuits' reliable operation, especially at nanometer length scales where the geometry in novel MOS devices tends to make heat removal more difficult.

Silicon-on-insulator (SOI) MOSFETs for the next generation of automotive, industrial and medical applications, will operate in the temperature range of –40 °C to 175 °C. When SOI technology is used, the very low thermal conductivity of the buried oxide layer (BOX in Fig. 1) significantly impedes heat transfer toward the substrate, particularly for thicknesses greater than 100 nm [1]. Additionally, confined dimensions can still augment self-heating [2], as the thermal conductivity of internal thin films is much lower than the corresponding bulk value [3-7]. In consequence, heat dissipation is sensitive to external

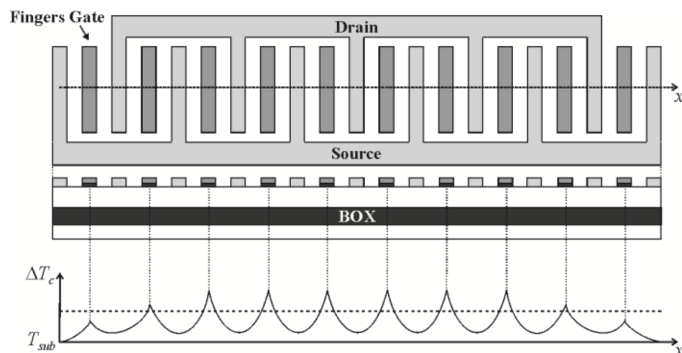


Fig. 1. Multi-finger device thermal coupling: Top view of transistor and schematic representation of the typical temperature rise in the channel, along the heat source in *x* direction.

contacts and gate geometry design, which must be optimized to efficiently reduce overheating in device performance [1][8][9].

Several precise techniques have been developed to measure thermal resistance in FETs. They are based on the AC conductance method [10][11], pulsed characteristics [12][13], IR and Raman thermographs [14], or even by extraction of a traps activation energy [15]. However, more progress is still needed to effectively model the thermal characteristics in SOI-MOSFETs, due to the thermal coupling that takes place in devices with nano-scale dimensions [1][2]. It can even lead to negative output conductance in low-frequency regimes [12].

The microelectronics community has made remarkable efforts towards the development of thermal models for MOSFETs [1][2][16-18]. Although detailed thermal models are desirable in order to achieve an exhaustive physical description [1][18], simplification is mandatory when dealing with compact models, such as BSIMSOI [19][20], for circuit simulation purposes. Thus, the thermal conductance in SOI-MOSFETs is usually modeled with a linear dependence on the gate width [21], without taking into consideration the number of fingers (no matter which gate configuration is used, the device's thermal resistance is estimated through the gate width), which is valid only when the thermal coupling is saturated. That is, when internal fingers determine the transistor temperature due to overheating [2][22][23]. For example, Fig. 1 shows a schematic distribution of the typical temperature rise in the channel of multi-finger devices, similar to that obtained using three-dimensional thermal TCAD simulations [22], where the thermal coupling between the gate

This work was supported by the Spanish MEC under Project GREENSENSE–TEC2015-67883-R.

B. González and R. Rodríguez are at the Institute for Applied Microelectronics, Universidad de Las Palmas de Gran Canaria, Campus Universitario de Tafira, Las Palmas, CO 35017 Spain (e-mail: benito@iuma.ulpgc.es and rrodriguez@iuma.ulpgc.es).

A. Lázaro is at the Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Escola Tècnica Superior d'Enginyeria, Av. Dels Països Catalans 26, Tarragona, CO 43007 Spain (e-mail: antonioramon.lazaro@urv.cat).

fingers increases the measured average temperature ΔT_c (dashed line).

Regarding variation in thermal resistance with gate length, SOI-MOSFETs' thermal resistance increases with reductions in channel length in the micrometer range (when BOX is thin enough). However, this dependence becomes weak in the cases of very long and short channel devices [20], as heat is mainly dissipated through the substrate (with the thermal resistance being evaluated as in [24]) and terminal contacts (as contacts do not scale with gate length), respectively. According to the International Technology Roadmap for Semiconductors (ITRSs) [25], and given that the BOX layer in the SOI-MOSFETs we investigated was thick enough to avoid heat dissipation through the substrate, this work does not consider variation in thermal resistance with gate length.

In this paper, we propose a simple model for circuit simulators for the thermal resistance of SOI-MOSFETs, accounting for the gradual thermal coupling when the number of fingers increases and including the substrate temperature dependence. The approach could be applied to higher drain current devices, which support higher operating temperatures, such as III-V devices and, particularly, GaN-based transistors (HEMTs) for high-power RF applications [26].

Thus, the SOI-MOSFETs under consideration, by varying the gate geometry, are presented in Section II. The experimental set-up for electrothermal characterization is described in Section III. Section IV devotes to thermal resistance characterization, extraction and modelling, and discusses the results. Finally, the conclusions are summarized in Section V.

II. Fabricated Devices

In order to validate the proposed model, eight partially depleted SOI N-channel MOSFETs, body tied to prevent the floating-body effect, were studied. The devices, which gate length was 180 nm, were built using XT018 0.18μm HV SOI-CMOS technology (by XFAB) within an 8-inch p-type SOI wafer process.

To this end, different multi-finger devices were designed, composed of 5, 10, 20, and 30 parallel fingers (N_f) (to exhibit considerable self-heating), each finger being 2 μm wide (W_f). Therefore, the total gate width ($W = N_f W_f$) was 10, 20, 40, and 60 μm, respectively. Identical gate widths were used to build four single-finger devices (to minimize self-heating), for comparison.

The devices were embedded in ground–signal–ground (GSG) on-wafer test structures, with co-planar waveguide access pads and grounded guard rings, to enable high frequency measurements [12][27]. For every transistor, three additional structures (single-open, single-short, and thru) were designed to perform the subsequent de-embedding technique [28], based on the four steps in [29], in order to eliminate the parasitic effects introduced by pads and the guard ring.

III. Experimental set-up

On-wafer measurements were performed with a CASCADE-Summit 9000 probe station. DC measurements were obtained using an Agilent B1500A Semiconductor Analyzer and the substrate temperature, T_{sub} (30 ºC to 150 ºC, in 20 ºC increments, to avoid damaging or degrading the performance of the device under test –DUT– through excessive threshold voltage displacement) was set through a thermal chuck.

The scattering parameters (S-parameters) were measured from 50 MHz to 1 GHz at the substrate temperatures indicated, using the Agilent 8720ES Vector Network Analyzer (with internal bias tees) and Cascade GSG microprobes as shown in Fig. 2(a), using the Agilent B1500A Semiconductor Analyzer for biasing. In order to calibrate the measurement system, the short-open-load-through method was implemented in a previous step.

For pulsed measurements, see Fig. 2(b), an Agilent HP8133 signal generator applied a pulse to the gate of the SOI-MOSFETs ($V_{g\text{-}pulse}$), with the pulse base being set at a level, 0 V, where the device is off; a PSPL5370 pick-off tee was used in the gate to allow non-intrusive monitoring of the gate pulse voltage, as in [27]. An Agilent HP54754 digitizing oscilloscope recorded the voltage pulse of the drain ($V_{d\text{-}pulse}$) through a bias tee, [30]. The bias tee has two roles in this set-up: it applies DC signals to the device (drain-to-source

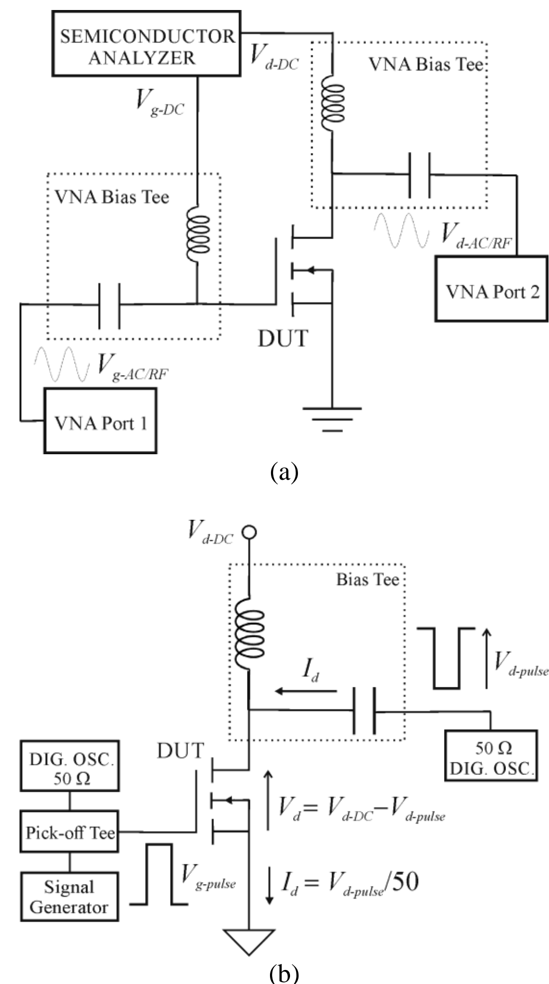


Fig. 2. Schematic of the measurement system: (a) AC/RF and (b) pulsed.

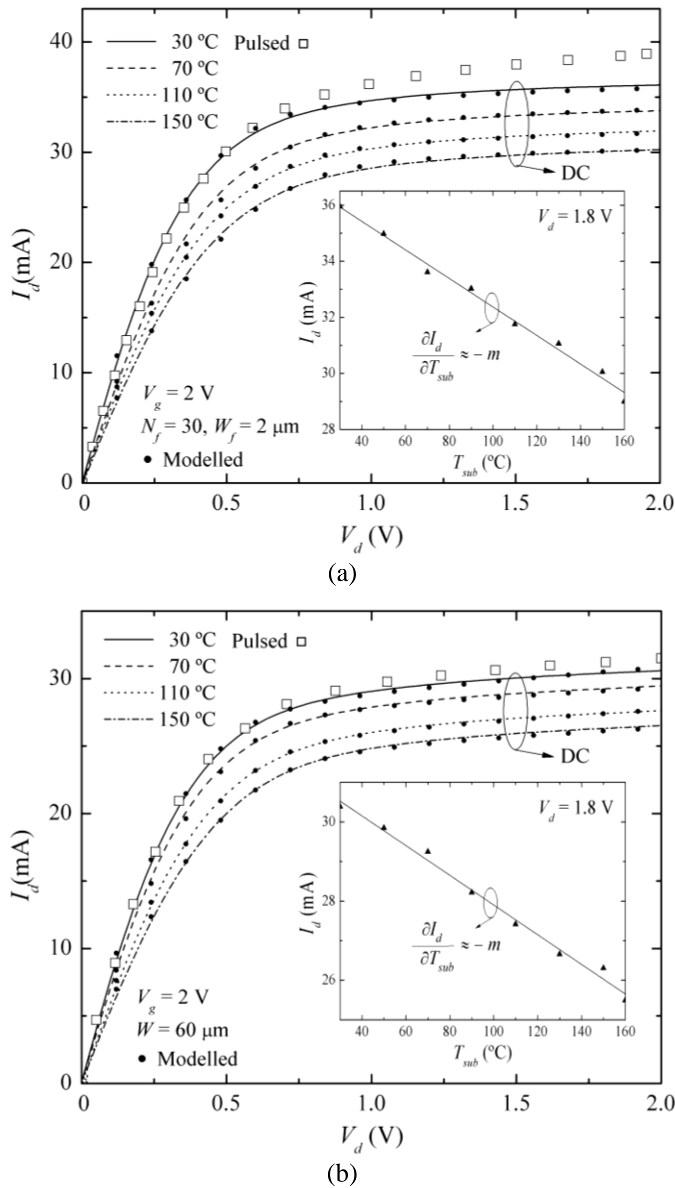


Fig. 3. Measured (lines) and modeled (circles) DC output characteristics at different substrate temperatures for (a) a multi-finger SOI-MOSFET (where N_f = 30 and W_f = 2 µm) and (b) a single-finger transistor (with W = 60 µm), and corresponding pulsed output characteristics at 30 °C (open squares); V_g = 2 V. The inset plot shows the resulting linear temperature dependence of the drain current with the substrate temperature, for V_d = 1.8 V.

voltage $V_{d\text{-}DC}$) whilst isolating the power supply from pulsed signals, and it allows pulsed signals to pass through the bias tee capacitor. Thus when the gate switches from 0 V to $V_{g\text{-}pulse}$, the (I_d, V_d) value switches from (0, $V_{d\text{-}DC}$) to ($V_{d\text{-}pulse}$ /50, $V_{d\text{-}DC} - V_{d\text{-}pulse}$). Output characteristics can be generated by varying $V_{d\text{-}DC}$. Finally, pulses 50 ns wide with a 0.01% duty cycle were used to avoid self-heating [12].

IV. Thermal Resistance Characterization

Self-heating effects were primarily demonstrated in the fabricated SOI-MOSFETs, by measuring their output characteristics using nanosecond pulses, as previously indicated. The corresponding results for the 30-fingers and single-finger transistors with the same total gate width (60 µm), a substrate temperature of 30 °C and a gate bias voltage of 2 V (to enhance self-heating effects) are presented (open squares) in Fig. 3(a) and 3(b) respectively, with DC measurements (solid lines) for comparison. It should be noted that in the saturation region the current increment cannot be obviated when self-heating is prevented (by using pulsed measurements), particularly in the case of the multi-finger device, where self-heating effects are more marked and the drain current greater, due to lower contact resistance at the source/drain terminals.

Therefore, thermal resistance characterization is mandatory in SOI technology. For this purpose, and because self-heating assessed by the pulsed technique might be underestimated [12], the AC conductance method is used as follows.

A. Extraction

The thermal resistance, R_{th}, is obtained for substrate temperatures up to 150 ºC by applying the AC conductance technique [10][12] as

$$R_{th}=\frac{g_{ddo}-g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT}+V_g g_{gdT}+I_d\right)} \quad (1)$$

where g_{ddo} and g_{ddT} are the conductance, g_{dd}, at low frequency (with dynamic self-heating present) and at high frequency (with dynamic self-heating removed), respectively, and g_{gdT} is $g_{gd}= \partial I_d/\partial V_{gd}$ without dynamic self-heating, which are derived from corresponding S parameters [12]. The rest of the parameters (g_{ddo}, which is approximated by the DC output conductance as source and drain access resistances are very low, I_d, and $\partial I_d/\partial T_{sub}$) are obtained from output characteristics at different substrate temperatures (lines and inset plot in Fig. 3(a) and 3(b)).

In SOI-MOSFETs, when dynamic self-heating vanishes g_{dd} plateaus at around 100 MHz [11][12][31][32]. Then, it is observed that $V_g g_{gdT} \ll V_d g_{ddT}$ and the thermal resistance can be approximated by

$$R_{th}\approx\frac{g_{ddo}-g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT}+I_d\right)} \quad (2)$$

The measured g_{dd} frequency response for a substrate temperature of 30 ºC (in a saturation regime where V_d = 1.8 V and V_g = 2 V, to enhance self-heating effects) is represented by lines in Fig. 4(a) and 4(b) for multi-finger and single-finger transistors, respectively. Similar results are obtained for the rest of the temperatures.

The increase in output conductance over a wide frequency range is due to substrate-related effects (majority carriers) at frequencies of some hundreds of megahertz, and gate resistance in the gigahertz range [11]. Inset plots show that conductance remained constant between 150 MHz and 200 MHz, where average g_{ddT} can be measured to be used in (2).

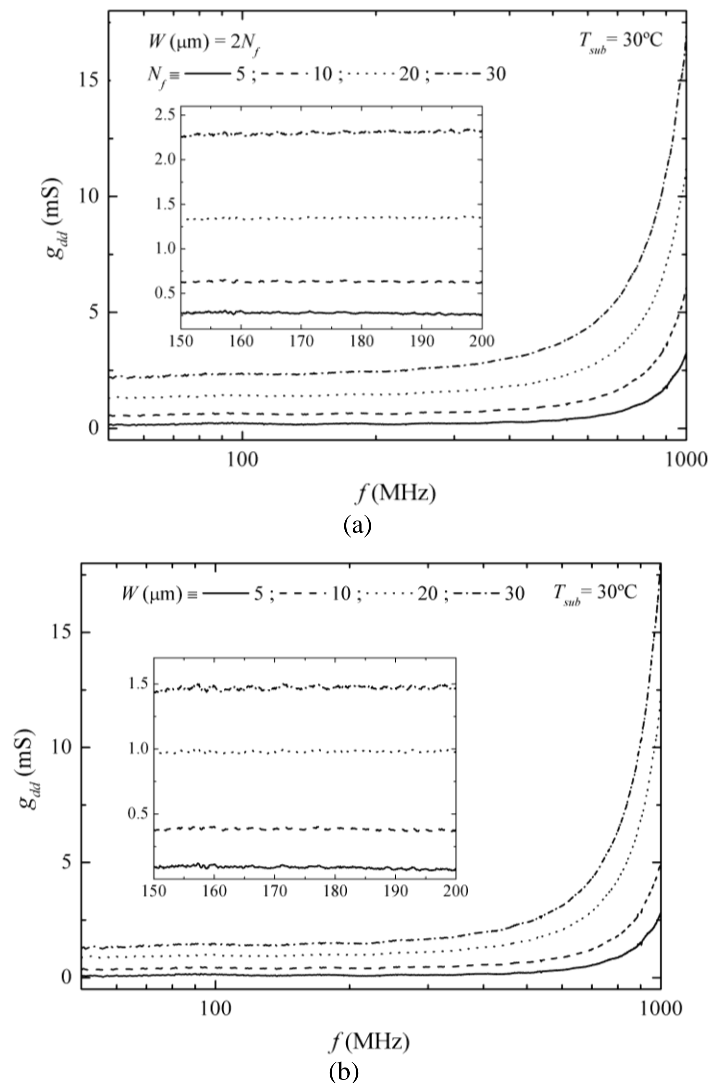


Fig. 4. Output conductance frequency response at 30 °C for (a) multi-finger transistors, and (b) single-finger transistors; V_g = 2 V, V_d = 1.8 V. Inset plots show the conductance plateau and the corresponding frequency range, where average g_{ddT} can be evaluated.

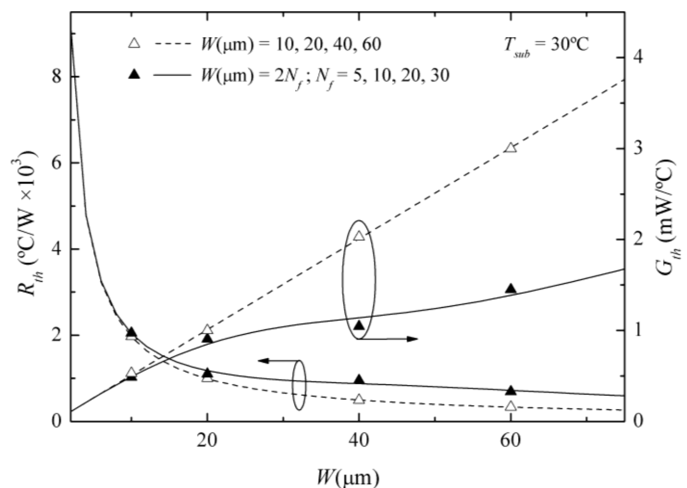


Fig. 5. Comparison of the thermal resistance (left axis) and conductance (right axis), as a function of gate width, extracted and modeled for multi-finger transistors (with solid symbols and solid line, respectively), and single-finger transistors (with open symbols and dashed line, respectively); T_{sub} = 30 ºC.

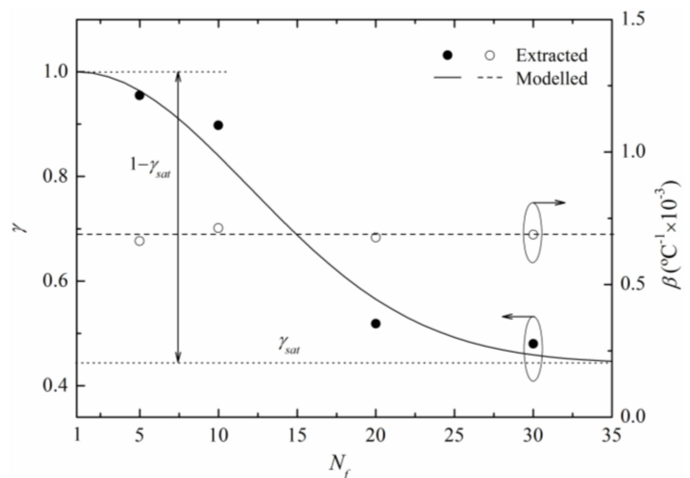


Fig. 6. Extracted (scattered), and modeled (line) finger width coefficient (left axis) and temperature coefficient (right axis), as a function of the number of fingers.

B. The model

The measured thermal resistance for the transistors, at a substrate temperature of 30 ºC, depends on the gate width, W, as indicated in Fig. 5, left axis; open and closed symbols represent single-finger and multi-finger devices, respectively. Similarly, the corresponding measured thermal conductance is represented on the right axis.

As mentioned previously, thermal resistance in SOI-MOSFETs is strongly dependent on technology and needs to be characterized experimentally for each one, making comparison of normalized thermal resistances ($R_{th}\times W$) a difficult task. Nevertheless, in this work the measured thermal resistance of single-finger devices was of the same order of magnitude as that of SOI-MOSFETs in [20] [32] [33], when normalized. Moreover, similar normalized thermal resistances were measured for multi-finger transistors in [11] for FinFETs.

Note that for the single-finger SOI-MOSFETs under investigation, the measured thermal conductance, $G_{th} = 1/R_{th}$, has a linear dependence on the gate width. Thus, it can usually be modeled as $G_{th} = (\alpha + W)/R_{tho}$ [21], where $\alpha = 0.19$ µm and $R_{tho} = 2\times10^4$ ºC-µm/W, which are technologically dependent fitting parameters. The modeled thermal conductance and the corresponding thermal resistance are plotted with dashed lines in Fig. 5, showing a good agreement with measured data.

Conversely, in multi-finger transistors, thermal coupling increases as the number of fingers, N_f, increases; this is made evident through the non-linear dependency of the measured thermal conductance on the gate width. In this case, the G_{th} augmentation with W diminishes as the number of fingers increases, with a linear dependence that is estabilished, because thermal coupling saturates, when the number of fingers is high enough ($N_f \gg 10$), as in [21][23].

The linear thermal conductance model for a single-finger transistor at 30 ºC can be extended to multi-finger devices, defining an effective finger width, $W_{f\text{-}eff}$, as

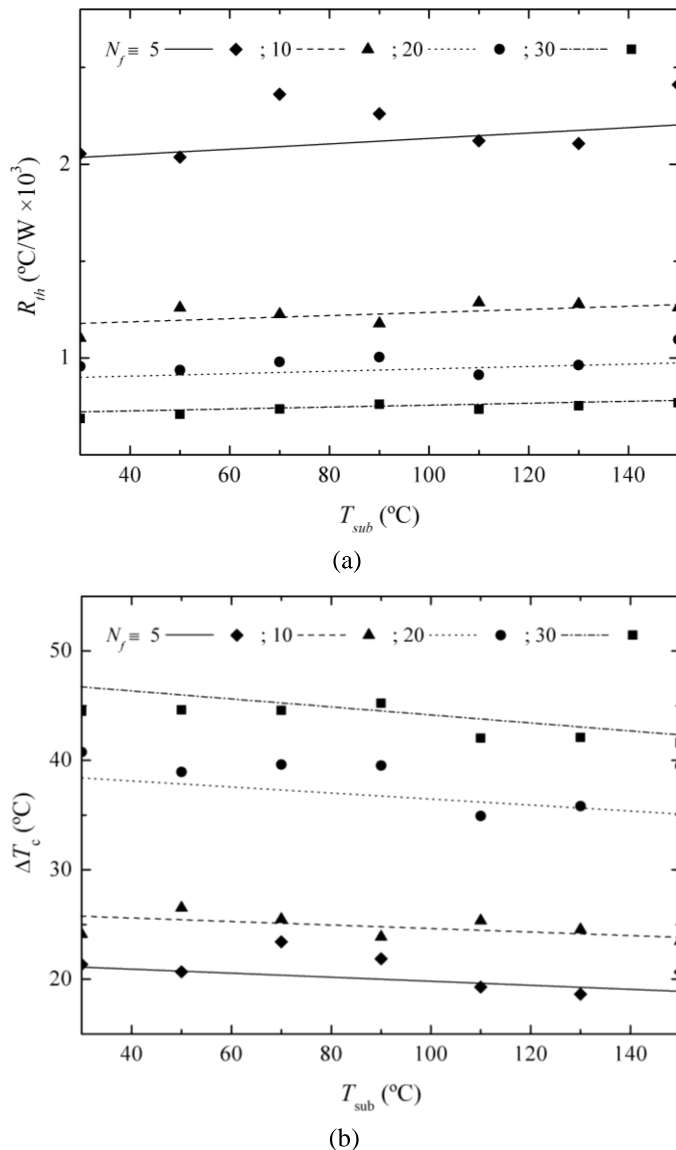


Fig. 7. Thermal resistance (a) and temperature rise in the channel (b), as a function of the substrate temperature, extracted from measurements (scattered) and modeled (lines) for multi-finger devices; V_g = 2 V, V_d = 1.8 V.

$$\frac{1}{R_{th\text{-}30ºC}} \approx \frac{\alpha + N_f\, W_{f\text{-}eff}}{R_{tho}}, \tag{3}$$

where the effective finger width accounts for the thermal coupling, $W_{f\text{-}eff} = \gamma W_f$ ($\gamma < 1$).

The finger width coefficient, γ, is extracted from the measured data using (3) and depends on the number of fingers as shown in Fig. 6 (left axis, with symbols). It can be modeled using a Gaussian function (with solid line) as:

$$\gamma = \gamma_{sat} + (1 - \gamma_{sat})\mathrm{e}^{-\frac{(N_f - 1)^2}{2\sigma^2}} \tag{4}$$

where γ_{sat} = 0.44; this being the reduction coefficient when thermal coupling saturates ($N_f \to \infty$), and σ = 10.9 is the standard deviation. Both fitting parameters are technologically dependent. Thus, a good agreement between modeled and extracted data for γ in multi-finger SOI-MOSFETs is achieved, as well as for G_{th} and R_{th}, with modeled data being represented by the solid line in Fig. 5. Note that for N_f = 1 (γ = 1) the thermal resistance predicted tends to be the same as that for a single-finger transistor 2 µm wide (i.e. the finger width).

Once thermal resistance has been characterized at 30 ºC, the substrate temperature incidence is analyzed. It was observed that the thermal resistance linearly increases with the substrate temperature, as Fig. 7(a) shows for multi-finger devices (with symbols), which can be modeled as in [34].

$$R_{th} \approx R_{th\text{-}30ºC}(1 + \beta \Delta T_{sub}) \tag{5}$$

where $R_{th\text{-}30ºC}$ is given by (3), ΔT_{sub} is the substrate temperature increment, T_{sub} − 30 ºC, and the temperature coefficient β is a technologically dependent fitting parameter, which is represented in Fig. 6 (right axis, with symbols). Practically no variation in temperature coefficient is observed for a different number of fingers, and an average value (the dashed line), β = 7×10^{-4} (ºC^{-1}), which is comparable to that found in [4] with SOI technology, is enough to model the substrate temperature dependence of the thermal resistance for any device. Fig. 7(a) shows the resulting thermal resistance modeled for multi-finger SOI-MOSFETs (with lines), with a maximum relative error of 10% with respect to measured data at any substrate temperature. Similar results are obtained for single-finger SOI-MOSFETs.

Finally, the temperature rise in the device channel above substrate temperature, $\Delta T_c = T_c - T_{sub}$, is obtained as $R_{th}V_dI_d$ in the saturation regime (with V_d = 1.8 V and V_g = 2 V, to enhance self-heating effects). For single-finger transistors, ΔT_c remains almost constant at approximately 19 ºC, for any substrate temperature. In the case of multi-finger devices, as expected, ΔT_c strongly depends on the number of fingers (by thermal coupling), as Fig. 7(b) indicates for measured data (with symbols). Furthermore, as substrate temperature rises, a slight decrease in ΔT_c is observed, its dependence diminishing as the number of fingers reduces. In case of the multi-finger SOI-MOSFET with 30 parallel fingers (i.e. the worst case), the channel temperature, $T_c = T_{sub} + \Delta T_c$, reaches around 190 °C (on average, along the channel) at a substrate temperature of 150 °C, which is close to the typical maximum operating temperature (200 °C) for complementary metal-oxide semiconductor (CMOS) logic.

When accounting for (5) and the linear temperature dependence of the drain current, $I_d \approx I_{d\text{-}30°C} - m\cdot\Delta T_{sub}$ (see inset plot in Fig. 3(a) and 3(b)), the resulting model (lines in Fig. 7(b)) predicts the measured temperature rise in the channel, with the same maximum relative error as obtained in the case of thermal resistance, 10%.

Additionally, electro-thermal simulations were performed with BSIMSOI (version 3.1) using the thermal-electrical analogy. BSIMSOI models DC self-heating by introducing an

internal temperature node into the device. This node is connected to ground through the thermal resistance, which is given by (5), and the nodal "voltage" is actually the device temperature when the current flowing through the thermal resistance equals the electrical power dissipated in the device, V_dI_d. Modeled output characteristics for 60 µm-wide multi-finger and single-finger SOI-MOSFETs at different substrate temperatures (with $V_g = 2$ V) are presented (closed circles) in Fig. 3(a) and 3(b) respectively, showing a good agreement with the corresponding DC measurements (lines).

Lastly, thermal coupling analysis also demands the extraction of thermal capacitance in order to determine the thermal cross talk/temperature rise and thermal time constant; this will the object of future work.

V. Conclusions

A thermal resistance model for SOI-MOSFETs, accounting for the multi-finger thermal coupling and the substrate temperature, has been presented. The model, incorporating the number of fingers, predicts device overheating for substrate temperatures up to 150 ºC, when the temperature rise in the channel ascends to 45ºC with maximum thermal coupling. Furthermore, as substrate temperature increases the temperature rise in the channel slightly diminishes, dependence vanishing as the thermal coupling is reduced. Finally, this modelling approach for thermal resistance can easily be added to other well-established models in circuit simulators.

References

[1] M. Shrivastava, M. Agrawal, S. Mahajan, H. Gossner, T. Schulz, D. K. Sharma, and V. R. Rao, "Physical insight toward heat transport and an improved electro-thermal modeling framework for FinFET architectures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1353–1363, May 2012, 10.1109/TED.2012.2188296.

[2] B. Swahn and S. Hassoun, "Electro-thermal analysis of multi-fin devices," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol.16, no. 7, pp. 816–829, July 2008, 10.1109/TVLSI.2008.2000455.

[3] M. von Arx, O. Paul, and H. Baltes, "Process-dependent thin-film thermal conductivities for thermal CMOS MEMS," *J. Microelectromech. Syst.*, vol. 9, no. 1, pp. 136–145, Jan. 2000, 10.1109/84.825788.

[4] J. B. Roldán, B. González, B. Iñiguez, A. M. Roldán, A. Lázaro, and A. Cerdeira, "In-depth analysis and modelling of self-heating effects in nanometric DGMOS-FETs," *Solid-State Electron.*, vol. 79, pp. 179–184, Jan. 2013, 10.1016/j.sse.2012.07.017.

[5] S. M. Lee and D. G. Cahill, "Heat transport in thin dielectric films," *J. Appl. Phys.*, vol. 81, no. 6, pp. 2590–2595, Mar. 1997, 10.1063/1.363923.

[6] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *in Proc. IEEE IEDM Tech. Dig.*, Washington, DC, USA, 1999, pp. 67–70, 10.1109/IEDM.1999.823848.

[7] J. F. Shackelford and W. Alexander, "Thermal properties of materials," in *Materials Science and Engineering Handbook*, 3rd ed. New York, NY, USA: CRC Press LLC, 2001, pp. 409–460.

[8] D. Ha, H. Takeuchi, Y. K. Choi, and T. J. King, "Molybdenum gate technology for ultrathin-body MOSFETs and FinFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 1989–1996, Dec. 2004, 10.1109/TED.2004.839752.

[9] L. S. Yojo, R. C. Rangel, K. R. A. Sasaki, and J. A. Martino, "Is there a zero temperature bias point (ZTC) on back enhanced (BE) SOI MOSFET?," *in Proc. IEEE S3S Conf.*, San Francisco, CA, USA, 2017, pp. 1–3, 10.1109/S3S.2017.8309258.

[10] N. Rinaldi, "Small-signal operation of semiconductor devices including selfheating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, 10.1109/16.902734.

[11] S. Makovejev, S. Olsen, and J.-P. Raskin, "RF extraction of self-heating effects in FinFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, 10.1109/TED.2011.2162333.

[12] S. Makovejev, S. H. Olsen, V. Kilchytska, and J. P. Raskin, "Time and frequency domain characterization of transistor self-heating," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1844–51, Jun. 2013, 10.1109/TED.2013.2259174.

[13] J. Joh, J. A. del Alamo, T. M. Chou, H. Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, Dec. 2009, 10.1109/TED.2009.2032614.

[14] M. H. H. Kuball and J. W. Pomeroy, "A review of Raman thermography for electronic and opto-electronic device measurement with submicron spatial and nanosecond temporal resolution," *IEEE Trans. Device Mater. Reliab.*, vol. 16, no. 4, pp. 667–684, Ap. 2016, 10.1109/TDMR.2016.2617458.

[15] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in GaN HEMTs-part II: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3182, Oct. 2013, 10.1109/TED.2013.2278290.

[16] J. S. Brodsky, R. M. Fox, D. T. Zweidinger, and S. Veeraraghavan, "A physics-based, dynamic thermal impedance model for SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 957–964, Jun 1997, 10.1109/16.585551.

[17] S. Hniki, G. Bertrand, S. Ortolland, M. Minondo, B. Rauber, C. Raynaud, A. Giry, O. Bon, H. Jaouen, and F. Morancho, "Thermal effects modeling of multi-fingered MOSFETs based on new specific test structures," *in Proc. IEEE ESSDERC*, Athens, Greece, 2009, pp. 296–299, 10.1109/ESSDERC.2009.5331544.

[18] F. Nasri, M. Fadhel, B. Aissa, and H. Belmabrouk, "Nonlinear electrothermal model for investigation of heat transfer process in a 22-nm FD-SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1461–1466, Ap. 2017, 10.1109/TED.2017.2666262.

[19] B. Hu, C. Wakayama, L. Zhou, and C. J. R. Shi, "Developing device models,", *IEEE Circuits and Devices Magazine*, vol. 21, no. 4, pp. 6–11, July-Aug. 2005, 10.1109/MCD.2005.1492712.

[20] P. Kushwaha, K. BalaKrishna, H. Agarwal, S. Khandelwal, J.-P. Duarte, C. Hu, and Y. S. Chauhan, "Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG," *Microelectron. J.*, vol. 56, pp. 171–176, Oct. 2016, 10.1016/j.mejo.2016.07.014.

[21] S. Lee, R. Wachnik, P. Hyde, L. Wagner, J. Johnson, A. Chou, A. Kumar, S. Narasimha, T. Standaert, B. Greene, T. Yamashita, J. Johnson, K. Balakrishnan, H. Bu, S. Springer, G. Freeman, W. Henson, and E. Nowak, "Experimental analysis and modeling of self heating effect in dielectric isolated planar and fin devices," *in Proc. IEEE Symp. on VLSI Technol.*, Kyoto, Japan, 2013, pp.T248–T249.

[22] M. Weiß, A. K. Sahoo, C. Raya, M. Santorelli, S. Fregonese, C. Maneux, and T. Zimmer, "Characterization of intra device mutual thermal coupling in multi finger SiGe:C HBTs," *in Proc. IEEE EDSSC*, Hong Kong, China, 2013, pp. 1–2, 10.1109/EDSSC.2013.6628109.

[23] B. González, J. B. Roldán, B. Iñiguez, A. Lázaro, and A. Cerdeira, "DC self-heating effects modelling in SOI and bulk FinFETs," *Microelectron. J.*, vol. 46, pp. 320–326, Ap. 2015, 10.1016/j.mejo.2015.02.003.

[24] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and modeling of self-heating in SOI nMOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 1, pp. 69-75, Jan. 1994, 10.1109/16.259622.

[25] International Technology Roadmap for Semiconductors; 2014. Available from: <http://www.itrs.net/reports.html>.

[26] R. Guggenheim and L. Rodes, "Roadmap review for cooling high-power GaN HEMT devices," *in Proc. IEEE COMCAS*, Tel-Aviv, Israel, 2017, pp. 1–6, 10.1109/COMCAS.2017.8244734.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

[27] C. D. Young, Y. Zhao, D. Heh, R. Choi, B. H. Lee, and G. Bersuker, "Pulsed I_d–V_g methodology and its application to electron-trapping characterization and defect density profiling," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1322–1329, Jun. 2009, 10.1109/TED.2009.2019384.

[28] I. Gutiérrez, J. Meléndez, J. García, I. Adin, G. Bistue, and J. de No, "Reliability Verification in a Measurement System of Integrated Varactors for RF Applications," *IEEE Lat. Am. Trans.*, vol. 3, no. 4, pp. 15–20, Oct. 2005, 10.1109/TLA.2005.1642424.

[29] T. E. Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 734–740, Ap. 2000, 10.1109/16.830987.

[30] K. A. Jenkins, J. Y. C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997, 10.1109/16.641362.

[31] S. Makovejev, J.-P. Raskin, M. K. Md Arshad, D. Flandre, S. Olsen, F. Andrieu, and V. Kilchytska, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs," Solid-State Electron., vol. 71, pp. 93–100, May 2012, 10.1016/j.sse.2011.10.027.

[32] W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C., "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 730-736, Apr. 2001, doi: 10.1109/16.915707.

[33] N. Rodriguez, C. Navarro, F. Andrieu, O. Faynot, F. Gamiz, and S. Cristoloveanu, "Self-heating effects in ultrathin FD SOI transistors," *in Proc. IEEE SOI Conf.*, Tempe, AZ, USA, 2011, pp. 1–2, 10.1109/SOI.2011.6081685.

[34] C. Anghel, R. Gillon, and A. M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141–143, March 2004, 10.1109/LED.2003.821669.

Benito González was born in Las Palmas de Gran Canaria, Spain, in May 1968. He received his MSc degree in physics from the University of Santiago de Compostela, Spain, in 1992, and a PhD from the Universidad de Las Palmas de Gran Canaria, in 2001. He was Associate Professor at the Universidad de Las Palmas de Gran Canaria from 1996 to 2003 and has been a permanent Faculty Member ever since. He was the Director of the División de Tecnología Microelectrónica, Instituto Universitario de Microelectronica Aplicada, Universidad de Las Palmas de Gran Canaria, from 2005 to 2008, leading several research projects. His research interests are in the areas of semiconductor device physics, modeling, and simulation, with an emphasis on integrated passive devices for RF applications, varactors and inductors, and high-frequency, integrated circuits for telecommunications.

Raúl Rodríguez received an MSc degree in telecommunication engineering and a PhD degree from the University of Las Palmas de Gran Canaria, Spain, in 2012 and 2017, respectively. He is currently a Researcher with the Institute for Applied Microelectronics, University of Las Palmas de G.C. His current research interests include electrical and thermal characterization, numerical simulation and modeling of GaN-based devices, and Verilog-A implementation of device models for circuit simulation.

Antonio Lázaro was born in Lleida, Spain, in 1971. He received an MSc and a PhD degree in telecommunication engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1994 and 1998, respectively. He then joined the faculty of UPC, where he currently teaches a course on microwave circuits and antennas. Since July 2004, he has been a Full-Time Professor at the Department of Electronic Engineering, Universitat Rovira i Virgili (URV), Tarragona, Spain. His research interests are microwave device modeling, on-wafer noise measurements, monolithic microwave integrated circuits (MMICs), low phase noise oscillators, MEMS, RFID, UWB and microwave systems.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

Thermal Resistance Characterization for Multi-Finger SOI-MOSFETs

Benito González, Raúl Rodríguez, Antonio Lázaro, *Senior Member, IEEE*

***Abstract*— Thermal conductance in multi-finger SOI-MOSFETs is usually modeled at room temperature with a linear dependence on the total gate width, which is valid only when thermal coupling saturates. This paper presents a physically based model for calculating the thermal resistance of SOI-MOSFETs that accounts for progressive thermal coupling as the number of fingers increases and the substrate temperature. The model, extracted from a variety of gate geometries using the AC conductance method, correctly predicts the temperature rise in the device channel up to a substrate temperature of 150 ºC. Finally, this simple thermal resistance model, which is applicable to nanometer-scale transistors, can easily be added to circuit simulators.**

Index Terms—**SOI-MOSFET, thermal resistance, electrothermal characterization, substrate temperature, multi-finger model.**

I. Introduction

Miniaturization of metal oxide semiconductor field effect transistors (MOSFETs) has led to massive integration levels, where heat generation causes chip temperatures that can prevent the circuits' reliable operation, especially at nanometer length scales where the geometry in novel MOS devices tends to make heat removal more difficult.

Silicon-on-insulator (SOI) MOSFETs for the next generation of automotive, industrial and medical applications, will operate in the temperature range of –40 °C to 175 °C. When SOI technology is used, the very low thermal conductivity of the buried oxide layer (BOX in Fig. 1) significantly impedes heat transfer toward the substrate, particularly for thicknesses greater than 100 nm [1]. Additionally, confined dimensions can still augment self-heating [2], as the thermal conductivity of internal thin films is much lower than the corresponding bulk value [3-7]. In consequence, heat dissipation is sensitive to external

This work was supported by the Spanish MEC under Project GREENSENSE–TEC2015-67883-R.

B. González and R. Rodríguez are at the Institute for Applied Microelectronics, Universidad de Las Palmas de Gran Canaria, Campus Universitario de Tafira, Las Palmas, CO 35017 Spain (e-mail: benito@iuma.ulpgc.es and rrodriguez@iuma.ulpgc.es).

A. Lázaro is at the Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Escola Tècnica Superior d'Enginyeria, Av. Dels Països Catalans 26, Tarragona, CO 43007 Spain (e-mail: antonioramon.lazaro@urv.cat).

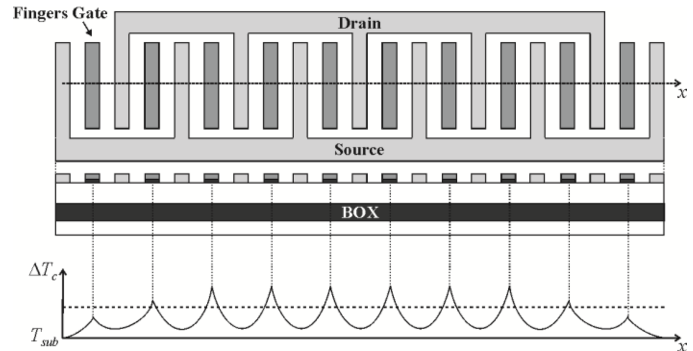


Fig. 1. Multi-finger device thermal coupling: Top view of transistor and schematic representation of the typical temperature rise in the channel, along the heat source in *x* direction.

contacts and gate geometry design, which must be optimized to efficiently reduce overheating in device performance [1][8][9].

Several precise techniques have been developed to measure thermal resistance in FETs. They are based on the AC conductance method [10][11], pulsed characteristics [12][13], IR and Raman thermographs [14], or even by extraction of a traps activation energy [15]. However, more progress is still needed to effectively model the thermal characteristics in SOI-MOSFETs, due to the thermal coupling that takes place in devices with nano-scale dimensions [1][2]. It can even lead to negative output conductance in low-frequency regimes [12].

The microelectronics community has made remarkable efforts towards the development of thermal models for MOSFETs [1][2][16-18]. Although detailed thermal models are desirable in order to achieve an exhaustive physical description [1][18], simplification is mandatory when dealing with compact models, such as BSIMSOI [19][20], for circuit simulation purposes. Thus, the thermal conductance in SOI-MOSFETs is usually modeled with a linear dependence on the gate width [21], without taking into consideration the number of fingers (no matter which gate configuration is used, the device's thermal resistance is estimated through the gate width), which is valid only when the thermal coupling is saturated. That is, when internal fingers determine the transistor temperature due to overheating [2][22][23]. For example, Fig. 1 shows a schematic distribution of the typical temperature rise in the channel of multi-finger devices, similar to that obtained using three-dimensional thermal TCAD simulations [22], where the thermal coupling between the gate

fingers increases the measured average temperature ΔT_c (dashed line).

Regarding variation in thermal resistance with gate length, SOI-MOSFETs' thermal resistance increases with reductions in channel length in the micrometer range (when BOX is thin enough). However, this dependence becomes weak in the cases of very long and short channel devices [20], as heat is mainly dissipated through the substrate (with the thermal resistance being evaluated as in [24]) and terminal contacts (as contacts do not scale with gate length), respectively. According to the International Technology Roadmap for Semiconductors (ITRSs) [25], and given that the BOX layer in the SOI-MOSFETs we investigated was thick enough to avoid heat dissipation through the substrate, this work does not consider variation in thermal resistance with gate length.

In this paper, we propose a simple model for circuit simulators for the thermal resistance of SOI-MOSFETs, accounting for the gradual thermal coupling when the number of fingers increases and including the substrate temperature dependence. The approach could be applied to higher drain current devices, which support higher operating temperatures, such as III-V devices and, particularly, GaN-based transistors (HEMTs) for high-power RF applications [26].

Thus, the SOI-MOSFETs under consideration, by varying the gate geometry, are presented in Section II. The experimental set-up for electrothermal characterization is described in Section III. Section IV devotes to thermal resistance characterization, extraction and modelling, and discusses the results. Finally, the conclusions are summarized in Section V.

II. Fabricated Devices

In order to validate the proposed model, eight partially depleted SOI N-channel MOSFETs, body tied to prevent the floating-body effect, were studied. The devices, which gate length was 180 nm, were built using XT018 0.18µm HV SOI-CMOS technology (by XFAB) within an 8-inch p-type SOI wafer process.

To this end, different multi-finger devices were designed, composed of 5, 10, 20, and 30 parallel fingers (N_f) (to exhibit considerable self-heating), each finger being 2 µm wide (W_f). Therefore, the total gate width ($W = N_f W_f$) was 10, 20, 40, and 60 µm, respectively. Identical gate widths were used to build four single-finger devices (to minimize self-heating), for comparison.

The devices were embedded in ground–signal–ground (GSG) on-wafer test structures, with co-planar waveguide access pads and grounded guard rings, to enable high frequency measurements [12][27]. For every transistor, three additional structures (single-open, single-short, and thru) were designed to perform the subsequent de-embedding technique [28], based on the four steps in [29], in order to eliminate the parasitic effects introduced by pads and the guard ring.

III. Experimental set-up

On-wafer measurements were performed with a CASCADE-Summit 9000 probe station. DC measurements were obtained using an Agilent B1500A Semiconductor Analyzer and the substrate temperature, T_{sub} (30 °C to 150 °C, in 20 °C increments, to avoid damaging or degrading the performance of the device under test –DUT– through excessive threshold voltage displacement) was set through a thermal chuck.

The scattering parameters (S-parameters) were measured from 50 MHz to 1 GHz at the substrate temperatures indicated, using the Agilent 8720ES Vector Network Analyzer (with internal bias tees) and Cascade GSG microprobes as shown in Fig. 2(a), using the Agilent B1500A Semiconductor Analyzer for biasing. In order to calibrate the measurement system, the short-open-load-through method was implemented in a previous step.

For pulsed measurements, see Fig. 2(b), an Agilent HP8133 signal generator applied a pulse to the gate of the SOI-MOSFETs ($V_{g\text{-}pulse}$), with the pulse base being set at a level, 0 V, where the device is off; a PSPL5370 pick-off tee was used in the gate to allow non-intrusive monitoring of the gate pulse voltage, as in [27]. An Agilent HP54754 digitizing oscilloscope recorded the voltage pulse of the drain ($V_{d\text{-}pulse}$) through a bias tee, [30]. The bias tee has two roles in this set-up: it applies DC signals to the device (drain-to-source

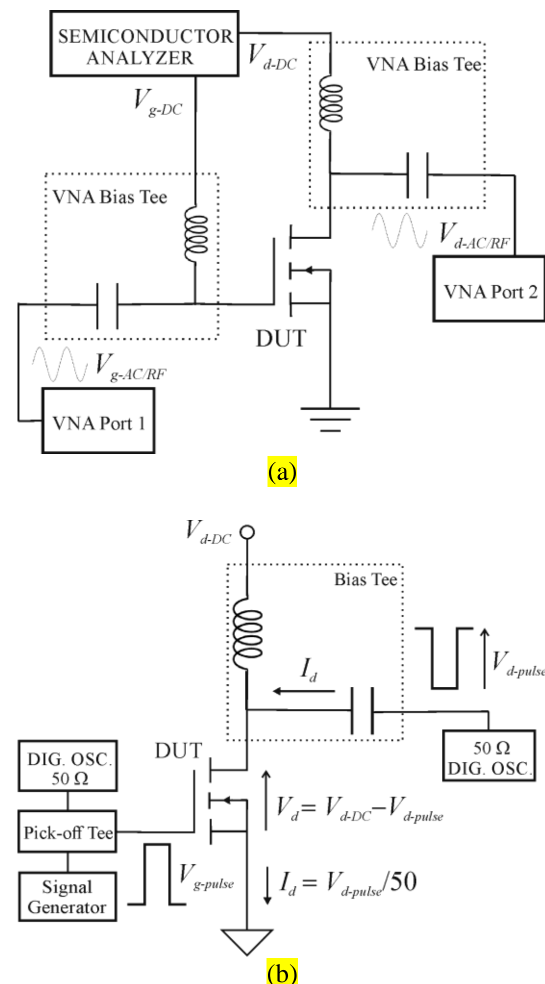
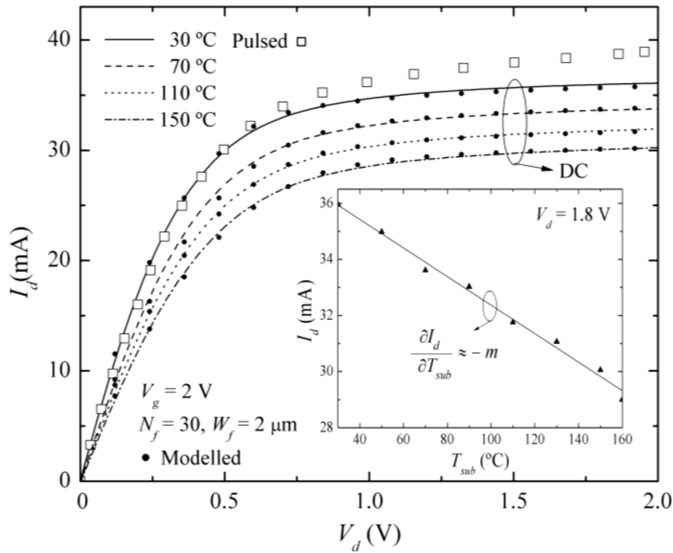
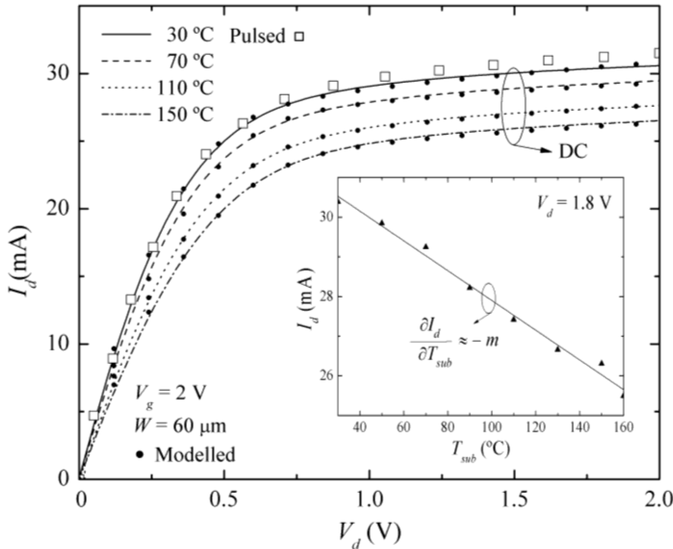


Fig. 2. Schematic of the measurement system: (a) AC/RF and (b) pulsed.



(a)



(b)

Fig. 3. Measured (lines) and modeled (circles) DC output characteristics at different substrate temperatures for (a) a multi-finger SOI-MOSFET (where N_f = 30 and W_f = 2 µm) and (b) a single-finger transistor (with W = 60 µm), and corresponding pulsed output characteristics at 30 °C (open squares); V_g = 2 V. The inset plot shows the resulting linear temperature dependence of the drain current with the substrate temperature, for V_d = 1.8 V.

voltage $V_{d\text{-}DC}$) whilst isolating the power supply from pulsed signals, and it allows pulsed signals to pass through the bias tee capacitor. Thus when the gate switches from 0 V to $V_{g\text{-}pulse}$, the (I_d, V_d) value switches from (0, $V_{d\text{-}DC}$) to ($V_{d\text{-}pulse}$ /50, $V_{d\text{-}DC} - V_{d\text{-}pulse}$). Output characteristics can be generated by varying $V_{d\text{-}DC}$. Finally, pulses 50 ns wide with a 0.01% duty cycle were used to avoid self-heating [12].

IV. Thermal Resistance Characterization

Self-heating effects were primarily demonstrated in the fabricated SOI-MOSFETs, by measuring their output characteristics using nanosecond pulses, as previously indicated. The corresponding results for the 30-fingers and single-finger transistors with the same total gate width (60 µm), a substrate temperature of 30 °C and a gate bias voltage of 2 V (to enhance self-heating effects) are presented (open squares) in Fig. 3(a) and 3(b) respectively, with DC measurements (solid lines) for comparison. It should be noted that in the saturation region the current increment cannot be obviated when self-heating is prevented (by using pulsed measurements), particularly in the case of the multi-finger device, where self-heating effects are more marked and the drain current greater, due to lower contact resistance at the source/drain terminals.

Therefore, thermal resistance characterization is mandatory in SOI technology. For this purpose, and because self-heating assessed by the pulsed technique might be underestimated [12], the AC conductance method is used as follows.

A. Extraction

The thermal resistance, R_{th}, is obtained for substrate temperatures up to 150 °C by applying the AC conductance technique [10][12] as

$$R_{th} = \frac{g_{ddo} - g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT} + V_g g_{gdT} + I_d\right)} \tag{1}$$

where g_{ddo} and g_{ddT} are the conductance, g_{dd}, at low frequency (with dynamic self-heating present) and at high frequency (with dynamic self-heating removed), respectively, and g_{gdT} is $g_{gd} = \partial I_d/\partial V_{gd}$ without dynamic self-heating, which are derived from corresponding S parameters [12]. The rest of the parameters (g_{ddo}, which is approximated by the DC output conductance as source and drain access resistances are very low, I_d, and $\partial I_d/\partial T_{sub}$) are obtained from output characteristics at different substrate temperatures (lines and inset plot in Fig. 3(a) and 3(b)).

In SOI-MOSFETs, when dynamic self-heating vanishes g_{dd} plateaus at around 100 MHz [11][12][31][32]. Then, it is observed that $V_g g_{gdT} \ll V_d g_{ddT}$ and the thermal resistance can be approximated by

$$R_{th} \approx \frac{g_{ddo} - g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT} + I_d\right)} \tag{2}$$

The measured g_{dd} frequency response for a substrate temperature of 30 ºC (in a saturation regime where V_d = 1.8 V and V_g = 2 V, to enhance self-heating effects) is represented by lines in Fig. 4(a) and 4(b) for multi-finger and single-finger transistors, respectively. Similar results are obtained for the rest of the temperatures.

The increase in output conductance over a wide frequency range is due to substrate-related effects (majority carriers) at frequencies of some hundreds of megahertz, and gate resistance in the gigahertz range [11]. Inset plots show that conductance remained constant between 150 MHz and 200 MHz, where average g_{ddT} can be measured to be used in (2).

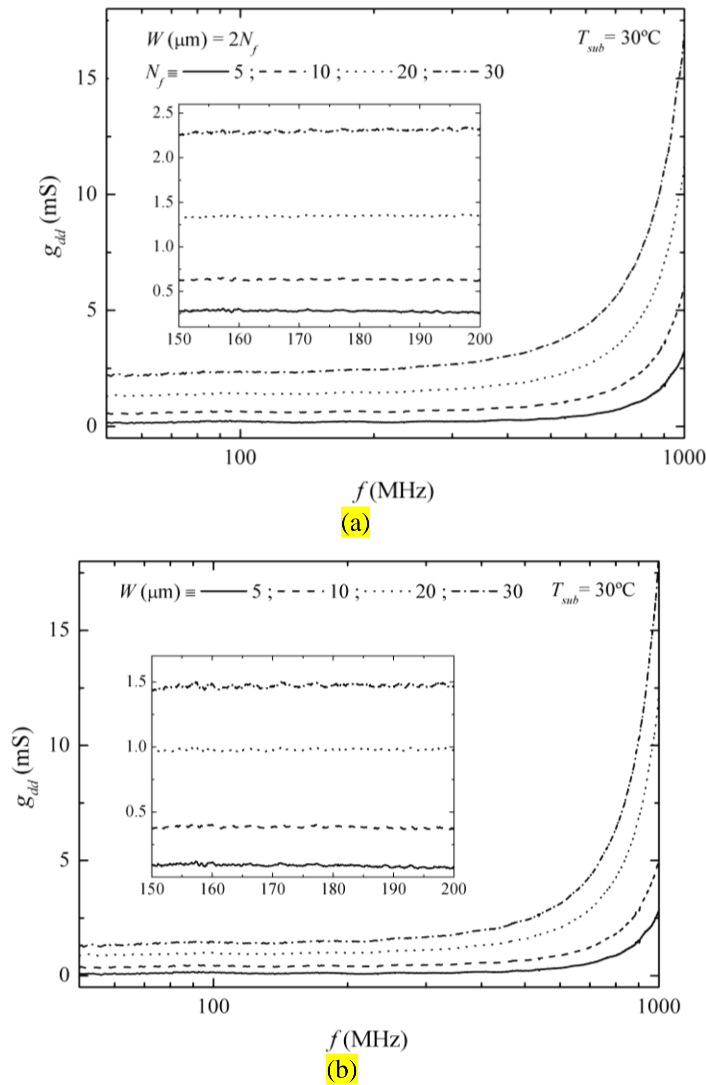


Fig. 4. Output conductance frequency response at 30 °C for (a) multi-finger transistors, and (b) single-finger transistors; V_g = 2 V, V_d = 1.8 V. Inset plots show the conductance plateau and the corresponding frequency range, where average g_{ddT} can be evaluated.

B. The model

The measured thermal resistance for the transistors, at a substrate temperature of 30 ºC, depends on the gate width, W, as indicated in Fig. 5, left axis; open and closed symbols represent single-finger and multi-finger devices, respectively. Similarly, the corresponding measured thermal conductance is represented on the right axis.

As mentioned previously, thermal resistance in SOI-MOSFETs is strongly dependent on technology and needs to be characterized experimentally for each one, making comparison of normalized thermal resistances ($R_{th}\times W$) a difficult task. Nevertheless, in this work the measured thermal resistance of single-finger devices was of the same order of magnitude as that of SOI-MOSFETs in [20] [32] [33], when normalized. Moreover, similar normalized thermal resistances were measured for multi-finger transistors in [11] for FinFETs.

Note that for the single-finger SOI-MOSFETs under

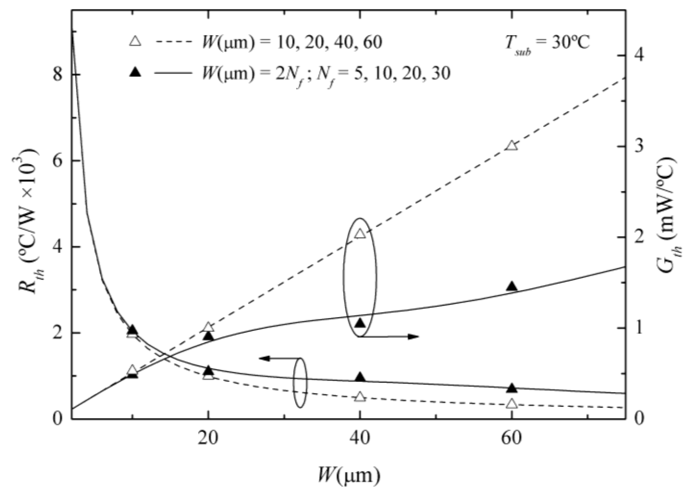


Fig. 5. Comparison of the thermal resistance (left axis) and conductance (right axis), as a function of gate width, extracted and modeled for multi-finger transistors (with solid symbols and solid line, respectively), and single-finger transistors (with open symbols and dashed line, respectively); T_{sub} = 30 ºC.

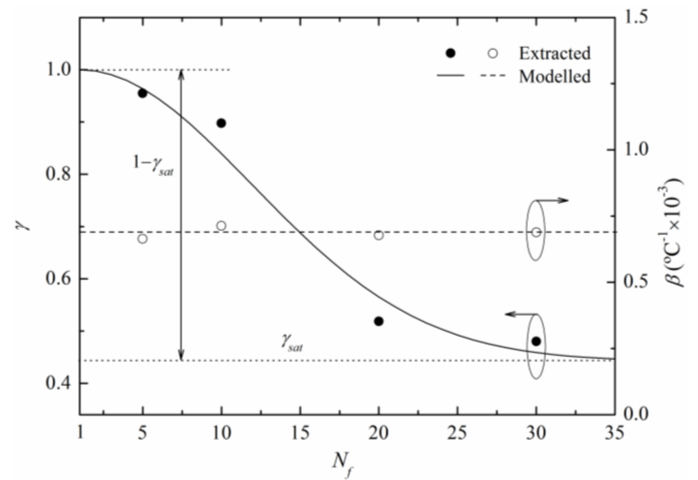


Fig. 6. Extracted (scattered), and modeled (line) finger width coefficient (left axis) and temperature coefficient (right axis), as a function of the number of fingers.

investigation, the measured thermal conductance, G_{th} = $1/R_{th}$, has a linear dependence on the gate width. Thus, it can usually be modeled as $G_{th} = (\alpha + W)/R_{tho}$ [21], where $\alpha = 0.19$ µm and R_{tho} = 2×10^4 ºC-µm/W, which are technologically dependent fitting parameters. The modeled thermal conductance and the corresponding thermal resistance are plotted with dashed lines in Fig. 5, showing a good agreement with measured data. Conversely, in multi-finger transistors, thermal coupling increases as the number of fingers, N_f, increases; this is made evident through the non-linear dependency of the measured thermal conductance on the gate width. In this case, the G_{th} augmentation with W diminishes as the number of fingers increases, with a linear dependence that is estabilished, because thermal coupling saturates, when the number of fingers is high enough ($N_f \gg 10$), as in [21][23].

The linear thermal conductance model for a single-finger transistor at 30 ºC can be extended to multi-finger devices, defining an effective finger width, $W_{f\text{-}eff}$, as

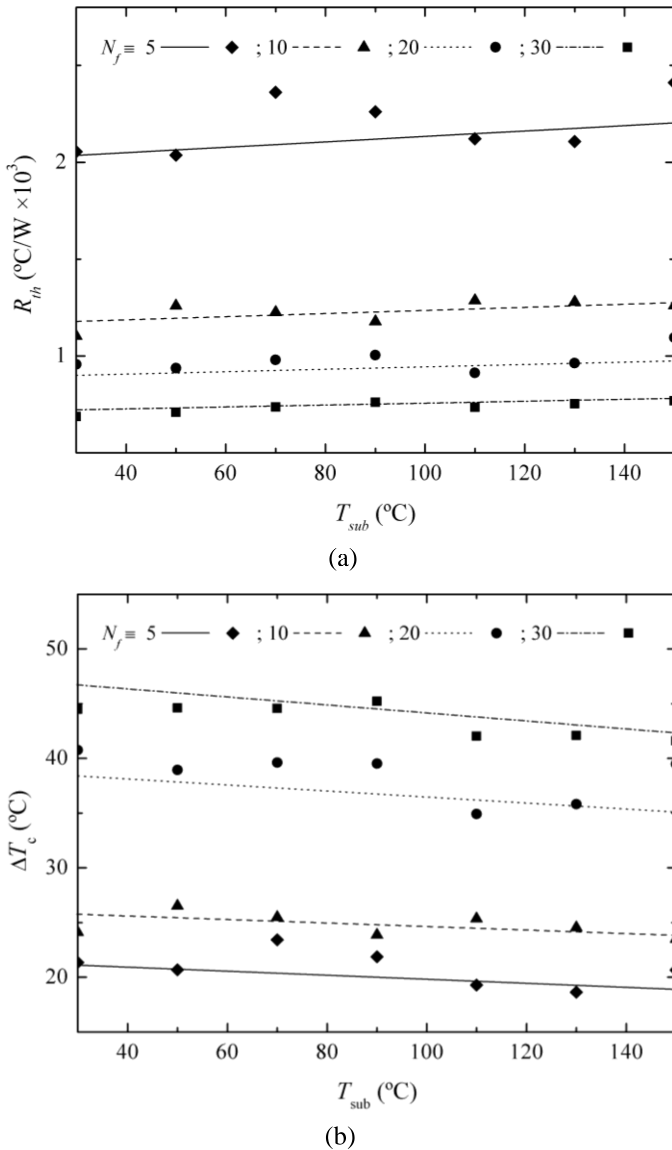


Fig. 7. Thermal resistance (a) and temperature rise in the channel (b), as a function of the substrate temperature, extracted from measurements (scattered) and modeled (lines) for multi-finger devices; V_g = 2 V, V_d = 1.8 V.

$$\frac{1}{R_{th\text{-}30ºC}} \approx \frac{\alpha + N_f\, W_{f\text{-}eff}}{R_{tho}}, \tag{3}$$

where the effective finger width accounts for the thermal coupling, $W_{f\text{-}eff} = \gamma W_f\,(\gamma < 1)$.

The finger width coefficient, γ, is extracted from the measured data using (3) and depends on the number of fingers as shown in Fig. 6 (left axis, with symbols). It can be modeled using a Gaussian function (with solid line) as:

$$\gamma = \gamma_{sat} + (1-\gamma_{sat})\mathrm{e}^{-\frac{(N_f-1)^2}{2\sigma^2}} \tag{4}$$

where γ_{sat} = 0.44; this being the reduction coefficient when thermal coupling saturates ($N_f \rightarrow \infty$), and σ = 10.9 is the standard deviation. Both fitting parameters are technologically dependent. Thus, a good agreement between modeled and extracted data for γ in multi-finger SOI-MOSFETs is achieved, as well as for G_{th} and R_{th}, with modeled data being represented by the solid line in Fig. 5. Note that for N_f = 1 (γ = 1) the thermal resistance predicted tends to be the same as that for a single-finger transistor 2 µm wide (i.e. the finger width).

Once thermal resistance has been characterized at 30 ºC, the substrate temperature incidence is analyzed. It was observed that the thermal resistance linearly increases with the substrate temperature, as Fig. 7(a) shows for multi-finger devices (with symbols), which can be modeled as in [34].

$$R_{th} \approx R_{th\text{-}30ºC}(1+\beta\Delta T_{sub}) \tag{5}$$

where $R_{th\text{-}30ºC}$ is given by (3), ΔT_{sub} is the substrate temperature increment, T_{sub} – 30 ºC, and the temperature coefficient β is a technologically dependent fitting parameter, which is represented in Fig. 6 (right axis, with symbols). Practically no variation in temperature coefficient is observed for a different number of fingers, and an average value (the dashed line), β = 7×10^{-4} (ºC^{-1}), which is comparable to that found in [4] with SOI technology, is enough to model the substrate temperature dependence of the thermal resistance for any device. Fig. 7(a) shows the resulting thermal resistance modeled for multi-finger SOI-MOSFETs (with lines), with a maximum relative error of 10% with respect to measured data at any substrate temperature. Similar results are obtained for single-finger SOI-MOSFETs.

Finally, the temperature rise in the device channel above substrate temperature, $\Delta T_c = T_c - T_{sub}$, is obtained as $R_{th}V_dI_d$ in the saturation regime (with V_d = 1.8 V and V_g = 2 V, to enhance self-heating effects). For single-finger transistors, ΔT_c remains almost constant at approximately 19 ºC, for any substrate temperature. In the case of multi-finger devices, as expected, ΔT_c strongly depends on the number of fingers (by thermal coupling), as Fig. 7(b) indicates for measured data (with symbols). Furthermore, as substrate temperature rises, a slight decrease in ΔT_c is observed, its dependence diminishing as the number of fingers reduces. In case of the multi-finger SOI-MOSFET with 30 parallel fingers (i.e. the worst case), the channel temperature, $T_c = T_{sub} + \Delta T_c$, reaches around 190 °C (on average, along the channel) at a substrate temperature of 150 °C, which is close to the typical maximum operating temperature (200 °C) for complementary metal-oxide semiconductor (CMOS) logic.

When accounting for (5) and the linear temperature dependence of the drain current, $I_d \approx I_{d\text{-}30°C} - m\cdot\Delta T_{sub}$ (see inset plot in Fig. 3(a) and 3(b)), the resulting model (lines in Fig. 7(b)) predicts the measured temperature rise in the channel, with the same maximum relative error as obtained in the case of thermal resistance, 10%.

Additionally, electro-thermal simulations were performed with BSIMSOI (version 3.1) using the thermal-electrical analogy. BSIMSOI models DC self-heating by introducing an

internal temperature node into the device. This node is connected to ground through the thermal resistance, which is given by (5), and the nodal "voltage" is actually the device temperature when the current flowing through the thermal resistance equals the electrical power dissipated in the device, V_dI_d. Modeled output characteristics for 60 µm-wide multi-finger and single-finger SOI-MOSFETs at different substrate temperatures (with V_g = 2 V) are presented (closed circles) in Fig. 3(a) and 3(b) respectively, showing a good agreement with the corresponding DC measurements (lines).

Lastly, thermal coupling analysis also demands the extraction of thermal capacitance in order to determine the thermal cross talk/temperature rise and thermal time constant; this will the object of future work.

V. Conclusions

A thermal resistance model for SOI-MOSFETs, accounting for the multi-finger thermal coupling and the substrate temperature, has been presented. The model, incorporating the number of fingers, predicts device overheating for substrate temperatures up to 150 ºC, when the temperature rise in the channel ascends to 45ºC with maximum thermal coupling. Furthermore, as substrate temperature increases the temperature rise in the channel slightly diminishes, dependence vanishing as the thermal coupling is reduced. Finally, this modelling approach for thermal resistance can easily be added to other well-established models in circuit simulators.

References

[1] M. Shrivastava, M. Agrawal, S. Mahajan, H. Gossner, T. Schulz, D. K. Sharma, and V. R. Rao, "Physical insight toward heat transport and an improved electro-thermal modeling framework for FinFET architectures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1353–1363, May 2012, 10.1109/TED.2012.2188296.

[2] B. Swahn and S. Hassoun, "Electro-thermal analysis of multi-fin devices," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol.16, no. 7, pp. 816–829, July 2008, 10.1109/TVLSI.2008.2000455.

[3] M. von Arx, O. Paul, and H. Baltes, "Process-dependent thin-film thermal conductivities for thermal CMOS MEMS," *J. Microelectromech. Syst.*, vol. 9, no. 1, pp. 136–145, Jan. 2000, 10.1109/84.825788.

[4] J. B. Roldán, B. González, B. Iñiguez, A. M. Roldán, A. Lázaro, and A. Cerdeira, "In-depth analysis and modelling of self-heating effects in nanometric DGMOS-FETs," *Solid-State Electron.*, vol. 79, pp. 179–184, Jan. 2013, 10.1016/j.sse.2012.07.017.

[5] S. M. Lee and D. G. Cahill, "Heat transport in thin dielectric films," *J. Appl. Phys.*, vol. 81, no. 6, pp. 2590–2595, Mar. 1997, 10.1063/1.363923.

[6] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *in Proc. IEEE IEDM Tech. Dig.*, Washington, DC, USA, 1999, pp. 67–70, 10.1109/IEDM.1999.823848.

[7] J. F. Shackelford and W. Alexander, "Thermal properties of materials," in *Materials Science and Engineering Handbook*, 3rd ed. New York, NY, USA: CRC Press LLC, 2001, pp. 409–460.

[8] D. Ha, H. Takeuchi, Y. K. Choi, and T. J. King, "Molybdenum gate technology for ultrathin-body MOSFETs and FinFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 1989–1996, Dec. 2004, 10.1109/TED.2004.839752.

[9] L. S. Yojo, R. C. Rangel, K. R. A. Sasaki, and J. A. Martino, "Is there a zero temperature bias point (ZTC) on back enhanced (BE) SOI MOSFET?," *in Proc. IEEE S3S Conf.*, San Francisco, CA, USA, 2017, pp. 1–3, 10.1109/S3S.2017.8309258.

[10] N. Rinaldi, "Small-signal operation of semiconductor devices including selfheating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, 10.1109/16.902734.

[11] S. Makovejev, S. Olsen, and J.-P. Raskin, "RF extraction of self-heating effects in FinFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, 10.1109/TED.2011.2162333.

[12] S. Makovejev, S. H. Olsen, V. Kilchytska, and J. P. Raskin, "Time and frequency domain characterization of transistor self-heating," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1844–51, Jun. 2013, 10.1109/TED.2013.2259174.

[13] J. Joh, J. A. del Alamo, T. M. Chou, H. Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, Dec. 2009, 10.1109/TED.2009.2032614.

[14] M. H. H. Kuball and J. W. Pomeroy, "A review of Raman thermography for electronic and opto-electronic device measurement with submicron spatial and nanosecond temporal resolution," *IEEE Trans. Device Mater. Reliab.*, vol. 16, no. 4, pp. 667–684, Ap. 2016, 10.1109/TDMR.2016.2617458.

[15] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in GaN HEMTs-part II: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3182, Oct. 2013, 10.1109/TED.2013.2278290.

[16] J. S. Brodsky, R. M. Fox, D. T. Zweidinger, and S. Veeraraghavan, "A physics-based, dynamic thermal impedance model for SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 957–964, Jun 1997, 10.1109/16.585551.

[17] S. Hniki, G. Bertrand, S. Ortolland, M. Minondo, B. Rauber, C. Raynaud, A. Giry, O. Bon, H. Jaouen, and F. Morancho, "Thermal effects modeling of multi-fingered MOSFETs based on new specific test structures," *in Proc. IEEE ESSDERC*, Athens, Greece, 2009, pp. 296–299, 10.1109/ESSDERC.2009.5331544.

[18] F. Nasri, M. Fadhel, B. Aissa, and H. Belmabrouk, "Nonlinear electrothermal model for investigation of heat transfer process in a 22-nm FD-SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1461–1466, Ap. 2017, 10.1109/TED.2017.2666262.

[19] B. Hu, C. Wakayama, L. Zhou, and C. J. R. Shi, "Developing device models,", *IEEE Circuits and Devices Magazine*, vol. 21, no. 4, pp. 6–11, July-Aug. 2005, 10.1109/MCD.2005.1492712.

[20] P. Kushwaha, K. BalaKrishna, H. Agarwal, S. Khandelwal, J.-P. Duarte, C. Hu, and Y. S. Chauhan, "Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG," *Microelectron. J.*, vol. 56, pp. 171–176, Oct. 2016, 10.1016/j.mejo.2016.07.014.

[21] S. Lee, R. Wachnik, P. Hyde, L. Wagner, J. Johnson, A. Chou, A. Kumar, S. Narasimha, T. Standaert, B. Greene, T. Yamashita, J. Johnson, K. Balakrishnan, H. Bu, S. Springer, G. Freeman, W. Henson, and E. Nowak, "Experimental analysis and modeling of self heating effect in dielectric isolated planar and fin devices," *in Proc. IEEE Symp. on VLSI Technol.*, Kyoto, Japan, 2013, pp.T248–T249.

[22] M. Weiß, A. K. Sahoo, C. Raya, M. Santorelli, S. Fregonese, C. Maneux, and T. Zimmer, "Characterization of intra device mutual thermal coupling in multi finger SiGe:C HBTs," *in Proc. IEEE EDSSC*, Hong Kong, China, 2013, pp. 1–2, 10.1109/EDSSC.2013.6628109.

[23] B. González, J. B. Roldán, B. Iñiguez, A. Lázaro, and A. Cerdeira, "DC self-heating effects modelling in SOI and bulk FinFETs," *Microelectron. J.*, vol. 46, pp. 320–326, Ap. 2015, 10.1016/j.mejo.2015.02.003.

[24] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and modeling of self-heating in SOI nMOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 1, pp. 69-75, Jan. 1994, 10.1109/16.259622.

[25] International Technology Roadmap for Semiconductors; 2014. Available from: <http://www.itrs.net/reports.html>.

[26] R. Guggenheim and L. Rodes, "Roadmap review for cooling high-power GaN HEMT devices," *in Proc. IEEE COMCAS*, Tel-Aviv, Israel, 2017, pp. 1–6, 10.1109/COMCAS.2017.8244734.

[27] C. D. Young, Y. Zhao, D. Heh, R. Choi, B. H. Lee, and G. Bersuker, "Pulsed I_d–V_g methodology and its application to electron-trapping characterization and defect density profiling," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1322–1329, Jun. 2009, 10.1109/TED.2009.2019384.

[28] I. Gutiérrez, J. Meléndez, J. García, I. Adin, G. Bistue, and J. de No, "Reliability Verification in a Measurement System of Integrated Varactors for RF Applications," *IEEE Lat. Am. Trans.*, vol. 3, no. 4, pp. 15–20, Oct. 2005, 10.1109/TLA.2005.1642424.

[29] T. E. Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 734–740, Ap. 2000, 10.1109/16.830987.

[30] K. A. Jenkins, J. Y. C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997, 10.1109/16.641362.

[31] S. Makovejev, J.-P. Raskin, M. K. Md Arshad, D. Flandre, S. Olsen, F. Andrieu, and V. Kilchytska, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs," Solid-State Electron., vol. 71, pp. 93–100, May 2012, 10.1016/j.sse.2011.10.027.

[32] W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C., "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 730-736, Apr. 2001, doi: 10.1109/16.915707.

[33] N. Rodriguez, C. Navarro, F. Andrieu, O. Faynot, F. Gamiz, and S. Cristoloveanu, "Self-heating effects in ultrathin FD SOI transistors," *in Proc. IEEE SOI Conf.*, Tempe, AZ, USA, 2011, pp. 1–2, 10.1109/SOI.2011.6081685.

[34] C. Anghel, R. Gillon, and A. M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141–143, March 2004, 10.1109/LED.2003.821669.

Benito González was born in Las Palmas de Gran Canaria, Spain, in May 1968. He received his MSc degree in physics from the University of Santiago de Compostela, Spain, in 1992, and a PhD from the Universidad de Las Palmas de Gran Canaria, in 2001. He was Associate Professor at the Universidad de Las Palmas de Gran Canaria from 1996 to 2003 and has been a permanent Faculty Member ever since. He was the Director of the División de Tecnología Microelectrónica, Instituto Universitario de Microelectronica Aplicada, Universidad de Las Palmas de Gran Canaria, from 2005 to 2008, leading several research projects. His research interests are in the areas of semiconductor device physics, modeling, and simulation, with an emphasis on integrated passive devices for RF applications, varactors and inductors, and high-frequency, integrated circuits for telecommunications.

Raúl Rodríguez received an MSc degree in telecommunication engineering and a PhD degree from the University of Las Palmas de Gran Canaria, Spain, in 2012 and 2017, respectively. He is currently a Researcher with the Institute for Applied Microelectronics, University of Las Palmas de G.C. His current research interests include electrical and thermal characterization, numerical simulation and modeling of GaN-based devices, and Verilog-A implementation of device models for circuit simulation.

Antonio Lázaro was born in Lleida, Spain, in 1971. He received an MSc and a PhD degree in telecommunication engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1994 and 1998, respectively. He then joined the faculty of UPC, where he currently teaches a course on microwave circuits and antennas. Since July 2004, he has been a Full-Time Professor at the Department of Electronic Engineering, Universitat Rovira i Virgili (URV), Tarragona, Spain. His research interests are microwave device modeling, on-wafer noise measurements, monolithic microwave integrated circuits (MMICs), low phase noise oscillators, MEMS, RFID, UWB and microwave systems.

Response to reviewers' comments to Author

Reviewer: 1

Comments to the Author

a) Concerning I/V pulsed measurement, pulses are applied to both gate and drain terminals? In the case of applying pulses just to gate terminal, maintaining the drain to a given DC voltage, additional self-heating could be added, even considering 50 ns pulse width and a duty cycle of 0.01%; have the authors considered this?

In response to the reviewer's comment, we have added a schematic drawing of the measurement system that uses this technique (Fig. 2(b)) and additional text to Section III of the manuscript to clarify that no self-heating is added.
In essence, a pulse generator applies a pulse to the gate ($V_{g\text{-pulse}}$, with the pulse base being selected at a level where the device is off), and a digitizing oscilloscope records the voltage of the drain ($V_{d\text{-pulse}}$). The bias tee has two roles: It applies DC signals (drain-to-source voltage, $V_{d\text{-DC}}$) to the device whilst isolating the power supply from pulsed signals, and it allows pulsed signals to pass through the bias tee capacitor. Pulses are short enough (50 ns) to avoid not only current flowing through the bias tee inductor, when the device is on, but also self-heating. In any case, were residual overheating to occur, the duty cycle selected (0.01%, for a fixed pulse period fixed of 0.5 ms) is short enough that we can assume that the device would cool down between applications of gate pulses.
Thus when the gate switches from 0 V to $V_{g\text{-pulse}}$, the (I_d, V_d) value switches from (0, $V_{d\text{-DC}}$) to ($V_{d\text{-pulse}}$ /50, $V_{d\text{-DC}} - V_{d\text{-pulse}}$), and output characteristics can be generated by varying $V_{d\text{-DC}}$.

b) It would be of interest, for comparison purposes, to present for a single-finger device with a total gate width of 60 microns the same results as depicted in figure 2, for a Nf=30 finger device.

As the reviewer suggests, for comparison purposes, we now show the results for a single-finger device, with a total gate width of 60 µm in Fig. 3(b), and we have added additional text to Section IV. Note that for a single-finger device, as self-heating is alleviated, pulsed and DC measurements are closer to each other; however the current obtained is lower, due to superior contact resistance at the source and drain terminals.

c) Have the authors applied this approach to higher drain current devices operating at higher drain voltages where self-heating is more evident (showing negative conductance) .

In response to the reviewer's comment the following text has been incorporated:

- Section I: "The approach could be applied to higher drain current devices, which support higher operating temperatures, such as III-V devices and, particularly, GaN-based transistors (HEMTs) for high-power RF applications [26]."
- Section IV-B: "In case of the multi-finger SOI-MOSFET with 30 parallel fingers (i.e. the worst case), the channel temperature already reaches around 190 °C (on average, along the channel) for a substrate temperature of 150 °C, which is close to the typical maximum operating temperature (200 °C) for complementary metal-oxide semiconductor (CMOS) logic."

Reviewer: 2

Comments to the Author

The authors deal with an interesting issue since self-heating effects are of great importance for modeling and FET operation in current ICs. The model introduced is interesting and useful; however, there are a few questions that should be answered prior to publication in the IEEE TED.

a) The authors should clarify the thermal simulation details of the simulator they employ. The values of the thermal conductivities used for the different materials, etc.

Fig. 1, a top view of a transistor and schematic representation of the typical temperature rise in the channel, represents a typical schematic distribution, similar to those obtained through thermal TCAD simulations of multi-finger devices [22].
As no thermal simulation was performed during this work the numerical data have been removed from Fig. 1 to avoid misunderstanding, and the caption and text in Section I have been rewritten accordingly.

b) Although it is difficult to find experimental data to compare, at least the authors should comment on published results to discuss the qualitatively features of their model.

We have followed the reviewer's suggestion and incorporated the following comment into the paper in Section IV-B (after first paragraph):

"Thermal resistance in SOI-MOSFETs is strongly dependent on technology and needs to be characterized experimentally for each one, making comparison of normalized thermal resistances ($R_{th} \times W$) a difficult task. Nevertheless, in this work the measured thermal resistance of single-finger devices was of the same order of magnitude as that of SOI-MOSFETs in [20] [32] [33], when normalized. Moreover, similar normalized thermal resistances were measured for multi-finger transistors in [11] for FinFETs."

And the following comment in paragraph after Eq. (5):

"…, which is comparable to that found in [4] with SOI technology, is enough to ..."

c) A discussion on the possible effects on the model when scaling leads to the shortest gate lengths would be interesting.

We have followed the reviewer suggestion and incorporated the following comment into the paper in Section I:

"Regarding variation in thermal resistance with gate length, SOI-MOSFETs' thermal resistance increases with reductions in channel length in the micrometer range (when BOX is thin enough). However, this dependence becomes weak in the cases of very long and short channel devices [20], as heat is mainly dissipated through the substrate (with the thermal resistance being evaluated as in [24]) and terminal contacts (as contacts do not scale with gate length), respectively. According to the International Technology Roadmap for Semiconductors (ITRSs) [25], and given that the BOX layer in the SOI-MOSFETs we investigated was thick enough to avoid heat dissipation through the substrate, this work does not consider variation in thermal resistance with gate length."

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

Reviewer: 3

Comments to the Author

The manuscript by Gonzalez et. al. presents an experimental as well as computational model of thermal resistance in multifinger SOI MOSFETs. The work can be accepted provided the authors justify the queries below:

a) **The abstract is too short to make any conclusion. This should be made more precise. There has been a lot of thermal coupling work in the area of SOI-MOSFETs. Therefore, the motivation should be very strong, which is currently lacking.**

Based on the reviewer's comment the Abstract has been rewritten as follows:

"Thermal conductance in multi-finger SOI-MOSFETs is usually modeled at room temperature with a linear dependence on the total gate width, which is valid only when thermal coupling saturates. This paper presents a physically based model for calculating the thermal resistance of SOI-MOSFETs that accounts for progressive thermal coupling as the number of fingers increases and the substrate temperature. The model, extracted from a variety of gate geometries using the AC conductance method, correctly predicts the temperature rise in the device channel up to a substrate temperature of 150 °C. Finally, this simple thermal resistance model, which is applicable to nanometer-scale transistors, can easily be added to circuit simulators."

b) **The experimental method is briefly described. The authors should mention the details.**

To make the experimental method clearer we have added a schematic drawing of the measurement systems (Fig. 2(a) and 2(b)) and additional explanatory text to the manuscript in Section III.

c) **The authors did not show the maximum temperature that the current in the fingers can withstand.**

As the reviewer advised, the maximum temperature that the current in the fingers withstand has been indicated in Section IV-B (please, see also answer c) to reviewer 1):

d) **Thermal coupling analysis demands also the extraction of thermal capacitance in order to get the thermal cross talk/temperature rise and thermal time constant. The authors did not mention these.**

This is indeed an important task and will be the object of future work, as indicated at the end of Section IV-B:

"Lastly, thermal coupling analysis also demands the extraction of thermal capacitance in order to determine the thermal cross talk/temperature rise and thermal time constant; this will the object of future work."

<u>**Reviewer: 4**</u>

Comments to the Author

In this manuscript, the authors present an scalable and temperature dependent analytical approach to calculate the thermal resistance of SOI MOSFET and validate their model with measurement data. This is an important and good work and the manuscript is generally well-written.

a) **However, there are some major concern from the reviewer, that need to be addressed for the completeness of the work. How this thermal model could be implemented in the compact model. I would like to see the validation of the model and its scalability through compact model simulations compared to measurements.**

   In response to the reviewer's comment we performed compact model simulations using BSIMSOI and compared the results with the measurements shown in Fig. 3(a) and 3(b). The following comment has been incorporated into the text, before the last paragraph of Section IV-B:

   "Additionally, electro-thermal simulations were performed with BSIMSOI (version 3.1) using the thermal-electrical analogy. BSIMSOI models DC self-heating by introducing an internal temperature node into the device. This node is connected to ground through the thermal resistance, which is given by (5), and the nodal "voltage" is actually the device temperature when the current flowing through the thermal resistance equals the electrical power dissipated in the device, $V_d I_d$. Modeled output characteristics for 60 µm-wide multi-finger and single-finger SOI-MOSFETs at different substrate temperatures (with V_g = 2 V) are presented (closed circles) in Fig. 3(a) and 3(b) respectively, showing a good agreement with the corresponding DC measurements (lines)."

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

Reviewer: 5

Comments to the Author

I found the subject of the paper worth of discussion. The paper presents some interesting original results. However, I have couple major concerns which from my point of view do not allow the paper to be published as it is and major revision is mandatory prior publication.

a) MA1: Experimental extraction procedure. While gdd versus f approach for SH extraction is good, its application in this work is not correct.

- **Rth in such approach is related to the variation of gdd (delta gdd) in certain frequency range. As there are many different effects which can result in gd variation with frequency, the main point/weakness of the method is to define the frequency range of extraction in which gd variation can be purely attributed to the self-heating. From the paper it is not clear why the authors decided that at 175 MHz, the device is free from self-heating. We still have gdd increase at f>225MHz…?**

  To provide evidence of the increment in the output conductance at higher frequencies, *S* parameters were measured from 50 MHz to 1 GHz, and the corresponding output conductance values are represented in Fig. 4(a) and 4 (b). Accordingly, the following text has been incorporated in Section IV-A:

  "The increase in output conductance over a wide frequency range is due to substrate-related effects (majority carriers) at frequencies of some hundreds of megahertz, and gate resistance in the gigahertz range [11]. Inset plots show that conductance remained constant between 150 MHz and 200 MHz, where average g_{ddT} can be measured and to be used in (2)."

  The Fig. 4 caption has also been modified.

- **Next to that, the authors calculate delta gdd from two different sets of measurements: low frequency values are extracted from IdVd (i.e. dc) measurements and high-frequency ones come from S-parameters measurements. The fact that the authors use different set-ups will introduce an uncertainty and error (most probably bias-dependent). Then, in S-parameters extraction, de-embedding techniques were applied (to withdraw parasitic effects), whereas this is not the case for dc measurements. It would be worth to show complete gdd vs frequency curve in a wide frequency range in order to identify on it SH related variation of gd (and justify the choice) and then make Rth extraction based on these curve/measurements.**

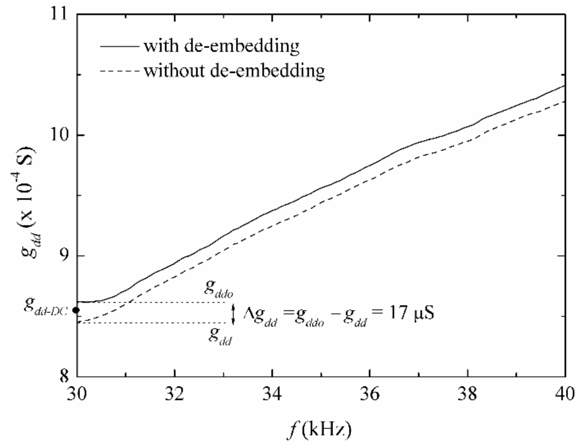
  50 MHz is the minimum operating frequency of the Agilent 8720ES Vector Network Analyzer. However, several authors have demonstrated that output conductance reaches a plateau when dynamic self-heating vanishes at around 100 MHz, using different SOI technologies and measurement techniques to obtain g_{dd}: FinFeTs in [11], partially depleted SOI MOSFETs in [12] and UTBB SOI MOSFETs in [31], with output conductance being measured with a vector network analyzer, and depleted and partially depleted SOI MOSFETs in [32], where output conductance was obtained with an impedance analyzer (all these references are now cited in Section IV-A).
  Additionally, we believe source/drain access resistances, R_s/R_d, are so low that they could be ignored in order to extract the output conductance at low frequencies, g_{ddo}, from DC characteristics, using the following equation:

$$g_{ddo} = \frac{g_{dd-DC}}{1 - g_m R_s - g_{dd}(R_s + R_d)}$$

  where $g_{dd\text{-}DC}$ and g_m are the extrinsic output conductance and transconductance, respectively. DC measurements were obtained using an Agilent B1500A Semiconductor Analyzer, RF coaxial cables with SMA connectors, and ACP-RF probes. Hence R_s and R_d must be similar to those obtained with the single-short structure, designed to perform the de-embedding technique, which was 0.4 Ω at 50 MHz (greater than expected for a DC regime). For example, the output conductance at low frequencies (with R_s ≈ Rd ≈

0.4 Ω) for the multi-finger transistor with 30 fingers, at room temperature, with $g_{dd\text{-}DC}$ = 0.85 mS and g_m = 29 mS at the biases for which the thermal resistances were evaluated (V_{gs} = 2 V, V_{ds} = 1.8 V) results $g_{ddo} = 1.01 \times g_{dd\text{-}DC} \approx g_{dd\text{-}DC}$.

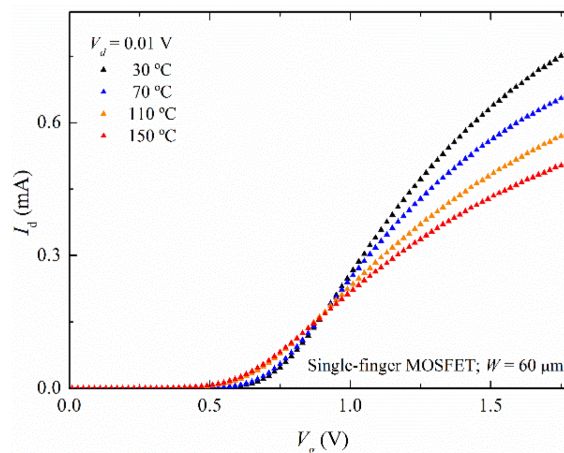
Furthermore, the output conductance at low frequencies has been measured using the Agilent FieldFox Handheld Analyzer N9913A, as next figure shows. The figure presents the total output conductance without dynamic self-heating, g_{dd}, and the corresponding conductance once the de-embedding process has been performed, g_{ddo}; the output conductance derived from DC characteristics, $g_{dd\text{-}DC}$, is also shown.



Note that all of them are similar, g_{ddo} and g_{dd} only differs 17 µS, and again $g_{ddo} \approx g_{dd\text{-}DC}$. Therefore, DC characteristics seem to an appropriate way to evaluate g_{ddo}, as indicated in the text of Section IV-A, so as in [11] (where Fig. 4 shows similar g_{ddo} and $g_{dd\text{-}DC}$ for FinFETs).

b) **MA2: Tsub dependence. First, it is not clear if S-parameters were measured at different temperatures. Temperature range of those measurements should be clearly indicated in the paper. Secondly, supposing that those measurements were done, the problem appears from the fact that the temperature rise in the channel (i.e. with respect to the substrate/chuck/ambience) of about 40°C for the Tsub=150°C is extracted from the dId/dT measurements upto 150°C (inset in fig.2). So, the range of dId/dT measurements is not sufficient to cover channel temperature. dId/dT should be measured at least upto 200°C (or even better 250°C).**

S-parameters were measured at various temperatures in order to model the resulting thermal resistance dependence (5) (this is now indicated in Section III).
On the other hand, all terms in (1), including dI_d/dT, were evaluated at the substrate temperature. XFAB recommends operating temperatures below 175 °C, but we limited our observations to substrate temperatures below 150 °C to avoid performance degradation, at least in the form of excessive threshold voltage displacement (now indicated in Section III), which occurs at temperatures as low as 150 °C, as the next figure shows. The figure presents transfers characteristics for a 60 µm-wide single-finger transistor, in linear regime, for the substrate temperatures considered (please, see also answer c) to reviewer 1).



1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

In any case in response to the reviewer's comment we evaluated dI_d/dT after increasing the substrate temperature to 160°C (see inset plot in Fig. 3(a) and 3(b)) and did not observe any significant variation as I_d-T_{sub} dependence remained linear.

c) **MA3: delta Tc versus Tsub dependence. In experiments, this dependence does not vanish with Nf , deltaTc/deltaTsub seems almost Nf independent from experimental data (e.g. delta Tc over 30-to-150°C range is ~2 for Nf=5, ~2 for Nf=20 and ~3 for Nf=30). However, model overestimates the slope of this dependence w.r.t experiments with Nf increase.**

We agree with the reviewer. What we should have said is that ΔT_c vs. T_{ub} dependence in multi-finger transistors diminishes as the number of fingers reduces (for single-finger ones ΔT_c is nearly constant with T_{sub}). This has now been corrected in the text of Section IV-B.
On the other hand, the model overestimates the slope of this dependence with respect to experiments with N_f increase. However, the channel temperature can still be predicted with a maximum relative error of 10% (also indicated in the text).
The temperature coefficient, β, accounting for variation in the number of fingers could be fitted in (5) to reduce the relative error even further, but as simplification is advisable when dealing with compact models, the model has been kept as simple as possible.
Compact model simulations using BSIMSOI, incorporating the modeled thermal resistance (5), have been performed and successfully compared to measurements in Fig. 3(a) and 3(b) (for more details, please see the response a) to the reviewer 4).

d) **MA4: Length dependence. I do not agree with authors' statement that Length dependence has a minor impact on self-heating and thus neglected. The authors refer to the papers that state just the opposite, showing L dependence of Rth ([20], [24]…)**

Regarding this issue, a better explanation has now been included in the text, in Section I, with updated references (also in the response c) to the reviewer 2). Please, see also Fig. 11 in [20].

And some "minor" remarks:

e) **MI1: What is the frequency range for S-parameters measurements?**

Frequency ranges from 50 MHz to 1 GHz for S-parameters measurements, as indicated now in Section III; 50 MHz is the minimum operating frequency for the Agilent 8720ES Vector Network Analyzer.

f) **MI1: Fig. 1 is not clear. What is the origin of deltaT(x) plot? Is it simulations ? measurements? or simply schematic representation of deltaT(x)?**

Fig. 1 is simply a schematic representation of $\Delta T_c(x)$. Please see answer a) to reviewer 2 for details.

g) **MI3: Mistake in symbols versus lines in Fig. 4.**
Thank you, we have corrected this error.

Some minor general changes:

- The figures numbering was updated after introducing Fig. 2(a), Fig. 2(b) and Fig. 3(c).
- References [24] and [25] were substituted by the new one [24].
- More references were incorporated: [25], [26], [31], [32] and [33].
- The references numbering was, therefore, updated.
- Reference [28] was updated.
- Number of papers in references, “no. -”, were included when available.
- Modelled has been substituted by modeled (American English style); not highlighted in the text.