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Hourglass-shaped impedance network based nonelectrolytic capacitors high step-up converter with low voltage stress

Guidong Zhang[1] | **Weichen Chen**[1] | **Samson S. Yu**[2] | **Abdelali El Aroudi**[3]

[1]Guangdong University of Technology, Guangzhou, China

[2]Deakin University, Victoria, Australia

[3]University Rovira i Virgili, Tarragona, Spain

Correspondence
Guidong Zhang, Guangdong University of Technology, Guangzhou, China.
Email: guidong.zhang@gdut.edu.cn

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Summary

In this study, a novel high-step-up converter is proposed with a new hourglass-shaped impedance network (HIN). Due to the short lifetime of electrolytic capacitors (ECs), the proposed converter uses nonelectrolytic capacitors (NECs), which however can realize all ECs' features. Besides, the proposed converter has low capacitor voltage stresses, ensuring it could be electrolytic-capacitors-free. With this feature, the proposed high step-up converter has smaller size, lighter weight, smaller parasitic resistance, and longer operation life than the conventional ones with ECs. In this paper, detailed operational principle and performance of the proposed converter are presented, to demonstrate its advanced features. Simulation and experimental studies are also carried out, which validate the feasibility and effectiveness of the proposed converter.

KEYWORDS

high step-up converters, hourglass impedance network, low capacitor voltage stresses, nonelectrolytic capacitors

1 | INTRODUCTION

The development of renewable energy can effectively mitigate a range of today's energy problems, such as greenhouse gas emissions and depletion of fossil fuels. Nonetheless, how to integrate the renewable energy into the power grid has emerged as another significant problem. For example, fuel cells and solar photovoltaic (PV) devices produce low voltages (lower than 50 V), which is too low to connect with the electric grid or supply residential loads. To solve this problem, a large number of DC-DC boost converters have been proposed.[1-5] The topologies of step-up converters can be divided in nonisolated and isolated,[6] noncoupled-inductor and coupled-inductor converters,[7] which have been extensively investigated in the past few decades.

The most simple step-up converter is the nonisolated and noncoupled-inductor converter. Initially, boost converters are cascaded to achieve a higher voltage gain.[8] But that voltage gain is limited and a huge current will flow through switch and inductor in the first stage due to the series-cascade structure. To avoid this problem, many specially designed topologies are applied in subsequent high step-up converters. A new high step-up converter with higher voltage gain than the traditional boost converter is proposed in Hwu et al., [9] which consists of a KY converter and a buck-boost converter. It utilizes fewer devices to achieve the same voltage gain by using switched-capacitors in Hu and Ioinovici,[10] and a family of similar converters have been developed. To design a higher voltage gain converter, a new quadratic boost converter is proposed in Yang et al.[11] Compared to the traditional quadratic boost converter, an additional capacitor-inductor-diode is employed to reduce the voltage stresses of switch and diodes. In Rosas-Caro et al., [12]

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a step-up converter is proposed using two parallel-connected input inductors, which can achieve a high voltage gain and a very low (almost zero) input current ripple. Another high step-up converter based on the quadratic boost converter is proposed in Pires et al., [13] whose superior performance includes a wide range of voltage gains to boost and equalize the low voltage of the fuel cells, which can be used to drive electric vehicles.

An easier high step-up converter design guideline is by cascading boost cells in series or in parallel.[14] A multilevel high step-up converter is proposed in Rosas-Caro et al., [15] which can realize a high voltage gain with several parallel boost cells. It consists of two capacitors and two diodes. Another multilevel high step-up converter in Zhu and Wang[16] boosts the voltage with several cascade boost cells, which consists of two capacitors, a diode and an inductor. High voltage gains can also be achieved by the converter in Zhu et al.[17] by replacing the boost inductor with a boost cell, and the voltage gain is extended by nesting boost cells. But cascading boost cells inevitably leads to higher voltage loss.

Different from the multilevel high step-up converter, coupled-inductor high step-up converters can achieve high voltage gains with higher efficiency.[18] A high step-up converter with a couple of interleaved coupled-inductors is proposed in Li and He.[19] The input current ripple of the converter is reduced by the interleaved coupled-inductors, and zero-voltage transition (ZVT) of the converter's switch is realized. To improve the efficiency of the converter in Zhao et al., [20] zero-current switching (ZCS) technology is used on its switch. ZCS and ZVT are two soft switching techniques widely used to improve the efficiency of converters.[21] Similar to Li and He,[19] the interleaved coupled-inductor converter has been investigated and developed in other studies[22,23] to reduce the input current ripple and the voltage stress of electronic components. Another coupled-inductor topology, named Y-source impedance network, is proposed in Siwakoti et al., [24] which can reduce the input current ripple. Because of its low input current ripple and high voltage gain characteristics, it can be used for distributed generation. To improve its performance, the Y-source impedance network is extended to the △-Y impedance network in Zhang et al.[25]

Combining the conventional topology with coupled inductors is a way to design better high step-up converters. In Saadat and Abbaszadeh,[26] the inductor of the traditional quadratic boost converter is replaced with a coupled-inductor to improve the voltage gain. A new boost cell with coupled-inductor in Schmitz et al.[27] is nested in conventional topology to build a new high step-up converter. An integrated coupled-inductor is applied in the high step-up converter proposed in Siwakoti and Blaabjerg.[28] Its voltage stress of the switch is reduced and the power density is improved. The high step-up converter with coupled-inductor has another advantage of being isolated between the energy source and load. The isolated high step-up converter always has the DC-AC-DC structure, and the coupled-inductor in the isolated high step-up converter acts like a boost transformer, bridging the energy source and the load.[29,30] The research in Chen et al.[31] elaborates on the ideas and derivation methods of the coupled-inductor boost converter.

However, the coupled-inductor is heavy and bulky and can cause current spikes. To solve the above problem, a novel high step-up converter based on a novel hourglass impedance network converter is proposed in this paper. The hourglass converter has a high voltage gain and low voltage stresses on the electronic components than the conventional high step-up converters. Moreover, the proposed HIN-based converter employs NECs, which reduces the size and weight of the converter. In the rest of the paper, the configuration and operation principle of the proposed hourglass network-based high step-up converters are presented in Section 2, followed by the analysis of the steady-state performance and comparison with other converters in Section 3. Parameters design is discussed in Section 4. Voltage loss analysis of the hourglass network converter is derived in Section 5. Simulation and experimental results are reported in Section 6. Finally, a conclusion is drawn in Section 7.

2 | CONFIGURATION AND OPERATION PRINCIPLE OF THE HIN-BASED CONVERTER

The topology of the HIN-based converter is shown in Figure 1, where the HIN consists of two inductors, two capacitors, two diodes and a switch, that is, L_1, L_2, C_1, C_2, D_1, D_2, and S_1. The remaining components of the converter are diode D_3, D_4, switch S_2, and two output capacitors C_3, C_4. Compared to conventional impedance network, the HIN has a lower capacitor voltage stress and higher voltage gain. It is worth noting that the current flows from inductors L_1 to L_2 through capacitors C_1 and C_2 during mode 1; and it flows back in mode 2.

To simplify the analysis of the operation principle, the following assumptions are made in this study:

(1) All components are ideal; and
(2) All capacitors are large enough that the voltage across each capacitor is considered constant during each subinterval.

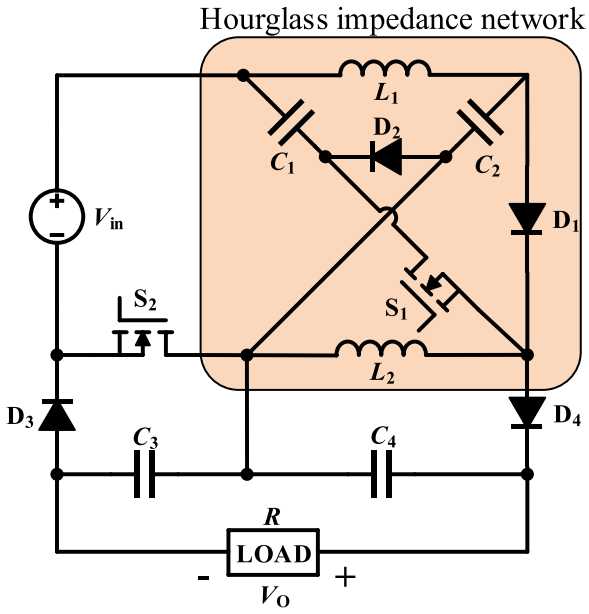

FIGURE 1 Configuration of the proposed hourglass impedance network based converter [Colour figure can be viewed at wileyonlinelibrary.com]

The HIN-based converter can operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), which is similar to the traditional boost converter and other impedance-network-based converters. However, because the CCM is usually preferred in many industrial applications to get higher efficiency, only operations in the CCM are presented for the proposed HIN-based converter in this paper. Based on the above assumptions, the operating process of the converter in a single switching period can be separated into two modes, that is, mode 1 (S_1 and S_2 are ON) and mode 2 (S_1 and S_2 are OFF). The equivalent circuits of the proposed converter in the two operating modes are shown in Figure 2A,B and key waveforms of the converter are given in Figure 3 to illustrate the time-domain operation. The two operating modes are described as follows,

Mode 1 $[0 \le \mathbf{t} \le \mathbf{t}_1]$: As shown in Figure 2A, switch S_1 and S_2 are turned ON, diode D_4 is in forward bias and diodes D_1, D_2 and D_3 are OFF because of reverse bias. Inductor L_1 is charged by the input voltage and capacitor C_2 through switch S_2 when its current i_{L_1} increases. Capacitor C_1 along with the input source through switch S_1 releases energy to inductor L_2 and capacitor C_4 when the current flowing through L_2 (i_{L_2}) increases. Capacitors C_3 and C_4 supply the load together. This mode lasts until switch S_1 and S_2 are turned OFF. State equations during this mode are as follows:

$$\begin{cases} L_1 \dfrac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = v_{\mathrm{in}} + v_{C_2}, \\ L_2 \dfrac{\mathrm{d}i_{L_2}}{\mathrm{d}t} = v_{\mathrm{in}} + v_{C_1} = v_{C_4}, \\ C_1 \dfrac{\mathrm{d}v_{C_1}}{\mathrm{d}t} = i_{L_1} - i_{\mathrm{in}}, \\ C_2 \dfrac{\mathrm{d}v_{C_2}}{\mathrm{d}t} = -i_{L_1}, \\ C_3 \dfrac{\mathrm{d}v_{C_3}}{\mathrm{d}t} = -i_{\mathrm{o}}, \\ C_4 \dfrac{\mathrm{d}v_{C_4}}{\mathrm{d}t} = i_{\mathrm{in}} - i_{L_1} - i_{L_2} - i_{\mathrm{o}}, \\ v_{\mathrm{o}} = v_{C_3} + v_{C_4}, \end{cases} \tag{1}$$

where v_{in} stands for the input voltage, v_{o} is the output voltage, i_{o} is the output current; v_{C_1}, v_{C_2}, v_{C_3} and v_{C_4} are the voltages of capacitor C_1, C_2, C_3 and C_4 respectively.

Mode 2 $[\mathbf{t}_1 < \mathbf{t} \le \mathbf{t}_2, t_2 = \mathbf{T}_{\mathrm{s}}]$: At t_1, switches S_1 and S_2 are turned OFF, and the operating mode of the converter changes to Mode 2. In this mode, all diodes are forward-biased except diode D_4. The energy stored in inductor L_1 is delivered to

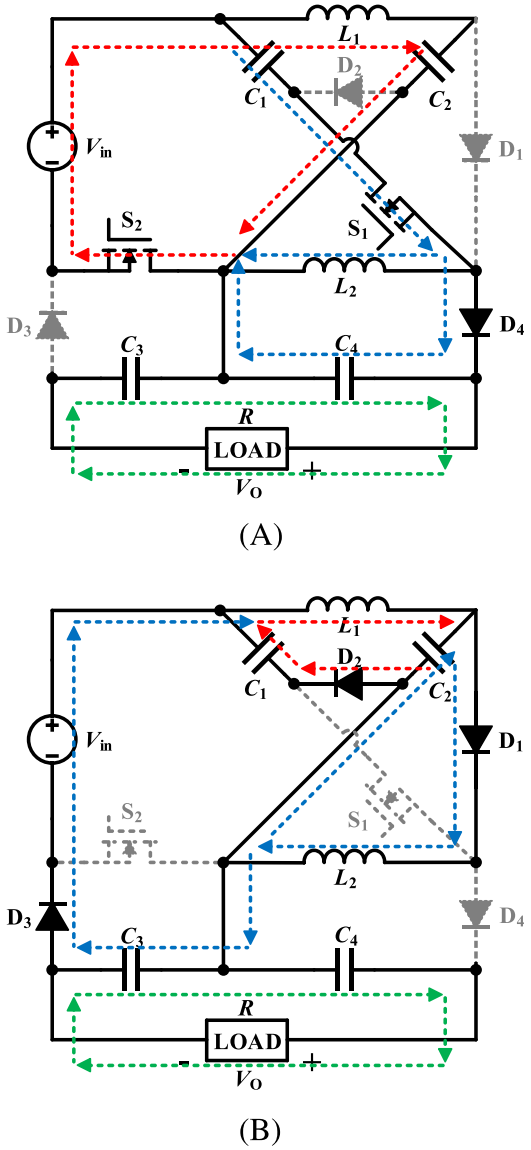

FIGURE 2 Equivalent circuits in different operation modes: (A) Mode 1 and (B) Mode 2 [Colour figure can be viewed at wileyonlinelibrary.com]

capacitor C_1 through diode D_2. Inductor current i_{L_1} decreases and the energy is stored in capacitor C_1. At the same time, the energy stored in inductor L_2 along with the energy produced by the input source is delivered to capacitors C_2 and C_3. Therefore, inductor current i_{L_2} decreases as shown in Figure 3. Capacitors C_3 and C_4 supply the load together. This mode lasts until the end of the switching period ($t = t_2$). State equations in this mode are shown as follows:

$$\begin{cases} L_1 \dfrac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = v_{C_2} - v_{C_1} = v_{\mathrm{in}} + v_{C_2} - v_{C_3}, \\ L_2 \dfrac{\mathrm{d}i_{L_2}}{\mathrm{d}t} = -v_{C_2}, \\ C_1 \dfrac{\mathrm{d}v_{C_1}}{\mathrm{d}t} = i_{L_1} - i_{\mathrm{in}}, \\ C_2 \dfrac{\mathrm{d}v_{C_2}}{\mathrm{d}t} = i_{L_2} - i_{L_1}, \\ C_3 \dfrac{\mathrm{d}v_{C_3}}{\mathrm{d}t} = i_{\mathrm{in}} - i_{\mathrm{o}}, \\ C_4 \dfrac{\mathrm{d}v_{C_4}}{\mathrm{d}t} = -i_{\mathrm{o}}, \\ v_{\mathrm{o}} = v_{C_3} + v_{C_4}. \end{cases} \tag{2}$$

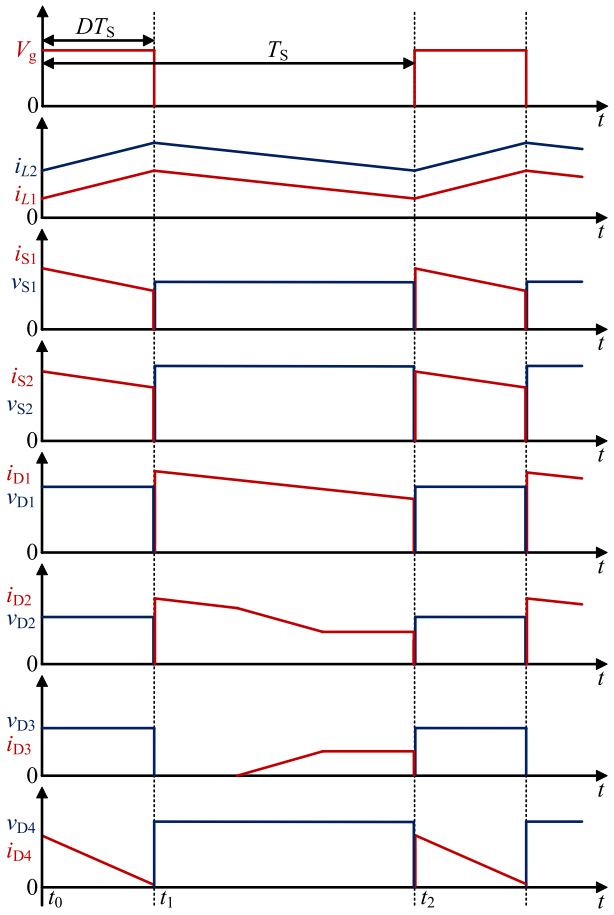

FIGURE 3 Key waveforms of the proposed HIN-based converter [Colour figure can be viewed at wileyonlinelibrary.com]

3 | PERFORMANCE ANALYSIS OF THE HIN-BASED CONVERTER

3.1 | Voltage conversion ratio

With small ripple approximation, and applying the voltage-second balance principle on the inductors L_1 and L_2, the following equations can be obtained:

$$\begin{cases} (V_{\text{in}} + V_{C_2})D + (V_{C_2} - V_{C_1})(1-D) = 0, \\ (V_{\text{in}} + V_{C_1})D - V_{C_2}(1-D) = 0, \\ V_{C_3} = V_{\text{in}} + V_{C_1}, \\ V_{C_4} = V_{\text{in}} + V_{C_1}, \end{cases} \tag{3}$$

where D is the steady-state duty cycle of switches S_1 and S_2.

Using (3), the capacitor voltages v_{C_1}, v_{C_2}, v_{C_3}, v_{C_4} and the output voltage V_{o} can be derived as

$$\begin{cases} V_{C_1} = \left(\dfrac{1-D}{D^2-3D+1} - 1\right) V_{\text{in}}, \\ V_{C_2} = \dfrac{D}{D^2-3D+1} V_{\text{in}}, \\ V_{C_3} = \dfrac{1-D}{D^2-3D+1} V_{\text{in}}, \\ V_{C_4} = \dfrac{1-D}{D^2-3D+1} V_{\text{in}}, \\ V_{\text{o}} = \dfrac{2(1-D)}{D^2-3D+1} V_{\text{in}}. \end{cases} \tag{4}$$

From (4), it can be found that the voltage stress of capacitors is far lower than the output voltage, with the highest capacitor voltage stress being half of the output voltage.

3.2 | Currents of the inductors

Assuming that the power losses are ignorable and that the output power is equal to input power. Using the voltage gain equation of the HIN converter, the relation between the input current (I_{in}) and output current (I_o) can be expressed as

$$I_{in} = \frac{2(1-D)}{D^2-3D+1} I_o. \tag{5}$$

Using (1), (2), (4), and (5) and applying ampere-second balance principle on the capacitors C_1 and C_2, the average values of the currents flowing through the inductors and amplitude of ripple in a single switching cycle can be derived as

$$\begin{cases} I_{avgL_1} = \dfrac{2(1-D)}{D^2-3D+1} I_o, \\ I_{avgL_2} = \dfrac{2}{D^2-3D+1} I_o, \\ \Delta i_{L_1} = \dfrac{V_{in} D(1-D)^2}{L_1 f_s (D^2-3D+1)}, \\ \Delta i_{L_2} = \dfrac{V_{in} D(1-D)}{L_2 f_s (D^2-3D+1)}, \end{cases} \tag{6}$$

where f_s is the switching frequency, I_{avgL_1} and I_{avgL_2} are the average currents of inductors L_1 and L_2 and Δi_{L_1} and Δi_{L_2} are the magnitudes of their ripples.

3.3 | Voltage and current stresses of the electronic devices

According to the analysis of the operation principle in Section 2 and Equation (4), the voltage stresses of semiconductors, namely V_{D_1}, V_{D_2}, V_{D_3}, V_{D_4}, V_{S_1} and V_{S_2}, can be expressed as

$$\begin{cases} V_{D_1} = \dfrac{1}{D^2-3D+1} V_{in}, \\ V_{D_2} = \dfrac{1-D}{D^2-3D+1} V_{in}, \\ V_{D_3} = \dfrac{1-D}{D^2-3D+1} V_{in}, \\ V_{D_4} = \dfrac{1}{D^2-3D+1} V_{in}, \\ V_{S_1} = \dfrac{D}{D^2-3D+1} V_{in}, \\ V_{S_2} = \dfrac{1-D}{D^2-3D+1} V_{in}. \end{cases} \tag{7}$$

By applying KCL in operation mode 2 and using (1), (2), (5), and (6), the average current of D_1, D_2 and D_3, namely, I_{avgD_1}, I_{avgD_2} and I_{avgD_3}, can be written as follows:

$$\begin{cases} I_{\text{avgD}_1} = \dfrac{2}{D^2-3D+1} I_{\text{o}}, \\ I_{\text{avgD}_2} = \dfrac{7-8D}{4(D^2-3D+1)} I_{\text{o}}, \\ I_{\text{avgD}_3} = \dfrac{1}{4(D^2-3D+1)} I_{\text{o}}, \\ I_{\text{avgD}_4} = \dfrac{2}{D} I_{\text{o}}, \\ I_{\text{avgS}_1} = \dfrac{2(1-D)^2}{D(D^2-3D+1)} I_{\text{o}}, \\ I_{\text{avgS}_2} = \dfrac{2(1-D)}{D(D^2-3D+1)} I_{\text{o}}. \end{cases} \tag{8}$$

Capacitor C_4 supplies load, and at the same time, capacitor C_1 along with the input source charge capacitor C_4. In other words, capacitors C_1, C_4 and the input source supply the load together during mode 1. Because of capacitor C_4 is charged by a capacitor instead of an inductor, the charging process of capacitor C_4 happens in two operation modes, which is the period of the switches being OFF. The charging circuit is shown in Figure 4. However, the parasitic resistance r effectively decreases the charging current between capacitors C_1 and C_4 (r is the sum of devices' parasitic resistance in Figure 4). Hence, it does not require a small inductor in the charging circuit for spike weakening. Based on these, the following equations can be derived:

$$\begin{cases} I_{\text{peakD}_4} = \dfrac{8V_{\text{in}}(1-D)}{DR(D^2-3D+1)}, \\ I_{\text{peakS}_1} = \dfrac{4V_{\text{in}}(1-D)(2D^2-5D+2)}{DR(D^2-3D+1)^2}, \\ I_{\text{peakS}_2} = \dfrac{4V_{\text{in}}(1-D)(D^2-4D+2)}{DR(D^2-3D+1)^2}, \end{cases} \tag{9}$$

where R is the load.

3.4 | Comparison results

As shown in Table 1, voltage gain, voltage stress on capacitor, voltage stress on switch, component counts, and efficiency are demonstrated. In Figure 5, voltage gain functions of converters in Table 1 are shown in terms of the duty cycle. For the proposed converter, it is noted that only a positive output voltage with d falling in $[0, 0.38)$ is depicted. The equivalent turns ratio of the coupled-inductor for the converter in Poorali and Adib[18] is set as $n_2 = 2$ and the number of boost cell for converter in Wu et al.[14] is set as $n_1 = 3$. From Figure 5, except the converters in the literature,[3,5] the voltage gain of the HIN converter is significantly higher than other converters when the duty cycle is around 0.3.

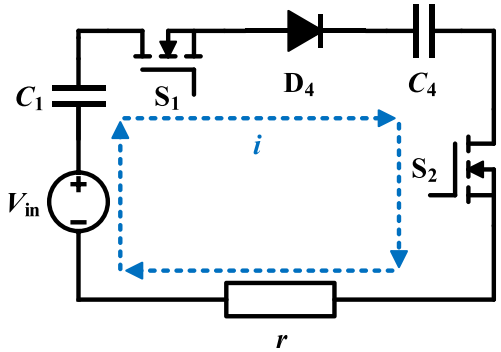

FIGURE 4 Charging circuit of capacitor C_4 [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Comparison of performance between hourglass converter and other converters

Reference	Voltage Gain	Voltage Stress on Capacitor	Voltage Stress on Switch	Component	Efficiency
3	$\frac{V_o}{V_{in}}=\frac{1}{1-4D}$	$V_{C_1}=V_{C_2}=2DV_o$ $V_{C_3}=V_o$	$V_{S_1}=V_{S_2}=V_o$	2 Switches 3 Diodes 2 Inductors 3 Capacitors	92.4%
11	$\frac{V_o}{V_{in}}=\frac{1+D}{(1-D)^2}$	$V_{C_1}=\frac{1-D}{1+D}V_o, V_{C_4}=V_o$ $V_{C_2}=V_{C_3}=\frac{V_o}{1+D}$	$V_S=\frac{V_o}{2-D}$	1 Switch 4 Diodes 3 Inductors 4 Capacitors	87.5%
4	$\frac{V_o}{V_{in}}=\frac{1}{(1-2D)}$	$V_{C_1}=\frac{1-2D}{1-D}V_o, V_{C_2}=\frac{D}{1-D}V_o$ $V_{C_o}=V_o$	$V_S=(1+D)V_o$	1 Switch 3 Diodes 3 Inductors 3 Capacitors	90%
14	$\frac{V_o}{V_{in}}=n_1$	$V_{C_1}=V_{C_2}=\ldots=V_{C_{2n_1-2}}=\frac{V_o}{n_1}$ $V_{C_1}=\frac{1-D}{1+n_2(1-D)}V_o$	$V_S=\frac{V_o}{n_1}$	2 Switches 2(n_1-1) Diodes 2(n_1-1) Capacitors 2 Switches	91.8%
18	$\frac{V_o}{V_{in}}=\frac{1+n_2(1-D)}{1-2D}$	$V_{C_2}=\frac{D}{1+n_2(1-D)}V_o$ $V_{C_{o1}}=\frac{1}{1+n_2(1-D)}V_o$ $V_{C_{o2}}=\frac{n_2(1-D)}{1+n_2(1-D)}V_o$	$V_S=\frac{V_o}{1+n_2(1-D)}$	2 Diodes 3 Inductors 4 Capacitors	93.6%
5	$\frac{V_o}{V_{in}}=\frac{1}{1-5D+2D^2}$	$V_{C_1}=2DV_o, V_{C_2}=(1-2D)V_o$ $V_{C_3}=V_{C_o}=V_o$	$V_{S_1}=(1-2D)V_o$ $V_{S_2}=V_o$	3 Switches 5 Diodes 2 Inductors 4 Capacitors	
The HIN Converter	$\frac{V_o}{V_{in}}=\frac{2(1-D)}{1-3D+D^2}$	$V_{C_1}=\frac{2D-D^2}{2(1-D)}V_o, V_{C_2}=\frac{D}{2(1-D)}V_o$ $V_{C_3}=V_{C_4}=\frac{V_o}{2}$	$V_{S_2}=\frac{D}{2(1-D)}V_o$ $V_{S_2}=\frac{V_o}{2}$	2 Switches 4 Diodes 2 Inductors 4 Capacitors	92.5%

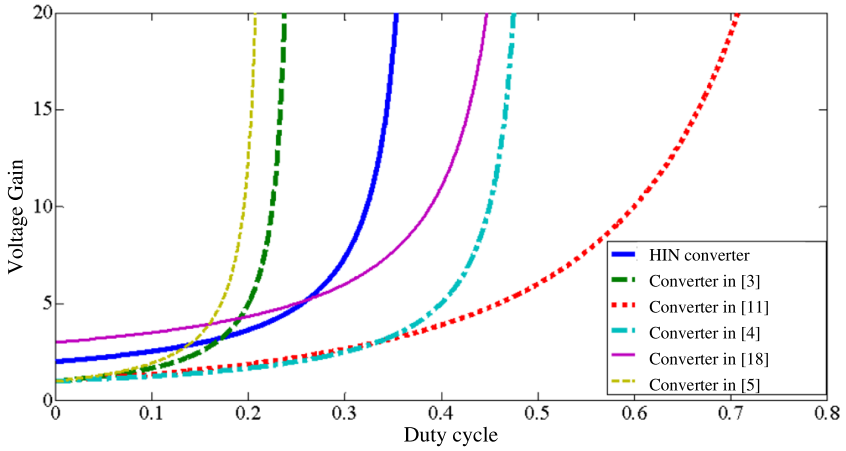

FIGURE 5 Comparison of voltage gains between the proposed HIN converter and other converters when $n_1=3, n_2=2$ [Colour figure can be viewed at wileyonlinelibrary.com]

Converters in other studies[3,5] are difficult to remain in stable operations when voltage gain is higher than 5. In other words, the voltage of the HIN converter is higher than converters in previous studies.[3,5] Compared to the converters in the literature,[4,11,14,18] the HIN converter can achieve a high voltage gain with a low duty cycle. Hence, the voltage stress

of devices in the HIN converter is lower than the voltage stress of devices in most other converters. In particular, the capacitor voltage stresses of C_1 and C_2 are much lower than the output voltage. The voltage stresses of devices in the multilevel high step-up converter in Wu et al.[14] becomes lower when the number of boost cells increases. But with an increasing number of boost cells, its power loss aggravates. A larger turns ratio lowers the capacitor voltage stress and switch voltage stress of the converter in Poorali and Adib,[18] but the coupled-inductor with a high turns ratio will cause high current spike and high inductor current leakage. The components count of the HIN converter is similar to other converters; however, the use of NECs in the HIN converter makes its size smaller. Therefore, the HIN converter performs better than other converters in terms of voltage stress on devices.

4 | PARAMETERS DESIGN

4.1 | Inductances

The current ripple is always predesigned in practical applications. Based on the predesigned current ripple, the inductances of the inductors L_1 and L_2 can be obtained as

$$\begin{cases} L_1 = \dfrac{V_{\text{in}} D(1-D)^2}{\Delta i_{L_1} f_{\text{s}} (D^2-3D+1)}, \\ L_2 = \dfrac{V_{\text{in}} D(1-D)}{\Delta i_{L_2} f_{\text{s}} (D^2-3D+1)}. \end{cases} \tag{10}$$

To ensure CCM operation, that is, the minimum inductor currents are greater than zero during the whole switching period, the inductances of the inductors are required to be greater than the critical inductances L_{1cri} and L_{2cri}, which can be derived as shown in (11) by setting $I_{\text{avg}L_1} - \Delta i_{L_1}/2$ and $I_{\text{avg}L_2} - \Delta i_{L_2}/2$ equal to zero as

$$L_{1\_\text{cri}} = L_{2\_\text{cri}} = \frac{RD(1-3D+D^2)}{8f_{\text{s}}}. \tag{11}$$

4.2 | Capacitances

The capacitances must have a suitable value to minimize the voltage ripples of the capacitors. The ripple amplitude of the capacitor voltages in the HIN converter, namely, Δv_{C_3} and Δv_{C_4} can be deduced from (1), (2), and (4) as

$$\begin{cases} \Delta v_{C_3} = \dfrac{V_{\text{in}} D(1-D)(1+D-D^2)}{RC_3 f_{\text{s}} (1-3D+D^2)^2}, \\ \Delta v_{C_4} = \dfrac{2V_{\text{in}} (1-D)(D^3-9D^2+11D-2)}{RC_4 f_{\text{s}} (1-3D+D^2)^2}. \end{cases} \tag{12}$$

According to the analysis in Section 3.1, $v_{C_3} = v_{C_4}$, thereby we can set $C_3 = C_4 = C$. Because the voltage ripples are normally predesigned in practical applications, the theoretical capacitances of the capacitors can be designed based on the permitted voltage ripples as

$$\Delta v_{\text{o}} = \frac{V_{\text{in}} D(D^3-17D^2+23D-4)}{RCf_{\text{s}} (1-3D+D^2)^2}, \tag{13}$$

then, one has

$$C = \frac{V_{\text{in}} D(D^3 - 17D^2 + 23D - 4)}{R\Delta v_{\text{o}} f_{\text{s}} (1 - 3D + D^2)^2}. \tag{14}$$

It is reasonable to select capacitances around the calculated values in practical applications, because usually, the parasitic parameters and the expected error between the actual value and the labelled value are small enough.

4.3 | Switches and diodes

The selection of the switch and diode is based on their rated voltage and current stresses. According to the analysis in Section 3.3, the rated parameters of the power devices can be easily determined and appropriate devices can then be selected.

5 | VOLTAGE DROP AND POWER LOSS OF THE HIN CONVERTER IN CCM

5.1 | Circuit description

The HIN network with parasitic resistance is shown in Figure 6. The ON-state resistances of switches and diodes is small enough to be ignored. Also, the parasitic resistances of output capacitors C_3 and C_4 are ignored because they connect with the load in parallel. Lastly, we assume that the parasitic resistances of L_1, L_2, C_1, and C_2 have the same value R'.

5.2 | Voltage drop analysis

Similar to Equations (1) and (2), the equations of the HIN converter with parasitic resistors in two modes can be derived as follows:

In mode 1:

$$\begin{cases} L_1 \dfrac{\mathrm{d}i_{L_1}}{\mathrm{d}t} + R' i_{L_1} = v_{\text{in}} + v_{C_2} - R' i_{L_1}, \\ L_2 \dfrac{\mathrm{d}i_{L_2}}{\mathrm{d}t} + R' i_{L_2} = v_{\text{in}} + v_{C_1} - R'(i_{\text{in}} - i_{L_1}) = v_{C_4}, \\ v_{\text{o}} = v_{C_3} + v_{C_4}. \end{cases} \tag{15}$$

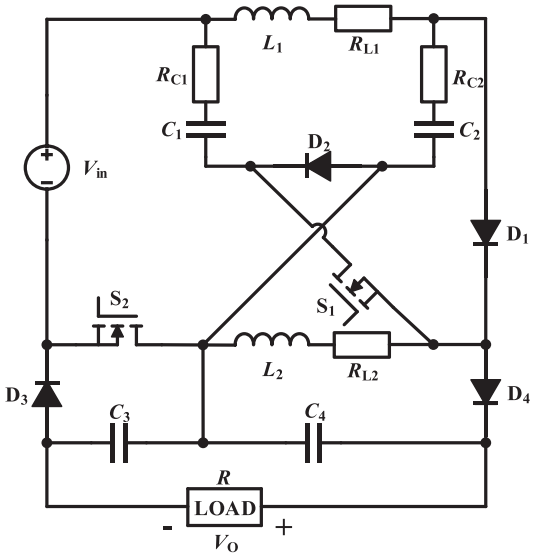

FIGURE 6 The HIN converter with parasitic resistances

In mode 2:

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L_1}}{\mathrm{d}t}+R'i_{L_1} & =v_{C_2}+R'i_{C_2}-v_{C_1}-R'i_{C_1} \\ & =v_{\mathrm{in}}+v_{C_2}+R'i_{C_2}-v_{C_3}, \\ L_2\dfrac{\mathrm{d}i_{L_2}}{\mathrm{d}t}+R'i_{L_2} & =-v_{C_2}-R'i_{C_2}, \\ v_{\mathrm{o}}=v_{C_3}+v_{C_4}. & \end{cases} \tag{16}$$

According to the vol-second balance principle on the inductors L_1 and L_2, the following equation can be obtained:

$$V'_{C_1}=\frac{V_{\mathrm{in}}D(1-D)}{1-3D+D^2}+\frac{4V_{\mathrm{in}}R'D(1-D)(D^3-4D^2+6D-4)}{R(1-3D+D^2)^3}, \tag{17}$$

where V'_{C_1} is the voltage of capacitor C_1 in the HIN converter with parasitic resistance.

Using (15), (16), (17) and $V'_{\mathrm{o}}=V'_{C_3}+V'_{C_4}$, the output voltage can be derived as

$$V'_{\mathrm{o}}=\left[\frac{2(1-D)}{1-3D+D^2}-\frac{8R'(1-2D)(1-D)^2}{RD(1-3D+D^2)^2}-\frac{8R'(1-D)(4-6D+4D^2-D^3)}{R(1-3D+D^2)^3}\right]V_{\mathrm{in}}. \tag{18}$$

The drop of the output voltage, namely, V_{loss}, can be derived as,

$$V_{\mathrm{loss}}=\frac{8R'(1-D)(1-2D+6D^2-5D^3+D^4)}{RD(1-3D+D^2)^3}V_{\mathrm{in}}. \tag{19}$$

5.3 | Power loss analysis

In this subsection, the power loss of the HIN converter is investigated. Parasitic resistances of the power electronics components used in this study are taken into account, including diode forward voltage V_{F}, diode conduction resistor R_D, winding resistor of inductor R_L, equivalent series resistance of capacitor R_C, the drain-source on-resistance of MOSFET R_{DS}, and the turn-on and turn-off time constants of MOSFET denoted as t_{on} and t_{off}.

The average value of the current of diodes D_1, D_2, D_3 and D_4 can be deduced as

$$I_{D_k(\mathrm{AVG})}=\frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}}i_{D_k}dt, \tag{20}$$

where $k=1,2,3,4$.

The total power loss of diodes is the power loss associated with the voltage source V_{F}. Assuming that all diodes are identical, according to (20), the total power loss of the diodes can be obtained as

$$P_D=\sum_{k=1}^{4}V_{\mathrm{F}}I_{D_k(\mathrm{AVG})}=\frac{2V_{\mathrm{F}}P_{\mathrm{o}}(3-6D+2D^2)}{V_{\mathrm{o}}(1-3D+D^2)}, \tag{21}$$

where P_{o} is the output power. The total conduction loss of the inductors due to their equivalent series resistance (ESR) is given by

$$P_{R_L}=\left(I^2_{L_{1(\mathrm{RMS})}}+I^2_{L_{2(\mathrm{RMS})}}\right)R_L=\frac{4R_LP_{\mathrm{o}}(2-2D+D^2)}{R(1-3D+D^2)^2}. \tag{22}$$

The RMS value of capacitor currents are given by

$$I_{C_k(\mathrm{RMS})} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{C_k}^2 dt}. \tag{23}$$

The total conduction loss of the buffer capacitors due to their ESR can be obtained as

$$\begin{aligned} P_{R_C} &= \sum_{k=1}^{4} I_{C_k(\mathrm{RMS})}^2 R_C \\ &= \frac{2R_C P_o(4-23D+48D^2-39D^3+16D^4-D^5)}{RD(1-3D+D^2)^2}. \end{aligned} \tag{24}$$

The RMS value of current of the switches can be obtained as

$$I_{S_{\mathrm{RMS}}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_S^2 dt}. \tag{25}$$

Considering the switching loss and conduction loss, the power loss of the MOSFET is thus

$$\begin{aligned} P_S &= P_{R_S} + P_{\text{on-off}} = \left(I_{S_{1(\mathrm{RMS})}}^2 + I_{S_{2(\mathrm{RMS})}}^2\right) R_S \\ &\quad + \frac{f_s(t_{\text{on}} + t_{\text{off}})\left(V_{S_1} I_{\text{avgS}_1} + V_{S_2} I_{\text{avgS}_2}\right)}{6} \\ &= \frac{4R_S P_o(2-2D+D^2)(1-D)^2}{RD(1-3D+D^2)^2} \\ &\quad + \frac{P_o f_s(t_{\text{on}} + t_{\text{off}})(1-D^2)}{6D(1-3D+D^2)}, \end{aligned} \tag{26}$$

where $P_{\text{on-off}}$ is the switching loss of S_1 and S_2. Then, the efficiency of the HIN converter can be calculated as

$$\eta = \frac{P_o \times 100\%}{P_o + P_{\text{Loss}}} = \frac{P_o \times 100\%}{P_o + P_D + P_{R_L} + P_{R_C} + P_S}. \tag{27}$$

6 | SIMULATION AND EXPERIMENTATION

6.1 | Simulation study

To verify the feasibility of the proposed converter, simulations in PSIM are conducted in this study. The parameters of the HIN converter are depicted in Table 2, and key waveforms are shown in Figure 7. The output voltage is 117.9 V,

TABLE 2 Simulation parameters

HIN Converter					
V_{in}	f_s	L_1, L_2	C_1, C_2, C_3, C_4	R'	R
20 V	100 kHz	330 μH	10 μF	0.2 Ω	300 Ω

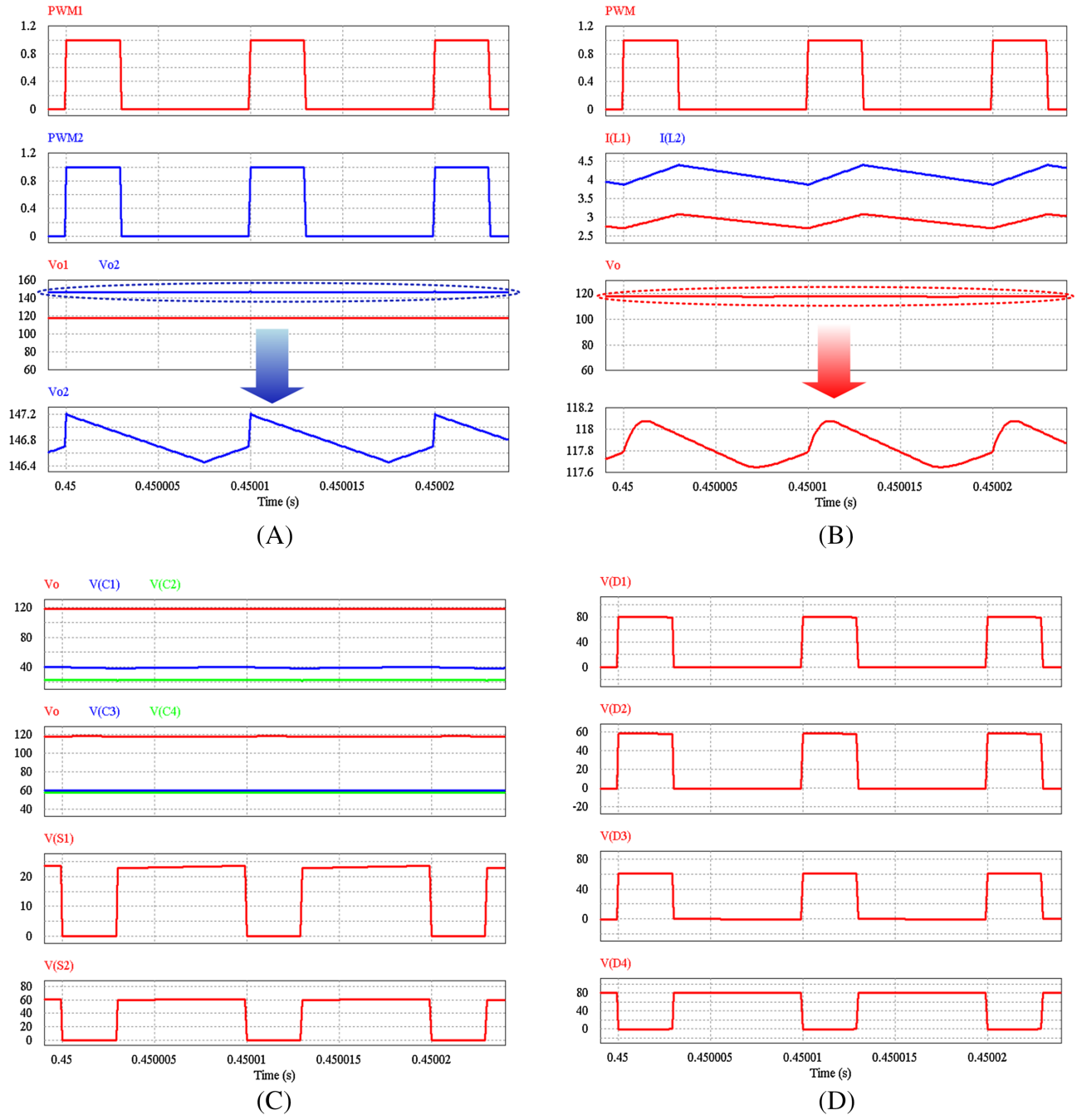

FIGURE 7 Simulation results under $d = 0.3$: (A) Waveforms of output voltages, where V_{o1} is the output voltage with parasitic resistances and V_{o2} is ideal output voltage, (B) Waveforms of inductor currents and output voltages, (C) Waveforms of capacitor voltages and switch voltages, (D) Waveform of diode voltages [Colour figure can be viewed at wileyonlinelibrary.com]

and its ripple needs to be less than 1% of its DC voltage. The voltage stresses of switches, diodes, and capacitors S_1, S_2, D_1, D_2, D_3, D_4, C_1, C_2, C_3, and C_4 are, respectively, 23.2, 60.7, 80.9, 59.0, 59.0, 80.9, 39.0, 23.2, 59.0, and 59.0 V. The voltage stresses of switches, diodes and capacitors are lower than the output voltage.

6.2 | Experimental results

In our laboratory environment, a 42.26 W low-power HIN converter is built, as shown in Figure 9. The main specifications and parameters of the components used in the prototype are listed in Table 3(Figure 8).

TABLE 3 Main specifications and parameters of the components used in the prototypes

Switching frequency (f_s)	**100 kHz**
Input voltage (V_{in})	20 V
Output voltage (V_o)	112.6 V
Load (R)	300 Ω
Inductor L_1 and L_2	330 μH
Capacitor (C_1, C_2, C_3, C_4)	10 μF

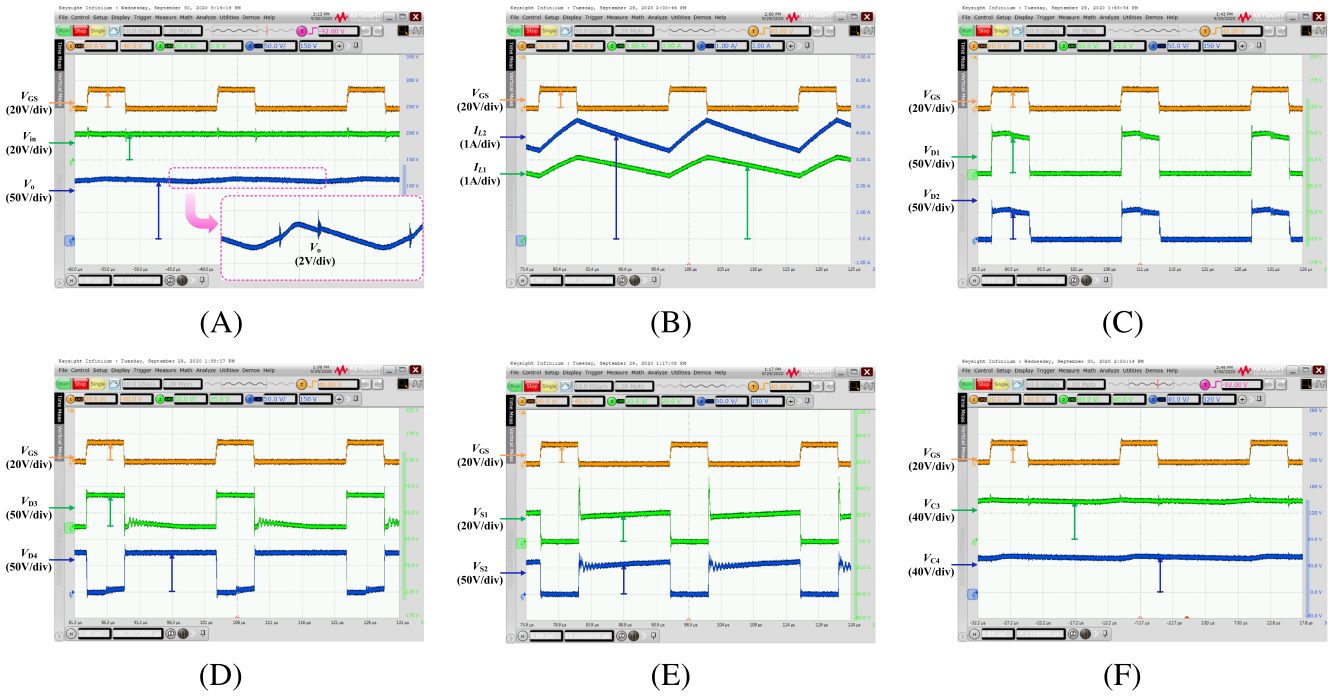

FIGURE 8 Experimental results: (A) input voltage and output voltage waveforms, (B) inductive current waveforms, (C) diode D_1 and D_2 voltage and current waveforms, (D) diode D_3 and D_4 voltage and current waveforms, and (E) switch S_1 and S_2 voltage and current waveforms [Colour figure can be viewed at wileyonlinelibrary.com]

Additionally, MOSFET IRF540N are used as switches S_1, S_2 and four MBR10200FCT diodes are used as diodes D_1, D_2, D_3, D_4. Switches S_1 and S_2 are driven by an integrated circuit (TLP250). PWR800L is used as the input power source and TLZ334WH is employed as the load in the experiments. The Agilent 1147A differential probes are used for measuring the voltages while an Agilent N2790A current probes are used for measuring currents. All the experimental waveforms are recorded by the oscilloscope Agilent DSO9104A. As shown in Figure 9, NECs are used in the HIN converter. Compared to ECs, NECs with big capacitances cannot be manufactured with the current manufacturing techniques. But the special topology structure of the HIN converter solves this problem because it only requires capacitors with small capacitances. Therefore, one of the advantages of the HIN converter is small size and high power density, due to the use of NECs, which is one of the main considerations for step-up converters design.

The experimental results shown in Figure 8 agree with the simulation results shown in Figure 7. The output voltage of the experiment is 112.6 V and the voltage stresses of switches, diodes and capacitors are $V_{S_1} = 22.3$ V, $V_{S_2} = 57.5$ V, $V_{D_1} = 77.4$ V, $V_{D_2} = 56.4$ V, $V_{D_3} = 56.7$ V, $V_{D_4} = 77.3$ V, $V_{C_1} = 36.3$ V, $V_{C_2} = 22.1$ V, $V_{C_3} = 56.3$ V and $V_{C_4} = 56.5$ V. The experimental voltages are slightly lower than the simulation voltages because the parasitic resistances in switches, diodes and output capacitors C_3, C_4 are ignored. These capacitor voltage stresses are much lower than the output voltage, which verifies the feature of the HIN converter of having low capacitor voltage stresses.

The efficiency curve of the HIN converter is shown in Figure 10. The HIN converter works at $V_o = 100V$. The prototype is designed to work in $40 \sim 50$ W; thus, the efficiency of the HIN converter decreases when $P_o = 100W$. But the

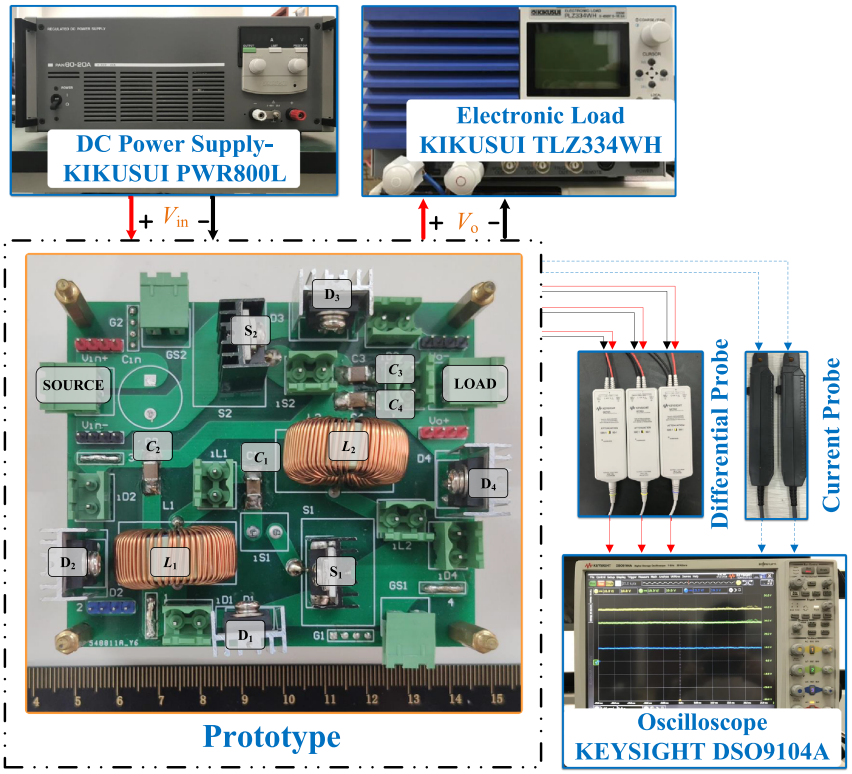

FIGURE 9 Prototype with the experimental environment [Colour figure can be viewed at wileyonlinelibrary.com]

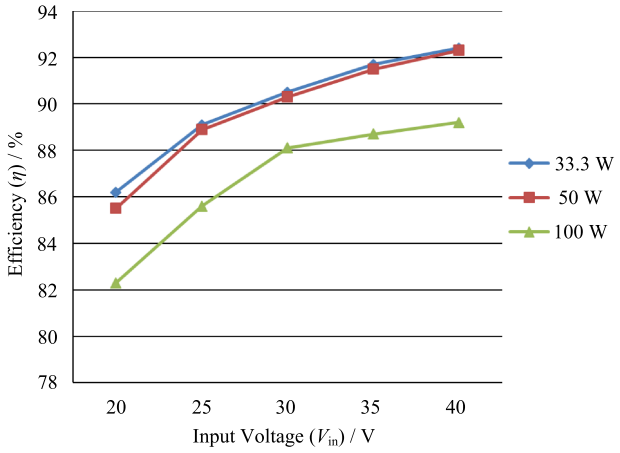

FIGURE 10 Efficiency of the proposed circuit with different output power [Colour figure can be viewed at wileyonlinelibrary.com]

efficiency is higher than 85% when P_o is lower than 50 W, and it can realize 92.5% of maximum value, note that the HIN converter has a high efficiency in most of the experiment time.

7 | CONCLUSION

A nonelectrolytic-capacitor HIN network converter with low capacitor voltage stress has been proposed in this study. Compared to conventional high step-up converters, the HIN converter has more switches and diodes. However, its voltage stresses of capacitors are lower than its conventional counterparts, with smaller size and lighter weight, due to the use of NECs. More importantly, its output voltage ripple is the same as the conventional ECs-based high step-up converters, which can substantially increase the service lifetime of the converter. The operating principle of the HIN converter in the CCM, the steady-state performance and parameters design have been detailed in this study. The features and effectiveness of the HIN converter have been verified by simulation and prototype experimentation conducted.

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ORCID

Guidong Zhang https://orcid.org/0000-0002-2371-2890
Samson S. Yu https://orcid.org/0000-0002-2983-7344
Abdelali El Aroudi https://orcid.org/0000-0001-9103-7762

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