Synthesis of Constant Power Loads Using Switching Converters under Sliding-Mode Control

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***Abstract*—This paper presents a systematic approach to synthetize constant power loads using switching converters under sliding-mode control. The generation of sliding motions is analyzed in converters with a series inductor in the input port and a switching function representing the error between the input power and a suitable power reference. The analysis establishes the existence conditions for sliding-mode and the stability of the resulting ideal dynamics. Simulation and experimental results verifying the theoretical predictions in boost, Ćuk and SEPIC converters illustrate the proposal. The design procedure yields a simple, economical and small-size prototype that can be useful in the experimental validation of converters supplying constant power loads.**

***Index Terms*—Power converters, constant power load, sliding-mode control**

I. Introduction

LOADS in dc-dc switching converters have been traditionally modelled by resistors in most cases and by current sources or voltage sources in few cases. For the first type of load, the output port is connected to an ideal resistor in the circuit description of the converter dynamic model, while it is in open circuit or short-circuited for the second and third type respectively. Therefore, in the absence of losses, only the resistive load connection results in an asymptotically stable converter in open-loop under Continuous Conduction Mode (CCM) operation [1].

More recently, due to the increasing use of multi-converters systems in electric and hybrid vehicles, the notion of constant power load (CPL) has emerged to characterize the powertrain behavior seen by its bidirectional dc-dc power converter when the vehicle motor speed is regulated under constant torque operation [2]. It also describes in a more general case of power distribution the cascade connection of two converters where the load converter operates with tightly regulated output voltage [3]. Unlike the case with resistive load, converters with CPL are unstable in open loop in CCM [4], so they can only operate in closed-loop in that mode if an appropriate feedback strategy is used.

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Ranging from linear to nonlinear techniques, different control strategies have been proposed to cope with the problem of regulating a power converter supplying a CPL. Linear strategies are based on cascade control whose inner loop uses inductor current feedback while the outer loop establishes the reference to the inner loop and regulates the output voltage [5]–[8]. Some nonlinear proposals are based on feedback linearization to either compensate the nonlinearity introduced by the CPL [9] or to create a virtual mesh to both stabilize the system and regulate the output voltage [10]. Other approaches have exhibited good performances under large-signal operation using boundary control [11], [12] or sliding-mode control (SMC) [13]–[19].

Those of the above strategies reporting experimental results have in common the use of a commercial electronic load operating as CPL. In this context, it can be expected that having a power circuit available that behaves like a CPL would be of a great help for engineers working on this topic due to size, simplicity, and cost reasons.

It has to be pointed out that power converters have already substituted commercial electronic loads with the aim of decreasing their size and cost. For instance, a bidirectional buck-boost converter emulating an electric vehicle features is presented in [20], a boost converter was used as a dc load with current source characteristics in [21], and a SEPIC converter has been implemented to operate as a dc electronic load in [22]. In the strict sense, the first antecedent of a CPL implementation is found in [23], in which no power converter is used but an analog circuit scheme with operational amplifiers is implemented, which eventually limits the device applications to a low power range (10 W). A second attempt is reported in [24], where a buck converter with PI control emulates different load profiles including a constant power mode. A third approach is based on the use of SMC with a nonlinear switching surface in a boost converter, which emulates successfully a CPL in [25] showing the advantages of this type of control in the presence of line and load perturbations. Nonetheless, the design is only applicable to the boost converter. Finally, the existence of a device behaving like a generic CPL is shown without details in the dc distribution test bed of a sea and undersea vehicle in [26].

In our previous publications [10], [18], [19] we have proposed different control strategies for a boost converter feeding CPLs. In [18], a variable frequency SMC has been used while in [10], a fixed frequency nonlinear PWM control approach was adopted where the power of the CPL is supposed to be known. In [19] a nonlinear PWM strategy with power

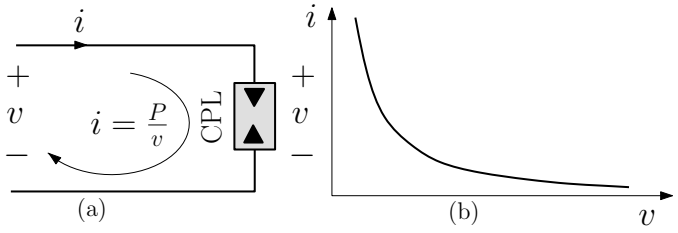

Fig. 1. Instantaneous constant power load (a) Symbol (b) Current-voltage characteristics.

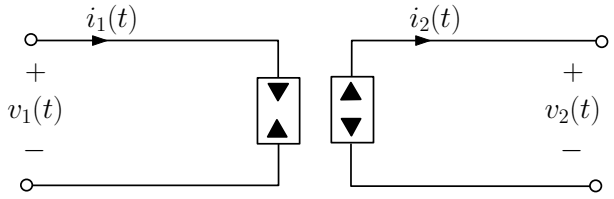

Fig. 2. Two-port model of a power converter with CPL characteristics in the input port.

estimation scheme was proposed. In the previous papers, the main objective was to regulate the output voltage of the converter being this loaded either by a known or an unknown CPL which was experimentally emulated by an electronic load or by a second stage converter absorbing a constant power. How to systematically synthesize this second stage converter to behave as a CPL has been left for a future research. Therefore, the aim of this paper is to present systematic approach based on SMC for synthesizing switching power converters with CPL characteristics. This control strategy is the natural way to synthetize the canonical elements for power processing, *i.e.*, dc transformers [27], power gyrators [28] and loss-free resistors (LFRs) [29]. The design is based on the inherent facility of SMC to impose the characteristic equation of the canonical element [30] and the fact that the latter is a two-port circuit of POPI nature, *i.e.*, the dc power output equals the dc power input in steady-state [31].

Unlike the two-port design of the canonical elements, this paper proposes the design of a one-port device with dc instantaneous CPL behavior. This feature is predicted analytically and verified by PSIM© simulations on the circuit-level switched model of the system, and by experimental measurements on ad-hoc prototypes. Converter candidates to emulate a CPL are analyzed under SMC, and the existence of sliding motions together with the calculation of the equivalent control and stability conditions in each case are presented.

The work here reported is an extension of a preliminary study presented in [32], where the synthesis of CPLs was partially validated by means of PSIM© simulations. In this paper, the theoretical parts have been extended and experimental results have been added. The rest of the paper is organized as follows: the notion of instantaneous CPL is reviewed in Section II together with the synthesis formulation. The sliding-mode analysis of potential converters for CPL emulation is performed in Section III. Simulation and experimental results are presented in Section IV and conclusions are summarized in Section V.

II. Synthesis of CPLs using Switching Converters under SMC

A. The instantaneous constant power load

A CPL is a one-port device absorbing constant power P, *i.e.* its current (i) versus voltage (v) characteristics is given by

$$vi = P, \qquad P \in \mathbb{R}^+,\ i \in \mathbb{R}^+,\ v \in \mathbb{R}^+ \tag{1}$$

The symbol of a CPL is a power sink as shown in Fig. 1(a), where the current absorbed by the sink is expressed as $i = \frac{P}{v}$. Fig. 1(b), in turn, depicts the corresponding $i - v$ characteristics.

B. Synthesis formulation

The purpose of the synthesis is the design of a dc–dc switching converter that is characterized by an input port behaving as an instantaneous CPL. Hence, the goal of the synthesis can be formulated as

$$v_1 i_1 = P_{\rm ref} \tag{2}$$

being $P_{\rm ref}$ a desired nominal power, v_1 and i_1 the respective averaged values of voltage and current in the input port. The fulfillment of (2) will guarantee that a desired constant power is absorbed at the input port of the switching converter.

Besides, since the power converter is a POPI circuit [31], its output port will deliver $P_{\rm ref}$. Hence, the following expression will be satisfied

$$V_1 I_1 = V_2 I_2, \tag{3}$$

where I_1, V_1 are the respective steady-state averaged values of voltage and current in the input port, and I_2, V_2 are the respective steady-state averaged values of voltage and current in the output port.

Therefore, the two-port model of a dc-dc switching converter implementing a CPL in the input port will consist of a power sink in the input port and a power source in the output port as depicted in Fig. 2. In order to impose the CPL behavior in the input port, we will follow a similar procedure to the one reported in [29] for the synthesis of LFRs using SMC. In that paper, the purpose of the control was to impose a proportional relationship between the averaged values of input current and input voltage while in this paper the goal of the sliding strategy is to force the fulfillment of expression (2). Given that the control pursues inducing sliding motions in the input port, the potential converters must have a series inductor in that port like in [29] because the construction of the switching function requires continuous variables.

Fig. 3 shows the block diagram of a generic dc-dc switching converter under a control law whose purpose is to impose a CPL behavior in the input port. The control law is implemented by a sliding-mode regulation loop whose switching surface is $\Sigma = \{x | S(x) = 0\}$, where $S(x)$ is given by

$$S(x) = v_1 i_1 - P_{\rm ref} \tag{4}$$

Note that $S(x)$ expression (4) is a nonlinear switching function representing a power control like the one proposed

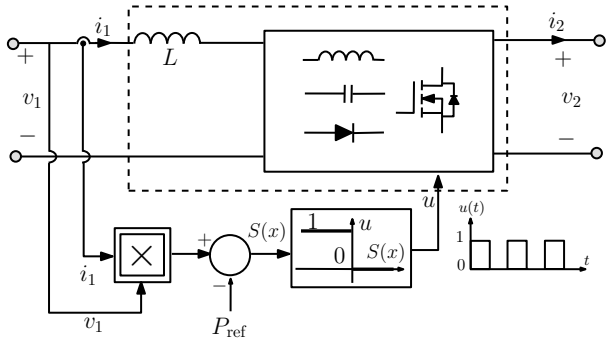

Fig. 3. Block diagram of a generic dc-dc switching converter under a control law whose purpose is to impose a CPL behavior in the input port.

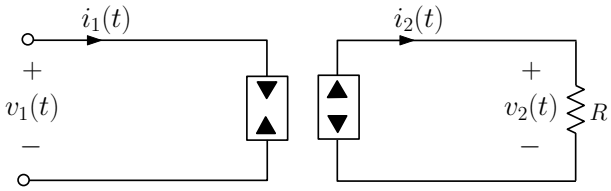

Fig. 4. Power sink (CPL)-power source terminated by a resistive load.

in [15] for the boost converter. However, while in [15], the switching function was built by using the product between the input current and the output voltage of the boost converter, here, the switching function $S(x)$ is built by using the voltage and current at the input port of different converter candidates. In this way, it is the power at the input port that is controlled to be constant hence emulating and ideal CPL when it is connected to another source converter.

Since we have to measure both input voltage and current, the latter being an inductor current, we can also use an equivalent approach based on a nonlinear switching function representing a current control as follows

$$S(x) = i_1 - \frac{P_{\text{ref}}}{v_1} \tag{5}$$

In sliding regime, $S(x) = 0$, in both cases, which implies the fulfillment of (2). Nevertheless, the aim of the synthesis is to implement a one-port device that can be used as a CPL in practical applications rather than to construct a two-port power sink-power source device shown in Fig. 2. Therefore, as in [29], the output port will be loaded with a linear resistor, so the model of the converter with CPL characteristics will be represented as shown in Fig. 4.

With this additional constraint, we can consider now same converters used in the synthesis of LFRs in [29], namely, boost, Ćuk, SEPIC, boost with output filter (BOF) and buck with input filter (BIF) as illustrated in Fig. 5.

The analysis of the sliding motions requires two circuit configurations, so CCM is assumed here. The sliding-mode approach requires the formulation of the state equations, the analysis of the existence conditions for sliding-mode, and the calculation of the equivalent control for the stability examination of the ideal sliding dynamics.

Although PSIM© simulations using switching functions (4) and (5) show identical results, the first one is preferable because tuning a multiplier is simpler than tuning a divider in the prototyping phase. Hence, the rest of the paper covers the theoretical analysis and the practical results based on the use of switching function (4). Nonetheless, the analytical approach required by (5) is developed in the boost converter in Appendix A. The control law to keep the system switching above and below the surface Σ is derived by imposing that the following conditions are satisfied [35], [36]

$$\begin{aligned} \frac{dS(x)}{dt} &< 0 \quad \text{if} \quad S(x) > 0 \\ \frac{dS(x)}{dt} &> 0 \quad \text{if} \quad S(x) < 0, \end{aligned} \tag{6}$$

implying that the change in the variable $S(x)$ is such that the system trajectory converges to Σ in its close neighborhood. These expressions lead to the following control law

$$u = \begin{cases} 1 & \text{if } S(x) < 0 \\ 0 & \text{if } S(x) > 0 \end{cases} \quad \Leftrightarrow \quad u = \frac{1}{2}(1 - \text{sign}(S(x))) \tag{7}$$

In Appendix B, the conditions for the trajectories of the boost converter to converge in finite time to the sliding surface given by (4) are given. The same analysis can be applied to other converter topologies. Under ideal sliding mode operation, such a control law would lead to infinite switching frequency. The usual approach to deal with this problem is to employ a regularization by replacing the previous control law by a closely similar one. The universal approach to regularization consists of introducing a hysteresis window around the switching manifold Σ such that the switching function $S(x)$ inside the hysteresis window. Therefore, the practical implementation of the previous control law uses a hysteresis comparator to control the switching frequency and limit it to a desired value. With a hysteretic controller, the control law can be expressed as follows

$$u = \begin{cases} 1 & \text{if } S(x) < -\frac{h}{2} \text{ or}(|S(x)| < \frac{h}{2} \text{ and } \frac{dS(x)}{dt} < 0) \\ 0 & \text{if } S(x) > +\frac{h}{2} \text{ or}(|S(x)| < \frac{h}{2} \text{ and } \frac{dS(x)}{dt} > 0) \end{cases} \tag{8}$$

where $h > 0$ represents the hysteresis width.

III. SMC OF POTENTIAL CONVERTERS FOR CPL OPERATION

To make the presentation clear, ideal reactive elements and switching devices are considered. In practice, these elements will present parasitic elements in the form ohmic losses among others [33], [34]. The same approach followed in this section can be used if the losses in the components are taken into account.

A. State equations

In CCM, the converters in Fig. 5 can be represented in compact form by the set of differential equations described below. The compact description uses the binary signal u depicted in Fig. 1, which takes values 1 and 0 during ON

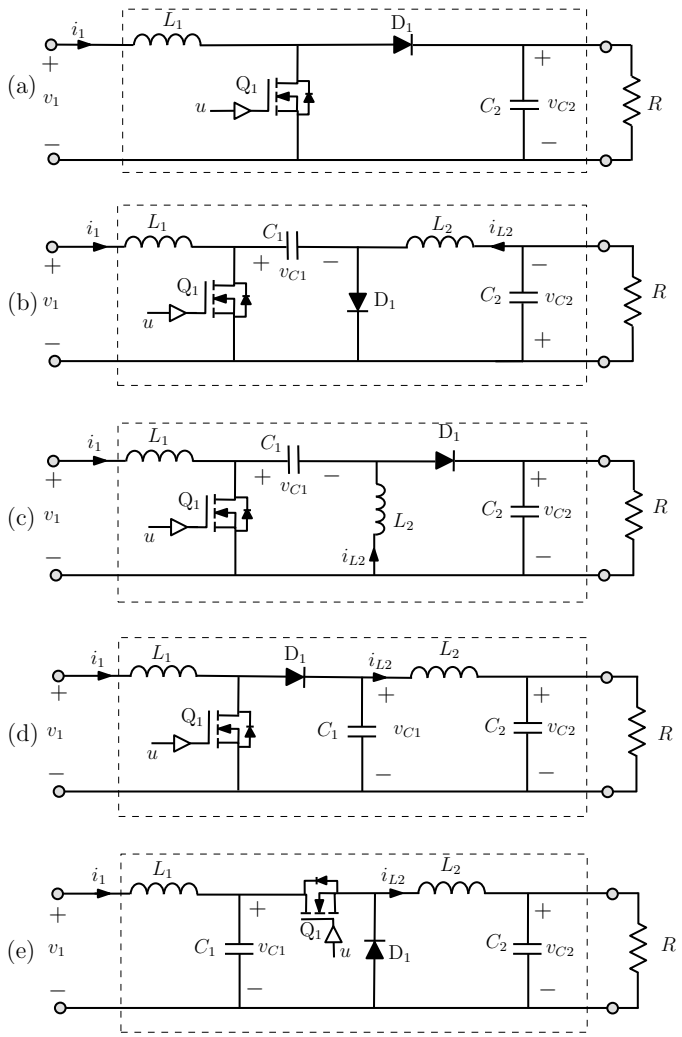

Fig. 5. Converters with non-pulsating input current (a) boost converter, (b) Ćuk converter, (c) SEPIC converter, (d) BOF, (e) BIF.

and OFF states respectively, according to (7).

(a) Boost converter

$$\begin{aligned}\frac{di_1}{dt} &= -\frac{v_{C2}}{L_1}(1-u)+\frac{v_1}{L_1}\\ \frac{dv_{C2}}{dt} &= \frac{i_1}{C_2}(1-u)-\frac{v_{C2}}{C_2R}\end{aligned} \tag{9}$$

where v_{C2} is the output capacitor voltage, i_1 is the inductor current and u is the binary control signal for the switch Q_1. All the other parameters appearing in (9) can be seen in Fig. 5.

(b) Ćuk converter

$$\begin{aligned}\frac{di_1}{dt} &= -\frac{v_{C1}}{L_1}(1-u)+\frac{v_1}{L_1}\\ \frac{di_{L2}}{dt} &= \frac{v_{C1}}{L_2}u-\frac{v_{C2}}{L_2}\\ \frac{dv_{C1}}{dt} &= \frac{i_1}{C_1}(1-u)-\frac{i_{L2}}{C_1}u\\ \frac{dv_{C2}}{dt} &= \frac{i_{L2}}{C_2}-\frac{v_{C2}}{RC_2}\end{aligned} \tag{10}$$

The parameters and variables appearing in (10) can be seen in Fig. 5-b.

(c) SEPIC converter

$$\begin{aligned}\frac{di_1}{dt} &= -\frac{v_{C1}+v_{C2}}{L_1}(1-u)+\frac{v_1}{L_1}\\ \frac{di_{L2}}{dt} &= \frac{v_{C1}}{L_2}u-\frac{v_{C2}}{L_2}(1-u)\\ \frac{dv_{C1}}{dt} &= \frac{i_1}{C_1}(1-u)-\frac{i_{L2}}{C_1}u\\ \frac{dv_{C2}}{dt} &= \frac{i_1+i_{L2}}{C_2}(1-u)-\frac{v_{C2}}{RC_2}\end{aligned} \tag{11}$$

The parameters and variables appearing in (11) can be seen in Fig. 5-c.

(d) Boost converter with output filter

$$\begin{aligned}\frac{di_1}{dt} &= -\frac{v_{C1}}{L_1}(1-u)+\frac{v_1}{L_1}\\ \frac{di_{L2}}{dt} &= \frac{v_{C1}-v_{C2}}{L_2}\\ \frac{dv_{C1}}{dt} &= \frac{i_1}{C_1}(1-u)-\frac{i_{L2}}{C_1}\\ \frac{dv_{C2}}{dt} &= \frac{i_{L2}}{C_2}-\frac{v_{C2}}{RC_2}\end{aligned} \tag{12}$$

The other parameters and variables appearing in (12) can be seen in Fig. 5-d.

(e) Buck converter with input filter

$$\begin{aligned}\frac{di_1}{dt} &= -\frac{v_{C1}}{L_1}+\frac{v_1}{L_1}\\ \frac{di_{L2}}{dt} &= \frac{v_{C1}}{L_2}u-\frac{v_{C2}}{L_2}\\ \frac{dv_{C1}}{dt} &= \frac{i_1}{C_1}-\frac{i_{L2}}{C_1}u\\ \frac{dv_{C2}}{dt} &= \frac{i_{L2}}{C_2}-\frac{v_{C2}}{RC_2}\end{aligned} \tag{13}$$

The parameters and variables appearing in (13) can be seen in Fig. 5-e.

B. Existence of sliding motions

The time derivative of $S(x)$ in (4) can be expressed as follows

$$\frac{dS(x)}{dt} = \frac{di_1}{dt}v_1 + i_1\frac{dv_1}{dt} \tag{14}$$

Below, we particularize expression (14) in each converter of Fig. 5 using the state equations written above.

(a) Boost converter

Introducing (9) into (14) yields

$$\frac{dS(x)}{dt} = -\frac{v_{C2}v_1}{L_1}(1-u)+\frac{v_1^2}{L_1}+i_1\frac{dv_1}{dt} \tag{15}$$

Particularizing (15) for $u=1$ and taking into account (7) and (6), we obtain

$$\left.\frac{dS(x)}{dt}\right|_{u=1} = \frac{v_1^2}{L_1}+i_1\frac{dv_1}{dt} > 0 \tag{16}$$

A sufficient condition for (16) to be fulfilled is

$$\left|\frac{dv_1}{dt}\right|_{\max} < \frac{v_{1,\min}^2}{i_1 L_1} \tag{17}$$

Similarly, for $u = 0$, one obtains the following inequality

$$\left.\frac{dS(x)}{dt}\right|_{u=0} = -\frac{v_1}{L_1}\left(v_{C2} - v_1 - \frac{i_1 L_1}{v_1}\frac{dv_1}{dt}\right) < 0, \quad (18)$$

which can be written in the following form

$$\left.\frac{dS(x)}{dt}\right|_{u=0} = -\frac{v_1}{L_1}\left(v_{C2} - kv_1\right) < 0, \quad (19)$$

where k is given by

$$k \triangleq 1 + \frac{i_1 L_1}{v_1^2}\frac{dv_1}{dt} \quad (20)$$

It can be observed that (19) will be always negative if k is negative. In case of $k > 0$, it will be necessary to guarantee that (19) is fulfilled. Let us consider the following cases for $k > 0$:

1) If $\frac{dv_1}{dt} < 0$, $\left|\frac{dv_1}{dt}\right|_{\max}$ and $v_{1,\min}$ in (17) are such that

$$0 < 1 - \frac{\left|\frac{dv_1}{dt}\right|_{\max}}{\frac{v_{1,\min}^2}{i_1 L_1}} < 1 \implies 0 < k < 1 \quad (21)$$

From (19) and (21) it can be seen that if $v_{C2} > v_1$, *i.e.* boost operation, condition (19) will be fulfilled.

2) If $\frac{dv_1}{dt} > 0$, $\left|\frac{dv_1}{dt}\right|_{\max}$ and $v_{1,\min}$ in (17) are such that

$$1 < 1 + \frac{\left|\frac{dv_1}{dt}\right|_{\max}}{\frac{v_{1,\min}^2}{i_1 L_1}} < 2 \implies 1 < k < 2 \quad (22)$$

Therefore, condition (18) holds if $v_{C2} > 2v_1$.

We can conclude that the system will have different existence conditions for the sliding motions depending on the time derivative of the input voltage.

On the other hand, considering a constant input voltage ($v_1(t) = V_g$), so $\frac{dv_1}{dt} = 0$, the following condition to ensure the existence of sliding mode is derived from (16) and (18)

$$0 < V_g < v_{C2}, \quad (23)$$

which is a necessary condition for the boost converter operation.

(b) Ćuk converter

From (10) and (14), we derive

$$\frac{dS(x)}{dt} = -\frac{v_1 v_{C1}}{L_1}(1-u) + \frac{v_1^2}{L_1} + i_1\frac{dv_1}{dt} \quad (24)$$

Note that (24) is identical to (15) if we substitute v_{C1} by v_{C2}. Hence, the existence of sliding motions in the Ćuk converter is imposed by its input stage that has boost converter behavior.

If a constant input voltage V_g is considered, expression (24) leads to

$$0 < V_g < v_{C1}, \quad (25)$$

which is the necessary condition to ensure existence of sliding motions.

(c) SEPIC converter

Combining (11) and (14) results in

$$\frac{dS(x)}{dt} = -\frac{v_1 v_{C1} + v_1 v_{C2}}{L_1}(1-u) + \frac{v_1^2}{L_1} + i_1\frac{dv_1}{dt} \quad (26)$$

For $u = 1$ expressions (6) and (26) lead to

$$\left.\frac{dS(x)}{dt}\right|_{u=1} = \frac{v_1^2}{L_1} + i_1\frac{dv_1}{dt} > 0 \quad (27)$$

Similarly, for $u = 0$ we obtain

$$\left.\frac{dS(x)}{dt}\right|_{u=0} = -\frac{v_1}{L_1}\left(v_{C1} + v_{C2} - v_1(1 + \frac{dv_1}{dt}\frac{L_1 i_1}{v_1^2})\right) < 0 \quad (28)$$

Inequality (28) can be expressed as follows

$$\left.\frac{dS(x)}{dt}\right|_{u=0} = -\frac{v_1}{L_1}(v_{C1} + v_{C2} - kv_1) < 0, \quad (29)$$

where k is given by expression (20).

In the vicinity of the equilibrium point $v_{C1} \approx v_1$. Therefore, the following condition is derived from (29)

$$\left.\frac{dS(x)}{dt}\right|_{u=0} = -\frac{v_1}{L_1}(v_{C2} + v_1(1-k)) < 0 \quad (30)$$

Inequality (29) is satisfied for $k < 0$. Nonetheless, for $k > 0$, the following cases are considered

1) If $\frac{dv_1}{dt} < 0$, $\left|\frac{dv_1}{dt}\right|_{\max}$ and $v_{1,\min}$ are such that $0 < k < 1$, then (29) will be fulfilled if $v_{C2} > 0$.
2) If $\frac{dv_1}{dt} > 0$, $\left|\frac{dv_1}{dt}\right|_{\max}$ and $v_{1,\min}$ are such that $1 < k < 2$, then (29) will be fulfilled if $v_{C2} > v_1$.

Therefore, the conditions for existence of sliding mode will be fulfilled when the SEPIC converter operates as a voltage step-up converter.

Finally, it can be observed that assuming $v_1 = V_g$, being V_g a constant input voltage, results in $\frac{dS(x)}{dt} > 0$ for $u = 1$ and the following condition for $u = 0$

$$V_g(V_g - v_{C1} - v_{C2}) < 0 \quad (31)$$

Condition (31) is always satisfied in the vicinity of the equilibrium point since $v_{C1} \approx V_g$ irrespective of the voltage step-up or voltage step-down operation of the converter.

(d) Boost converter with output filter

From (12) and (14) we obtain

$$\frac{dS(x)}{dt} = -\frac{v_1 v_{C1}}{L_1}(1-u) + \frac{v_1^2}{L_1} + i_1\frac{dv_1}{dt} \quad (32)$$

We can observe that expression (32) is identical to (24) and equivalent to (15) if we substitute v_{C1} by v_{C2}. Hence, the BOF converter and Ćuk converter have the same conditions for existence of sliding motions, which are eventually equal to those of the boost converter.

(e) Buck converter with input filter

From (13) and (14) we obtain

$$\frac{dS(x)}{dt} = -\frac{v_1 v_{C1}}{L_1} + \frac{v_1^2}{L_1} + i_1\frac{dv_1}{dt} \quad (33)$$

Note that in this case, the time derivative of the switching function is independent of control signal. Therefore, sliding motions cannot be induced in the buck converter with input filter and hence it cannot be used to operate as CPL.

C. Equivalent control

The next step in the analysis consists in deriving the expression of the equivalent control, *i.e.* a continuous-time signal with a bounded range between 0 and 1 that describes the averaged dynamics of the controlled converter on the sliding surface. Besides the constraint $S(x) = 0$, *i.e.*, the state trajectory being on the switching surface, we add the following restriction that guarantee the trajectory to remain on the surface

$$\frac{dS(x)}{dt} = 0 \tag{34}$$

From (14) and the state equations (9)–(12), the expression of the equivalent control are derived below for the four converters in which sliding motions can be induced.

(a) Boost converter

$$u_{eq} = 1 - \frac{v_1^2 + L_1 i_1 \dfrac{dv_1}{dt}}{v_1 v_{C2}} \tag{35}$$

The equivalent control u_{eq} is the continuous and smooth control law that would lead to the same behavior and system response as with the switched control law u under sliding mode conditions. If a constant input voltage V_g is considered, expression (35) becomes

$$u_{eq} = \frac{v_{C2} - V_g}{v_{C2}} \tag{36}$$

(b) Ćuk converter

$$u_{eq} = 1 - \frac{v_1^2 + L_1 i_1 \dfrac{dv_1}{dt}}{v_1 v_{C1}} \tag{37}$$

For a constant input voltage V_g, expression (37) leads to

$$u_{eq} = \frac{v_{C1} - V_g}{v_{C1}} \tag{38}$$

(c) SEPIC converter

$$u_{eq} = 1 - \frac{v_1^2 + L_1 i_1 \dfrac{dv_1}{dt}}{v_1 (v_{C1} + v_{C2})} \tag{39}$$

Considering the input voltage v_1 as constant (V_g), the above expression results in

$$u_{eq} = \frac{v_{C2}}{V_g + v_{C2}} \tag{40}$$

(d) Boost converter with input filter

$$u_{eq} = 1 - \frac{v_1^2 + L_1 i_1 \dfrac{dv_1}{dt}}{v_1 v_{C1}} \tag{41}$$

For a constant input voltage $v_1 = V_g$, the equivalent control will be given by

$$u_{eq} = \frac{v_{C1} - V_g}{v_{C1}} \tag{42}$$

D. Ideal sliding dynamics

The ideal sliding dynamics describes the motion along a subset of the manifold Σ, where the binary control u is substituted by the equivalent control u_{eq}. The first constraint results in one-order reduction of the converter state equations while the introduction of the equivalent control leads to an averaged description of the system dynamics. The resulting equations for boost, Ćuk , SEPIC and BOF are given next for the case of constant input voltage ($v_1 = V_g$).

(a) Boost converter

$$\frac{dv_{C2}}{dt} = \frac{P_{\text{ref}}}{C_2 v_{C2}} - \frac{v_{C2}}{C_2 R} \tag{43}$$

(b) Ćuk converter

$$\begin{aligned} \frac{di_{L2}}{dt} &= \frac{v_{C1}}{L_2} - \frac{v_{C2}}{L_2} - \frac{V_g}{L_2} \\ \frac{dv_{C1}}{dt} &= \frac{P_{\text{ref}}}{C_1 v_{C1}} - \frac{i_{L2}}{C_1} + \frac{i_{L2} V_g}{C_1 V_{C1}} \\ \frac{dv_{C2}}{dt} &= \frac{i_{L2}}{C_2} - \frac{v_{C2}}{C_2 R} \end{aligned} \tag{44}$$

(c) SEPIC converter

$$\begin{aligned} \frac{di_{L2}}{dt} &= \frac{v_{C1}}{L_2} - \frac{V_g}{L_2} \\ \frac{dv_{C1}}{dt} &= \frac{1}{C_1} \frac{P_{\text{ref}}}{v_{C1} + v_{C2}} - \frac{i_{L2}}{C_1} + \frac{i_{L2}}{C_1} \frac{V_g}{v_{C1} + v_{C2}} \\ \frac{dv_{C2}}{dt} &= \frac{1}{C_2} \frac{P_{\text{ref}}}{v_{C1} + v_{C2}} + \frac{i_{L2}}{C_2} \frac{V_g}{v_{C1} + v_{C2}} - \frac{v_{C2}}{C_2 R} \end{aligned} \tag{45}$$

(d) Boost converter with output filter

$$\begin{aligned} \frac{di_{L2}}{dt} &= \frac{v_{C1} - v_{C2}}{L_2} \\ \frac{dv_{C1}}{dt} &= \frac{P_{\text{ref}}}{C_1 v_{C1}} - \frac{i_{L2}}{C_1} \\ \frac{dv_{C2}}{dt} &= \frac{i_{L2}}{C_2} - \frac{v_{C2}}{C_2 R} \end{aligned} \tag{46}$$

E. Stability analysis

The coordinates of the equilibrium point in equations (43)–(46) have in common the values corresponding to input current, and output voltage given respectively by

$$I_1^* = \frac{P_{\text{ref}}}{V_g} \tag{47}$$

$$V_{C2}^* = \sqrt{P_{\text{ref}} R} \tag{48}$$

In addition, the equilibrium coordinate of inductor current i_{L2} in Ćuk, SEPIC and BOF is given by

$$I_{L2}^* = \sqrt{\frac{P_{\text{ref}}}{R}} \tag{49}$$

The remaining coordinate is specific of each converter. In particular, this coordinate is as follows

$$V_{C1}^* = V_g + V_{C2}^* \quad \text{in the Ćuk converter} \tag{50}$$

$$V_{C1}^* = V_g \quad \text{in the SEPIC converter} \tag{51}$$

$$V_{C1}^* = V_{C2}^* \quad \text{in the BOF converter} \tag{52}$$

Regarding the stability of the equilibrium point, we will consider first the case of the boost converter and then the three fourth–order converters.

(a) Boost converter

In the boost converter, the change of variable $z = \frac{1}{2}C_2 v_{C2}^2$ in (43) results in the following linear differential equation

$$\frac{dz}{dt} = P_{\rm ref} - \frac{2z}{C_2 R}, \tag{53}$$

whose solution is given by

$$z(t) = P_{\rm ref}\frac{C_2 R}{2} + (z(0) - P_{\rm ref}\frac{C_2 R}{2})e^{-\frac{2t}{C_2 R}}, \tag{54}$$

where $z(0)$ is the initial value of $z(t)$. Since $z(t)$ is bounded, v_{C2} will be bounded because $v_{C2} = \sqrt{\frac{2z}{C_2}}$. Hence the ideal sliding dynamics is stable in the boost converter.

(b) Ćuk, SEPIC and BOF

Unlike the boost converter, a linearization around the equilibrium point is required in the fourth-order candidates resulting in the characteristic equations given in (55)–(57) at the top of the next page.

Applying the Routh-Hurtwitz's criterion to (55)–(57) reveals that Ćuk and BOF are always stable while the SEPIC converter will be always stable if the following condition is satisfied

$$\frac{V_{C2}^*}{C_1} > \frac{V_g}{C_2} \tag{58}$$

Or equivalently

$$\frac{\sqrt{P_{\rm ref} R}}{C_1} > \frac{V_g}{C_2} \tag{59}$$

Observe that (58) is the sufficient condition reported in [37] for stable operation of the SEPIC converter when it is used for ac–dc power factor correction with regulated output current.

IV. Simulation and Experimental Results

The theoretical predictions have been validated in three laboratory prototypes corresponding to boost, Ćuk and SEPIC converter respectively. They have in common the controller shown in Fig. 6, which implements the switching function given by (4) and a slight modification of the control law (7). The latter implies the use of an ideal comparator that has been replaced by a hysteretic one to limit the switching frequency. The implemented law is given by (8).

The controller has four blocks, *i.e.* input power, power reference, power error and hysteresis comparator. The power input $P_{\rm in}$ is calculated first by multiplying the inductor current and the input voltage by means of IC AD633. Then, a circuit based on operational amplifier LF347 provides the switching function $S(x)$ from the previous signal $P_{\rm in}$ and an external signal that constitutes the power reference. The hysteresis comparator, in turn, is based on LM319 to establish both upper and lower limits of the hysteresis window. The hysteresis output is adapted to the switch driver by flip-flop CD4027, which eventually provides the activation/deactivation pulses of the control law.

The input inductor current is sensed in the three converters by current sensor LA 25NP. Inductors in all cases have been implemented in-house with a toroidal core from MAGNETICS. Nominal values of input voltage, output voltage, power and switching frequency are 200 V, 350 V, 1 kW, and 100 kHz respectively in the three converters.

Fig. 7 shows simulated and measured waveforms of the converter start-up in the three cases. A good agreement is observed between them. It has to be pointed out that the power at the input port reaches the power reference almost instantaneously while the output power attains the same value after a short transient time.

Finally, Fig. 8 illustrates the transient response of the converter in reaction to variations of the power reference. First, the power reference changes from 1 kW to 0.5 kW, and then from 0.5 kW to 1 kW. Note that both input power and output power follow accurately the power reference. Besides, the controlled input power reaches almost instantaneously the desired power.

Traditionally converters with tight voltage control using a fixed frequency PWM are considered as CPLs. With this control strategy, since the power delivered to the load is proportional to the squared voltage, if this voltage is tightly regulated, the power will be practically constant. However, since any control strategy based on PWM technique would have finite bandwidth, the CPL behavior will also present a finite bandwidth. This is not the case of SMC approach which guarantees convergence to the sliding manifold almost instantaneously as can be noticed in Fig. 7 and Fig. 8. Moreover, while with SMC approach only the desired power has to be selected and little effort must be done for tuning the controller, in the PWM-based approach, a careful selection of the controller poles, zeros and gain must be done for guaranteeing a tight regulation of the output voltage and therefore the output power.

V. Conclusions

Switching converters exhibiting constant power load characteristics at their input port can be synthesized under certain topological constraints using sliding-mode control. The topological constraints impose the existence of a series inductor in the input port. The SMC uses, in turn, a switching surface made up of the input power error, *i.e.* the difference between the product of input current and input voltage of the converter and a power reference. The analysis of sliding motions has demonstrated that stable CPL behavior can be induced in boost, Ćuk and SEPIC converters. The theoretical predictions have been verified by both PSIM© simulations and measurements in a prototype of each converter. The reported technique results in an efficient design of simple and inexpensive CPL emulators.

Appendix A
Analysis of the Alternative Sliding Surface

The time derivative of the sliding function (5) becomes as follows

$$\frac{dS(x)}{dt} = \frac{di_1}{dt} + \frac{P_{\rm ref}}{v_1^2}\frac{dv_1}{dt} \tag{A.1}$$

$$s^3+(\frac{P_{\rm ref}+I_{L2}^*V_g}{C_1V_{C1}^{*2}}+\frac{1}{RC_2})s^2+(\frac{P_{\rm ref}+I_{L2}^*V_g}{RC_2C_1V_{C1}^{*2}}+\frac{1}{L_2C_2}+\frac{V_{C2}^*}{L_2C_1V_{C1}^*})s+\frac{V_{C2}^*}{L_2C_1V_{C1}^*}\frac{1}{RC_2}+\frac{P_{\rm ref}+I_{L2}^*V_g}{L_2C_2C_1V_{C1}^{*2}}=0 \text{ (Ćuk)} \quad (55)$$

$$s^3+(\frac{P_{\rm ref}(C_1+C_2)}{(V_g+V_{C2}^*)V_{C2}^*C_1C_2}+\frac{1}{RC_2})s^2+\frac{1}{(V_g+V_{C2}^*)C_1}(\frac{P_{\rm ref}}{V_{C2}^*}\frac{1}{RC_2}+\frac{V_{C2}^*}{L_2})s+\frac{1}{L_2C_2}\frac{2I_{L2}^*}{C_1(V_g+V_{C2}^*)}=0 \text{ (SEPIC)} \quad (56)$$

$$s^3+(\frac{1}{RC_1}+\frac{1}{RC_2})s^2+(\frac{C_1+C_2}{L_2C_1C_2}+\frac{1}{R^2C_1C_2})s+\frac{2}{RL_2C_1C_2}=0 \quad \text{(BOF)} \quad (57)$$

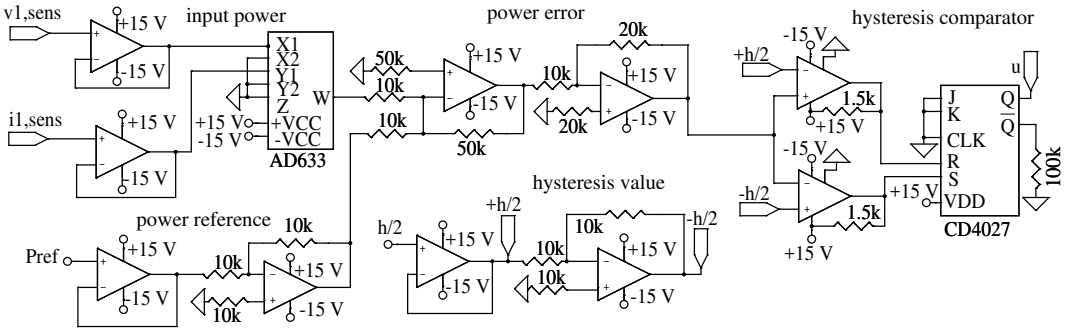

Fig. 6. Circuit scheme of the proposed SMC for CPL synthesis.

The following analysis corresponds to the boost converter. Hence, from (7), (6) and (9), the conditions for the existence of sliding mode are given by

$$\left.\frac{dS(x)}{dt}\right|_{u=1} = \frac{v_1}{L_1}+\frac{P_{\rm ref}}{v_1^2}\frac{dv_1}{dt}>0 \quad (A.2)$$

$$\left.\frac{dS(x)}{dt}\right|_{u=0} = -\frac{v_{C2}}{L_1}+\frac{v_1}{L_1}+\frac{P_{\rm ref}}{v_1^2}\frac{dv_1}{dt}<0 \quad (A.3)$$

Note that (A.2) can be rewritten as follows

$$-\frac{dv_1}{v_1^3}<\frac{1}{L_1P_{\rm ref}}dt \quad (A.4)$$

Integrating the above equation leads to

$$\frac{1}{v_1^2(t)}-\frac{1}{v_1^2(t_0)}<2\frac{t-t_0}{L_1P_{\rm ref}} \quad (A.5)$$

On the other hand, considering that $v_{C2}=\alpha v_1$ and $\alpha>1$, (A.3) becomes as follows

$$\frac{dv_1}{v_1^3}<(\alpha-1)\frac{1}{L_1P_{\rm ref}}dt \quad (A.6)$$

Integrating (A.6), we obtain

$$-\left(\frac{1}{v_1^2(t)}-\frac{1}{v_1^2(t_0)}\right)<2(\alpha-1)\frac{t-t_0}{L_1P_{\rm ref}} \quad (A.7)$$

In order to ensure existence of sliding motions, from (A.5) and (A.7) the following constraints must be satisfied

$$\frac{1}{v_1^2(t_0)}-2(\alpha-1)\frac{t-t_0}{L_1P_{\rm ref}}<\frac{1}{v_1^2(t)}<\frac{1}{v_1^2(t_0)}+2\frac{t-t_0}{L_1P_{\rm ref}} \quad (A.8)$$

for $t>t_0$.

Particularizing (34) for (A.1), the equivalent control (u_{eq}) results in

$$u_{eq}=1+\frac{v_1}{v_{C2}}+\frac{L_1P_{\rm ref}}{v_{C2}v_1^2}\frac{dv_1}{dt} \quad (A.9)$$

The ideal sliding dynamics is obtained by substituting the signal control u by the equivalent control u_{eq} and imposing the condition $S(x)=0$, which yields to

$$C_2v_{C2}\frac{dv_{C2}}{dt}=P_{\rm ref}-\frac{v_{C2}^2}{R}+\frac{L_1P_{\rm ref}^2}{v_1^3}\frac{dv_1}{dt} \quad (A.10)$$

Defining $x=\frac{1}{2}C_2v_{C2}^2$, (A.10) becomes

$$\frac{dx}{dt}=-\frac{2}{RC_2}x+P_{\rm ref}+\frac{L_1P_{\rm ref}^2}{v_1^3}\frac{dv_1}{dt} \quad (A.11)$$

Note that in steady-state, it can be considered that $\frac{dx}{dt}=\frac{dv_1}{dt}=0$, which implies

$$X^*=\frac{RC_2P_{\rm ref}}{2} \quad \Rightarrow \quad V_{C2}^*=\sqrt{RP_{\rm ref}} \quad (A.12)$$

Consequently, if $\frac{dv_1}{dt}$ is equal to zero, the equilibrium point in (A.12) is asymptotically stable.

Nonetheless, in the case that $\frac{dv_1}{dt}$ will be different from zero, solving (A.11), we have

$$x(t)=e^{-\frac{2}{RC_2}t}x(0)+\frac{RC_2P_{\rm ref}}{2}(1-e^{-\frac{2t}{RC_2}})+\int_0^t\frac{L_1P_{\rm ref}^2}{v_1^3(\tau)}\frac{dv_1(\tau)}{d\tau}e^{-2\frac{t-\tau}{RC_2}}d\tau \quad (A.13)$$

It can be observed that (A.13) will be bounded provided that the function $\frac{L_1P_{\rm ref}^2}{v_1^3(t)}\frac{dv_1}{dt}$ will be also bounded. Besides, if the existence of sliding motions is guaranteed, we obtain the following condition for stability

$$-P_{\rm ref}<\frac{L_1P_{\rm ref}^2}{v_1^3(t)}\frac{dv_1}{dt}<\left(\frac{v_{C2}}{v_1}-1\right)P_{\rm ref} \quad (A.14)$$

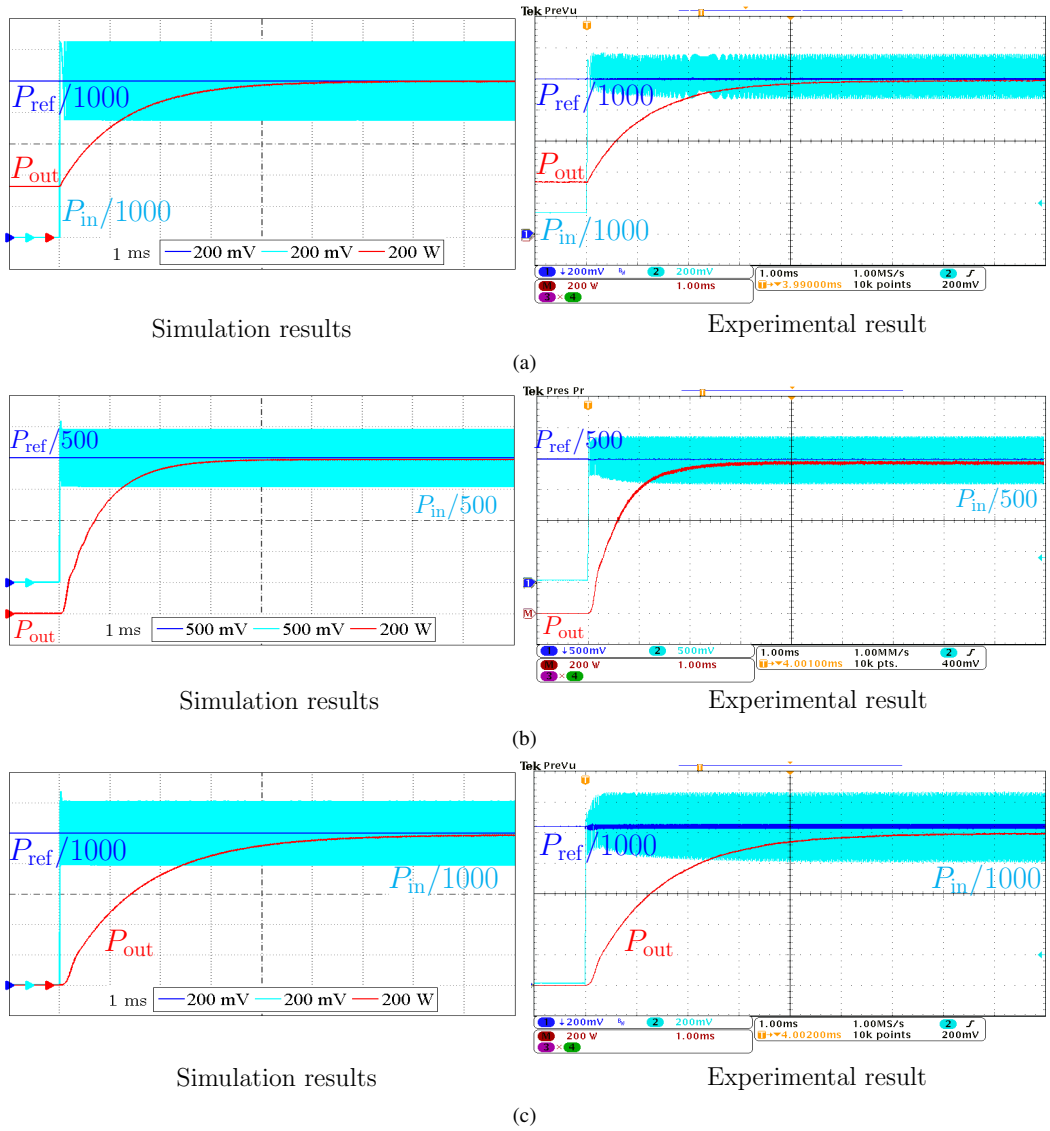

Fig. 7. Simulated and experimental waveforms of input power, power reference and output power in the a) boost converter, b) Ćuk converter and c) SEPIC converter operating as instantaneous CPL during start-up and steady-state.

APPENDIX B
FINITE-TIME CONVERGENCE

The sliding-mode existence conditions (6) can be written as follows

$$S(x)\frac{dS(x)}{dt} \leq -m|S(x)|, \quad m > 0 \tag{B.1}$$

where $m \leq |S(x(0))|/T_r$ is selected to guarantee a given finite reaching time T_r. Let us assume that $dS(x)/dt$ is given by (A.1) which is particularized here in compact form for the boost converter

$$\frac{dS(x)}{dt} = -\frac{v_{C2}}{L_1}\frac{1+\text{sign}(S(x))}{2} + \frac{v_1}{L_1} + \frac{P_{\text{ref}}}{v_1^2}\frac{dv_1}{dt} \tag{B.2}$$

For $S(x) > 0$, (B.2) becomes

$$\frac{dS(x)}{dt} = -\frac{v_{C2}}{L_1} + \frac{v_1}{L_1} + \frac{P_{\text{ref}}}{v_1^2}\frac{dv_1}{dt} \leq -m \tag{B.3}$$

If $v_{C2} > v_1$, $dS(x)/dt$ in (B.2) will be always negative if $dv_1/dt < 0$. We define M_1 as follows

$$M_1 \geq \frac{v_1}{L_1} + \left|\frac{P_{\text{ref}}}{v_1^2}\frac{dv_1}{dt}\right| \tag{B.4}$$

Hence, $dS(x)/dt$ in (B.3) will be also negative for $dv_1/dt > 0$ provided that $v_{C2}/L_1 > M_1$. Therefore, we obtain in (B.3)

$$M_1 - \frac{v_{C2}}{L_1} \leq -m \tag{B.5}$$

Equivalently

$$\frac{v_{C2}}{L_1} \geq m + M_1 \tag{B.6}$$

Similarly, for $S(x) < 0$, we obtain

$$\frac{dS(x)}{dt} = \frac{v_1}{L_1} + \frac{P_{\text{ref}}}{v_1^2}\frac{dv_1}{dt} \tag{B.7}$$

which is always positive for $dv_1/dt > 0$. Let M_2 be a positive constant such that

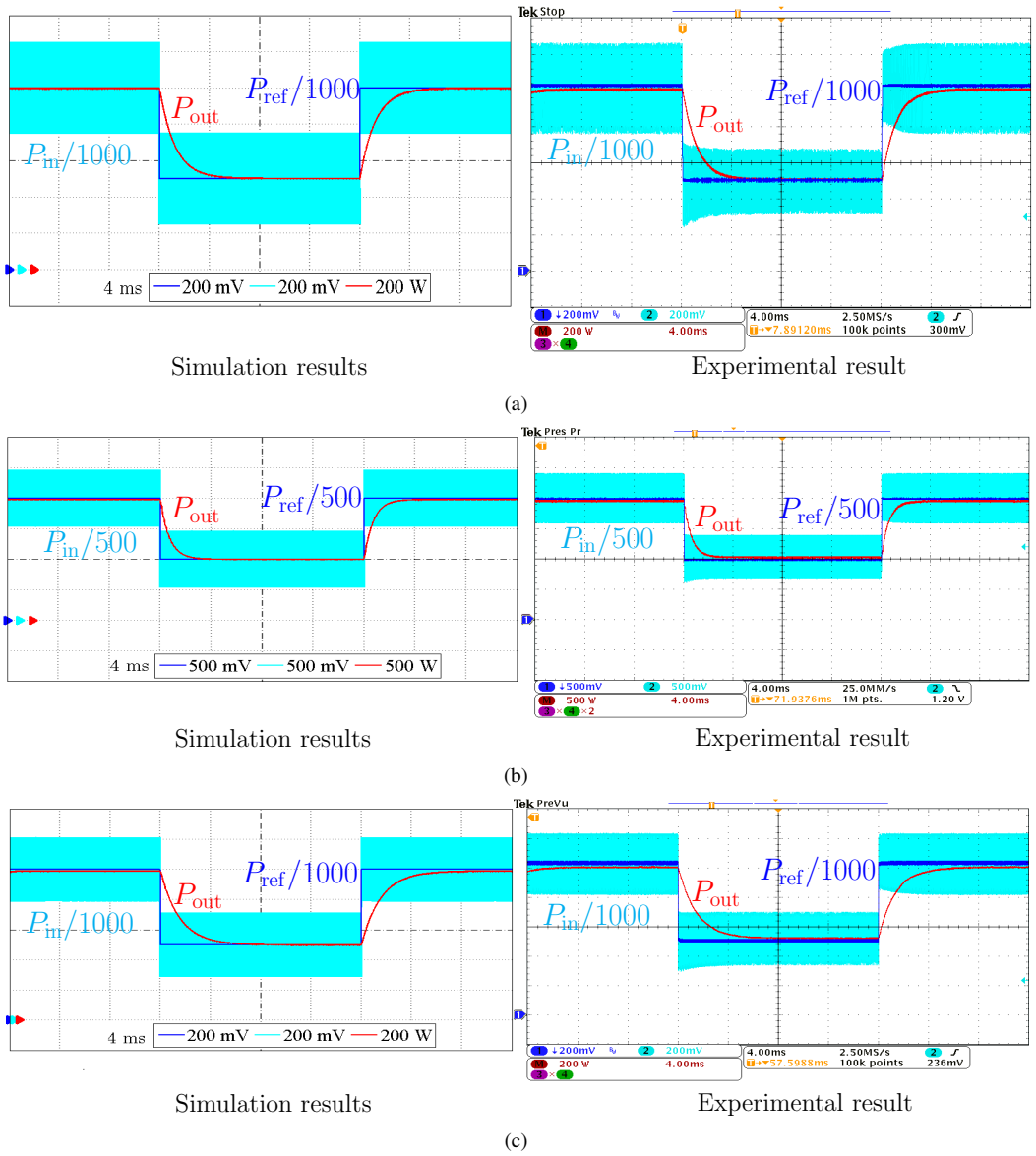

Fig. 8. Transient response of input power and output power in the a) boost converter, b) Ćuk converter and c) SEPIC converter when the power reference changes.

$$M_2 > \left| \frac{P_{\text{ref}}}{v_1^2} \frac{dv_1}{dt} \right| \tag{B.8}$$

Therefore, $dS(x)/dt$ will be also positive in (B.7) for $dv_1/dt < 0$ provided that

$$\frac{v_1}{L_1} > M_2 \tag{B.9}$$

Note that for $S(x) < 0$, one has

$$S(x)\frac{dS(x)}{dt} = -|S(x)| \left(\frac{v_1}{L_1} + \frac{P_{\text{ref}}}{v_1^2} \frac{dv_1}{dt} \right) \leq -m|S(x)| \tag{B.10}$$

Hence, we derive from (B.10)

$$\frac{v_1}{L_1} + M_2 \leq m \tag{B.11}$$

Equivalently,

$$\frac{v_1}{L_1} \leq m - M_2 \tag{B.12}$$

Taking into account constraints (B.6) and (B.12), we finally obtain

$$\frac{v_1}{L_1} + M_2 \leq m \leq \frac{v_{C2}}{L_1} - M_1 \tag{B.13}$$

which guarantees finite-time convergence to the switching surface Σ. In the particular case of $v_1 = V_g = \text{const.}$, (B.13) becomes

$$\frac{v_1}{L_1} \leq m \leq \frac{v_{C2}}{L_1} - \frac{V_g}{L_1} \tag{B.14}$$

The conditions (B.13) and (B.14) guarantee respectively finite-time convergence to the switching manifold in the case of variable and constant input voltage v_1.

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