Fast-Scale Stability Analysis of a DC-DC Boost Converter with a Constant Power Load

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***Abstract*—This paper focuses on analyzing the fast scale stability in a peak current-mode-controlled boost converter with a constant power load. Since with this kind of nonlinear loads the analytical expression of the discrete time model is not available and the existing averaged models are inadequate in describing accurately the fast scale dynamics of these converters, a piecewise linear switched model is established by approximating the constant power load by a composite linear load. The model is first demonstrated to predict accurately the same bifurcation points predicted by the switched model using the nonlinear load. The bifurcation analysis using Floquet theory and the resulting monodromy matrix and its eigenvalues loci clearly shows the effect of system parameters on its stability. The fast scale stability boundaries in terms of suitable parameters are obtained by using eigenvalues analysis. The effect of the proportional gain of the voltage controller is studied. Finally, experimental results are further given to verify the theoretical analysis and simulation results obtaining a good agreement.**

***Index Terms*—switching converters, conversion, nonlinear load, constant power load, stability analysis, fast scale stability, sunharmonic oscillation**

I. Introduction

ELECTRIC energy systems reliability is fundamental to guarantee their correct operation. Many undesired nonlinear phenomena can arise in dc-dc switching converters that are indispensable parts of modern energy systems. These phenomena can significantly downgrade the system performance. Understanding the behavior of switching power converters is essential to determine the safe operating conditions, and subsequently, prevent undesired operating behavior. Bifurcation analysis can offer an in-depth understanding of these behaviors. In recent years, this approach has been used in a substantial amount of research works. The analysis, prediction and control of these behaviors have increasingly become of great concern of many researchers all over the world [1]–[12].

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Switching converters with a resistive load are piecewise linear systems. In the past, these systems have been widely studied and it has been shown that they can exhibit a rich variety of complex nonlinear dynamic phenomena such as subharmonic oscillation [13], [14] known also as fast-scale instability [15] or period-doubling bifurcation [1], [10], [16]. They also can exhibit Hopf or Neimark-Sacker bifurcation [9], [17] and Border collision bifurcations [18], [19]. Bifurcations taking place at the slow scale such as Hopf bifurcation can be predicted by averaged models [20]. However, this model cannot predict fast scale instabilities such as period doubling bifurcation leading to subharmonic oscillation. Fast scale bifurcations require more accurate mathematical tools such as discrete-time models [1], [12], [15], [18], [19], [21], [22] and Floquet theory combined with Filippov method [1], [23]. Both approaches lead to the derivation of the monodromy matrix which is an effective tool to accurately analyze the stability of dc-dc switching converters at both fast and slow scale.

The load types for dc-dc switching power converters could be mainly resistive or constant impedance load, capacitive load, constant voltage or battery load, constant current load or inductive impedance load. Most of the existing research papers on nonlinear dynamics of switching converters have focused on the previous linear loads. The derivation of the discrete-time models in this case is based on the description of dc-dc switching converters as piecewise linear system. Nevertheless, it has been shown in the literature that in some industrial applications such as in distributed power systems [24], [25], power factor correction [26], electrical vehicles [27], [28], microgrids [29], [30], more electric aircrafts [31] and electric ships [32] the load is of a constant power nature. With this kind of load, the switched model is no more piecewise linear and the nonlinearity of the resulting differential equation precludes the use of matrix-based system state solutions for obtaining the discrete time model since the model of the power stage becomes nonlinear and these solutions are not available in closed form. Therefore, the existing used techniques for linear resistive loads are not directly applicable to the case of a Constant Power Load (CPL). This explains why the vast majority of existing works considering nonlinear CPL deals only with the low frequency behavior of the converter using averaged models.

Obtaining suitable ways for accurately tackling the problem is extremely important for dealing with accurate fast scale stability analysis of switching converters loaded by a CPL. Some works have been carried out recently in [33], [34] using discrete time models obtained numerically. Although these

works provide faithful results, the complexity of the techniques used to obtain them prevents their use by power electronics researchers.

This paper presents a new alternative approach to obtain a piecewise linear switched model for accurate fast scale stability analysis which is as easy to use as with the case of linear loads but still providing the accuracy of the original switched model with a nonlinear CPL. Reasonable approximation of the nonlinear load is applied to provide a simple model for fast-scale stability analysis resulting in accurate determination of parametric regions where stability at the fast scale is guaranteed. It is worth to note that the dynamics of the inductor current is linear and in the case of open voltage loop the results available for the case of resistive load can be applied to the case of a CPL. However, it is well known that the voltage loop ripple can have either a stabilizing or a destabilizing effect on the subharmonic oscillation boundary [3], [8]. Therefore, with voltage loop closed, the study of subharmonic oscillation in switching converters with CPLs becomes challenging. Our conjecture is that the subharmonic oscillation is a local instability of the limit cycle of the switched system that can be predicted by a piecewise linear (PWL) switched model which can be obtained by linearizing the CPL in the vicinity of its operating point.

This paper uses bifurcation analysis to study the fast scale stability in a dc-dc boost converter with CPL in terms of system parameters. Using the nonlinear models of the converter and the CPL, the dynamics of the system is first explored in terms of the voltage feedback gain using a circuit-level switched model. It is first shown that the stability of the fundamental periodic orbit may be lost by a period-doubling bifurcation leading to the exhibition of subharmonic oscillation and other complex nonlinear behaviors. In particular, for duty cycle values lower than, ideally, 0.5, the feedback gain has a destabilizing effect while for duty cycle values larger than 0.5, this gain has a stabilizing effect. Experimental measurements are provided to validate the theoretical predictions and the numerical simulations resulting in a good agreement.

The rest of this paper is organized as follows. After this introduction, from here forward, Section II presents the description of the system under study which consists of a dc-dc boost converter loaded by a CPL. The dynamics of the system is explored in Section III in terms of the system parameters using a circuit-level switched model of the boost converter implemented in PSIM© software and the nonlinear model of the CPL by varying different parameters. Simulations are repeated for the same system by substituting the CPL by its linearized model showing that for predicting subharmonic oscillations and other kind of fast scale instabilities, the nonlinearity of the CPL is not relevant and that a linear model can be used. In section IV the piecewise linear model of the system is obtained from which an approximate and accurate stability analysis is performed in Section V. Stability boundaries in terms of some parameters are obtained in Section VI. An experimental validation of some of the results is provided in Section VII and finally concluding remarks are given in Section VIII.

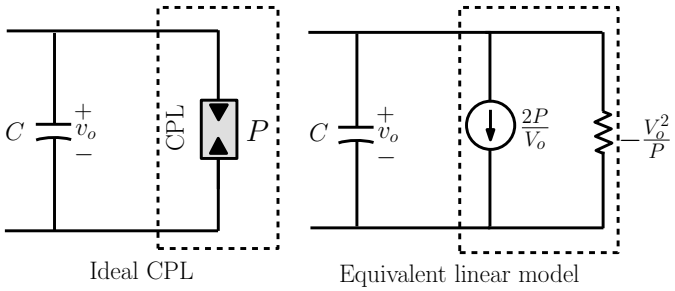


Fig. 1. Output terminal of a dc-dc converter showing the capacitor in parallel with the CPL.

II. The nonlinear model of the CPL

Fig. 1-a shows the output terminals of a dc-dc converter with a CPL. This load can be described by the following nonlinear model [28]

$$i_o = \frac{P}{v_o} \tag{1}$$

Therefore, the describing equation for output terminal of a dc-dc converter with capacitor in parallel with the CPL can be expressed as follows

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_X}{C} - \frac{P}{v_o C} \tag{2}$$

where i_X is the current flowing to the output terminal which coincides with the inductor current for the case of the buck converter and with the diode current for the boost and buck-boost converters. The nonlinear nature of the capacitor voltage dynamics, due to its connection with the CPL can clearly be observed (2).

The CPL can be linearized around its operating point of voltage V_o and power P as shown in Fig. 1-b. Following the same procedures as in [28], once the system is working close to operating point, the model of the CPL can be substituted by its linear Norton equivalent circuit which includes a current source I_o in parallel with the dynamic negative resistance R_o [28].

$$i_o = \frac{v_o}{R_o} + I_o \tag{3}$$

where R_o and I_o are given by the following equations

$$R_o = -\frac{V_o^2}{P}, \quad I_o = \frac{2P}{V_o} \tag{4}$$

After linearizing the CPL, the capacitor voltage equation becomes as follows

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_X}{C} - \frac{2P}{CV_o} - \frac{v_o}{R_o C} \tag{5}$$

Then, the resulting negative incremental resistance can be used in a mathematical description similar to the case of resistive load while the current source can be considered as an external input. Definitely, the CPL can be represented with a composite load consisting of the parallel connection of a negative resistance and a dc current source.

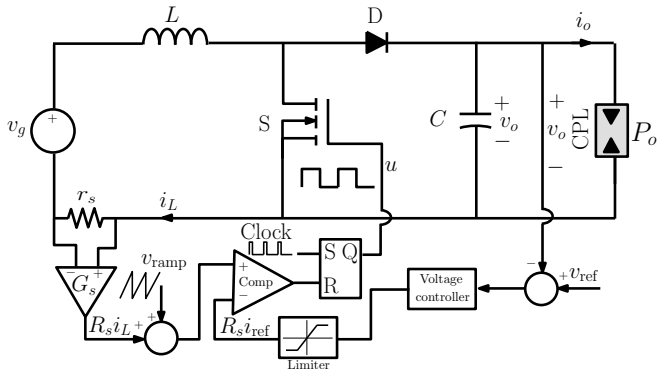


Fig. 2. Schematic circuit diagram of a boost converter under current mode control with a PWM strategy and loaded by a CPL.

III. The boost converter loaded by a CPL

The system under study is presented in Fig. 2. The power processing unit is a dc-dc boost converter with a constant input voltage and loaded by a CPL. The power converter stage is controlled using a two loop strategy where the outer voltage loop provides the reference signal for the inner current loop using fixed frequency peak current mode control. The ON/OFF binary driving signal u for the switch S is generated by a comparator and a set-reset (SR) latch as shown in Fig. 2. Its duty cycle is generated according to the comparison between the sensed current $R_s i_L$ and its reference $R_s i_{\text{ref}}$ after subtracting a compensating ramp signal v_{ramp} whose amplitude is V_M and whose period is T hence with a slope $m_a = V_M/T$.

The reference signal $R_s i_{\text{ref}}$ is provided by the outer voltage loop regulating the CPL voltage v_o to a desired voltage v_{ref}. The outer voltage controller is a PI compensator having a proportional gain κ_p and a time constant τ. The control logic works as follows. The switch S is forced to be ON at the starting of each switching cycle. If $R_s i_L$ reaches $R_s i_{\text{ref}} - v_{\text{ramp}}$, the switch S is turned OFF.

During start-up, a dc-dc converter may exhibit an unacceptable inrush current. To avoid this, a limiter is placed at the output of the PI compensator.

IV. Steady-state Behavior of the System: Simulation Results from the Circuit-level Switched Model

TABLE I
The fixed parameter values

v_{ref}	L	C	P	V_M	T	τ
48 V	200 μH	130 μF	48 W	1 V	25 μs	1 ms

In this section, the dynamical behavior of the system is explored in order to gain insight on suitable ways of obtaining an appropriate model that can be used for a mathematical stability analysis. First, the system has been carefully studied through simulations using the switched model of the converter loaded with the ideal nonlinear model of the CPL. Bifurcation diagrams have been obtained using the exact circuit-level switched model of PSIM© by varying the proportional gain κ_p for two different values of the steady duty cycle. The fixed parameter values used for the rest of the study are reported in Table I.

A convenient way of having a panoramic view of the stability status under the varying parameter without any mathematical analysis and using the nonlinear model of the system is through the brute force bifurcation diagrams. In obtaining such diagrams, a suitable variable is sampled at every clock instant and the corresponding data is represented when a parameter varies. If the system exhibits a $T-$periodic regime in steady-state, all the sampled points will have the same value and they will represent a single point. When $2T-$ periodic subharmonic regime takes place in steady-state, one gets two points instead of one, and so on. The simulation is run for sufficiently long time to allow the system to reach its steady-state. The bifurcation diagrams represented below are obtained by computing the inductor current i_L at every switching cycle nT during a sufficiently large time interval $(0, t_{\text{sim}})$, $t_{\text{sim}} > t_c$, where t_c is the time instant at which the average voltage $\overline{v}_o$ reaches the desired voltage v_{ref} which is approximately given by [35]

$$t_c = t_r + \frac{R_s C}{2((R_s I_{\text{lim}} - m_a T)v_g - R_s P)}(v_{\text{ref}}^2 - v_g^2) \quad (6)$$

where t_r is the time instant at which the current line $\overline{i}_L$ reaches the current limit I_{lim} established by the limiter at the output of the PI voltage controller.

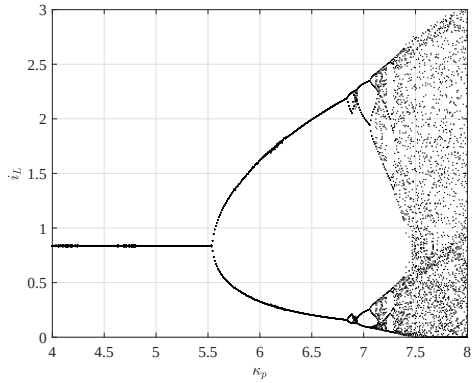
$$t_r = \frac{R_s I_{\text{lim}} - m_a T}{R_s m_1} \quad (7)$$

where $m_1 = v_g/L$ is the inductor current slope during the ON interval.

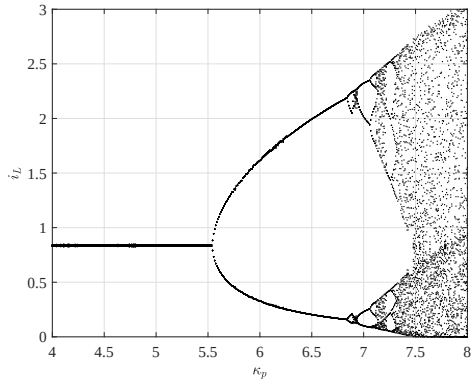
The data obtained during time transient within the startup phase and during the transient regime of the regulation phase are fully eliminated. Only the last 50 samples of the state variables are considered as steady-state in the computed bifurcation diagrams.

Fig. 3-a shows the bifurcation diagram of the system without slope compensation ($m_a = 0$) a steady-state duty cycle $D = 0.33$. Fig. 3-b shows the bifurcation under the same conditions but with the nonlinear CPL substituted by its linearized composite model constituting of a linear negative resistance and a current sink. It can be observed that the matching between the two bifurcation diagrams is excellent. It is widely believed among power electronics community that with values of steady-state duty cycles less than 0.5, no external ramp is needed to achieve a stable and well-damped, wide bandwidth current control and this could lead to simplifying the control integrated-circuit design and reduce the cost. However, from the previous bifurcation diagrams it is clear that the system is still prone to subharmonic oscillation even for $D < 0.5$ if the gain is increased beyond $\kappa_p = 5.5$. Therefore, a ramp slope compensation is also necessary for duty cycle values less than 0.5 like with the case of a resistive load [3], [8].

Fig. 4-a shows the bifurcation diagram of the system with slope compensation and with a steady-state duty cycle

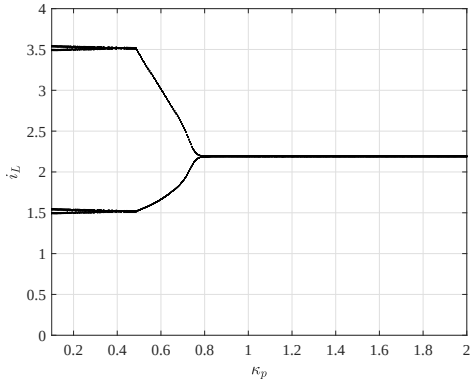


(a) $v_g = 32$ V ($D \approx 0.33 < 0.5$) and $m_a = 0$

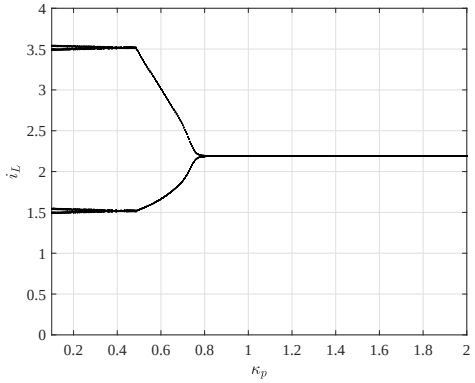


(b) $v_g = 32$ V ($D \approx 0.33 < 0.5$) and $m_a = 0$

Fig. 3. Bifurcation diagrams of the boost converter loaded by a CPL showing the inductor current i_L at time instants nT by taking the voltage proportional gain κ_p as a bifurcation parameter for $v_g = 32$ V ($D = 0.33$) showing that a slope compensation is needed even for $D < 0.5$ if $\kappa_p \geq 5.5$ hence the voltage feedback has a destabilizing effect in this case.



(a) $v_g = 16$ V ($D \approx 0.66 > 0.5$) and $m_a = 40$ kV/s



(b) $v_g = 16$ V ($D \approx 0.66 > 0.5$) and $m_a = 40$ kV/s

Fig. 4. Bifurcation diagrams of the boost converter loaded by a CPL showing the inductor current i_L at time instants nT by taking the voltage proportional gain κ_p as a bifurcation parameter for $v_g = 16$ V ($D \approx 0.66$) showing that by increasing the proportional gain κ_p the system is stabilized. Indeed, in this case the needed ramp slope m_a is smaller than the predicted by the conventional approach ignoring the effect of the outer loop.

$D \approx 0.66$. Fig. 4-b shows the bifurcation under the same conditions but with the nonlinear CPL substituted by its linearized composite model. Again, the matching between the two bifurcation diagrams is remarkable.

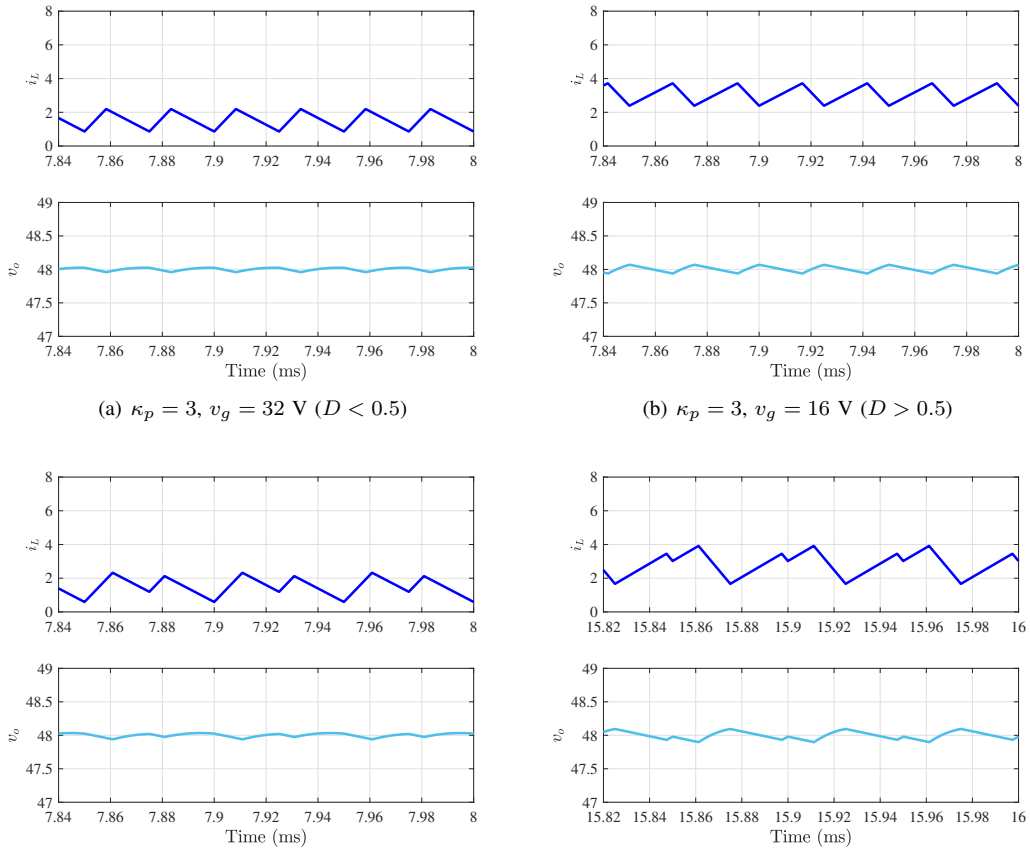
It can be observed that for $D > 0.5$, the voltage loop has a stabilizing effect since when the proportional gain κ_p is increased beyond a critical value $\kappa_p \approx 0.79$, subharmonic oscillation disappears. Furthermore, the ramp slope m_a needed for $\kappa_p > 0.79$ is smaller than the one obtained when ignoring the effect of the voltage loop. Note that with a higher value of κ_p not only the system is more stable at the fast scale hence having the tendency to remove subharmonic oscillation, but also the performance of the system is better in terms of settling time and overshoot at the slow scale. However, there is a limit for the proportional gain beyond which the system can undergo slow scale instability [35].

The effect of the voltage-loop on the fast scale stability has been analytically derived in [3] and [8] for different conventional converter topologies with a constant resistance or with a constant current sink as loads. In particular, for the boost converter with the previous linear loads, it has been shown that the output voltage feedback loop has a stabilizing effect on the subharmonic oscillation for values of duty cycle D larger than 0.5. This is also the case for the same converter with a CPL.

Numerical simulations using PSIM© were performed to check the dynamics of the system in both sides of the period doubling bifurcation point. The steady-state waveforms obtained at both sides are depicted in Fig. 5 for two different values of the considered duty cycles. Fig. 5-a and Fig. 5-b show the time domain waveforms of the state variables in the case of a stable periodic regime.

Let $v_g = 32$ V ($D < 0.5$) . According to Fig. 3, the critical value of the proportional gain is $\kappa_p \approx 5.55$. Let $\kappa_p = 3$, the converter is stable as predicted in Fig. 3 and confirmed by time domain numerical simulations depicted in Fig. 5(a). Let $\kappa_p = 6.5$, the converter exhibits subharmonic oscillation as predicted in Fig. 3 and confirmed by the simulations shown in Fig. 5(c).

Let $v_g = 16$ V ($D > 0.5$) . According to Fig. 4, the critical value of the proportional gain is $\kappa_p \approx 0.79$. Let $\kappa_p = 3$, the converter is stable as predicted in Fig. 4 and confirmed by time domain numerical simulations depicted in Fig. 5(b). Let $\kappa_p = 0.4$, the converter exhibits subharmonic oscillation as predicted in Fig. 4 and confirmed by the simulations shown in Fig. 5(d).



(a) $\kappa_p = 3$, $v_g = 32$ V ($D < 0.5$)

(b) $\kappa_p = 3$, $v_g = 16$ V ($D > 0.5$)

(c) $\kappa_p = 6.5$, $v_g = 32$ V ($D < 0.5$)

(d) $\kappa_p = 0.4$, $v_g = 16$ V ($D > 0.5$)

Fig. 5. Simulated time domain waveforms showing the steady-state inductor current i_L and the output capacitor voltage v_o for two different values of steady-state duty cycle D and κ_p before and after subharmonic oscillation takes place.

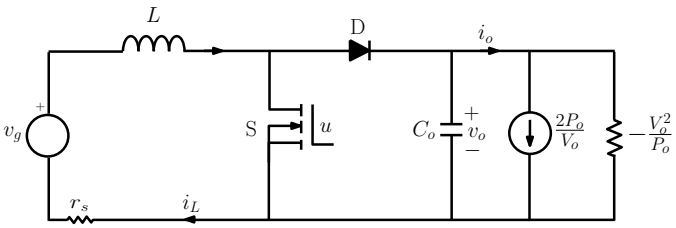


Fig. 6. Schematic diagram of the boost converter after linearizing the CPL.

V. State-space switched piecewise linear model for fast scale stability analysis

The mathematical model developed here reveals the impact of parameter variations on system steady-state behavior. Let $\mathbf{x} = (v_o,\ i_L)^\intercal$. By replacing the model of the CPL by its linearized expression, the boost converter with a CPL can be described by the schematic circuit diagram depicted in Fig. 6. If this circuit diagram is used instead of the one with the nonlinear CPL, the system can be described by a piecewise linear switched model as follows on system steady-state behavior. Let $\mathbf{x} = (v_o,\ i_L)^\intercal$. By replacing the model of the CPL by its linearized expression, the boost converter with a CPL can be described by the schematic circuit diagram depicted in Fig. 6. If this circuit diagram is used instead of the one with the nonlinear CPL, the system can be described by a piecewise linear switched model as follows

$$\dot{\mathbf{x}} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{w}, \quad \text{for} \quad u = 1, \tag{8a}$$
$$\dot{\mathbf{x}} = \mathbf{A}_0\mathbf{x} + \mathbf{B}_0\mathbf{w}, \quad \text{for} \quad u = 0, \tag{8b}$$
$$\dot{v}_i = v_{\text{ref}} - v_o, \tag{8c}$$

where $v_i := \int (v_{\text{ref}} - v_o)\mathrm{d}t$ is the integral of the error signal $v_{\text{ref}} - v_o$, $\mathbf{A}_0 \in \mathbb{R}^{2\times2}$, $\mathbf{A}_1 \in \mathbb{R}^{2\times2}$, $\mathbf{B}_0 \in \mathbb{R}^{2\times2}$ and $\mathbf{B}_1 \in \mathbb{R}^{2\times2}$ are the system state matrices presented below and $\mathbf{w}$ is the vector of the external inputs of the system supposed to be constant within a switching cycle. By using Fig. 6, the system matrices and vectors are given as follows:

$$\mathbf{A}_1 = \begin{pmatrix} \frac{P}{v_{\text{ref}}^2 C} & 0 \\ 0 & -\frac{r_s}{L} \end{pmatrix}, \mathbf{A}_0 = \begin{pmatrix} \frac{P}{v_{\text{ref}}^2 C} & \frac{1}{C} \\ -\frac{1}{L} & -\frac{r_s}{L} \end{pmatrix}, \tag{9a}$$

$$\mathbf{B}_1 = \mathbf{B}_0 = \begin{pmatrix} 0 & -\frac{1}{C} \\ \frac{1}{L} & 0 \end{pmatrix}, \ \mathbf{w} = \begin{pmatrix} v_g \\ \frac{2P}{v_{\text{ref}}} \end{pmatrix} \tag{9b}$$

With both inner current and outer voltage loops closed, the current reference $R_s i_{\text{ref}}$ for the inner loop is provided by the

output of the voltage controller according to the following expression:

$$R_s i_{\rm ref} = \kappa_p(v_{\rm ref} - v_o) + W_i v_i, \tag{10}$$

where $W_i = \kappa_p/\tau$ is the integral gain of the PI compensator, τ being its time constant. The closed loop model can be obtained by taking into account the switching condition which dictates the duty cycle cyclically. The switching from the ON to the OFF phase takes place whenever the signal $R_s i_L$ and the signal $R_s i_{\rm ref} - v_{\rm ramp} := \kappa_p(v_{\rm ref} - v_o) + W_i v_i - v_{\rm ramp}$ intersect, i.e, whenever the following equality holds:

$$\kappa_p(v_{\rm ref} - v_o) + W_i v_i - R_s i_L - v_{\rm ramp} = 0, \tag{11}$$

where $v_{\rm ramp} = m_a t \bmod T$. The expression (11) can be written as follows

$$\kappa_p v_{\rm ref} + W_i v_i(d_n T) + \mathbf{K}\mathbf{x}(d_n T) - v_{\rm ramp}(d_n T) = 0, \tag{12}$$

where $\mathbf{K} = (-\kappa_p, \quad -R_s)$ is the vector of feedback gains and d_n is the discrete-time duty cycle during the $n^{\rm th}$ switching cycle. The system of equations (8a)-(8c) together with (12) establish the nonlinear switched model of the system. The steady-state duty cycle D can be obtained by simply performing a net volt-second balance in steady-state regime [36] leading to

$$D = \frac{2(v_{\rm ref} + V_F) - v_g}{2(v_{\rm ref} + V_F)} - \sqrt{\frac{v_g^2}{4(v_{\rm ref} + V_F)^2 - \frac{r_s}{R_o}}}. \tag{13}$$

Hence, for a fixed value of the desired output voltage $v_{\rm ref}$, if the input voltage v_g is fixed, the steady-state operating duty cycle D is determined according to (13) where the value of $V_F = 0.7$ V has been considered for the forward voltage of the diode. This value has been introduced to improve the matching between the simulation results and the experimental measurements to be presented later. Therefore, there is no need to numerically solve the equation resulting from the switching condition (12) to obtain the steady-state duty cycle D.

VI. Orbital stability analysis

The stability of periodic orbits of a nonlinear system can be analyzed by checking the evolution of a small perturbation in the vector of the state variables within one period. This problem can be tackled by different ways. One of the most used techniques is to analyze the stability of the fixed points of the Poincaré map of the system by using its Jacobian matrix. The periodic orbit will be stable if this matrix evaluated at the associated fixed point has all the eigenvalues with modulus less than 1. Another technique is by using Floquet theory combined with Filippov method which leads to the same results [23]. The Jacobian matrix of the Poincaré map (discrete-time model) coincides with the monodromy matrix.

To perform a stability analysis of the system, Floquet theory is used here and therefore the monodromy matrix $\mathbf{M}$ is first obtained. Let $\mathbf{x}(DT) = (\mathbf{I} - \mathbf{\Phi})^{-1}\mathbf{\Psi}$ be the steady-state value of $\mathbf{x}(t)$ at time instant DT, where $\mathbf{\Phi} = \mathbf{\Phi}_1\mathbf{\Phi}_0$, $\mathbf{\Phi}_1 = e^{\mathbf{A}_1 DT}$, $\mathbf{\Phi}_0 = e^{\mathbf{A}_0(1-D)T}$, $\mathbf{\Psi}_1 = (e^{\mathbf{A}_1 DT} - \mathbf{I})\mathbf{A}_1^{-1}\mathbf{B}\mathbf{w}$, $\mathbf{\Psi}_0 = (e^{\mathbf{A}_0(1-D)T} - \mathbf{I})\mathbf{A}_0^{-1}\mathbf{B}\mathbf{w}$, $\mathbf{\Psi} = \mathbf{\Phi}_1\mathbf{\Psi}_0 + \mathbf{\Psi}_1$. Let $\mathbf{m}_1(\mathbf{x}(t)) = \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{w}$ and $\mathbf{m}_0(\mathbf{x}(t)) = \mathbf{A}_0\mathbf{x}(t) + \mathbf{B}_0\mathbf{w}$.

The integral variable has a negligible effect on the fast scale stability boundary apart from fixing the steady-state duty cycle [7]. However, to take into account the integral variable and the integral gain in the analysis, let us define the augmented state vector $\mathbf{x}_a = (v_o,\ i_L,\ v_i)^\intercal$. Let the augmented matrices $\mathbf{A}_{a1}$, $\mathbf{B}_{a1}$, $\mathbf{A}_{a0}$, $\mathbf{B}_{a0}$, augmented feedback vector $\mathbf{K}_a$ and augmented vector of external parameters $\mathbf{w}_a$ be as follows

$$\mathbf{A}_{a1} = \begin{pmatrix} \mathbf{A}_1 & \mathbf{0} \\ -1 & \mathbf{0} \end{pmatrix},\ \mathbf{B}_{a1} = \begin{pmatrix} \mathbf{B}_1 & 0 \\ \mathbf{0} & 1 \end{pmatrix} \tag{14a}$$

$$\mathbf{A}_{a0} = \begin{pmatrix} \mathbf{A}_0 & \mathbf{0} \\ -1 & \mathbf{0} \end{pmatrix},\ \mathbf{B}_{a0} = \begin{pmatrix} \mathbf{B}_0 & 0 \\ \mathbf{0} & 1 \end{pmatrix} \tag{14b}$$

$$\mathbf{K}_a = \begin{pmatrix} \mathbf{K} & W_i \end{pmatrix}, \mathbf{w}_a = \begin{pmatrix} \mathbf{w} \\ v_{\rm ref} \end{pmatrix} \tag{14c}$$

Let us also define the augmented state transition matrices $\mathbf{\Phi}_{a1} = e^{\mathbf{A}_{a1}DT}$ and $\mathbf{\Phi}_{a0} = e^{\mathbf{A}_{a0}DT}$ and the augmented vector fields $\mathbf{m}_{a1}(\mathbf{x}_a(t)) = \mathbf{A}_{a1}\mathbf{x}_a(t) + \mathbf{B}_{a1}\mathbf{w}_a$ and $\mathbf{m}_{a0}(\mathbf{x}_a(t)) = \mathbf{A}_{a0}\mathbf{x}_a(t) + \mathbf{B}_{a0}\mathbf{w}_a$. Then, the full-order monodromy matrix can be expressed as follows

$$\mathbf{M} = \mathbf{\Phi}_{a0}\mathbf{S}\mathbf{\Phi}_{a1}, \tag{15}$$

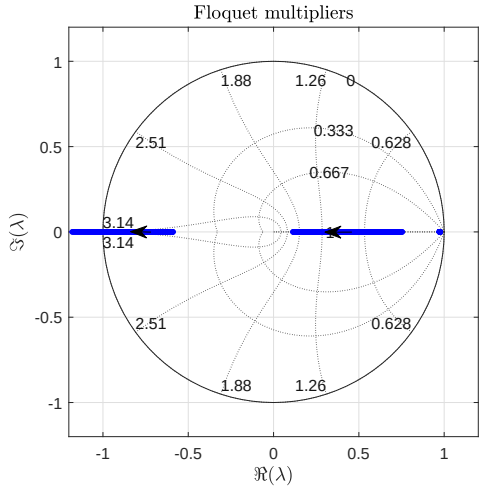
where $\mathbf{S}$ is the saltation matrix adapted from [23] as follows

$$\mathbf{S} = \mathbf{I} + \frac{(\mathbf{m}_{a0}(\mathbf{x}_a(DT)) - \mathbf{m}_{a1}(\mathbf{x}_a(DT)))\mathbf{K}_a^\intercal}{W_i(v_{\rm ref} - v_o(DT)) + \mathbf{K}^\intercal\mathbf{m}_1(\mathbf{x}(DT)) - m_a}. \tag{16}$$

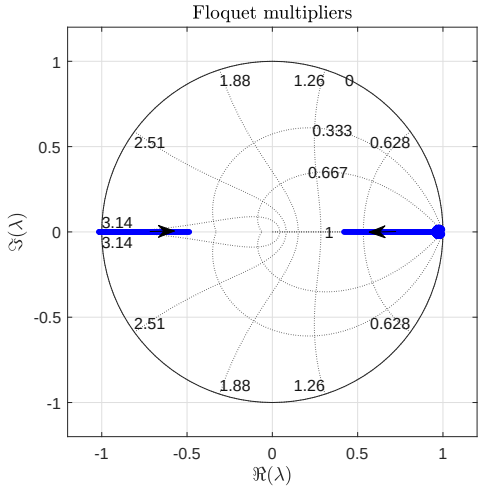
The steady-state duty cycle D is determined according to (13). The expression of $v_i(DT)$, the third component in $\mathbf{x}_a(DT)$, can be obtained from (12) in steady-state:

$$v_i(DT) = \frac{m_a DT - \mathbf{K}^\intercal\mathbf{x}(DT) - \kappa_p v_{\rm ref}}{W_i} \tag{17}$$

In order to locate the critical value of the gain for which the desired $T-$periodic regime loses its stability, the eigenvalues of the monodromy matrix called also Floquet multipliers were obtained. By varying the gain κ_p, the operating point of the system was first calculated and the monodromy matrix was evaluated at this point. The same two different values of the duty cycles considered for computing the bifurcation diagrams presented previously were used for computing the Floquet multipliers when the proportional gain of the voltage controller is varied. At a point where a $2T$-periodic regime develops, one of the eigenvalues is equal to -1. Fig. 7 shows the evolution of the Floquet multipliers in the complex plane for both values of the steady-state duty cycle. For $v_g = 32$ V ($D \approx 0.33$), the proportional gain has been varied in the range (0.1, 5) and the critical value of κ_p leading to one Floquet multiplier being located at -1 is $\kappa_p \approx 0.79$. For $v_g = 16$ V ($D \approx 0.66$), the proportional gain has been varied in the range (2, 7) and the critical value of κ_p leading to one Floquet multiplier being located at -1 is $\kappa_p \approx 5.55$. Both values are in perfect agreement with the bifurcation diagrams presented in Section IV.



(a) $v_g = 32$ V ($D < 0.5$)



(b) $v_g = 16$ V ($D > 0.5$)

Fig. 7. Eigenvalues of the monodromy matrix of the boost converter loaded by a CPL when the proportional gain κ_p is varied for two fixed values of the input voltage corresponding to two different values of the steady-state duty cycle. (a) $v_g = 32$ V ($D < 0.5$): when the proportional gain increases, the eigenvalue at the left side crosses the unit circle from its inside to its outside at $\kappa_p \approx 5.55$. (b) $v_g = 16$ V ($D < 0.5$): when the proportional gain increases, the eigenvalue at the left side crosses the unit circle from its outside to its inside at $\kappa_p \approx 0.79$.

VII. Stability Boundaries in the Parameter Space

One of the ways to locate subharmonic oscillation boundary is by using the expression of the characteristic equation $\det(\mathbf{M} - \lambda\mathbf{I}) = 0$, imposing the period-doubling condition in the eigenvalue λ and solving the resulting equation together with the steady-state condition. Therefore at the boundary of this bifurcation, the following conditions hold

$$\det(\mathbf{M} + \mathbf{I}) = 0 \tag{18a}$$

$$\mathbf{x}(DT) - \mathbf{x}((D+1)T) = \mathbf{0} \tag{18b}$$

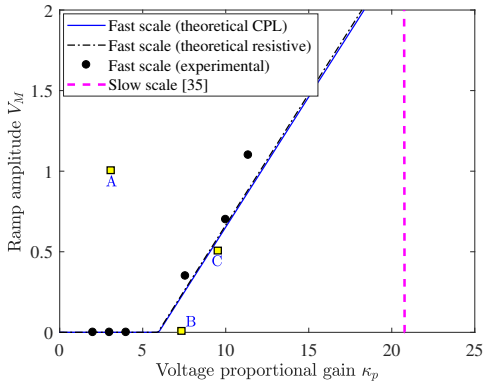
where $\mathbf{0} \in \mathbb{R}^2$ is a null vector. Note that the integral state variable can be determined by (17).

Equations (18a)-(18b) will be used later and the results from them will be contrasted with experimental measurements from a laboratory prototype.

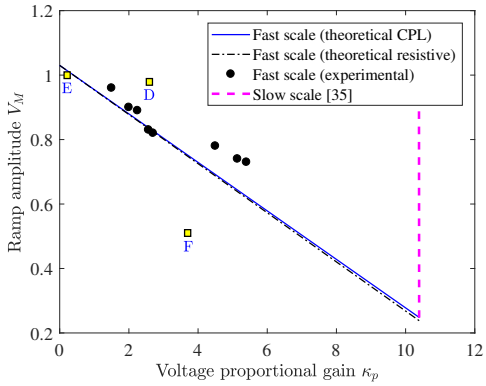
VIII. Experimental Validation

Based on the system structure in Fig. 2 and parameters in Table I, an experimental prototype has been constructed to validate the theoretical results and the numerical simulations. The feedback circuit uses a PI controller to fix the desired steady-state of the output voltage at $v_{\text{ref}} = 48$ V. The changes in the steady-stare duty cycle D were provoked by varying the input voltage v_g. In order to emulate an ideal constant power load at the converter output, an electronic load (ELEKTRO-AUTOMATIK EL3400-25) was used. This electronic load has four different operating modes: constant power, constant voltage, constant current and constant resistance. In all experiments presented in this work, the constant power mode was used. In this mode, the electronic load behaves as a nonlinear current sink maintaining the product of the voltage and the current in its terminal constant.

The inductor was built using toroidal Magnetics Kool-mu© core. The current is sensed using the hall effect current



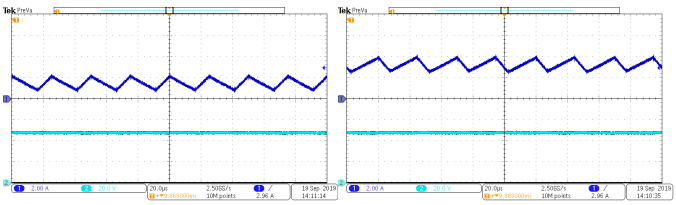
(a) $v_g = 32$ V ($D < 0.5$)



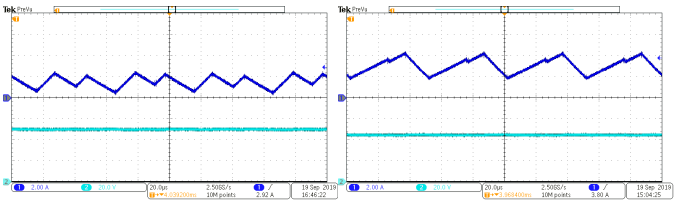
(b) $v_g = 16$ V ($D > 0.5$)

Fig. 8. The fast scale stability boundary from theoretical analysis using (18a)-(18b) (solid) and experimentally (dots) in terms of the current proportional gain κ_p and the amplitude of the ramp compensating signal V_M. The theoretical fast scale stability boundary (dash-doted) corresponding to a resistive load consuming the same power is also shown in the same figure for comparison.

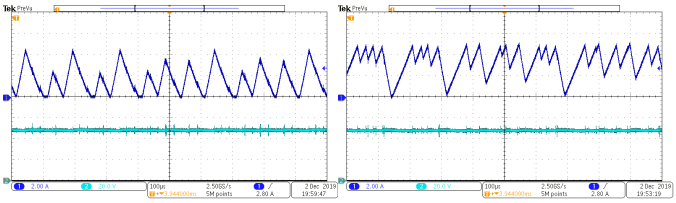
sensor LEM LA25NP with total conversion ratio 1 volts per amperes and an equivalent resistance $r_s = 6.3$ mΩ. Tektronix digital oscilloscope was employed to record the time-domain waveforms. A comparison between the responses from numerical simulation and the ones obtained from prototype measurements was conducted. The experimental results are discussed below.



(a) $\kappa_p = 3$, $v_g = 32$ V $V_M = 1$ V. (b) $\kappa_p = 3$, $v_g = 16$ V, $V_M = 1$ V.



(c) $\kappa_p = 7$, $v_g = 32$ V, $V_M = 1$ V. (d) $\kappa_p = 0.5$, $v_g = 16$ V, $V_M = 1$ V.

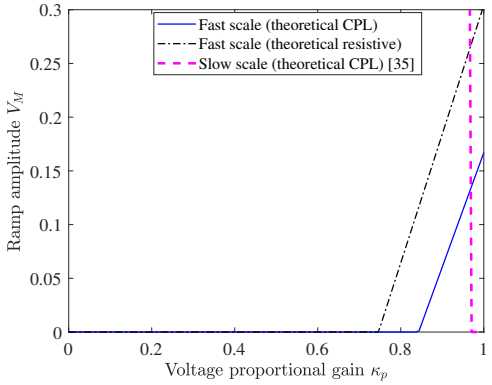


(e) $\kappa_p \approx 8.62$, $v_g = 32$ V, $V_M = 0.5$ V(f) $\kappa_p \approx 3.74$, $v_g = 16$ V, $V_M = 0.5$ V.

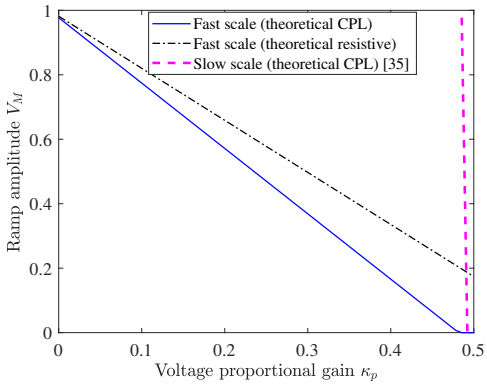
Fig. 9. Measured time domain waveforms showing the steady-state inductor current i_L and the output capacitor voltage v_o for two different values of steady-state duty cycles D and κ_p before (a) and (b) and after (c) subharmonic oscillation takes place. Chaotic behavior can also take place if the ramp amplitude is is decreased for both $D < 0.5$ and $D > 0.5$ (e) and (f).

Fig. 8 shows the boundary between stable and unstable regions in the parameter space (κ_p, V_M) obtained from (18a)-(18b) for two different values of the input voltage v_g. Some experimental points obtained from measurements using the boost converter prototype with a CPL are also depicted. It can be observed that a good matching exists between the theoretical results and the experimental measurements which validates the approach and the methodology followed in this study to locate the fast scale stability boundary of switching converters with nonlinear loads such as a CPL. The observed discrepancies between the experimental and the theoretical results can be attributed to non modeled parasitic elements such as small resistances in the reactive components and in the switching devices.

The theoretical fast scale stability boundary corresponding to a resistive load consuming the same power is also depicted in Fig. 8. For both the CPL and the resistive load, in the stability region depicted in Fig. 8, one can note that for $D < 0.5$ the higher the feedback gain κ_p the smaller the minimum amplitude of the ramp compensator needed for stabilizing the converter. On the contrary, for $D < 0.5$ the higher the feedback gain κ_p the larger the minimum amplitude of the ramp compensator needed for stabilizing the converter. Hence, the stabilizing and the destabilizing effects of the voltage loop in the different ranges of the steady-sate duty cycle values can be clearly noticed.



(a) $v_g = 32$ V ($D < 0.5$)



(b) $v_g = 16$ V ($D > 0.5$)

Fig. 10. The fast scale stability boundary from theoretical analysis for different values of power P using (18a)-(18b) (solid) in terms of the current proportional gain κ_p and the amplitude of the ramp compensating signal V_M.

To check the obtained fast scale stability boundary obtained before, Fig. 9 shows the experimental waveforms of the system at both sides of the instability boundary depicted in Fig. 8 for two different values of the considered duty cycles in different points in the plane (κ_p, V_M). Fig 9-a and Fig. 9-b show stable periodic regime and they correspond to Point A in Fig. 8-a and Point D in Fig. 8-b. Fig. 9-c and Fig. 9-d show subharmonic oscillation and they correspond to Point B in Fig. 8-a and Point E in Fig. 8-b. The experimental results depicted in Fig. 9-a,b,c and d correspond to the numerical simulations presented in Fig. 5. As can be observed, a very good matching between the results is obtained. Further increasing the gain for $D < 0.5$ or decreasing it for $D > 0.5$ leads to chaotic oscillation as can be observed in Fig. 9-e and Fig. 9-f. These chaotic time domain waveforms correspond to Point C in Fig. 8-a and Point F in Fig. 8-b respectively.

From Fig. 8, it can be observed that for the considered values of parameters and in particular for the used power value

$P = 48$ W, there is only a small difference between the results corresponding to a CPL and those corresponding to a resistive load. However, for large value of power, the difference starts to be appreciated. Fig. 10 shows the theoretical fast scale stability boundaries for $P = 1$ kW. As can be observed, the fast scale stability curves corresponding to the CPL and the resistive load are quite different.

IX. Conclusions

In this paper, the nonlinear dynamics and fast scale stability analysis of boost converter under constant power load conditions were addressed. By using bifurcation diagrams computed from the circuit-level switched model of the system with the nonlinear model of the constant power load it was shown that it could exhibit nonlinear phenomena in the form of fast scale instabilities leading to period doubling and subharmonic oscillation. The same behavior and the same bifurcation patterns were observed when a piecewise linear model was used hence justifying the use of this simple model to perform the stability analysis of the system and demonstrating that our conjecture that the subharmonic oscillation is a local instability of the limit cycle of the switched system that can be predicted by a piecewise linear switched model is reasonable. The key point to ensure a small error in the prediction of the fast scale stability boundary by using this simplified model is that the ripple in the CPL voltage be small enough in such a way that the linearized model of the CPL is accurate during the entire switching cycle. Under this condition which is widely satisfied in a practical design, it was shown how the proposed simplified model can be used to mathematically locate the stability boundary in terms of the system parameters with a high accuracy. Furthermore, its compatibility with simulation software allows an easy analysis of the system behavior. The theoretical results was validated by numerical simulations and experimental measurements from a laboratory prototype showing a perfect agreement in most of the cases.

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