




Article

Modelling of SEPIC, Ćuk and Zeta Converters in Discontinuous Conduction Mode and Performance Evaluation

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Abstract: High-order switched DC-DC converters, such as SEPIC, Ćuk and Zeta, are classic energy processing elements, which can be used in a wide variety of applications due to their capacity to step-up and/or step-down voltage characteristic. In this paper, a novel methodology for analyzing the previous converters operating in discontinuous conduction mode (DCM) is applied to obtain full-order dynamic models. The analysis is based on the fact that inductor currents have three differentiated operating sub-intervals characterized by a third one in which both currents become equal, which implies that the current flowing through the diode is zero (DCM). Under a small voltage ripple hypothesis, the currents of all three converters have similar current piecewise linear shapes that allow us to use a graphical method based on the triangular shape of the diode current to obtain the respective non-linear average models. The models' linearization around their steady-state operating points yields full-order small-signal models that reproduce accurately the dynamic behavior of the corresponding switched model. The proposed methodology is applicable to the proposed converters and has also been extended to more complex topologies with magnetic coupling between inductors and/or an RC damping network in parallel with the intermediate capacitor. Several tests were carried out using simulation, hardware-in-the-loop, and using an experimental prototype. All the results validate the theoretical models.

Keywords: discontinuous conduction mode; full-order dynamic models; high-order switched converters



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1. Introduction

Discontinuous conduction mode (DCM) appears in current unidirectional DC-DC elementary switching converters such as buck, boost or buck-boost, whose switch consists of a transistor (usually a MOSFET or an IGBT) and diode, when the inductor current becomes zero in the diode conduction subinterval. The diode turns OFF and a third subinterval appears in which both transistor and diode are OFF [1,2]. In these converters a continuous conduction mode (CCM) is easily achieved by using synchronous switching, that is, replacing the diode with a transistor and applying complementary switching signals to the resulting current-bidirectional half-bridge structure [1,2].

However, the unidirectional switch is easier to implement and sometimes DCM operation is preferred because it reduces problems related to the diode reverse recovery current [3]. Further, DCM operation in boost and buck-boost converters has been proposed to eliminate the right half-plane zero that can limit the voltage control loop bandwidth [3]. In addition, paralleling DCM converters (with or without interleaving) is achieved naturally without a dedicated control strategy [4].

In single phase AC-DC power factor correction (PFC) applications based on the boost converter, the inductor current becomes discontinuous in the vicinity of the zero-crossings

of the line voltage. In fact, some PFC circuits are intentionally designed to always operate in DCM to simplify their control law [3,5–8] or to reduce the switching loss and the power consumption [9]. The loss free resistor characteristics of the buck-boost converter operating in DCM exhibits a resistive input impedance naturally providing PFC, however because of the discontinuous nature of the buck-boost input current it is sometimes replaced by higher order structures with a series-inductor at its input, such as Single-Ended Primary-Inductor converter (SEPIC) and Ćuk converters [10,11].

Zeta converter is another high order step-up/step-down topology with a switch in series at its input, reason why it has received less attention [12]. The switching cell of the SEPIC, Ćuk and Zeta converters can be easily derived from the buck-boost cell. It has two inductors and an additional intermediate capacitor in addition to the transistor and diode. Since the intermediate and the additional output filter capacitors are usually designed to operate with small voltage ripples, a high frequency transformer can also be added to the basic topologies to provide electrical isolation between the power grid and the load. Because of their high order, all these step-up/step-down converters (SEPIC, Ćuk and Zeta) can exhibit several discontinuous conduction modes [13]. The most usual DCM operation occurs when the diode turns OFF without the MOSFET still turning ON. At this instant, the sum of the two inductor currents which corresponds to the diode current becomes zero [14].

In the literature there are many applications of high order converters such as the basic and modified versions from SEPIC, Ćuk and Zeta topologies operating in DCM. The applications include renewable energies, supplying LED loads, electronic systems, motor drives and electrical vehicles, among others. In the case of the SEPIC converter, it has been the most used in applications like three phase rectifier [11], low power and high power factor correctors [10,15,16], interleaved with coupled inductors [4], PFC with higher output voltage [17] and DC-DC conversion with high voltage gain [18]. In the case of the Ćuk converter the most common applications are bridgeless PFCs [15,19,20] and motor drives [21]. A particular high-order topology combines Ćuk and SEPIC converters to be used in a switched reluctance motor drive [22]. Isolated SEPIC and Ćuk converters are usually in two-stages buck-boost inverters [23]. Finally, in the case of the Zeta converter, there are applications reported in topics such as renewable sources [24], power supplies [25] and electric vehicle battery chargers [26].

The dynamic analysis of the converters is an important topic to design controllers that guarantee the correct operation of the systems. Therefore, it is important to have dynamic models that accurately reproduce the behavior of the switched converter. Modelling methodologies in DCM have been addressed by following analytical or equivalent circuit approaches. On the one hand, the main analytical approach, proposed by Ćuk and Middlebrook, is based on a unified representation of state spaces [2]. This analytical methodology has been used also in high-order converters [3,14,27,28]. On the other hand, the equivalent circuit methodology is an approach which is known in literature as generalized switch averaging technique, first proposed by Vorperian [6]. This methodology applies directly to converters in DCM having a canonical three-terminal switch-cell constituted by the active and passive switch pair. Connecting the canonical cell to a single inductor conforms the core of the well-known basic converters buck, boost and buck-boost. The canonical cell also appears in the Ćuk converter but not in the SEPIC and Zeta converters. The direct application of Vorperian's analysis methodology requires the converter to have a common configuration for the DCM switch. An example of this methodology is the model of the modified Zeta converter presented in [29].

Analytical and equivalent circuit approaches can be used to obtain reduced or full-order models as is proposed in a complete analysis with comparisons of both approaches in [3]. The main feature of reduced-order models is that they are only capable of accurately predicting the converter dynamics at low frequencies. For instance, the model presented in [27] can accurately predict small-signal responses up to one-tenth of the switching frequency.

After an intense search of high-order converters in the literature, it is concluded that the scientific community is more focused on the application than on the modelling of high order converter operating in DCM. The motivation of this research emerges from the fact that the methodology proposed in [28] to model the DCM of the Ćuk converter does not work properly in the case of the SEPIC converter in DCM. There were problems to identify a key current component denoted as i_x in the differential equation of the intermediate capacitor voltage. In this work, a novel full-order method based on including explicitly the diode average current in the system equations is proposed. The diode average current is obtained for the SEPIC converter by means of a graphical procedure adapted from the procedure followed for the Ćuk converter in [28] and for the interleaved converters in [30]. The use of the diode average current allows us to extend easily the model developed for the SEPIC converter to the Ćuk and Zeta converters. In fact, it provides better results for the Ćuk converter than using the model in [28]. In practice, it is a common procedure to magnetically couple the inductors to reduce from two to one the magnetic core to implement both inductors [31]. Another typical procedure is adding a damping network to improve the transient converter behavior. The damping network is a simple way to minimize the settling time and suppress current and voltage spikes preserving the semiconductor devices. It is also well known that the addition of a damping network in parallel to some capacitors considerably improves the converter's dynamics (see Chapter 16 in [1]). Another example of the improvement of a converter's dynamics can be found in [32], where the use of magnetic coupling and a damping network moves the right half plane zeroes to the left half plane in a similar high-order switched converter operating in CCM. The prize to pay for the mentioned improvements is a slightly reduced conversion efficiency due to the added resistive losses in the damping network. In all the cases, the model proposed in this work can also be easily adapted to versions of the SEPIC, Ćuk and Zeta converters depicted in Figure 1 in which the inductors are magnetically coupled and/or an RC damping network is added in parallel to the intermediate capacitor. The main benefits of the proposed methodology are listed below:

- Because it is based in simple graphical representations of inductor's and diode current waveforms it is easy to understand and apply;
- Provides a full-order model that can be particularized to any of the three high-order step up/down switching converters with or without positive/negative magnetic coupling between inductors and damping networks in the intermediate capacitor;
- The three converters and its variants can be analyzed in the classical forms depicted in Figure 1, where the MOSFET and diode do not share any common node. To apply Vorperian's method, which also provides full-order models, the structures of two of the converters must be modified to a "common-common" configuration of the DCM switch.

This paper is a contribution to full-order modeling of the SEPIC, Zeta, and Ćuk DCM converters, and it includes simulation, hardware-in-the-loop, and experiments in power circuits to validate the obtained models. Most works in the literature perform only theoretical analysis and simulations. The remainder of the article is organized as follows: Section 2 proposes the modelling procedure, first in a detailed way for the SEPIC converter, and later its generalization to Ćuk and Zeta converters. The model performance in terms of frequency and transient responses are verified in Section 3 by comparing the theoretical predictions with ideal simulations of the switched converters using PSIM software. In addition, hardware-in-the-loop tests and experimental results are presented. Finally, the conclusions and proposal for future works are discussed in Section 4.

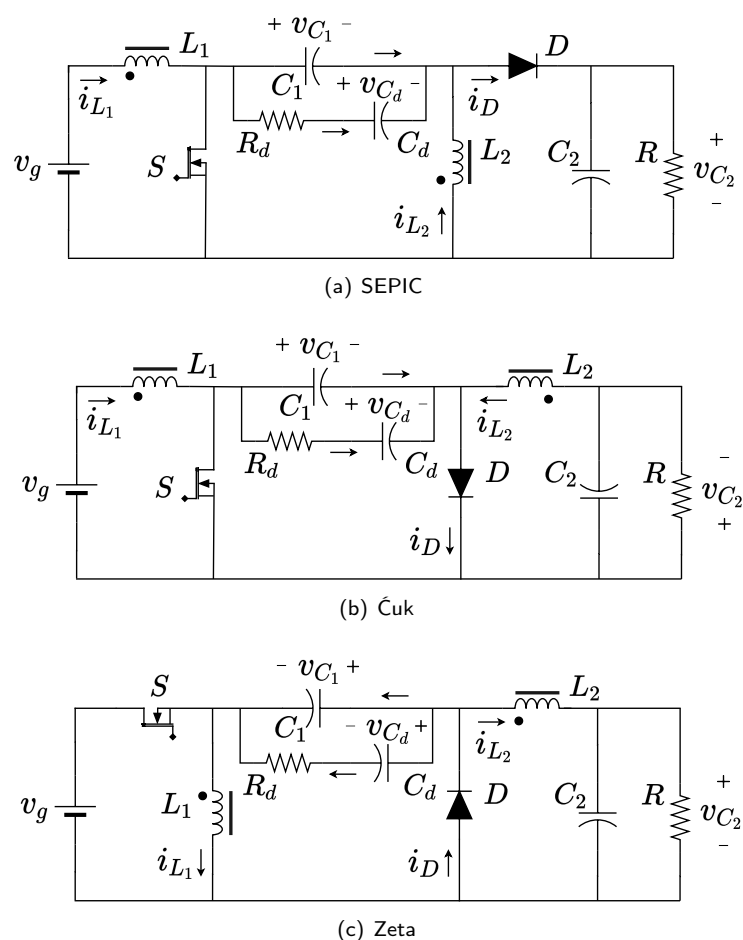


Figure 1. High-order converters: (a) SEPIC, (b) Ćuk, (c) Zeta.

2. Modeling in Discontinuous Mode of SEPIC, Ćuk and Zeta Converters

The proposed modelling procedure will be applied first in a detailed manner to the SEPIC converter. Afterwards, the method is generalized to the above mentioned high-order converters in DCM: Ćuk and Zeta. The non-linear model provided initially by the proposed method, that will be linearized around the steady-state equilibrium point, has considered the following assumptions:

- Ideal no-losses components, without parasitics;
- Constant switching frequency f_s and period T ;
- Capacitors large enough so that their average voltages can be considered approximately constant through a switching cycle and small voltage ripple amplitudes.

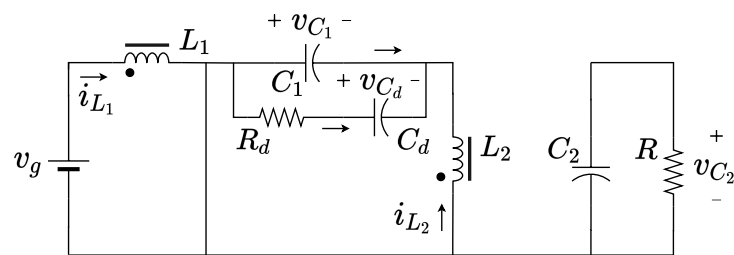
2.1. Analysis and Modeling of SEPIC Converter in DCM

The proposed methodology starts with the obtention of three ideal subcircuits assuming DCM depicted in Figure 2 from which, by following Kirchhoff's voltage laws, the inductor current slopes at each subinterval are obtained (1) and (2). Subcircuits in Figure 2 are defined by the conduction states of the converter semiconductors (MOSFET and diode) along a switching cycle of constant duration T . At the first subinterval, whose duration is $d_1 T$, the MOSFET is ON and the diode is OFF (Figure 2a). The duration of the second subinterval is $d_2 T$. In this subinterval (Figure 2b) the MOSFET is turned OFF and the energy stored at the inductors produce the diode activation. Finally, with the MOSFET still OFF, a third subinterval (DCM) appears when both inductor currents combine so that the diode current is zero and the diode turns OFF (Figure 2c). The duration of the third subinterval in which both switches' semiconductors are OFF is $(1 - (d_1 + d_2))T$. The state variables of the model are average inductor currents and capacitors voltages \bar{i}_{L1} , \bar{i}_{L2} , \bar{v}_{C1} ,

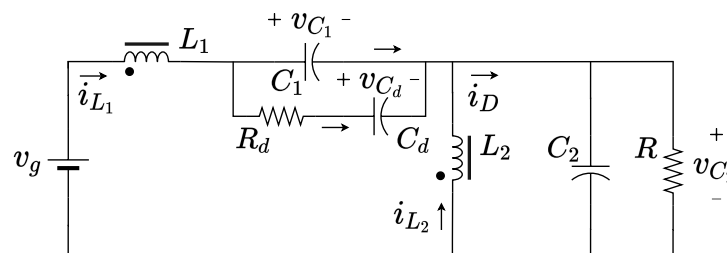
\bar{v}_{C_2} , and \bar{v}_{C_d} . Magnetic coupling M between inductors L_1 and L_2 has been considered. A damping ($R_d C_d$) network connected in parallel to the intermediate capacitor has also been taken into account as shown in Figure 2.

$$\frac{d}{dt}i_{L_1} = \begin{cases} m_{11}, & 0 \leq t < d_1 T \\ m_{21}, & d_1 T \leq t < (d_1 + d_2) T \\ m_3, & (d_1 + d_2) T \leq t < T \end{cases} \quad (1)$$

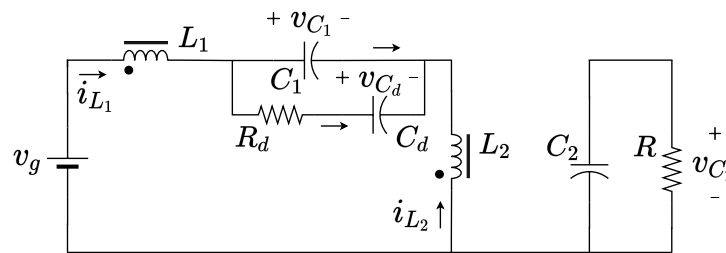
$$\frac{d}{dt}i_{L_2} = \begin{cases} -m_{12}, & 0 \leq t < d_1 T \\ -m_{22}, & d_1 T \leq t < (d_1 + d_2) T \\ -m_3, & (d_1 + d_2) T \leq t < T. \end{cases} \quad (2)$$



(a) MOSFET ON, diode OFF



(b) MOSFET OFF, diode ON



(c) MOSFET OFF, diode OFF

Figure 2. SEPIC converter circuits on DCM operation: (a) MOSFET ON, diode OFF, (b) MOSFET OFF, diode ON, (c) MOSFET OFF, diode OFF.

Figure 3a shows a simulation of the two inductor current waveforms in which the converter starts up from zero initial conditions under a constant duty cycle control signal (open loop). Three main behaviours can be observed in the enlarged sections in the bottom plots: in Figure 3b the currents increase in a switching cycle, they decrease in the Figure 3c, finally Figure 3d corresponds to a steady-state situation. The derivatives of the averaged inductor currents are obtained as a linear combination of the three current slopes weighted by the relative duration of their associate subintervals, in accordance with the piece-wise waveforms depicted in Figure 3b–d. Current slopes have been denoted as m_{ij} , where subindex i corresponds to the subinterval number and subindex j to the inductor.

A particular case are slopes in the third subintervals, since they are equal for both currents they have been renamed with just one subindex as $m_{31} = m_{32} = m_3$.

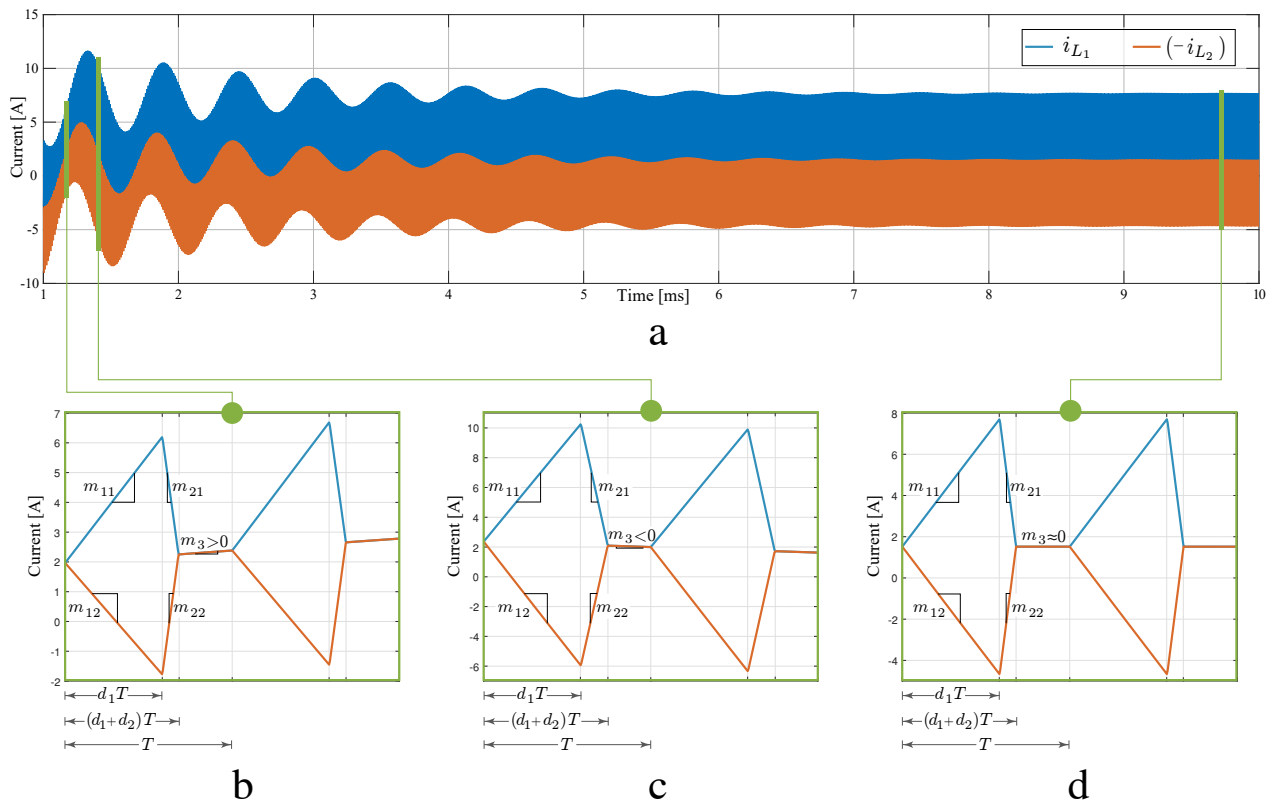


Figure 3. Responses in inductor currents: (a) dynamic response for inductor currents, (b) current transient with positive slope, (c) current transient with negative slope, (d) currents in steady state.

The current slopes, obtained from Figure 2 using Kirchhoff voltage law, have been summarized in Table 1. As expected, the slopes depend on the average voltages and the parameters of the magnetic elements (L_1 , L_2 and M) compacted by using additional parameters ΔL and L_S , the determinant of the magnetic parameter matrix and the equivalent inductance in the DCM subinterval, respectively.

$$\begin{aligned}
 \frac{d}{dt} \bar{i}_{L_1} &= m_{11}d_1 + m_{21}d_2 + m_3(1 - d_1 - d_2) \\
 \frac{d}{dt} \bar{i}_{L_2} &= -(m_{12}d_1 + m_{22}d_2 + m_3(1 - d_1 - d_2)) \\
 \frac{d}{dt} \bar{v}_{C_1} &= \frac{1}{C_1} (\bar{i}_D - \bar{i}_{L_2} - \frac{1}{R_d} (\bar{v}_{C_1} - \bar{v}_{C_d})) \\
 \frac{d}{dt} \bar{v}_{C_2} &= \frac{1}{C_2} (\bar{i}_D - \frac{\bar{v}_{C_2}}{R}) \\
 \frac{d}{dt} \bar{v}_{C_d} &= \frac{1}{R_d C_d} (\bar{v}_{C_1} - \bar{v}_{C_d}).
 \end{aligned} \tag{3}$$

The inductor current average state equations obtained as described previously are the first two of the non-linear model in (3). The remaining equations in the model are the average capacitor voltages that are derived from Kirchhoff current laws. In the equations corresponding to intermediate capacitor C_1 and output capacitor C_2 , the proposed model introduces the diode average current (\bar{i}_D) and the relative duration of the second subinterval (d_2) as auxiliary key variables that will be determined graphically in the next subsection. As will be seen, these two variables contribute significantly to the non-linearity of the

model, that has as inputs the relative duration of the first subinterval (d_1) and the assumed constant input voltage value ($\bar{v}_g = V_g$). Note that d_1 represents the nominal duty cycle of the converter.

Table 1. Dynamic model slopes for the SEPIC converter.

Slope	Equation
m_{11}	$\frac{L_2 \bar{v}_g - M \bar{v}_{C_1}}{\Delta L}$
m_{21}	$\frac{L_2 (\bar{v}_g - (\bar{v}_{C_1} + \bar{v}_{C_2})) + M \bar{v}_{C_2}}{-L_1 \bar{v}_{C_1} + M \bar{v}_g}$
m_{12}	$\frac{-L_1 \bar{v}_{C_1} + M \bar{v}_g}{\Delta L}$
m_{22}	$\frac{L_1 \bar{v}_{C_2} + M (\bar{v}_g - (\bar{v}_{C_1} + \bar{v}_{C_2}))}{\bar{v}_g - \bar{v}_{C_1}}$
m_3	$\frac{\bar{v}_g - \bar{v}_{C_1}}{L_s}$

with $\Delta L = L_1 L_2 - M^2$, $L_s = L_1 + L_2 - 2M$.

2.2. Nonlinear Model of Average Values Based on a Graphical Method for the SEPIC Converter in DCM

The full-order non-linear model of average values of the SEPIC converter shown in (3) allows us to analyze the converter behavior in the operation interval. In general, the inductors currents have a damped oscillatory behavior (see Figure 3a) where, as mentioned previously, it is possible to identify three operating conditions as a function of the average slope: current transient with positive slope (Figure 3b), current transient with negative slope (Figure 3c) and inductor current in steady state (Figure 3d) with zero slope. In Figure 3b it is observed how the average values of the currents increase. This behavior is directly associated with the positive sign of the m_3 slope. Likewise, in Figure 3c the current average values decrease ($m_3 < 0$) while in Figure 3d the average currents reach a steady state value ($m_3 \approx 0$). It is important to note in Figure 3 that i_{L_2} has been intentionally plotted with a negative sign to show that in the third sub-interval, slopes of i_{L_1} and $-i_{L_2}$ have equal magnitude (m_3) as seen in (1) and (2).

In steady state, inductor currents exhibit slopes of opposite signs in the first and second subintervals, and zero slope in the third subinterval ($m_3 = 0$). The slopes and durations of the first and second subintervals result in a constant average inductor current. Due to the rectilinear behavior of the inductor currents in each subinterval, it is possible to obtain their average values from the areas of the triangles between the curves and the horizontal axis. In (4), a general expression of the average inductor current is shown, where m_{1j} is the slope of the inductor current in the first sub-interval and I_3 is the constant value of the current in the third sub-interval.

$$\bar{i}_{L_j} = \frac{1}{T} \int_0^T i_{L_j} dt = \frac{1}{2} m_{1j} d_1 T (d_1 + d_2) \pm I_3. \quad (4)$$

Replacing the slope and evaluating the sign of I_3 in (4), Equations (5) and (6) are obtained. Constant I_3 is eliminated by adding the previous equations so that the second subinterval duration is obtained (7). On the other hand, (8) allows calculation of the average diode current. This equation is obtained by adding the average inductor currents in the second subinterval. \bar{i}_D is proportional to the area between the inductor currents as shown in Figure 4a and redrawn as a right triangle in Figure 4b.

$$\bar{i}_{L_1} = \frac{1}{2}m_{11}d_1T(d_1 + d_2) + I_3 \quad (5)$$

$$\bar{i}_{L_2} = \frac{1}{2}(-m_{12})d_1T(d_1 + d_2) - I_3 \quad (6)$$

$$d_2 = \frac{2(\bar{i}_{L_1} + \bar{i}_{L_2})}{(m_{11} - m_{12})d_1T} - d_1 \quad (7)$$

$$\bar{i}_D = \frac{1}{2}(m_{11} - m_{12})d_1d_2T. \quad (8)$$

Since the nonlinear model will be later linearized around the steady-state equilibrium point, it has been assumed that the proposed method, which derives the different average current values from the triangular areas in the steady-state waveforms, will provide simple and precise enough expressions of d_2 (7) and \bar{i}_D (8) to complete the model in (3). Both expressions will introduce additional nonlinearities to the dynamical model of the SEPIC converter.

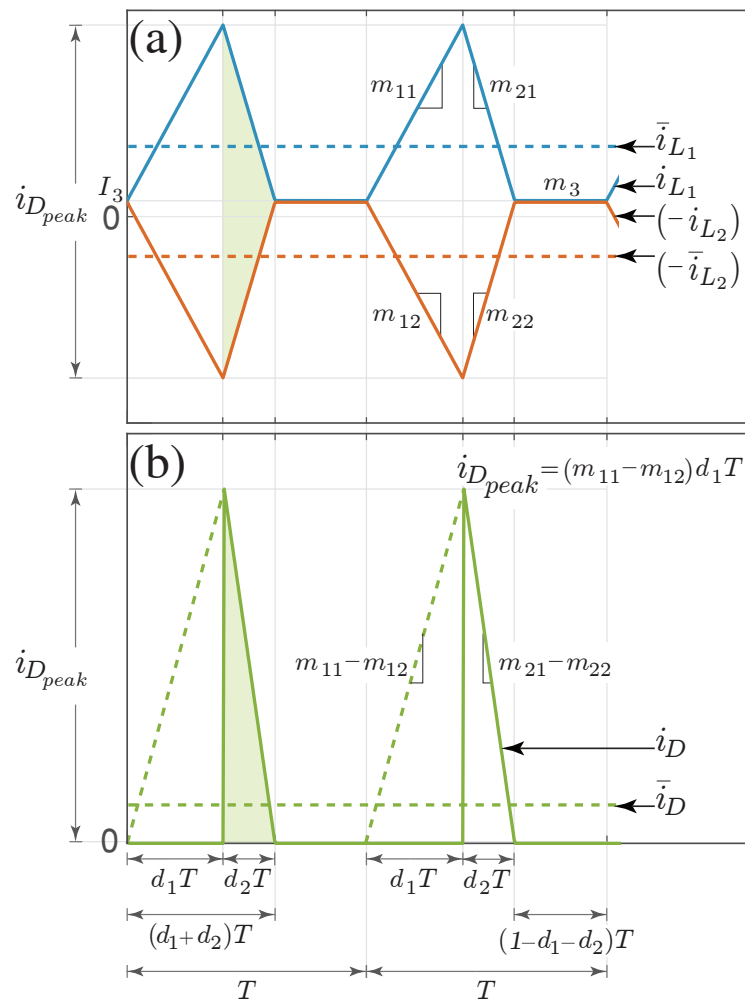


Figure 4. Relation between inductor and diode currents in steady state: (a) inductor currents, (b) diode current.

2.3. Steady State Operating Point of the SEPIC Converter in DCM

The steady state operating point (9) has been obtained by replacing (7) and (8) in (3) and equating the derivatives to zero.

$$\begin{aligned}\bar{i}_{L_1} &= \frac{\bar{v}_g T}{2L_E} d_1^2 \\ \bar{i}_{L_2} &= \bar{i}_D = \frac{\bar{v}_g}{R} \left(\frac{d_1}{d_2}\right) \\ \bar{v}_{C_1} &= \bar{v}_g \\ \bar{v}_{C_2} &= R\bar{i}_{L_2} = \bar{v}_g \left(\frac{d_1}{d_2}\right) \\ \bar{v}_{C_d} &= \bar{v}_{C_1} = \bar{v}_g,\end{aligned}\quad (9)$$

where

$$\begin{aligned}L_E &= \frac{\Delta L}{L_s} \\ d_2 &= \sqrt{\frac{2L_E}{RT}}.\end{aligned}\quad (10)$$

As expected in a DCM SEPIC converter in open loop [10,11] an equivalent pure resistive input impedance is deduced from the input current expression.

$$Z_{in} = \frac{\bar{v}_g}{\bar{i}_{L_1}} = R_{in} = \frac{2L_E}{T d_1^2}.\quad (11)$$

2.4. Generalized Model

2.4.1. Full-Order Dynamic Model

The non-linear model of average values of the SEPIC converter established in (3) can be extended to the Ćuk and Zeta topologies, changing the slope values according to Table 2. Furthermore, because of differences in the output section of the converters, it is necessary to include in the \bar{v}_{C_2} 's equation the variable ς that depends on the converter type to unify the general model. To complete the generalized nonlinear model d_2 and \bar{i}_D equations must be included. The resulting model is given in (12).

$$\begin{aligned}\frac{d}{dt}\bar{i}_{L_1} &= m_{11}d_1 + m_{21}d_2 + m_3(1 - d_1 - d_2) \\ \frac{d}{dt}\bar{i}_{L_2} &= -(m_{12}d_1 + m_{22}d_2 + m_3(1 - d_1 - d_2)) \\ \frac{d}{dt}\bar{v}_{C_1} &= \frac{1}{C_1}(\bar{i}_D - \bar{i}_{L_2} - \frac{1}{R_d}(\bar{v}_{C_1} - \bar{v}_{C_d})) \\ \frac{d}{dt}\bar{v}_{C_2} &= \frac{1}{C_2}(\varsigma\bar{i}_D + (1 - \varsigma)\bar{i}_{L_2} - \frac{\bar{v}_{C_2}}{R}) \\ \frac{d}{dt}\bar{v}_{C_d} &= \frac{1}{R_d C_d}(\bar{v}_{C_1} - \bar{v}_{C_d}) \\ d_2 &= \frac{2(\bar{i}_{L_1} + \bar{i}_{L_2})}{(m_{11} - m_{12})d_1 T} - d_1 \\ \bar{i}_D &= \frac{1}{2}(m_{11} - m_{12})d_1 d_2 T,\end{aligned}\quad (12)$$

where ς is a function of the converter:

$$\varsigma = \begin{cases} 1; & \text{SEPIC} \\ 0; & \text{Ćuk, Zeta.} \end{cases}\quad (13)$$

Note that variables d_2 and \bar{i}_D have the same expressions for the three converters: SEPIC, Ćuk and Zeta.

Table 2. Generalized slope of the inductor current waveform in the SEPIC, Ćuk and Zeta converters.

Slope	SEPIC	Ćuk	Zeta
m_{11}	$\frac{L_2\bar{v}_g - M\bar{v}_{C_1}}{\Delta L}$	$\frac{L_2\bar{v}_g - M(\bar{v}_{C_1} - \bar{v}_{C_2})}{\Delta L}$	$\frac{L_2\bar{v}_g - M(\bar{v}_g + \bar{v}_{C_1} - \bar{v}_{C_2})}{\Delta L}$
m_{21}	$\frac{L_2(\bar{v}_g - (\bar{v}_{C_1} + \bar{v}_{C_2})) + M\bar{v}_{C_2}}{-L_1\bar{v}_{C_1} + M\bar{v}_g}$	$\frac{L_2(\bar{v}_g - \bar{v}_{C_1}) + M\bar{v}_{C_2}}{-L_1(\bar{v}_{C_1} - \bar{v}_{C_2}) + M\bar{v}_g}$	$\frac{-L_2\bar{v}_{C_1} + M\bar{v}_{C_2}}{-L_1(\bar{v}_g + \bar{v}_{C_1} - \bar{v}_{C_2}) + M\bar{v}_g}$
m_{12}	$\frac{\Delta L}{L_1\bar{v}_{C_2} + M(\bar{v}_g - (\bar{v}_{C_1} + \bar{v}_{C_2}))}$	$\frac{\Delta L}{L_1\bar{v}_{C_2} + M(\bar{v}_g - \bar{v}_{C_1})}$	$\frac{\Delta L}{L_1\bar{v}_{C_2} - M\bar{v}_{C_1}}$
m_{22}	$\frac{\Delta L}{\bar{v}_g - \bar{v}_{C_1}}$	$\frac{\Delta L}{\bar{v}_g - \bar{v}_{C_1} + \bar{v}_{C_2}}$	$\frac{\Delta L}{\bar{v}_{C_2} - \bar{v}_{C_1}}$
m_3	$\frac{\Delta L}{L_s}$	$\frac{\Delta L}{L_s}$	$\frac{\Delta L}{L_s}$

2.4.2. Steady State Operation Point

The methodology to obtain the steady state operating point of the SEPIC converter is valid for all three converters. Equations of \bar{i}_{L_1} , \bar{i}_{L_2} , \bar{v}_{C_2} and \bar{v}_{C_d} shown in (9) are equivalent for Ćuk and Zeta topologies. The only difference is for \bar{v}_{C_1} . Additionally, d_2 included in (10) is valid for any of the three converters. The generalized expressions of the operating point are given in (14) where having a pure resistive input impedance in terms of average voltage and current is a common characteristic of the SEPIC, Ćuk and Zeta converters in DCM. Note that the input current of the Zeta converter has the same average value than its L_1 inductor current.

$$\begin{aligned}
 \bar{i}_{L_1} &= \frac{\bar{v}_g T}{2L_E} d_1^2 \\
 \bar{i}_{L_2} &= \bar{i}_D = \frac{\bar{v}_g}{R} \left(\frac{d_1}{d_2} \right) \\
 \bar{v}_{C_1} &= \begin{cases} \bar{v}_g, & \text{SEPIC} \\ \bar{v}_g + \bar{v}_{C_2}, & \text{Ćuk} \\ \bar{v}_{C_2}, & \text{Zeta} \end{cases} \quad (14) \\
 \bar{v}_{C_2} &= R\bar{i}_{L_2} = \bar{v}_g \left(\frac{d_1}{d_2} \right) \\
 \bar{v}_{C_d} &= \bar{v}_{C_1} = \bar{v}_g \\
 d_2 &= \sqrt{\frac{2L_E}{RT}}
 \end{aligned}$$

Note that Equation (11) is valid for all three converters.

2.4.3. Boundary between Continuous and Discontinuous Conduction Mode

Continuous and discontinuous operation modes can be defined according to constant $k = \frac{2L_E}{RT}$ as,

$$\begin{cases} \text{if } k > k_c, & \text{continuous conduction mode (CCM),} \\ \text{if } k < k_c, & \text{discontinuous conduction mode (DCM)} \end{cases} \quad (15)$$

where k_c is the k value in the boundary between operation modes. It can be easily verified that

$$d_2 = \sqrt{k}. \quad (16)$$

By replacing this result in the boundary condition $d_1 = 1 - d_2$ and solving for k_c , it is obtained

$$k_c = (1 - d_1)^2, \quad (17)$$

which corresponds exactly with the expression of k_c presented in the literature for buck-boost converters [2].

Furthermore, if the load resistance is constant then d_2 is also a constant in DCM, while d_2 satisfies the equation $d_1 + d_2 = 1$ in CCM. Based on these features it is possible to find the relation between d_1 and d_2 shown in Figure 5. The boundary between both modes is the common point between the lines $d_2 = \sqrt{k}$ and $d_1 + d_2 = 1$.

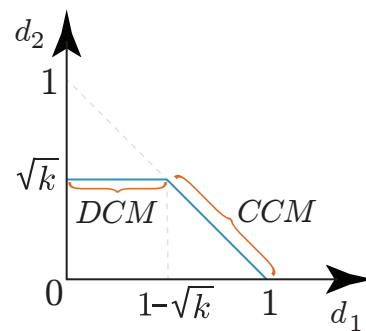


Figure 5. Operation zones of high-order converters.

2.4.4. Linearized Model

The linearization procedure is well known. The full-order nonlinear model of any of the three converters can be represented as

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}. \quad (18)$$

where \mathbf{x} is the state vector and \mathbf{u} is the input vector defined as $\mathbf{x} = (\bar{i}_{L1} \bar{i}_{L2} \bar{v}_{C1} \bar{v}_{C2} \bar{v}_{Cd})^T$ and $\mathbf{u} = (d_1 \bar{v}_g)^T$. To obtain the small signal model, the non-linear model is linearized around an operating point (\mathbf{x}_o). The small signal model can be expressed as

$$\hat{\mathbf{x}} = \mathbf{A}_o \hat{\mathbf{x}} + \mathbf{B}_o \hat{\mathbf{u}}, \quad (19)$$

where \mathbf{A}_o and \mathbf{B}_o defined in (20) are the Jacobian matrices evaluated at the operating point.

$$\mathbf{A}_o = \left. \frac{\partial f}{\partial \bar{\mathbf{x}}} \right|_{\bar{\mathbf{x}}=\mathbf{x}_o}, \quad \mathbf{B}_o = \left. \frac{\partial f}{\partial \mathbf{u}} \right|_{\bar{\mathbf{x}}=\mathbf{x}_o}. \quad (20)$$

Analytical expressions of the small signal model are very complex, therefore it is usually more practical to obtain numerical expressions for each particular case.

3. Results

Comparisons between the theoretical and the switched models in time and frequency domains are presented in this section by means of PSIM simulations, hardware-in-the-loop (HIL) tests and experimental results. A description of the nomenclature used is presented below:

- Theoretical results: these are results in the time or frequency domains obtained from the transfer functions of the small-signal models;
- Switched results: they are obtained from simulations in the PSIM software;
- Hardware-in-the-loop results: measurements carried out on the hardware-in-the-loop tools (PLECS RT-box 1, Interface and Texas Instruments LAUNCHXL-F28069M);
- Experimental results: direct measurements in a real proof-of-concept reconfigurable prototype of high-order converters.

In order to explore the scope of the proposed theoretical model, the three high-order converter structures have been used with different magnetic couplings: null, positive and negative. A base set of circuit parameters has been proposed for all three converters. Some parameters were intentionally changed to analyze the response under non-fulfillment of design criteria (high voltage ripple capacitors or inductor currents without triangular waveform).

It is relevant to clarify the notation used to present the results. Until now in this paper, average values nomenclature has been used to express variables from the theoretical model according to equation $\bar{x} = X + \hat{x}$; where \bar{x} is an average value, X is a steady state value, and \hat{x} is the small signal value. Thereby \bar{i}_{L_1} , \bar{i}_{L_2} , \bar{v}_{C_1} , \bar{v}_{C_2} represent theoretical model variables and i_{L_1} , i_{L_2} , v_{C_1} , v_{C_2} will be used to denote switched model variables.

3.1. Component Description

The selection criteria for the inductors is to keep a fixed value of the self inductance with or without magnetic coupling. The value of L_1 and L_2 have been selected equal to 56.4 μH . Additionally, the inductors selection fulfills a compromise between a high operating margin in DCM and an acceptable current ripple. A mutual inductance of 47.4 μH is achieved with the chosen inductors array, so a coupling factor of $k_a = 0.84$ is obtained. The mutual inductance can be considered positive or negative depending on the component ports connection. In some cases it has been considered that there is no coupling between L_1 and L_2 ($M = 0$).

The values of the capacitors C_1 and C_2 were selected considering the criteria of reduced size and approximately constant average voltage. Capacitor values of $C_1 = C_2 = 5.0 \mu\text{F}$ ensure peak-to-peak ripple capacitor voltage amplitudes less than 4%. Regarding the damping network, its values have been selected, taking into account the guidelines provided in [32]. A capacitor ten times larger than the intermediate one has been selected while the series resistor has been adjusted by simulation so that it ensures a sufficient damping of the internal dynamics. The selected values were 1.5 Ω for R_d and 50 μF for C_d . The load resistance has also been selected as $R = 100 \Omega$ to ensure DCM at the operation points considered in the study.

Three parameter sets have been defined for the proposed model validation. They are summarized in Table 3. Because of a temporary unavailability of the initially selected loosely-coupled magnetic components [31], an almost equivalent arrangement using Coilcraft's Hexa-Path perfectly magnetic coupled inductors and other non-coupled inductors has been used. A description of each arrangement is given below:

- Test-1: Base set formed by coupled inductors L_1 , L_2 with mutual inductance M , capacitors C_1 and C_2 and a load resistor R ;
- Test-2: Corresponds with Test-1 but with damping network;
- Test-3: Corresponds with Test-1 with an intermediate capacitor reduced ten times. This test has been defined to study the proposed model under a high voltage ripple condition.

Table 3. Test parameters.

Parameter	Test-1	Test-2	Test-3
L_1 [μH]	56.4	56.4	56.4
L_2 [μH]	56.4	56.4	56.4
M [μH]	47.4	47.4	47.4
C_1 [μF]	5.0	5.0	0.5
C_2 [μF]	5.0	5.0	5.0
C_d [μF]	—	50.0	—
R_d [Ω]	—	1.5	—
R [Ω]	100.0	100.0	100.0

Table 4. Theoretical operation points for the Test-1 parameters.

Parameter	Ćuk ($M = 0$)	SEPIC ($M > 0$)	Zeta ($M < 0$)
\bar{i}_{L_1} [A]	0.2837	0.1541	1.7778
\bar{i}_{L_2} [A]	0.1684	0.1242	0.4216
\bar{v}_{C_1} [V]	26.8430	10.0000	42.1637
\bar{v}_{C_2} [V]	16.8430	12.4154	42.1617
d_2 [-]	0.2375	0.3222	0.0949
I_3 [A]	0.0596	0.01845	0.7095
k [-]	0.0564	0.1038	0.0090

3.2. Operation Points

Taking into account the three high-order converter structures and the three possible types of coupling (positive, negative or zero), three case studies have been defined to verify the performance of the proposed full-order model in a broad enough way. The case studies are: Ćuk without magnetic coupling between the inductors, SEPIC with positive magnetic coupling and Zeta with negative magnetic coupling. The operating points listed in Table 4 are obtained by replacing in the theoretical expressions the base set of circuit parameters (Test-1) and the simulation parameters ($V_g = 10$ V, $d_1 = 0.4$, $f_s = 100$ kHz). In this table the constant (k) allows determining the conduction mode in which the converter operates. This value is less than $k_{crit} = (1 - d_1)^2 = 0.36$, and therefore the converters operate in DCM, as it is verified for all presented cases. Finally, it is satisfied that $v_{C_d} = v_{C_1}$ in steady state.

3.3. Transfer Functions

Tables 5–7 includes the theoretical transfer functions of inductor currents and capacitor voltages that have been considered in time and frequency domain analysis. In this work, transfer functions can be a function of the input voltage or the duty cycle. The transfer functions can be of 4 or 5 order depending on the addition of the damping network in the topologies. In Tables 5–7, it can be seen that the transfer function of i_{L_1}/v_g is the only one that has all its zeros in the left half-plane in all cases. The other transfer functions have at least one zero in the right half-plane. Another important finding is seen in the analysis of the damping network effect. In the absence of the damping network, the transfer function presents a pair of complex poles with a very small real part 32.48 and very little damped. In fact, they are the dominant poles. With a damping network, the effect of these poles is well damped and the dominant pole becomes a real pole with value of 4012. From the point of view of pole analysis, there is a good damping.

3.4. Time Domain Responses

3.4.1. Small Signal Response

The objective in small signal is to verify the correspondence between switched and theoretical model responses. The structure used in this comparison is the Ćuk converter without magnetic coupling with the parameter set for the power circuit Test-1. To obtain the results depicted in Figure 6, a reference change in the input voltage of 1 V has been applied. The input voltage v_g changes from 9 V to 10 V at $t = 10$ ms and decreases again to 9 V at $t = 15$ ms. The theoretical model results correspond to a linearized model for the operating point $v_g = 10$ V. In Figure 6a, the averaged model currents have a constant behavior, except during transitions where a small disturbance occurs, but the steady state condition is quickly reached. In Figure 6b it can be observed that the average voltages of the proposed model follow the behavior of the switched model even after the disturbance. The magnitudes obtained by the theoretical model for $v_g = 10$ V are approximately equal to the operating point values listed in Table 4. Currents and voltages averaged values of both switched and theoretical model for $v_g = 9$ V and $v_g = 10$ V are given in Table 8. These results validate the good performance of the theoretical model calculated for $v_g = 10$ V

condition to approximate the average values of the responses obtained from the switched simulations for $v_g = 9$ V and $v_g = 10$ V. The relative error (RE) were less than 0.51% in all cases. The results show that the $v_g = 9$ V condition is a small signal operation as had been supposed before.

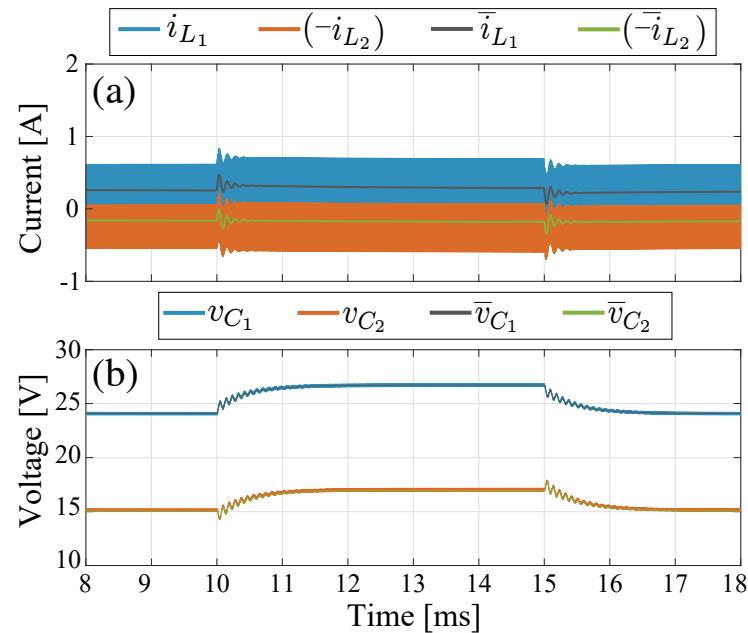


Figure 6. Comparison results in Ćuk converter without coupled inductors: (a) inductor currents, (b) capacitor voltages.

Table 5. Theoretical transfer functions of the Ćuk converter under the tests conditions depicted in Table 3.

Description	Transfer Function
Ćuk ($M = 0$, Test-1)	$\frac{\hat{i}_{L1}(s)}{\hat{v}_g(s)} = \frac{(s + 1080.26)(s + 22366.82)(s + 291761.29)}{(s + 2004.87)(s + 841142.14)((s + 1920.90)^2 + 59481.49^2)} = \frac{\mathcal{N}_1(s)}{\mathcal{D}_1(s)}$
	$\frac{\hat{i}_{L1}(s)}{\hat{v}_g(s)} = \frac{(s + 1542.11)((s + 1335.31)^2 + 75958.36^2)}{(s + 1542.11)((s + 1335.31)^2 + 75958.36^2)}$
	$\frac{\hat{d}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_1(s)}{\mathcal{D}_1(s)}$
	$\frac{\hat{i}_{L2}(s)}{\hat{v}_g(s)} = \frac{(s + 2000)(s - 6740.96)(s - 1183456.26)}{\mathcal{D}_1(s)}$
	$\frac{\hat{i}_{L2}(s)}{\hat{v}_g(s)} = \frac{(s + 1542.11)((s + 1335.31)^2 + 75958.36^2)}{\mathcal{D}_1(s)}$
	$\frac{\hat{d}(s)}{\hat{v}_{C1}(s)} = \frac{\mathcal{D}_1(s)}{(s + 10972.63)(s + 406309.64)(s - 1267635.58)}$
	$\frac{\hat{v}_{C1}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_1(s)}{\mathcal{D}_1(s)}$
	$\frac{\hat{v}_{C2}(s)}{\hat{v}_g(s)} = \frac{(s - 6740.96)(s - 1183456.26)}{\mathcal{D}_1(s)}$
	$\frac{\hat{v}_{C2}(s)}{\hat{v}_g(s)} = \frac{((s - 1535.74)^2 + 36313.79^2)}{\mathcal{D}_1(s)}$
	$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C1}(s)} = \frac{((s - 1535.74)^2 + 36313.79^2)}{(s + 1542.11)((s + 1335.31)^2 + 75958.36^2)}$
	$\frac{\hat{v}_{C2}(s)}{\hat{i}_{L2}(s)} = \frac{((s - 1535.74)^2 + 36313.79^2)}{(s + 1542.11)((s + 1335.31)^2 + 75958.36^2)}$
	$\hat{Z}_{in}(s) = \frac{\mathcal{D}_1(s)}{(s + 1080.26)(s + 22366.82)(s + 291761.29)}$
	$\hat{Z}_{out}(s) = \frac{(s + 844748.93)((s + 119.93)^2 + 42042.65^2)}{\mathcal{D}_1(s)}$

Table 6. Theoretical transfer functions of the SEPIC converter under the tests conditions depicted in Table 3.

Description	Transfer Function	
SEPIC ($M > 0$, Test-1)	$\frac{\hat{i}_{L1}(s)}{\hat{d}(s)} = \frac{(s + 4011.73)((s + 9394.93)^2 + 110381.85^2)}{(s + 4012.47)(s + 620234.85)((s + 32.48)^2 + 105290.84^2)} = \frac{\mathcal{N}_2(s)}{\mathcal{D}_2(s)}$	
	$\frac{\hat{i}_{L2}(s)}{\hat{d}(s)} = \frac{(s + 2000.45)((s + 9427.05)^2 + 99109.72^2)}{\mathcal{D}_2(s)}$	
	$\frac{\hat{v}_{C1}(s)}{\hat{v}_g(s)} = \frac{(s + 4014.30)(s + 547190.15)(s - 8148514.90)}{\mathcal{D}_2(s)}$	
	$\frac{\hat{v}_{C2}(s)}{\hat{v}_g(s)} = \frac{(s - 1398640.41)((s - 2042.34)^2 + 126032.83^2)}{\mathcal{D}_2(s)}$	
	$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C2}(s)} = \frac{(s - 499856.40)((s - 71.80)^2 + 105424.37^2)}{\mathcal{D}_2(s)}$	
	$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C2}(s)} = \frac{(s - 499856.40)((s - 71.80)^2 + 105424.37^2)}{\mathcal{D}_2(s)}$	
	$\frac{\hat{i}_{L1}(s)}{\hat{v}_{C2}(s)} = \frac{(s + 4011.73)((s + 9394.93)^2 + 110381.85^2)}{(s - 499856.40)((s - 71.80)^2 + 105424.37^2)}$	
	$\frac{\hat{i}_{L2}(s)}{\hat{v}_{C2}(s)} = \frac{(s + 2000.45)((s + 9427.05)^2 + 99109.72^2)}{(s - 499856.40)((s - 71.80)^2 + 105424.37^2)}$	
	$\hat{Z}_{in}(s) = \frac{\mathcal{D}_2(s)}{(s + 275.00)(s + 4014.35)(s + 149581.03)(s + 542015.57)}$	
	$\hat{Z}_{out}(s) = \frac{(s + 622241.00)((s + 35.65)^2 + 105284.65^2)}{\mathcal{D}_2(s)}$	
	SEPIC ($M > 0$, Test-2)	$\frac{\hat{i}_{L1}(s)}{\hat{d}(s)} = \frac{(s + 3995.17)(s + 16523.76)((s + 74474.66)^2 + 66313.01^2)}{(s + 4012.47)(s + 16534.61)(s + 620635.63)((s + 64898.11)^2 + 68718.26^2)} = \frac{\mathcal{N}_3(s)}{\mathcal{D}_3(s)}$
		$\frac{\hat{i}_{L2}(s)}{\hat{d}(s)} = \frac{(s + 2005.69)(s + 16545.91)((s + 55630.71)^2 + 69796.15^2)}{\mathcal{D}_3(s)}$
		$\frac{\hat{v}_{C1}(s)}{\hat{v}_g(s)} = \frac{(s + 4014.30)(s + 13333.33)(s + 547190.15)(s - 8148514.90)}{\mathcal{D}_3(s)}$
		$\frac{\hat{v}_{C2}(s)}{\hat{v}_g(s)} = \frac{(s + 15256.57)(s - 1398991.10)((s + 63838.05)^2 + 99029.19^2)}{\mathcal{D}_3(s)}$
		$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C2}(s)} = \frac{(s + 16534.58)(s - 499885.01)((s + 65008.55)^2 + 68817.48^2)}{\mathcal{D}_3(s)}$
$\frac{\hat{v}_{C2}(s)}{\hat{v}_{C2}(s)} = \frac{(s + 16534.58)(s - 499885.01)((s + 65008.55)^2 + 68817.48^2)}{\mathcal{D}_3(s)}$		
$\frac{\hat{i}_{L1}(s)}{\hat{v}_{C2}(s)} = \frac{(s + 3995.17)(s + 16523.76)((s + 74474.66)^2 + 66313.01^2)}{(s + 16534.58)(s - 499885.01)((s + 65008.55)^2 + 68817.48^2)}$		
$\frac{\hat{i}_{L2}(s)}{\hat{v}_{C2}(s)} = \frac{(s + 2005.69)(s + 16545.91)((s + 55630.71)^2 + 69796.15^2)}{(s + 16534.58)(s - 499885.01)((s + 65008.55)^2 + 68817.48^2)}$		
$\hat{Z}_{in}(s) = \frac{\mathcal{D}_3(s)}{(s + 275.00)(s + 4014.35)(s + 149581.03)(s + 542015.57)}$		
$\hat{Z}_{out}(s) = \frac{(s + 16535.58)(s + 622638.33)((s + 64902.52)^2 + 68703.34^2)}{\mathcal{D}_3(s)}$		

Table 7. Theoretical transfer functions of the Zeta converter under the tests conditions depicted in Table 3.

Description	Transfer Function
Zeta ($M < 0$, Test-1)	$\frac{\hat{i}_{L_1}(s)}{\hat{v}_g(s)} = \frac{(s + 1616.65)((s + 840.76)^2 + 56857.98^2)}{(s + 2011.00)(s + 2107171.60)((s + 9390.14)^2 + 42766.67^2)} = \frac{\mathcal{N}_4(s)}{\mathcal{D}_4(s)}$ $\frac{\hat{i}_{L_1}(s)}{\hat{v}_{C_1}(s)} = \frac{\hat{d}(s)}{(s + 1788.37)((s - 824.70)^2 + 59014.74^2)}$ $\frac{\hat{i}_{L_2}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_4(s)}{(s + 2000)((s + 29.18)^2 + 24897.89^2)}$ $\frac{\hat{i}_{L_2}(s)}{\hat{v}_{C_2}(s)} = \frac{\mathcal{D}_4(s)}{(s + 2000.00)((s - 1669.26)^2 + 19146.43^2)}$ $\frac{\hat{v}_{C_1}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_4(s)}{(s - 37732.47)(s + 46662.86)(s + 547162.16)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_4(s)}{((s + 29.18)^2 + 24897.89^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{v}_{C_1}(s)} = \frac{\mathcal{D}_4(s)}{((s - 1669.26)^2 + 19146.43^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{i}_{L_2}(s)} = \frac{\mathcal{D}_4(s)}{((s - 1669.26)^2 + 19146.43^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{i}_{L_1}(s)} = \frac{\mathcal{D}_4(s)}{(s + 1788.37)((s - 824.70)^2 + 59014.74^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{v}_{C_1}(s)} = \frac{\mathcal{D}_4(s)}{((s - 1669.26)^2 + 19146.43^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{i}_{L_2}(s)} = \frac{\mathcal{D}_4(s)}{(s + 2000.00)((s - 1669.26)^2 + 19146.43^2)}$ $\hat{Z}_{in}(s) = \frac{\mathcal{D}_4(s)}{(s + 2001.98)(s + 2107184.16)((s + 499.48)^2 + 43880.90^2)}$ $\hat{Z}_{out}(s) = \frac{\mathcal{D}_4(s)}{(s + 2120818.47)((s + 2572.21)^2 + 30838.87^2)}$
Zeta ($M < 0$, Test-3)	$\frac{\hat{i}_{L_1}(s)}{\hat{v}_g(s)} = \frac{(s + 3489.33)((s + 5746.21)^2 + 122263.61^2)}{(s + 3622.05)(s + 2223842.84)((s + 30249.00)^2 + 95764.65^2)} = \frac{\mathcal{N}_5(s)}{\mathcal{D}_5(s)}$ $\frac{\hat{i}_{L_1}(s)}{\hat{v}_{C_1}(s)} = \frac{\hat{d}(s)}{(s + 3552.63)((s - 10081.49)^2 + 132036.58^2)}$ $\frac{\hat{i}_{L_2}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_5(s)}{(s + 2000)((s + 291.81)^2 + 78733.56^2)}$ $\frac{\hat{i}_{L_2}(s)}{\hat{v}_{C_2}(s)} = \frac{\mathcal{D}_5(s)}{(s + 2000.00)((s - 16692.26)^2 + 58438.68^2)}$ $\frac{\hat{v}_{C_1}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_5(s)}{(s - 37732.47)(s + 46662.86)(s + 547162.16)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{v}_g(s)} = \frac{\mathcal{D}_5(s)}{((s + 291.81)^2 + 78733.56^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{v}_{C_1}(s)} = \frac{\mathcal{D}_5(s)}{((s - 16692.62)^2 + 58438.68^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{i}_{L_2}(s)} = \frac{\mathcal{D}_5(s)}{((s - 16692.62)^2 + 58438.68^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{i}_{L_1}(s)} = \frac{\mathcal{D}_5(s)}{(s + 3552.63)((s - 10081.49)^2 + 132036.58^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{v}_{C_1}(s)} = \frac{\mathcal{D}_5(s)}{((s - 16692.62)^2 + 58438.68^2)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{i}_{L_2}(s)} = \frac{\mathcal{D}_5(s)}{(s + 2000.00)((s - 16692.26)^2 + 58438.68^2)}$ $\hat{Z}_{in}(s) = \frac{\mathcal{D}_5(s)}{(s + 3640.91)(s + 2102679.05)((s + 1932.57)^2 + 102995.44^2)}$ $\hat{Z}_{out}(s) = \frac{\mathcal{D}_5(s)}{(s + 2236967.59)((s + 24497.65)^2 + 92082.31^2)}$

Table 8. Small signal results in Ćuk converter without coupled inductors.

v_g	Model	\bar{i}_{L_1} [A]	\bar{i}_{L_2} [A]	\bar{v}_{C_1} [V]	\bar{v}_{C_2} [V]
9 V	Switched	0.2566	0.1518	24.1798	15.1798
	Theoretical	0.2553	0.1516	24.1587	15.1587
	RE [%]	0.51	0.13	0.09	0.14
10 V	Switched	0.2851	0.1687	26.8665	16.8665
	Theoretical	0.2837	0.1684	26.8430	16.8430
	RE [%]	0.49	0.18	0.09	0.14

3.4.2. Damping Network Effect

A damping network can be used in parallel with the intermediate capacitor to decrease the settling time. In the analysis carried out in this work, the SEPIC converter was the topology that, without a damping network, requires the longest time to reach a steady state. For this reason, the positive-coupled SEPIC converter was used specifically to analyze the damping network effect on the capacitors voltage. Two parameter sets have been used in the simulation: Test-1 for response without damping network and Test-2 for the analysis of the damping network effect. Switched and theoretical model responses are depicted in Figure 7a,b. In the presented results, the input voltage changes from 9 V to 10 V at time $t = 120$ ms. The direct effect of the damping network is observed in the intermediate capacitor voltage. In the absence of the damping network, the voltage requires a significant settling time (in the order of 80 ms) to reach steady state. On the other hand, with the addition of the damping network, the settling time is minimal. These behaviors are equivalent in both switched and theoretical models. It can be verified in graphs from Figure 7 that the theoretical model of average values also has an equivalent performance to the switched model when the damping network is added to the power circuit of the higher-order converter.

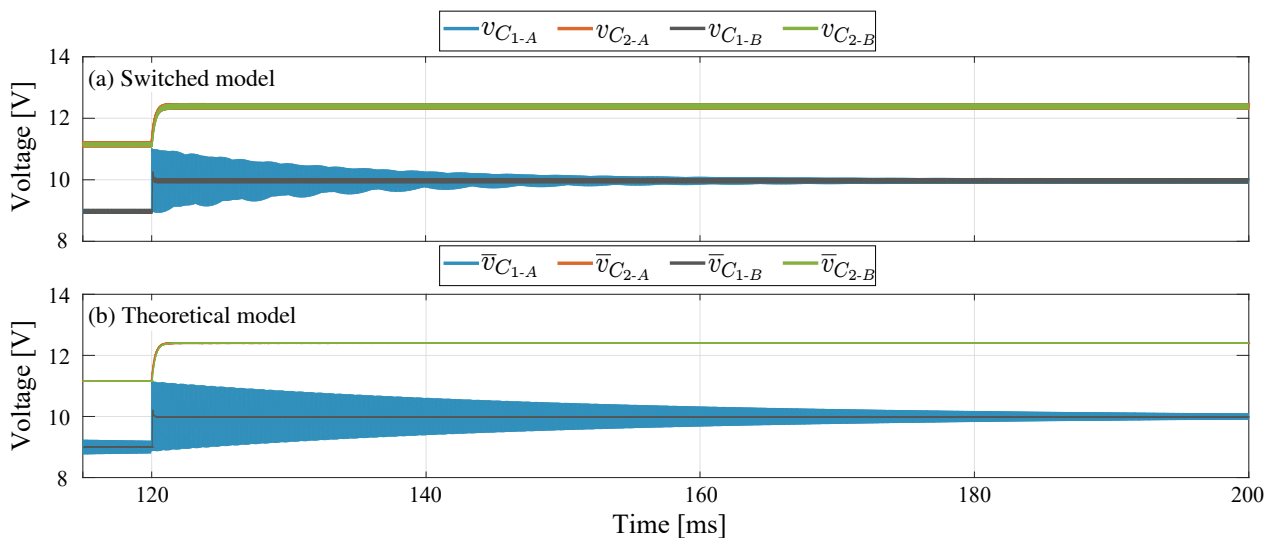


Figure 7. Comparison results for capacitor voltages in SEPIC converter with positive magnetic coupling, (A) without damping network, (B) with damping network: (a) switched model, (b) theoretical model.

3.4.3. Non-Fulfillment of Design Criteria

The topology considered in this case is the negative-coupled Zeta converter. The purpose of this analysis is to show that, when the low ripple condition is not fulfilled in the capacitors, the theoretical averaged model does not approximate accurately the switched model. In this section, the Test-1 and Test-3 parameter sets have been considered. The difference is that the value of C_1 passed from 5 μF in Test-1 to 0.5 μF in Test-3. Derating the capacitor by a factor of 10 times is a violation of the design criteria of approximately

constant capacitor voltage. Note that in the Zeta converter the averaged voltages in C_1 and C_2 are equal. According to Table 4 this value is 42.16 V. It can be verified in Figure 8 that \bar{v}_{C_1} and \bar{v}_{C_2} are equal to the theoretical value in all cases, since the operation point in steady state does not depend of the capacitor values. It is also observed that for the condition $C_1 = 5 \mu\text{F}$ the average values of the switched model voltages are approximately equal to the theoretical model values. When the capacitor C_1 changes to $0.5 \mu\text{F}$ two situations are evident: (i) the voltage ripple in C_1 increases from 3.1% under design conditions to 34%, while the ripple of C_2 remains constant, (ii) the average values voltages in C_1 and C_2 for the switched model increase and differ from the theoretical model values.

In Figure 8d, it is observed that \bar{v}_{C_2} does not correspond to the average value of v_{C_2} . It can also be easily verified by area analysis in Figure 8d, that \bar{v}_{C_1} does not correspond to the average value of v_{C_1} . In fact the new average value of v_{C_1} and v_{C_2} is 45.3 V. It is concluded that the theoretical model values do not correspond with the average value of the switched model, which increased by 3.1 V with the decrement in C_1 capacitor. An important comment on the currents comparison in Figure 8 is about their waveform shapes. In Figure 8e both currents, i_{L_1} and i_{L_2} , have a piecewise linear function of triangular shape while in Figure 8f, the triangular waveform is not completely linear. Logically the capacitors ripple increment affects the currents triangular shape, which also demonstrates that in the high voltage ripple condition the theoretical model does not faithfully reproduce the switched model results.

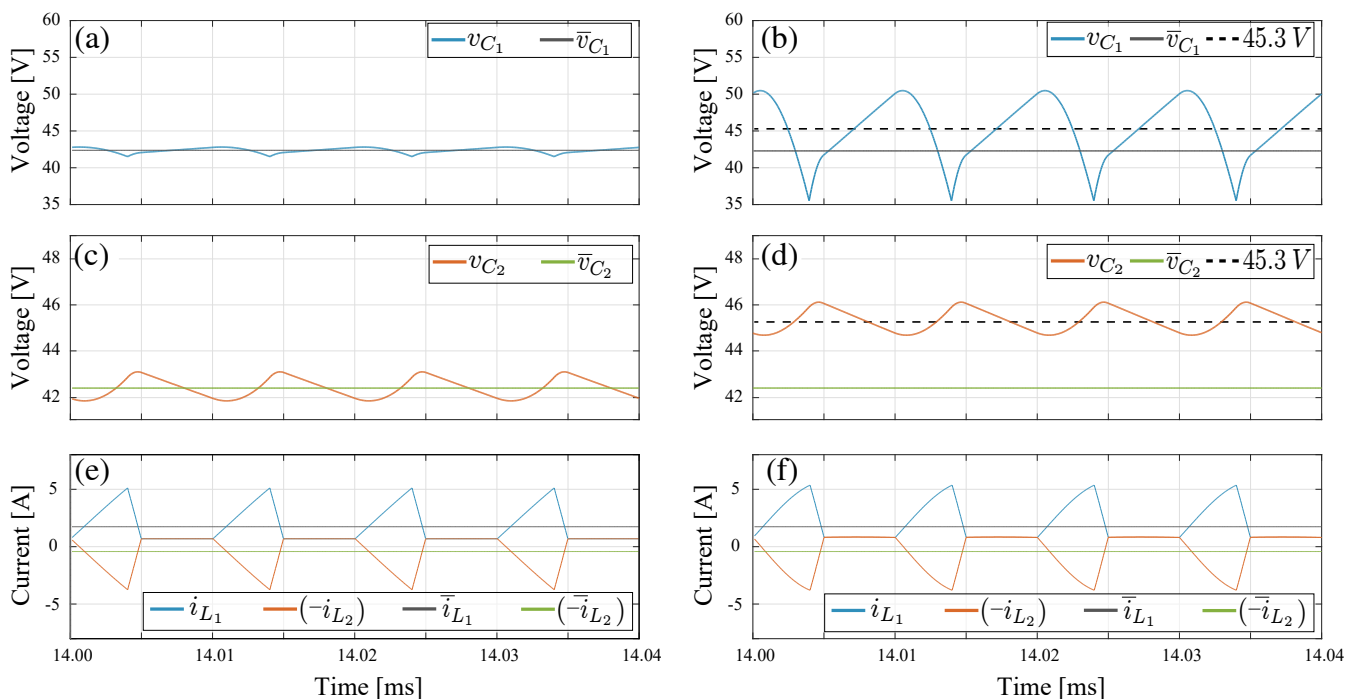


Figure 8. Comparison results for capacitor voltages in Zeta converter with negative magnetic coupling: (a,b) intermediate capacitor voltage (v_{C_1}), (c,d) output capacitor voltage (v_{C_2}), (e,f) inductor current, (a,c,e) $C_1 = 5 \mu\text{F}$, (b,d,f) $C_1 = 0.5 \mu\text{F}$.

3.4.4. HIL Validation

Nowadays, the use of Hardware-in-the-loop (HIL) tools to validate the controllers performance is more popular [33]. In this paper, different tests have been carried out in HIL to validate the simulation results in the high-order switched DC-DC converters previously presented by means of the experimental setup shown in Figure 9. The HIL testing system consists of:

- A TI 28069M LaunchPad;
- An RT Box LaunchPad Interface;
- A laptop with the PLECS software;

- An oscilloscope Keysight MSOX2014A, where the evaluation kit, a TI 28069M LaunchPad (the red board), is connected to the RT Box via an RT Box LaunchPad Interface (the green board). The different high-order switched DC-DC converters has been modelled using PLECS RT Box 1. In this way, the converter duty cycle has been generated using TI 28069M LaunchPad, which is a Texas Instrument microcontroller.

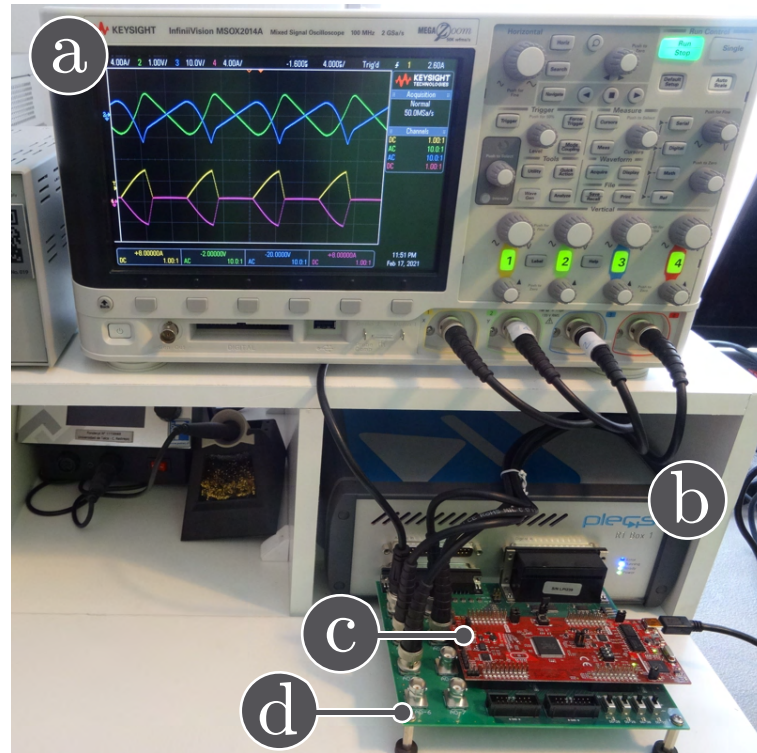


Figure 9. Hardware-in-the-loop experimental setup: (a) oscilloscope, (b) PLECS RT-box 1, (c) Texas Instruments LAUNCHXL-F28069M, (d) RT Box LaunchPad Interface.

In this subsection, the HIL test is presented with the goal of validating the time domain responses presented in the previous subsections. Figure 10 shows the HIL test to compare the proposed model and the simulation of the switched model using PSIM of the Ćuk converter without coupled inductors shown in Figure 6. In addition, the HIL test to validate the proposed model and the simulation of the switched model using PSIM of the SEPIC converter with positive magnetic coupling shown in Figure 7 is presented in Figure 11. Finally, the proposed model and simulation in Figure 8 correspond with the the HIL test of the Zeta converter with negative magnetic coupling shown in Figure 12. A good agreement between the model, the switching simulations and the HIL results is observed in all the cases. Therefore, the proposed procedure models correctly the considered high order step-up and down converter topologies (SEPIC, Ćuk or Zeta) operating in DCM.

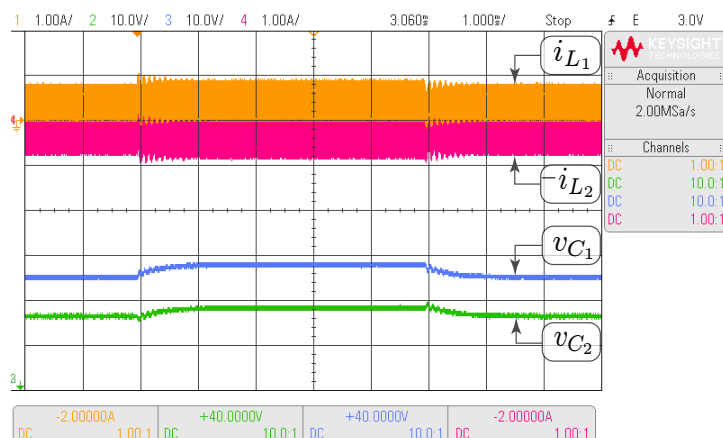
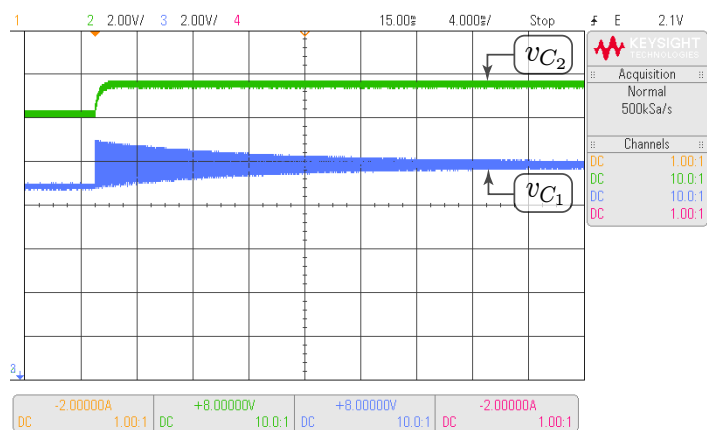
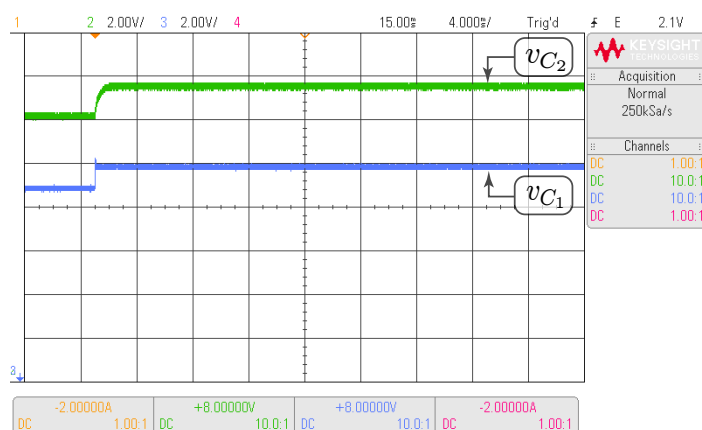


Figure 10. HIL test to validate the proposed model and the simulation of the switched model using PSIM by the Ćuk converter without coupled inductors shown in Figure 6. CH1: i_{L1} (1 A/div), CH2: v_{C2} (10 V/div), CH3: v_{C1} (10 V/div), CH4: $-i_{L2}$ (1 A/div), and time base of 1 ms.



(a) without damping network



(b) with damping network

Figure 11. HIL test to validate the proposed model and the simulation of the switched model using PSIM by the SEPIC converter with positive magnetic coupling shown in Figure 7: (a) without damping network, (b) with damping network. (CH2: v_{C2} (2 V/div), CH3: v_{C1} (2 V/div), and time base of 4 ms).

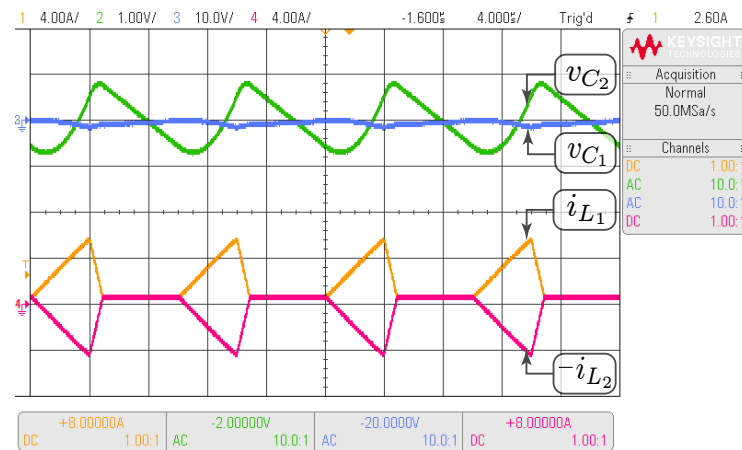
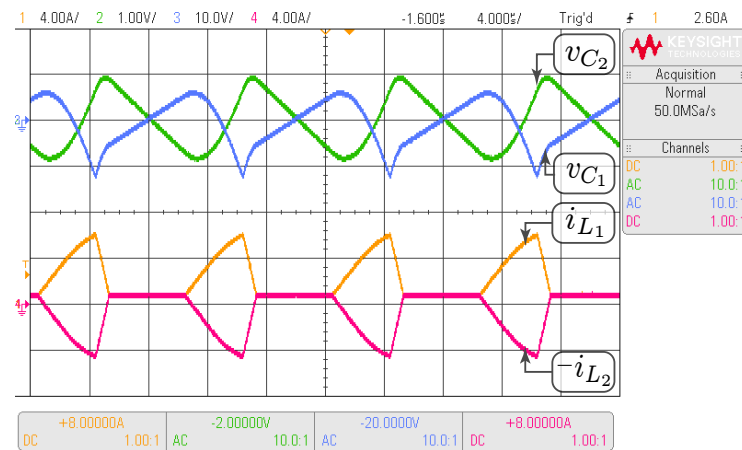
(a) $C_1 = 5 \mu\text{F}$ (b) $C_1 = 0.5 \mu\text{F}$

Figure 12. HIL test to validate the proposed model and the simulation of the switched model using PSIM by the Zeta converter with negative magnetic coupling shown in Figure 8: (a) $C_1 = 5 \mu\text{F}$, (b) $C_1 = 0.5 \mu\text{F}$. CH1: i_{L1} (4 A/div), CH2: v_{C2} (1 V/div, ac coupling), CH3: v_{C1} (10 V/div, ac coupling), CH4: $-i_{L2}$ (4 A/div), and time base of 4 ms.

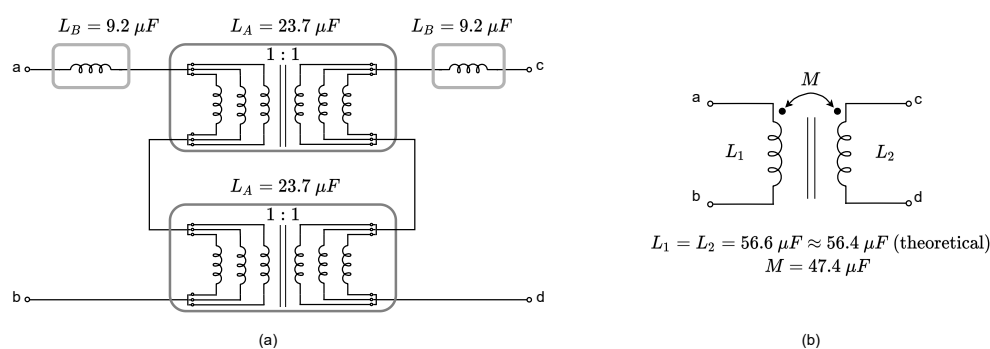
3.4.5. Experimental Results

A reconfigurable power converter was built to validate the theoretical models and the HIL results. Its design allows the implementation of any topology and any magnetic coupling. The components description of the power converter is presented in Table 9. Considering the reconfigurable characteristic of the power converter, series and parallel interconnections between inductors or capacitors have been done to obtain the closest values to the parameters listed in Table 3. The components configurations are given below:

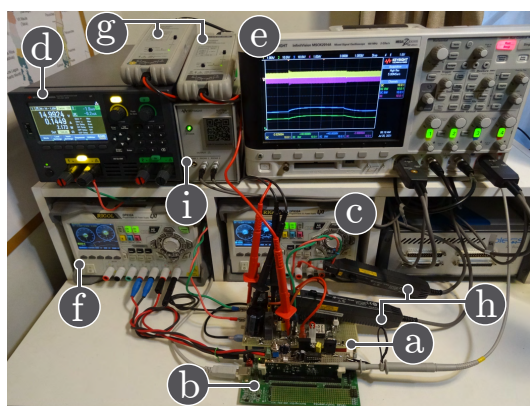
- Coupled inductors: the arrangement to obtain the inductors with magnetic coupling consist of two perfectly magnetic coupled inductors of $9.2 \mu\text{H}$ with two external inductors of $23.7 \mu\text{H}$. The result is two coupled inductors with a mutual inductance of $47.4 \mu\text{H}$ and equal self inductance of $56.6 \mu\text{H}$. The inductors arrangement and its equivalent circuit are shown in Figure 13;
- Non-coupled inductors: it is a series arrangement of inductors of $47 \mu\text{H}$ and $9.2 \mu\text{H}$;
- Intermediate capacitor $0.5 \mu\text{F}$: 5 capacitors of 100 nF connected in parallel;
- Intermediate capacitor $5 \mu\text{F}$: 2 capacitors of $10 \mu\text{F}$ connected in series;
- Damping network capacitor $50 \mu\text{F}$: 5 capacitors of $10 \mu\text{F}$ connected in parallel.

Table 9. Components description of the reconfigurable power converter.

Component	Description	Type
S	Power MOSFET	IRFB4510PBF
L_A	Inductor	Coilcraft's Hexa-Path HPH4-0140L, 23.7 μ H
L_B	Inductor	Wurth Elektronik 7443551920, 9.2 μ H
L_C	Inductor	Wurth Elektronik 74435584700, 47 μ H
C_1 (Test 1, 2)	Multilayer Ceramic Capacitor	TDK C5750X7S2A106M230KB, 2×10 μ F
C_1 (Test 3)	Multilayer Ceramic Capacitor	Murata GRM31C2C1H104JA01L, 5×100 nF
C_2 (Test 1, 2, 3)	Multilayer Ceramic Capacitor	TDK C5750X7S2A106M230KB, 2×10 μ F
C_d (Test 2)	Multilayer Ceramic Capacitor	TDK C5750X7S2A106M230KB, 5×10 μ F
R_d (Test 2)	Damping Resistor	Panasonic ERX5SJ1R5, 1.5 Ω , 5 W

**Figure 13.** Arrangement to obtain the inductors with magnetic coupling: (a) interconnections between inductors, (b) equivalent coupled inductors.

The same tests carried out with HIL have been performed with the converter prototype. The experimental setup of the power circuit is shown in Figure 14. Voltage and current waveforms for a Ćuk converter without magnetic coupling are shown in Figure 15. The effect of the damping network in the SEPIC converter with positive magnetic coupling is shown in Figure 16. Finally, the results of the Zeta converter with negative magnetic coupling are shown in Figure 17. The waveforms in Figures 15 and 16 show good agreement with waveforms in Figures 10 and 11. The results shown in Figure 17 have some distortion due to resonances with parasitic capacitances, but they are similar to the ideal waveforms shown in Figure 12.

**Figure 14.** Experimental setup: (a) reconfigurable power converter, (b) digital signal controller, (c) input dc power supply, (d) dc electronic load in constant resistance mode of 100 Ω , (e) oscilloscope, (f) auxiliary power supply, (g) voltage differential probes, (h) current probes, (i) power supply for the current probes.

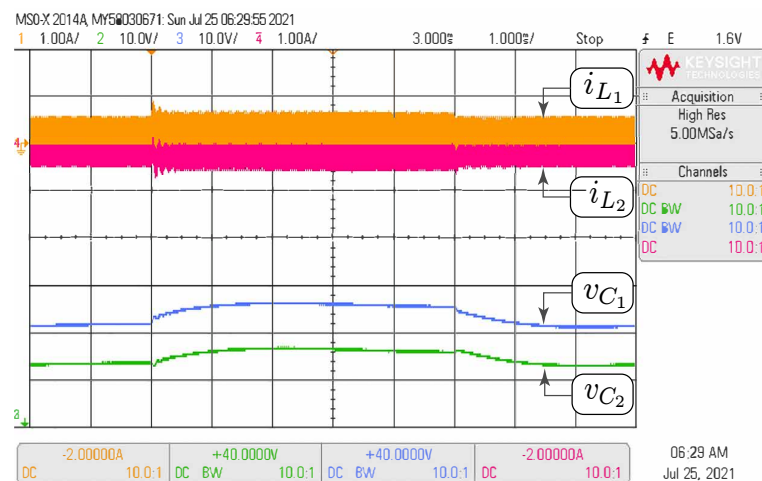
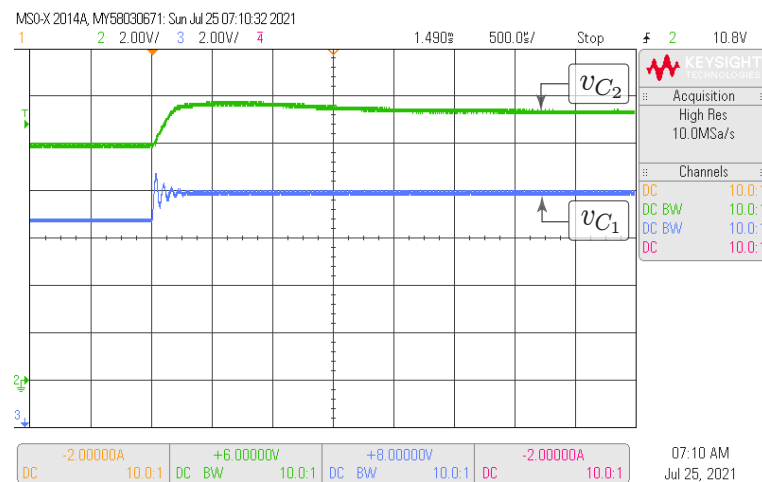
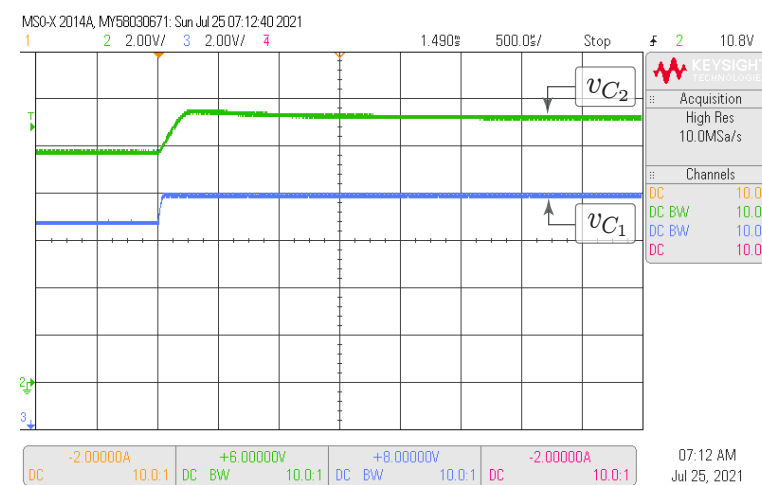


Figure 15. Experimental results for the Ćuk converter without coupled inductors which validate HIL results showed in Figure 10. CH1: i_{L1} (1 A/div), CH2: v_{C2} (10 V/div), CH3: v_{C1} (10 V/div), CH4: $-i_{L2}$ (1 A/div), and time base of 1 ms.



(a) without damping network



(b) with damping network

Figure 16. Experimental results for the SEPIC converter with positive magnetic coupling which demonstrate good agreement with HIL results showed in Figure 11: (a) without damping network, (b) with damping network. (CH2: v_{C2} (2 V/div), CH3: v_{C1} (2 V/div), and time base of 500 μ s).

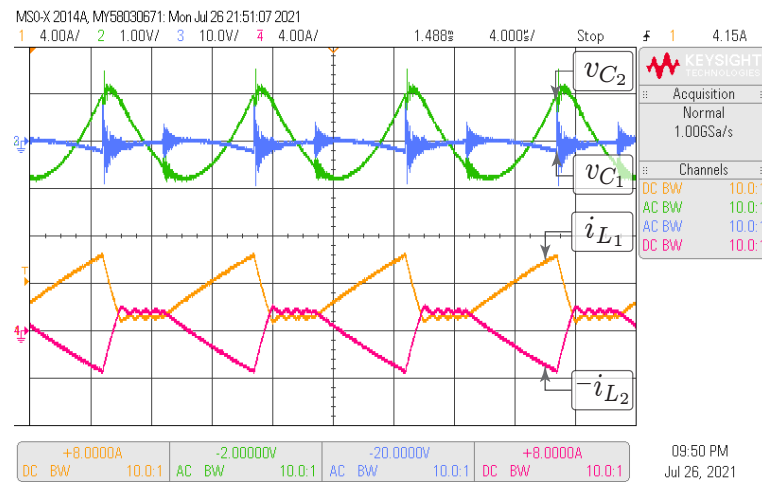
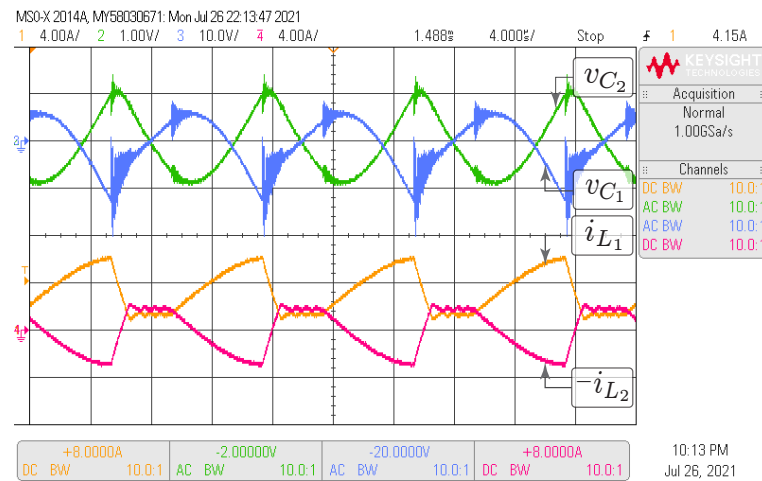
(a) $C_1 = 5 \mu\text{F}$ (b) $C_1 = 0.5 \mu\text{F}$

Figure 17. Experimental results for the Zeta converter with negative magnetic coupling which validate HIL results showed in Figure 12: (a) $C_1 = 5 \mu\text{F}$, (b) $C_1 = 0.5 \mu\text{F}$. CH1: i_{L1} (4 A/div), CH2: v_{C2} (1 V/div, ac coupling), CH3: v_{C1} (10 V/div, ac coupling), CH4: $-i_{L2}$ (4 A/div), and time base of 4 μs .

3.5. Frequency Domain Responses

The Ćuk converter without magnetic coupling has been used to analyze the theoretical model's performance. The same topology was used in the small signal validation. The variables selected for this analysis are one current and one voltage, specifically i_{L1} and v_{C2} . To obtain broad information on the frequency domain response, transfer functions were considered a function of the input voltage and the duty cycle, which are included in Table 5. The lower limit of the frequency analysis is 100 Hz and the upper limit is 50 kHz, a value that corresponds to half the switching frequency. It is observed in all the bode plots shown in Figure 18 that the theoretical model is equivalent to the switched model response. Another common feature is a resonance that occurs at approximately 10 kHz.

3.6. Frequency Domain Validation

Another way to validate the good performance of the proposed methodology is by comparing results with the generalized switch averaging technique [6] in a specific case using frequency responses. To make a fair comparison with the literature, a full-order dynamic model of a Zeta converter in DCM presented in [29] was chosen. The power circuit parameters used to calculate the transfer functions and to obtain the frequency responses are the same as those proposed in [29]. The transfer functions obtained with both

methodologies are given in Table 10. Note that all of the models are fourth order transfer functions and the numerator polynomial is second order. The corresponding frequency responses are shown in Figure 19. Both theoretical responses show a good agreement of the frequency response of the switched model up to a frequency about 1/5 of the switching one. Note that frequency response of reduced-order models is usually considered accurate up to about 1/20–1/10 of the switching frequency.

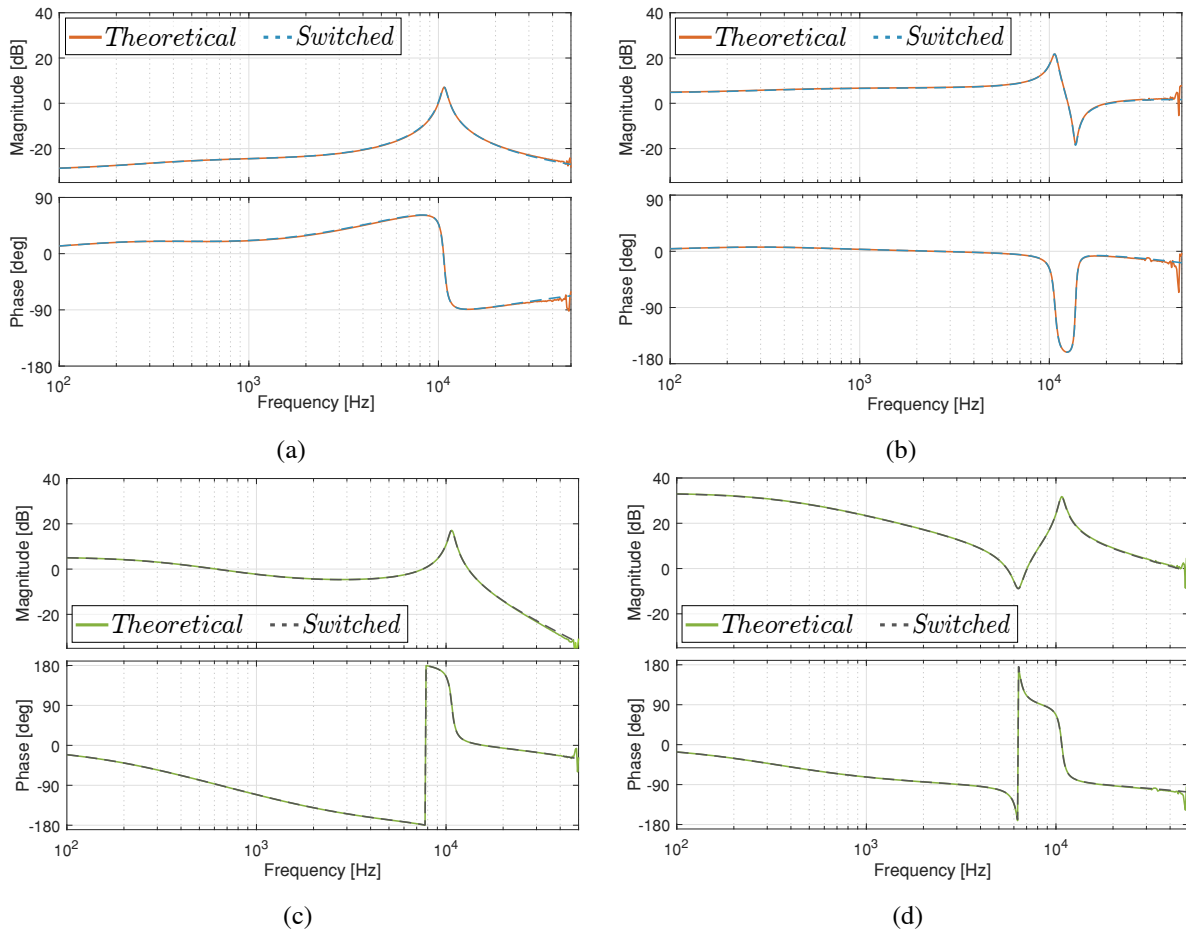
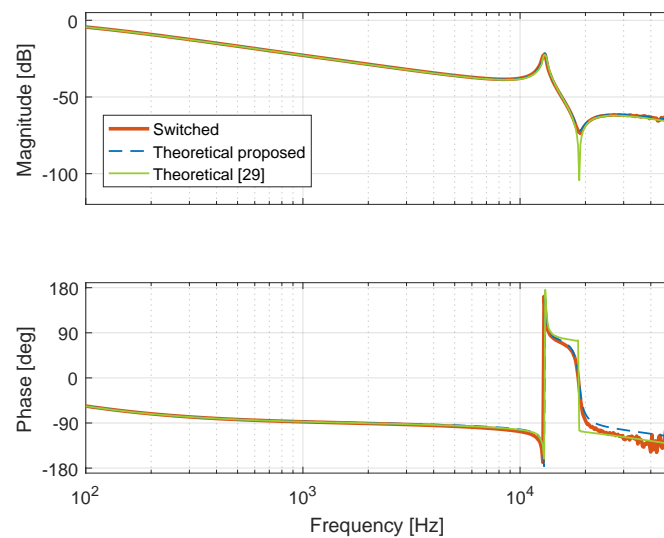


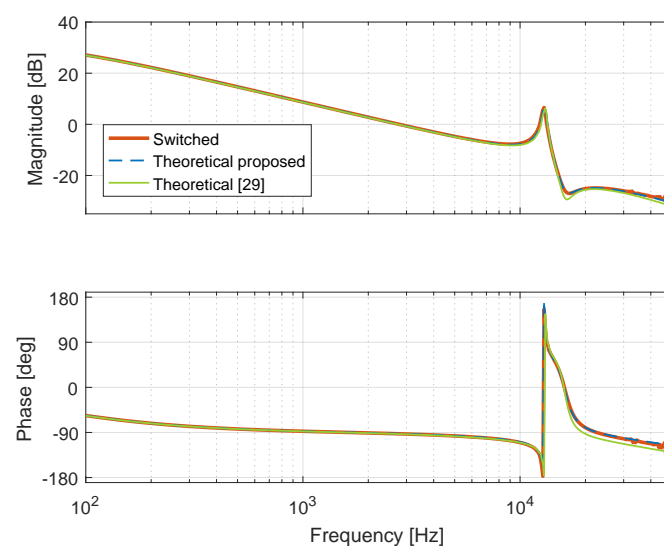
Figure 18. Frequency response of theoretical and switched models for: (a) $\frac{\hat{i}_{L_1}(s)}{\hat{v}_g(s)}$, (b) $\frac{\hat{i}_{L_1}(s)}{\hat{d}(s)}$, (c) $\frac{\hat{v}_{C_2}(s)}{\hat{v}_g(s)}$, and (d) $\frac{\hat{v}_{C_2}(s)}{\hat{d}(s)}$.

Table 10. Theoretical transfer functions of the Zeta converter presented in [29].

Description	Transfer Function
Theoretical proposed	$\frac{\hat{v}_{C_2}(s)}{\hat{v}_g(s)} = \frac{(s + 4348.24)^2 + 117485.36^2}{(s + 421.48)(s + 544303.36)((s + 1292.38)^2 + 81548.65^2)} = \frac{\mathcal{N}_1(s)}{\mathcal{D}_1(s)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{d}(s)} = \frac{(s + 8301.02)^2 + 100829.19^2}{\mathcal{D}_1(s)}$
Theoretical [29]	$\frac{\hat{v}_{C_2}(s)}{\hat{v}_g(s)} = \frac{s^2 + 117564.93^2}{(s + 417.24)(s + 339468.02)((s + 1333.55)^2 + 81988.22^2)} = \frac{\mathcal{N}_2(s)}{\mathcal{D}_2(s)}$ $\frac{\hat{v}_{C_2}(s)}{\hat{d}(s)} = \frac{(s + 5955.04)^2 + 100994.30^2}{\mathcal{D}_2(s)}$



(a)



(b)

Figure 19. Frequency response comparison: (a) $\frac{\hat{v}_{C_2}(s)}{\hat{v}_g(s)}$, (b) $\frac{\hat{v}_{C_2}(s)}{\hat{a}(s)}$.

4. Conclusions

In this paper, a methodology for analyzing high-order switched converters, specifically SEPIC, Ćuk and Zeta, operating in discontinuous conduction mode, is proposed to obtain a full-order dynamic model. The studied converters have very similar piecewise linear current functions if small capacitor voltage ripples are assumed. These converters present a special discontinuity mode where the inductor currents are constant and different from zero. This behavior occurs at the third sub-interval of the switching period in which neither the MOSFET nor the diode conduct. On the basis of the triangular shape of the current diode non-linear average models are obtained. The methodology can be applied to any high-order converter even if additional attributes, such as magnetic coupling or a damping network, are considered. A generalized full-order dynamic model and the steady state operation point summarize the theoretical analysis. Simulations, HIL tests and experimental results validated some full-order small signal models. The comparison of the results demonstrate that theoretical small signal models accurately reproduce the switched models around the operation points as long as the low ripple condition is satisfied. Future

research will deepen in the applications, such as power factor correction or visible light communication, the use of the dynamic DCM model to design control laws of the analyzed high-order converters, and the extension of the proposed model's methodology to other converter topologies not modeled in DCM to date.

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Abbreviations

The following abbreviations are used in this manuscript:

CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
HIL	Hardware In The Loop
PFC	Power Factor Correction
SEPIC	Single-Ended Primary-Inductor Converter

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