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Step up and down converter integrated with motor inverter for powertrain applications

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***Abstract*—Motor inverter high voltage regulation improves the system efficiency and reduce the dimensions of a permanent magnet synchronous motor (PMSM). This paper presents an isolated inverter with step up and step down dc link voltage regulation for an electrical vehicle powertrain system, which will improve the system performance in wide ranges of load and battery levels. Step up and down converter and the motor inverter are merged into a single converter. Bidirectional and galvanically isolated energy transmission between battery and motor with reduced semiconductors number, easy control and high efficiency are demonstrated. In addition, inverter transistors RMS current results lower than in common solutions. Topology waveforms, devices losses and zero voltage switching condition are analyzed. Based on this study, a converter design procedure to meet main electrical vehicles requirements is proposed. Converter operation and design procedure are verified by simulation and experiment in two prototypes of 3.3 kW and 300 W.**

***Index Terms*—Motor, step up, step down, converter, combined, electrical vehicle, dc-ac, high efficiency.**

I. Introduction

The electric propulsion boom into the automotive sector during last years due to new regulations has promoted the use of power converters in the vehicles: [1]–[3]. Inside current vehicle architectures, it may appear up to three voltage levels [4]: high voltage battery working around 400 V which is recharged through the mains, the regenerative braking or from the combustion engine in case of hybrid vehicle. This battery provides energy to the traction system which operates between 200 V and 800 V. Additionally, it exists the low voltage system working at 12 V. Due to multiple DC voltage levels that can coexist in the same vehicle and in order to reduce the large energy storage systems, DC-DC converters have become essential.

This document focuses on the step up and down voltage converter stage and the inverter located between battery and the motor. Commonly used power-train system is described and evaluated in [5], [6] and shown in Fig.1. Battery voltage v_{bat} is elevated with a boost converter till motor inverter bus voltage v_b, thus electrical machine dimensions, as described in [7], can be reduced or the constant torque operation area can be increased. Moreover, [8], [9] explain how motor inverter voltage regulation improves overall system efficiency. In [10], a converter adjusts the DC-link voltage, adding a degree of freedom in the loss minimization control and noticeable energy savings. This voltage control task is usually performed by a boost converter operating under continuous conduction mode. As described in [11], [12], boost converter results a reliable and an easy solution to implement, but large losses exists in converter semiconductors, especially when it operates at high duty cycles. Besides conduction losses, hard switching

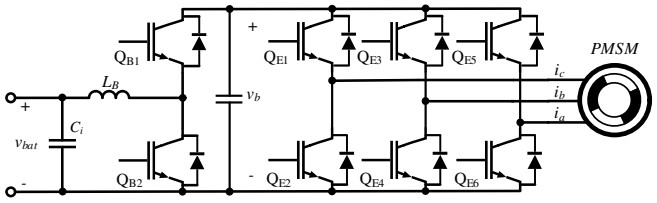

Fig. 1. Classic powertrain system.

events at large currents and voltages occur. This implies large energy spikes that generate electrical noise and a significantly temperature increment in the semiconductors. Boost converter power density is small because of large semiconductors losses, thus complicated cooling system becomes mandatory. Moreover, continuous mode boost converter requires high inductor L_B values. As detailed in [13], converters located between the battery and the motor inverter as well as presenting high efficiency at maximum inverter peak power, they must provide relatively high efficiency, elevated power density and low cost at high, medium and low power. Based on some of this requirements, several converters are placed on same system and they are partially activated/ deactivated depending on vehicle battery and motor status. High efficiencies for all loads and all battery levels were achieved, but cost, size and simplicity result a drawback. In [9], a variable voltage control method for PMSM driven by a Quasi-Z-source inverter is presented. Low number of components is achieved, but the required Z-source capacitances and inductances are relatively large. Similar situation occurs in the Z-Source/Quasi Z-Source comparative evaluated in [14]. The converter topology presented in this paper achieves control simplicity, small component number and high reliability, which are key factors into the automotive sector without neglecting high efficiencies. These characteristics are obtained combining two converters: a zero voltage switching (ZVS) step up and down converter and a motor inverter, into one topology.

Next section presents the proposed converter fundamentals and operation modes. Subsequently, in Section III, topology mathematical analysis is performed where power losses calculation and zero voltage switching condition are evaluated. In order to match electrical vehicle powertrain requirements, converter design procedure is proposed in Section IV. Converter analysis and design procedure are verified by simulation and experimental results in Section V. Finally, Section VI contains paper conclusions.

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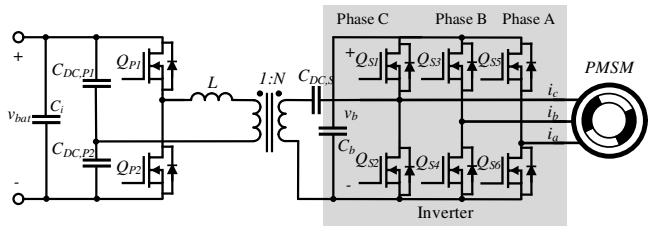

Fig. 2. Proposed converter placing one step up and down stage common to all motor phases. As example, it is implemented using half- bridge configuration.

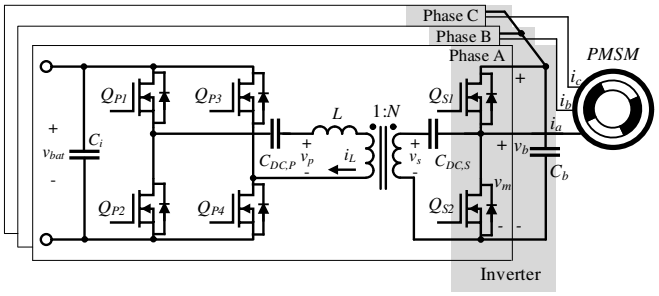

Fig. 3. Proposed converter placing one step up and down stage at each inverter leg. As example, it is implemented using full-bridge configuration.

II. Wide range step up and down inverter

Proposed topology depicted in Fig. 2 integrates the motor inverter and a step up and down stage into one converter. Secondary side transistors Q_S act as a common motor inverter. The step up and down part, which regulates v_b, is composed by the primary side transistors Q_P and a small inductance value L. Bus voltage is fixed and smoothed by the DC-link capacitor C_b, while series capacitors $C_{DC,P}$ and $C_{DC,S}$ block low harmonic signal content avoiding magnetic components saturation. Additionally, nominal voltage gain and galvanic isolation are provided by the transformer with turns relationship N. Proposed converter can be viewed as an extra transistor branch, an inductance and a transformer added to the common motor inverter.

Due to high power levels, in the classic powertrain system shown in Fig. 1, several MOSFETs are used in parallel in the boost stage with the corresponding problems which are described in [15]. Instead MOSFET paralleling, the proposed converter allows to place one step up and down stage at each inverter branch, as shown in Fig. 3. The main difference between Fig. 2 and Fig. 3 is whether to place the step-up and step-down stages in one phase of the inverter or in all three. Fig. 3 solution is preferred because the component stress is better balanced and depending on the motor demanded power, step up and down stages can be activated or deactivated. It also reduces the voltage ripple at C_b. Moreover, depending on current levels, output voltage range and cost requirements; half-bridge or full-bridge in Fig.2 and Fig.3 can be selected indistinctly in the step up and down stage. If the choice is made to implement the full-bridge configuration, it is possible to increase the operating range, as it can be converted into a half-bridge configuration. The converter in Fig.2 is more suitable for low power and low cost systems, while the topology in Fig.3 is recommended for higher powers and efficiencies. It is important to note that the converter, at the output, is capable of step up and down around its optimum point, the input voltage multiplied by N in the case of a half-bridge or $2N$ in the case of a full-bridge. The presented converter does not suffer, as the typical boost converter, of high voltage elevation ratios. It allows to reduce and increase the input voltage, achieving a wide operating range. In contrast to the conventional boost stage, the presented solution achieves zero voltage switching (ZVS) in the step up and down stage reducing switching losses and electromagnetic emissions. Moreover, RMS current in the inverter stage semiconductors is slightly smaller since part of the power is transferred directly from the primary side transistors to the motor.

Analyzing the phase A of Fig. 3, Fig.4 describes the eight states that the converter can be in. States I-IV correspond to positive phase current i_a values, while V-VIII match with negative i_a values. During State I, i_L current reverses from negative to positive. At the beginning of the state, primary side MOSFETs body diodes are conducting and then MOSFETs channels are activated under ZVS condition. Energy is transferred directly from the battery in State I and along Q_{S1} in State II. Until State II is completed, primary positive current is transferred directly to the motor. Similar to State I, i_L current direction changes from positive to negative in State III. In this state and in State IV, C_b feeds the motor and also provides recirculating current to the primary side that makes easier to obtain ZVS. It is important to note that in previous states C_b is being discharged. This situation is reversed when i_a turns negative. Thus states V-VIII arise and capacitor is charged. States V to VIII are analogous to States III to IV. It must be highlighted that part of the current is transferred directly from the primary to the motor or vice-versa without circulating through the secondary side transistors, the inverter ones, relieving stress on them.

For better states operation understanding, main converter waveforms are depicted in Fig.5. As it can be observed, primary inductance current i_L depends on the voltage difference between v_p and v_s. In Fig.3, primary side full-bridge generates v_p which corresponds to a square wave with peak voltage $\pm v_{bat}$ and period T_{sw}. Secondary side voltage v_s is given by the half-bridge which acts also as a common motor inverter branch. Period of v_s is set equal to v_p period, T_{sw}. Motor inverter branch duty cycle d_2 is specified by motor control. Q_S follows the modulation signal of the inverter control. Permanent magnet synchronous motors control, detailed in [16], [17], is usually based on space vector algorithm which handles inverter activation signals using pulse width modulation. Voltage bus regulation is done using a Phase Shift Control strategy, implying primary side duty cycle d_1 must be identical to d_2. Therefore, d_1 is copied from the conventional motor inverter control which handles d_2. The phase shift between v_p and v_s, named as ϕ, is the control variable which is adjusted in order to transfer required motor power from the battery and regulate the bus voltage. Higher ϕ values imply more power transfer from primary side to secondary side. Positive ϕ values transfer energy from the battery to the engine, while negative values transfer energy from the motor to the battery.

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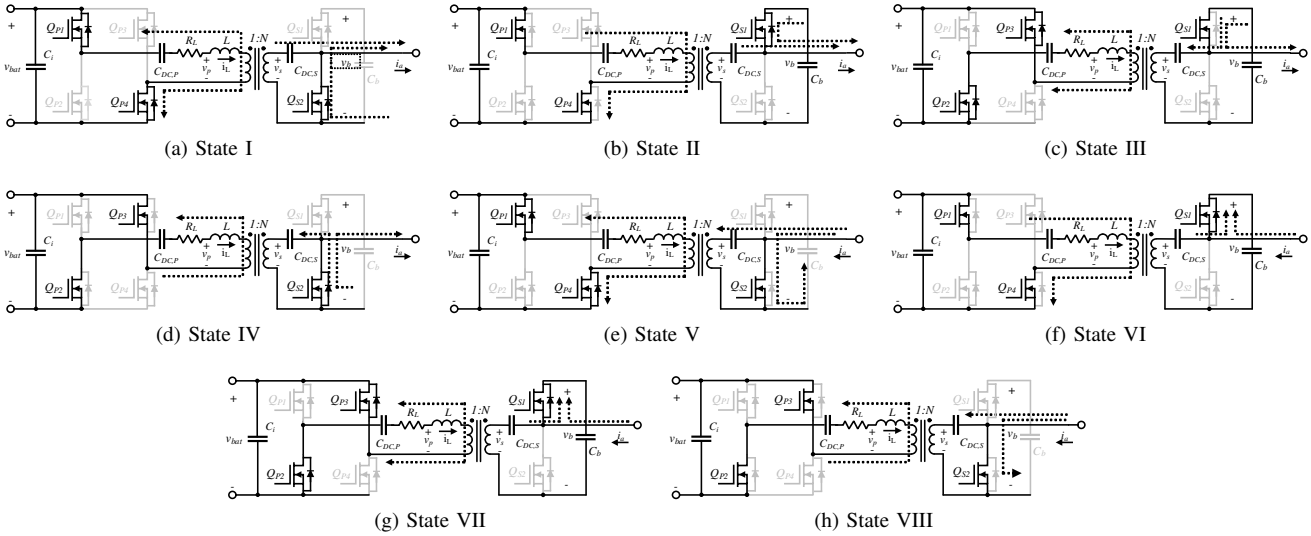

(a) State I (b) State II (c) State III

(d) State IV (e) State V (f) State VI

(g) State VII (h) State VIII

Fig. 4. Circuit states of Phase A converter. States I-IV correspond to positive i_m current and VI-VIII fits negative i_m current.

This bi-directional energy transfer capability can be used in regenerative braking task, which is explained in [18].

III. Analysis

This section describes analytically the converter operation including the waveform shapes, the power loss model and the zero voltage switching condition. With that purpose, converter located in phase A in Fig.3 is analyzed.

A. Waveforms

Detailed devices waveforms at different points of one phase current period are shown in Fig.5. Three different i_a points are depicted: 1, when i_a is positive; 2, when i_a is zero and 3 when i_a is negative. In each point, the duty cycle is different and the corresponding states of Fig. 4 are identified. Assuming ϕ is between 0 and $\min(d_1, d_2, 1-d_1, 1-d_2)$, four current slopes can be distinguished in the inductor L depending on the voltage difference between v_p and v_s:

$$m_{i_L}(\tau) = \begin{cases} m_{i_L,1} & 0 < \tau \leq \phi T_{sw} \\ m_{i_L,2} & \phi T_{sw} < \tau \leq d_1 T_{sw} \\ m_{i_L,3} & d_1 T_{sw} < \tau \leq (d_2+\phi) T_{sw} \\ m_{i_L,4} & (d_2+\phi) T_{sw} < \tau \leq T_{sw} \end{cases} \quad (1)$$

where $\tau = t - nT_{sw}$.

$$m_{iL,1} = \frac{d_2 v_b + (2-2d_1)\, N\, v_{bat}}{LN} \quad (2)$$

$$m_{iL,2} = \frac{(d_2-1)\, v_b + (2-2d_1)\, N\, v_{bat}}{LN} \quad (3)$$

$$m_{iL,3} = \frac{-(1-d_2)\, v_b/N - 2d_1 v_{bat}}{L} \quad (4)$$

$$m_{iL,4} = \frac{d_2 v_b/N - 2d_1 v_{bat}}{L} \quad (5)$$

Once inductor current slope is obtained. instant inductor current i_L can be determined as the initial current $i_L(nT_{sw})$ plus the increment $\Delta i_L(\tau)$:

$$i_L(t) = i_L(nT_{sw}) + \Delta i_L(\tau) \quad (6)$$

$$\Delta i_L(\tau) = \begin{cases} \Delta i_{L,1}(\tau) & 0 < \tau \leq \phi T_{sw} \\ \Delta i_{L,2}(\tau) & \phi T_{sw} < \tau \leq d_1 T_{sw} \\ \Delta i_{L,3}(\tau) & d_1 T_{sw} < \tau \leq (d_2+\phi) T_{sw} \\ \Delta i_{L,4}(\tau) & (d_2+\phi) T_{sw} < \tau \leq T_{sw} \end{cases} \quad (7)$$

where

$$\Delta i_{L,1}(\tau) = m_{iL,1}\tau \quad (8)$$

$$\Delta i_{L,2}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(\tau - \phi T_{sw}) \quad (9)$$

$$\Delta i_{L,3}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(d_1 - \phi) T_{sw} + m_{iL,3}(\tau - d_1 T_{sw}) \quad (10)$$

$$\Delta i_{L,4}(\tau) = m_{iL,1}\phi T_{sw} + m_{iL,2}(d_1 - \phi) T_{sw} + m_{iL,3}(d_2 + \phi - d_1) T_{sw} + m_{iL,4}(\tau - (\phi + d_2) T_{sw}) \quad (11)$$

Since series capacitor exist, average current must be zero. It is assumed that the time constant imposed by the series capacitors $C_{DC,x}$ is small and do not affect the system. That means, the value that makes the average current equal to zero corresponds to $i_L(nT_{sw})$ during each switching period:

$$i_L(nT_{sw}) + \frac{1}{T_{sw}} \int_0^{T_{sw}} \Delta i_L(\tau) \mathrm{d}\tau = 0 = i_L(nT_{sw}) + \frac{1}{T_{sw}} \left(\int_0^{\phi T_{sw}} \Delta i_{L,1}(\tau) \mathrm{d}\tau + \int_{\phi T_{sw}}^{d_1 T_{sw}} \Delta i_{L,2}(\tau) \mathrm{d}\tau + \int_{d_1 T_{sw}}^{(d_2+\phi) T_{sw}} \Delta i_{L,3}(\tau) \mathrm{d}\tau + \int_{(d_2+\phi) T_{sw}}^{T_{sw}} \Delta i_{L,4}(\tau) \mathrm{d}\tau \right) \quad (12)$$

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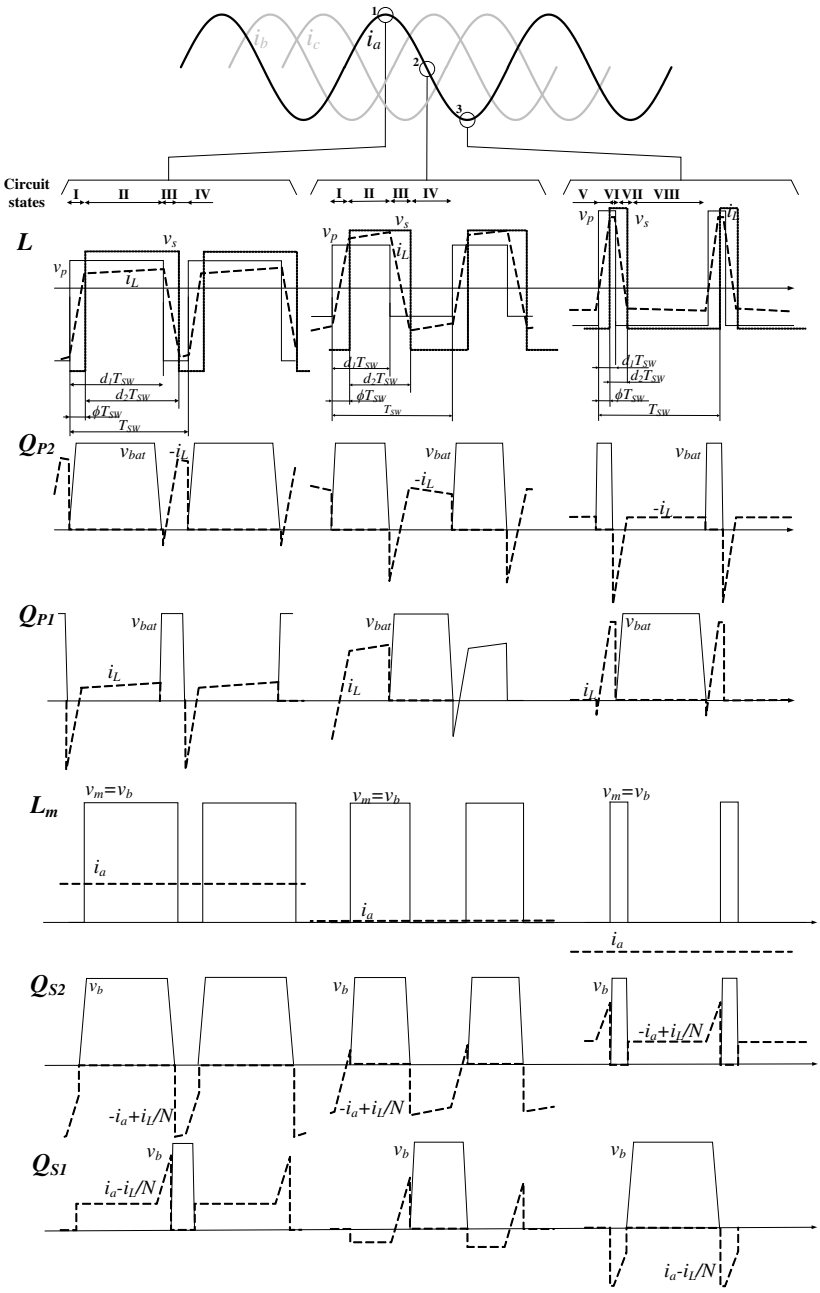

Fig. 5. Device waveforms of the proposed converter.

Once i_L current is obtained, input power P_i can be calculated as the current flowing through the inductor multiplied by the applied input voltage at the first inductor terminal:

$$\langle P_i \rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_p(t) i_L(t)\ \mathrm{d}t = \frac{1}{T_{sw}} \left(E_1 + E_2 + E_3 + E_4\right) \quad (13)$$

where

$$E_1 = \int_0^{\phi T_{sw}} 2v_{bat}(1-d_1) i_L(\tau))\ \mathrm{d}\tau \quad (14)$$

$$E_2 = \int_{\phi T_{sw}}^{d_1 T_{sw}} 2v_{bat}(1-d_1) i_L(\tau)\ \mathrm{d}\tau \quad (15)$$

$$E_3 = \int_{d_1 T_{sw}}^{d_2+\phi T_{sw}} -2v_{bat} d_1 i_L(\tau)\ \mathrm{d}\tau \quad (16)$$

$$E_4 = \int_{d_2+\phi T_{sw}}^{T_{sw}} -2v_{bat} d_1 i_L(\tau)\ \mathrm{d}\tau \quad (17)$$

Assuming high efficiency, the output power P_o equals P_i:

$$\langle P_o \rangle_{T_{sw}} = \frac{\left(\phi^2 - \left(2d_1 d_2 + 2d_1\right)\phi - d_1 {d_2}^2\right) v_{bat} v_b}{L\, f_{sw} N} + \frac{\left(\left({d_1}^2 + d_1\right) d_2 - {d_1}^2\right) v_{bat} v_b}{L\, f_{sw} N} \quad (18)$$

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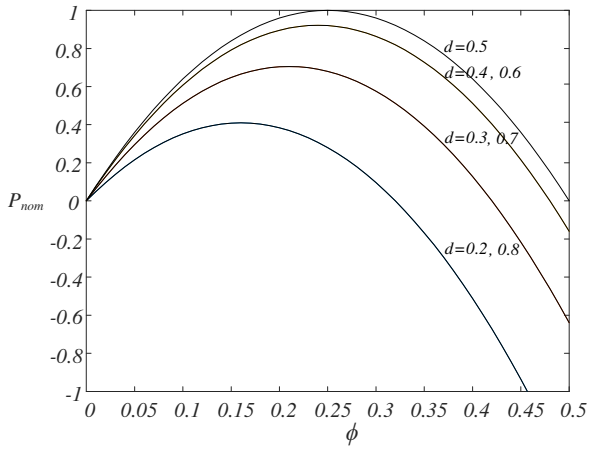

Fig. 6. Normalized output power. Valid for $0 < \phi < min(d, 1-d)$.

If $d_1 = d_2 = d$, condition which simplifies the converter control, equation (18) can be rewritten as:

$$\langle P_o \rangle_{T_{sw}} = \frac{\left(-\phi^2 + \left(-2d^2 + 2d\right)\phi\right) v_{bat} v_b}{L\, f_{sw} N} \tag{19}$$

Considering normalized output power P_{nom} as:

$$P_{nom} = \frac{P_o}{P_{o,max}} \tag{20}$$

Fig.6 arises, where it can be observed that maximum output power is achieved with $d = 0.5$. As long as duty cycle deviates from its central value, output power decreases. Lower ϕ values implies lower output power. If ϕ goes further than half the duty cycle, power transfer starts to decrease. Symmetrical graph is obtained when ϕ takes negative values. If ϕ is negative, power transfer direction reverses and power energy flows from the output bus to the battery. It is important to note that P_o refers to the power transferred through the transformer to the output.

B. Efficiency

Efficiency is defined as:

$$\eta = \frac{P_o}{P_i} = \frac{P_i - P_{loss}}{P_i} \tag{21}$$

where P_{loss} represents the total power losses across the circuit. Main converter losses occur at primary and secondary switching devices, Q_p and Q_s, and the magnetic parts: L and transformer. Total losses P_{loss} are obtained by adding conduction P_{cond}, switching P_{sw} and magnetic losses P_{mag}. Regarding switching devices, conduction and switching losses are evaluated.

1) Conduction losses: Conduction looses depend on the RMS current. Primary side RMS current that flows through $Q_{p,1}$ and $Q_{p,3}$ from $\tau = 0$ to $\tau = d_1 T_{sw}$ is given by:

$$I_{p,rms,0\_d_1} = \left(\frac{1}{T_{sw}} \int_0^{d1T_{sw}} i_L(\tau)^2 \, \mathrm{d}\tau\right)^{1/2} \tag{22}$$

Primary side RMS current during remaining switching cycle that affects Q_{p_2} and $Q_{p,4}$ from $d_1 T_{sw}$ to T_{sw} results:

$$I_{p,rms,d_1\_T} = \left(\frac{1}{T_{sw}} \int_{d1T_{sw}}^{T_{sw}} i_L(\tau)^2 \, \mathrm{d}\tau\right)^{1/2} \tag{23}$$

In case secondary side switching devices, RMS current from ϕT_{sw} to $(d_2 + \phi)T_{sw}$ is:

$$I_{s,rms,\phi\_d_2\phi} = \frac{1}{T_{sw}} \left(\int_{\phi T_{sw}}^{(d_2+\phi)T_{sw}} \left(-\frac{i_L(\tau)}{N} + i_a\right)^2 \, \mathrm{d}\tau\right)^{1/2} \tag{24}$$

From $(d_2 + \phi)T_{sw}$ till ϕT_{sw} obtained current is:

$$I_{s,rms,d_2\phi\_\phi} = \left[\frac{1}{T_{sw}} \left(\int_{(d_2+\phi)T_{sw}}^{T_{sw}} \left(\frac{i_L(\tau)}{N} - i_a\right)^2 \, \mathrm{d}\tau + \int_0^{\phi T_{sw}} \left(\frac{i_L(\tau)}{N} - i_a\right)^2 \, \mathrm{d}\tau\right)\right]^{1/2} \tag{25}$$

Finally, each MOSFET conduction losses P_{cond} can be obtained multiplying the squared RMS current by the MOSFET channel resistance $R_{ds,on}$.

2) Switching losses: Switching losses are relevant in the application since large voltages and currents are switched at reasonable high frequency. Primary side switches Q_p are expected to operate under ZVS conditions at turn on, while hard switching occurs at turn off. Given this situation, Q_p turn on switching losses are neglected while turn off switching losses are dominated by the MOSFET output capacitance C_{oss}. Voltage across C_{oss} at the end of the switching off is:

$$v_{SW,Coss}(t_f) = \int_0^{t_f} \frac{I_{ini} t}{C_{oss} t_f} \mathrm{d}t = \frac{I_{ini} t_f}{2C_{oss}} \tag{26}$$

Where I_{ini} makes reference to the current value at the turn off instant and t_f refers to the MOSFET current falling time. Current through the MOSFET during switching is:

$$i_{SW,C_{oss}} = I_{ini}\left(1 - \frac{t}{t_f}\right) \tag{27}$$

Assuming linear charging/ discharging process, power losses caused by non-zero turn off time is given by:

$$P_{SW,C_{oss}}(I_{ini}) = \frac{1}{T_{sw}} \int_0^{t_f} v_{SW,C_{oss}} i_{SW,C_{oss}} \mathrm{d}t = \frac{{I_{ini}}^2 f_{sw} {t_f}^2}{24 C_{oss}} \tag{28}$$

As detailed in equation (28), higher C_{oss} value leads to lower switch off losses. This is due to passive snubber effect which minimizes the voltage slope. It is important to highlight that large C_{oss} values require higher current values or higher dead time to ensure the complete capacity discharge. Two turn off primary side switching events occur during each switching cycle:

$$P_{SW,C_{oss},1} = P_{SW,C_{oss}}(I_{ini} = i_L(d_1 T_{sw})) \tag{29}$$

$$P_{SW,C_{oss},2} = P_{SW,C_{oss}}(I_{ini} = i_L(T_{sw})) \tag{30}$$

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In contrast with primary side, secondary side semiconductors operate under hard switching conditions. Along each transition, one MOSFET branch turns on and one turn off:

$$P_{SW,Hard}(I_{ini}) = \frac{1}{2} v_b I_{ini}(t_{ri} + t_{fv}) f_{sw} + \frac{1}{2} v_b I_{ini}(t_{rv} + t_{fi}) f_{sw} \quad (31)$$

Parameters t_{ri}, $t_{f,v}$, t_{rv}, t_{fi} refer to current rise time, voltage fall time, voltage rise time and current fall time respectively. Since two switching events occurs during each T_{sw}, substituting I_{ini} in equation (31) results:

$$P_{SW,Hard,1} = P_{SW,Hard}(I_{ini} = \frac{i_L(\phi T_{sw})}{N} - i_a) \quad (32)$$

$$P_{SW,Hard,2} = P_{SW,Hard}(I_{ini} = \frac{i_L((d_2 + \phi) T_{sw})}{N} - i_a) \quad (33)$$

3) Passive components: Magnetic components are relevant in this application since the ratio between L and f_{sw} determines the output power and also establish a correlation between losses and volume. Higher frequencies leads to reduced components volume: smaller L, transformer magnetizing inductance L_{mag} and capacitor values are required; but looses will increase. Magnetic looses can be separated into core losses and winding losses. Improved Generalized Steinmetz Equation detailed in [19], allows to calculate core losses for arbitrary shape waveforms:

$$P_{core} = \frac{1}{T_{sw}} \int_0^{T_{sw}} k_1 \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right| B(t)^{\beta - \alpha} \mathrm{d}t \; v \quad (34)$$

where

$$k_1 = \frac{k}{2\pi^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} |\sin\theta|^{\beta-\alpha} \mathrm{d}\theta} \quad (35)$$

B represents the magnetic flux density and v the core volume. Constants k, α and β are provided by core materials manufacturers, which are obtained by experimental measurements. Flux density in the inductor can be obtained in terms of:

$$B_L(t) = \frac{L i_L(t)}{n A_e} \quad (36)$$

where A_e is the effective core area and n is the number of turns. In case of the transformer, flux results:

$$B_T(t) = \frac{1}{n_p A_e} \int \frac{v_b(t)}{N} \mathrm{d}t \quad (37)$$

being n_p the number of turns at the primary. Regarding winding losses, as well as presenting low frequency conduction losses, high frequency losses appear. The most significant high frequency losses that exist are skin effect and proximity effect. Dowell's method is a simply and reasonably accurate way to obtain coils losses representation. Dowell's high frequency resistance of the coil approximation for Litz wire, R_{ac}, is described in [20]:

$$R_{ac} = R_{dc} \left(1 + \frac{(\pi n_s N_w)^2 d_s^6}{192 \delta^4 b^2} \right) \quad (38)$$

where b is the windings window height, n_s is the strands number, N_w is the winding turns number and δ is the skin depth:

$$\delta = \sqrt{\frac{\rho}{\pi f_{sw} \mu_0}} \quad (39)$$

Constant μ_0 is the free space permeability and constant ρ is the conductor resistivity. Low frequency windings resistance results:

$$R_{dc} = \rho \frac{N_w M}{\left(\frac{d_s}{2}\right)^2 \pi n_s} \quad (40)$$

where M is the mean length per turn. Finally, winding losses can be obtained as:

$$P_{winding,h} = I_{L,rms,h}^2 R_{ac,h} \quad (41)$$

Sub-index h makes reference to the harmonic. If the current signal contains several relevant high order harmonics, they must be taken into account. Also, if several windings appear on same magnetic component, as in a transformer, losses in each winding needs to be included. Both, transformer and series inductor must be considered in the magnetic losses:

$$P_{mag} = P_{core,L} + P_{windings,L} + P_{core,T} + P_{windings,T} \quad (42)$$

The capacitor losses P_c can be calculated as:

$$P_c = R_{C_{DC,P}} I_{p,rms}^2 + R_{C_{DC,S}} I_{s,rms}^2 \quad (43)$$

C. ZVS condition

Primary side semiconductors must operate under ZVS condition to avoid extra looses and EMI issues. In order to guarantee that condition, switches must be turned on during anti-parallel diodes conduction time. Since two switching instants occur at primary side during T_{sw}, the following conditions must be satisfied:

$$i_{L,sw1} = i_L(\tau = 0) < 0 \quad (44)$$

$$i_{L,sw2} = i_L(\tau = d_1 Tsw) > 0 \quad (45)$$

Moreover, external MOSFETs parallel capacities C_{oss} must be charge-discharged before current changes direction. As described in [21], to achieve ZVS in primary side full-bridge, stored energy in inductor L must be large enough to discharge / charge the four parallel capacities $C_{oss,eq}$. Additional parasitic capacitance C_{stray} must be also considered and be charged/discharged.

$$|i_{L,sw1}, i_{L,sw2}| > \sqrt{\frac{(4C_{oss,eq} + C_{stray}) v_{bat}^2}{L}} \quad (46)$$

IV. Design procedure

This section presents a design methodology to meet common electrical vehicle powertrain specifications: battery and motor bus voltage range, maximum and minimum inverter duty cycle, and output power. The United States Environmental Protection Agency (EPA) defines three different drive schedules in [22]: Urban Dynamometer Drive Schedule (UDDS) that is focused on city driving conditions, the Highway Fuel Economy Test (HWFET) that aims highway driving and the US06 centered in competitive driving. According to

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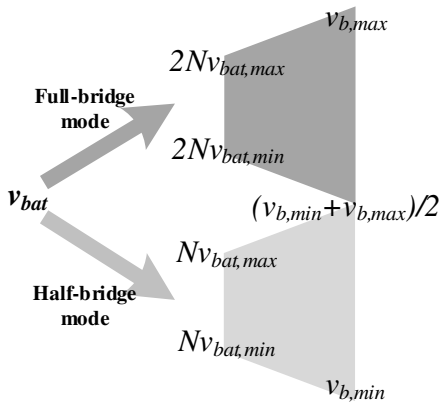

Fig. 7. Operation modes.

that, output power during city driving is less than 10% of the maximum and the motor inverter operates at low voltages. Highway driving cycle is characterized by handling mid output voltages and 20% of the maximum power. US06 implies working at maximum output power and high voltages. In other words, maximum output power is given at higher bus voltages and low output power corresponds to lower bus voltages. Given previous condition, full-bridge configuration can be implemented for high output voltages and switch to half-bridge configuration when low output voltages are required. Toggling between full-bridge and half-bridge configurations with the same hardware can be done by maintaining enabled Q_{P4} and Q_{P3} disabled. Maximum converter efficiency is stated when converter operates close to its natural voltage amplification given by N for half-bridge or $2N$ for full-bridge. To meet wide input and output voltage ranges and ensure converter gain operates close to its maximum efficiency point a full-bridge configuration is implmented. Half-bridge and full-bridge operation modes are defined in Fig.7 and converter may switch into one mode or the other. In order to make the transition between the two modes, a soft transition procedure must be implemented in the primary side semiconductors to avoid current spikes. As shown in Fig. 7 and to cover the wide operating range, N can be calculated as:

$$N = \frac{(v_{b,min} + v_{b,max})/2 + v_{b,min}}{v_{bat,min} + v_{bat,max}} \tag{47}$$

Once N is obtained, f_{sw} is taken from motor inverter control parameters. The inverter can operate with a modulation index from 0 to 1, which may involve extremal duty cycles. As shown in Fig. 6, instantaneous minimum output power by the step and down part is delivered at d_{min} or d_{max} duty cycles values. This means that when one phase of the inverter is operating at duty cycles lower or higher than d_{min} or d_{max} respectively, the step up and down stage of that phase will not be able to deliver the instantaneous power needed to maintain the bus voltage. When this occurs, the other two phases operate around d=0.5 and can supply the power needed, allowing the use of a small value capacitor. As a design criteria, d_{min} and d_{max} define the range of duty cycles where a maximum power can be supplied by one individual phase. It is important to remark that for values closer to d=0.5, the stage would instantly be able to deliver more instantaneous power than nominal power and maintain v_b. Selecting maximum and minimum cycles close to 0.5 (i.e., d_{max}=0.6, d_{min} =0.4) will increase v_b ripple, while very extreme values will increase losses (i.e., d_{max} =0.9, d_{min} =0.1). It is therefore recommended to use an intermediate term: d_{max}=0.8, d_{min}=0.2. Variables d_{max}, d_{min} are used to adjust the value of L, not to limit the inverter duty cycle. Consequently, inductance L must be selected to provide required maximum power at critical condition: minimum duty cycle and minimum battery level. It can be calculated rewriting equation (19) and substituting ϕ by $d_{min}(1 - d_{min})$, where according to (19), the maximum output power is given:

$$L = \frac{\left(d_{min}^4 - 2d_{min}^3 + d_{min}^2\right) v_{bat,min} v_{b,min}}{\langle P_o \rangle_{T_{sw}} f_{sw} N} \tag{48}$$

The DC blocking capacitors $C_{DC,P}$ and $C_{DC,S}$, as in typical DC-DC converters, should be chosen appropriately so they are not too small to cause a large voltage drop across the voltage square waveforms, v_p and v_s, under steady-state operating condition and not to large to avoid affecting transient behavior. For full-bridge implementation, the minimum value of $C_{DC,P}$ and $C_{DC,S}$ can be obtained by:

$$C_{DC,P} = \frac{P_o d_{max}}{v_{bat,min} f_{sw} v_{drop}} \tag{49}$$

$$C_{DC,S} = \frac{P_o d_{max}}{v_{bat,min} f_{sw} v_{drop} N} \tag{50}$$

where v_{drop} represents the allowed voltage drop of the square waveforms. It is recommended to be between 5 and 10% of v_{bat} or v_b. In case half-bridge is implemented, obtained capacitors values using (49) and (50) must be multiplied by 2. Averaged phase angle, which is the control signal, during one motor sinusoidal current cycle $\langle \phi \rangle_{T_m}$ must be calculated to obtain averaged looses. $\langle \phi \rangle_{T_m}$ is obtained from equation (19):

$$\langle \phi \rangle_{T_m} = \left(d_{avg} - {d_{avg}}^2\right) + \frac{\sqrt{\left({d_{avg}}^4 - 2{d_{avg}}^3 + {d_{avg}}^2\right) v_{bat} v_b - L \langle P_o \rangle_{T_{sw}} f_{sw} N}}{\sqrt{v_{bat}}\sqrt{v_b}} \tag{51}$$

where d_{avg} is the average duty cycle value over a quarter of a motor phase current sinusoidal cycle. Then, P_{loss} and currents are calculated substituting d_{avg} and $\langle \phi \rangle_{T_m}$ in equations given in subsection III-B. ZVS conditions in equations (44) and (45) must be checked. If they are not satisfied, lower L value should be selected or $\langle P_o \rangle_{T_{sw}}$ must be limited when duty cycle is at extreme values. Given that situation, at least one stage per inverter branch is required. When one phase is at extreme duty cycle, another phase will be close to $d = 0.5$ and will be able to provide more power and compensate the phase which provides less power. Another way to increment delivered power and maintain ZVS is slightly reduce f_{sw} for a fixed L. If motor control allows, several procedure iterations varying f_{sw} and L can be done, which permits an optimization between power density and losses.

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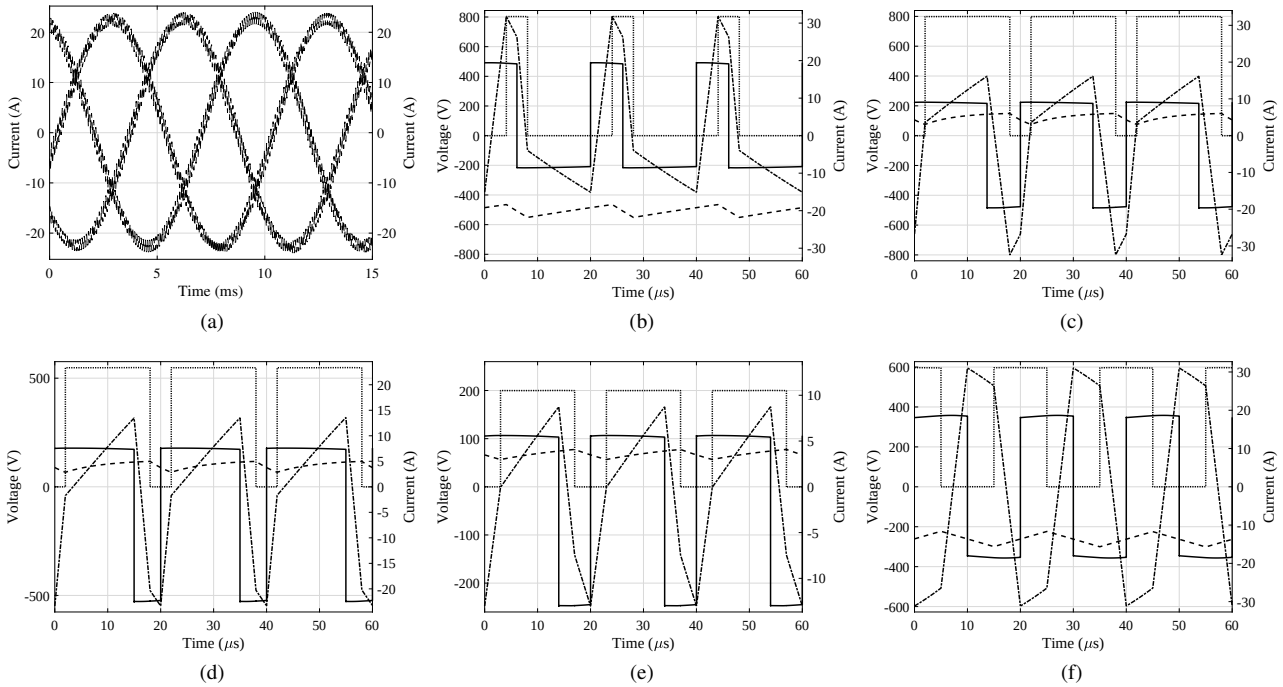

Fig. 8. Proposed design simulations results operating at 3300 W per phase in different conditions. Solid trace v_p, dotted trace v_m, dash-dot trace i_p and dash trace i_a. (a) Phase currents: i_a, i_b and i_c. (b) d_2=0.2, v_b=800 v_{bat}=350 V. (c) d_2=0.8, v_b=800 v_{bat}=350 V. (d) d_2=0.8, v_b=550 v_{bat}=350 V. (e) Half-bridge operation: d_2=0.8, v_b=200 v_{bat}=350 V.(d) Reverse operation: d_2=0.5, v_b=600 v_{bat}=350 V.

TABLE I
SYSTEM DESIGN PARAMETERS

Parameter	Value
Battery voltage range, V_{bat}	290-420 V
Motor bus voltage range, V_b	200-800 V
Maximum phase output power, $P_{o,max}$	3.3 kW
Turns ratio, N	1
Inductor, L	59 μH
Blocking capacitors, $C_{DC,P}$ and $C_{DC,S}$	10 μF
Switching frequency, f_{sw}	50 kHz

TABLE II
PMSM SPECIFICATIONS

Parameter	Value
Pole pairs	4
Rated torque, $T_{m,nom}$	50 Nm
Rated speed, $w_{m,nom}$	200 rad/s
Rated power, $P_{m,nom}$	10 kW
Armature inductance, L_m	3 mH
Stator resistance, R_m	1.5 Ω
Torque constant, K_T	1.8 Nm/A

V. SIMULATION AND EXPERIMENTAL RESULTS

Considering typical automotive industry voltage levels and following the proposed design methodology, the converter parameters listed in TABLE I are obtained. Each of the three phases has one converter which is designed to withstand 3.3 kW, making possible to supply a motor of 10 kW. To evaluate the feasibility of the proposal and the performance of the whole system, different tests of the designed converter supplying a 10 kW PMSM are done by simulation using MATLAB-Simulink. Focusing on the behavior of a single phase operating at 3.3 kW, Fig. 8 shows the simulation results of different situations or critical points that the designed converter must deal with during a switching cycle. Fig. 8b shows the waveforms of the converter when the bus voltage is boosted to its maximum, 800 V, with the minimum duty condition. Fig. 8c demonstrates that 800 V can be also obtained with the maximum duty cycle. According with the operation modes described in Fig. 7; when the converter works in full-bridge mode, the minimum bus voltage before changing to half-bridge mode must be guaranteed. This bus voltage is 550 V and the converter operation is depicted by Fig. 8d. Fig. 8e shows the feasibility to reach the minimum bus voltage, 200 V with a high battery voltage level thanks to the half-bridge mode. In all cases, ZVS is accomplished in the primary side at turn on, since (44) and (45) are satisfied, ensuring the MOSFET body diode conducts before the channel activation. Regenerative braking or reverse operation is illustrated in Fig. 8f. It can be distinguished from normal application because phase ϕ is negative. ZVS situation is now achieved at the secondary side. Additionally, in Fig. 8a, the three phase converters are operated simultaneously at 3.3 kW each during multiple switching cycles generating the motor phases currents.

From the motor control point of view, the proposed converter acts as a typical inverter. It is able to generate the slow phase currents varying the duty cycle. The operation of the PMSM with the properties contained in TABLE II is simulated. Fig. 9a depicts the simulation results of the start-up transient of the motor with a speed reference of 200 rad/s. At

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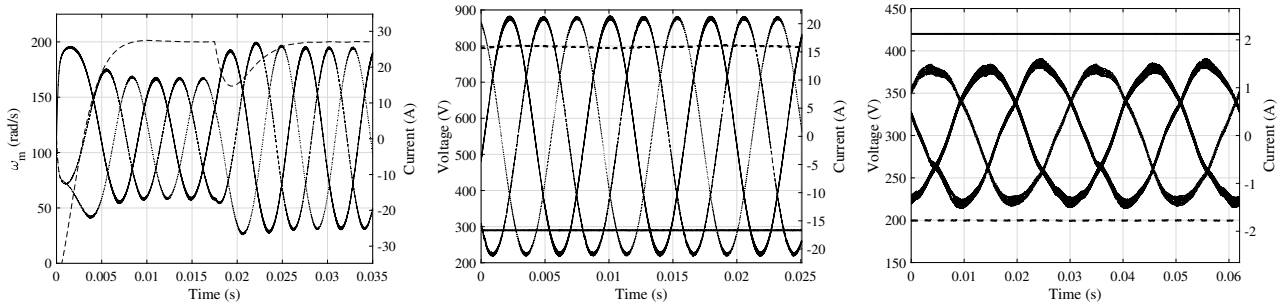
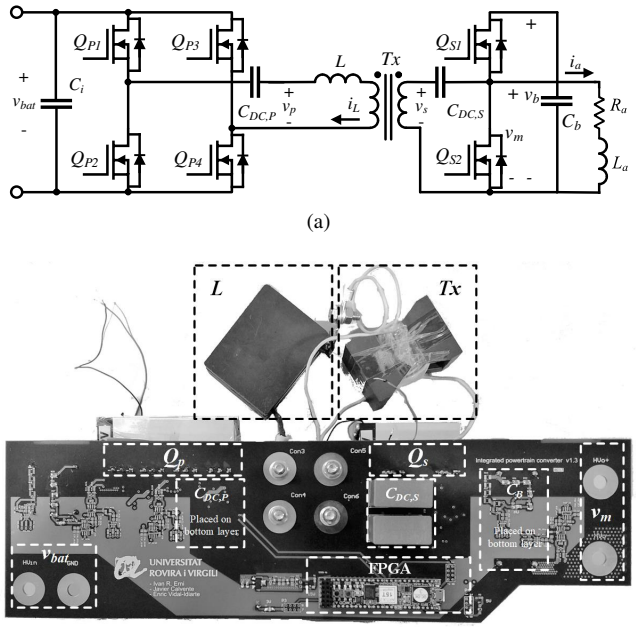


(a) (b) (c)

Fig. 9. Inverter stage simulations. Solid lines: Phase motor currents: i_a, i_b and i_c (a) $w_{m,ref} = 200$ rad/s. At 0.015 s, T_m is increased by 25%. Dashed line: ω_m. (b) Minimum battery voltage to provide maximum output voltage: $v_{bat} = 290$ V, $v_b = 800$ V. (c) Maximum battery voltage to provide minimum output voltage: $v_{bat} = 420$ V, $v_b = 200$ V.

the beginning, the motor currents increase until the reference is reached. Then, a perturbation is introduced at 0.015 s, the mechanical torque grows from 37.5 Nm to the rated value, 50 Nm. Thus, the speed control increments the amplitude values of the phase currents to maintain the speed reference. Fig. 9b shows the phase currents flowing through the motor and the converter under the maximum bus voltage gain: $v_{b,max}$ and $v_{bat,min}$. In the opposite way, Fig. 9c shows the motor phase currents with the maximum bus voltage reduction: $v_{b,min}$ and $v_{bat,max}$.

Two experimental prototypes have been built. The aim of the first one is to validate the feasibility of the converter itself: high-voltage operation and step up and down DC voltage capabilities while the secondary side transistors are also able to generate a DC square waveform with a peak voltage value of v_b and a constant output current i_a, like a common inverter. To do that, one phase of the converter using the parameters of Table I is connected to an inductive load, L_a, of 700 μH. The schematic and hardware implementation of the experimental set are represented in Fig.10. Converter prototype was implemented according to the design procedure in previous section with the parameters described in TABLE I. Digital PI control strategy using a FPGA was implemented. Bus voltage v_b is measured and compared with desired bus voltage v_{ref}. The control signal ϕ is used to regulate v_b. Fig.11 shows main waveforms at $P_o = 3300$ W. Input battery voltage v_{bat} is placed at 400 V and bus voltage v_b is set at 800 V. It can be demonstrated that output motor phase current is decoupled from the primary side current i_L and that high voltage elevation ratio is achieved. Fig. 12 corroborates that ZVS condition is maintained in the step up and down part for critical operating points: low load, low battery and extreme duty cycle values. Efficiency measurements are done using Yokogawa WT3000 power analyser. Measured and calculated efficiency values are plotted in Fig. 13, where a peak frequency of 97.6% is achieved at nominal output power and v_{bat}=350 V. The estimated distribution losses in this operating point are represented in Fig. 14. The prototype of Fig. 10 is reconfigured to be equivalent to a phase of Fig. 1, obtaining the schematic of Fig.15. In this way, the same semiconductors and the same volume are used. It is important to note that the transformer disappears, but the inductor required by the boost stage is



(a)

(b)

Fig. 10. 3.3 kW experimental set. (a) Proposed solution schematic. (b) Experimental.

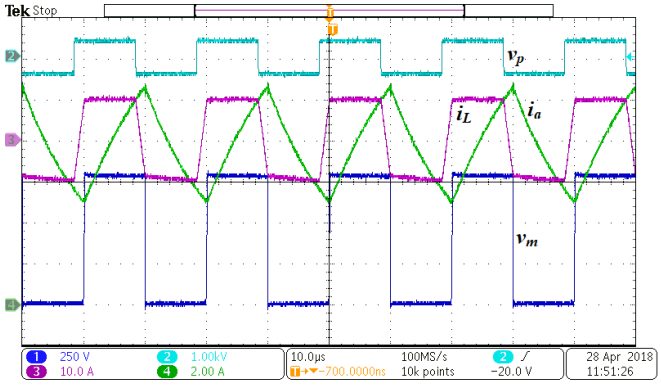


Fig. 11. Measured converter main waveforms supplying 3300 W to the load, d=0.5, v_{bat}=400 V, v_b=800 V. Primary side voltage v_p (1 kV/div), inductor current i_L (10 A/div), inverter output voltage v_m (250 V/div), current flowing to the inductive load i_a (5 A/div).

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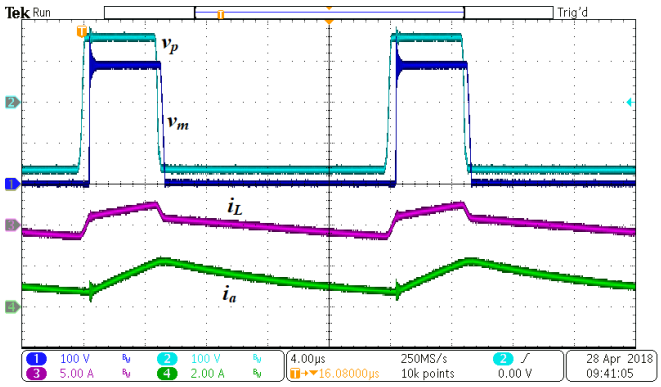

Fig. 12. Measured converter main waveforms supplying 300 W to the load, d=0.2, v_{bat}=150V, v_b=300V. Primary side voltage v_p (100 V/div), inverter output voltage v_m (100 V/div), inductor current i_L (5 A/div), current flowing to the inductive load i_a (2 A/div).

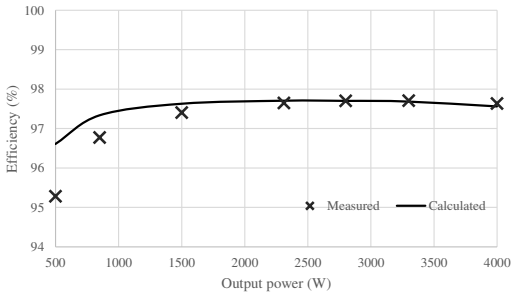

Fig. 13. Calculated versus measured efficiency results of the proposed converter.

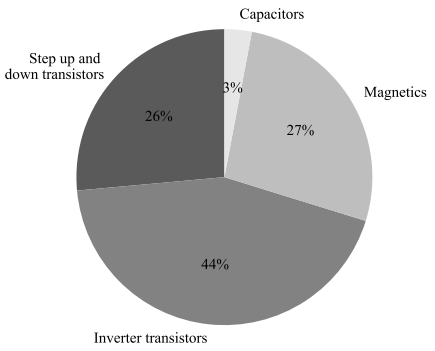

Fig. 14. Estimated distribution losses.

of much higher value, 280 μH, so the size of the resulting magnetic components is similar. In the boost topology of the conventional solution, several transistors are usually placed in parallel in order to handle the current levels. Therefore, the system is implemented with 2 transistors in parallel.

Comparing both solutions at several bus voltages, 3300 W and v_{bat}=350 V, the obtained efficiency results are shown in Fig.16. It can be seen that at higher voltages the efficiency of the proposed converter results higher where maximum efficiency point occurs at $v_b = 2Nv_{bat}$. The rapid efficiency

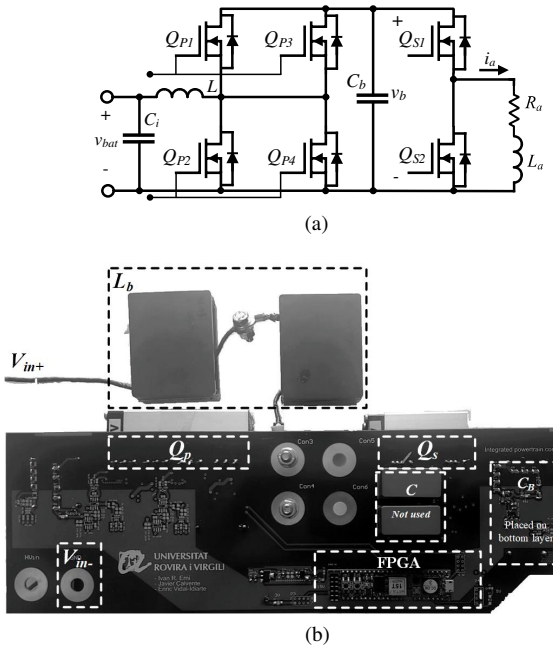

Fig. 15. 3.3 kW boost based conventional solution. (a) Schematic. (b) Experimental.

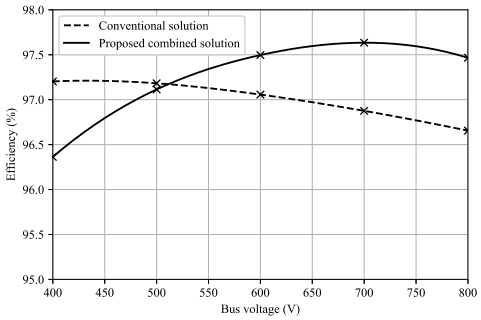

Fig. 16. Comparison of efficiencies between the conventional solution and the combined stage at 3300 W and v_{bat}=350 V.

drop of the proposed converter at low voltages is due to the loss of ZVS, since the design of previous section is intended to maintain ZVS up to 550 V. Below 550 V, where lower power is required by the PMSM, it is recommended to change the operating mode to half-bridge, which varies the new point of maximum efficiency. Fig.16 shows how for lower power and lower bus voltages, the proposed half-bridge stage is again more efficient than the conventional solution. In addition, the proposed converter allows to step down v_b with regards to v_{bat}.

A second prototype has been built to validate the performance of the whole system presented in this paper, merging the motor inverter and a step up and down stage into a single converter to operate a PMSM. This low power system, depicted in Fig. 18 with the parameters of TABLE III, is based on Fig. 3, placing one step up and down stage at each inverter leg and using half bridge configuration. The PMSM described in TABLE IV is connected as load. The semiconductors used in the step up and down stage, operating in ZVS, and in the

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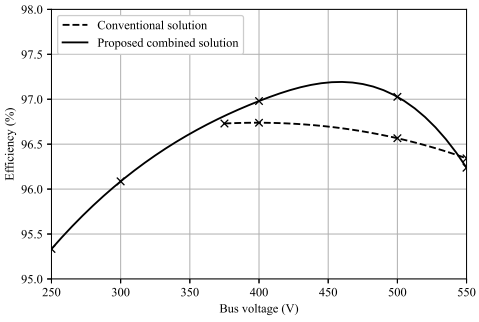

Fig. 17. Comparison of efficiencies between the conventional solution and the combined stage at 1150 W and v_{bat}=350 V.

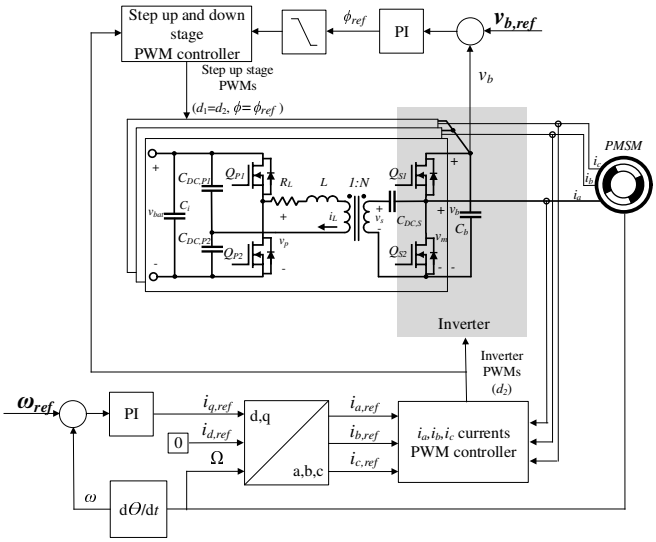

Fig. 18. Full system experimental set with PMSM as load and Phase Shift DC bus control.

inverter are the same: STP11N60DM2. A field oriented control (FOC) to regulate the motor speed and a bus voltage control is implemented in a TMS320F280049C C2000 DSP. The FOC inverter modulation provides with the inverter duty cycle. The step up and down part uses the same duty cycle as the inverter and employs the phase shift ϕ signal to regulate the bus voltage v_b. Magnetic components are made of N87 ferrite. Fig. 19 shows the experimental results of the converter operating with v_b at 200 V and v_{bat} at 100 V. After a torque perturbation of 33 %, the system recovers the steady state without stationary error. In that point, the PMSM is absorbing 300 W at 1000 rpm. Looking in more detail one phase at the operation point shown in Fig. 19, Fig. 20 and Fig. 21 are obtained. In Fig. 20, phase current is negative, close to its minimum peak value, which corresponds to duty cycles lower than 0.5. In contrast, in Fig. 21 the current flows to the motor, close to its maximum peak value, which implies duty cycles greater than 0.5.

The experimental results validates the feasibility of the converter to perform both tasks with a single stage converter: Generate the low frequency AC currents to drive a PMSM and regulate the bus voltage.

TABLE III
LOW POWER SYSTEM DESIGN PARAMETERS

Parameter	Value
Battery voltage, V_{bat}	100 V
Motor bus voltage range, V_b	200 V
Maximum phase output power, $P_{o,max}$	300 W
Turns ratio, N	2
Inductor, L	45 μH
Primary side blocking capacitor $C_{DC,P}$	4.4 μF
Secondary side blocking capacitor $C_{DC,S}$	2.2 μF
Switching frequency, f_{sw}	60 kHz
SPWM amplitude modulation index, M	0.6

TABLE IV
LOW POWER PMSM SPECIFICATIONS

Parameter	Value
Pole pairs	4
Rated torque, $T_{m,nom}$	1.27 Nm
Rated speed, $w_{m,nom}$	100 rad/s
Rated power, $P_{m,nom}$	300 W
Armature inductance, L_m	1 mH
Stator resistance, R_m	2.25 Ω
Torque constant, K_T	0.564 Nm/A

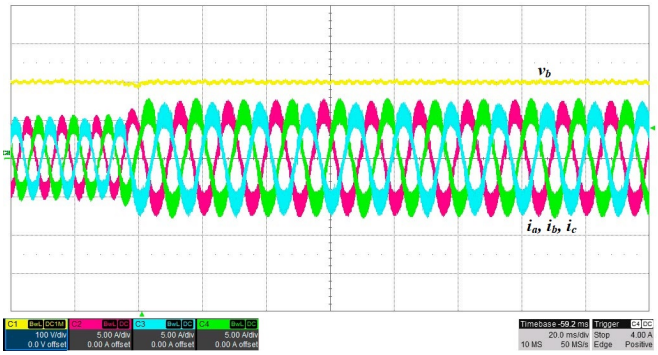

Fig. 19. Measured converter main waveforms when the PMSM, after a torque perturbation of 33 %, operates at 1000 rpm, absorbs 300 W and v_{bat}=100 V. Bus voltage v_b (100 V/div) and the phase currents flowing to the motor: i_a, i_b and i_c (5 A/div).

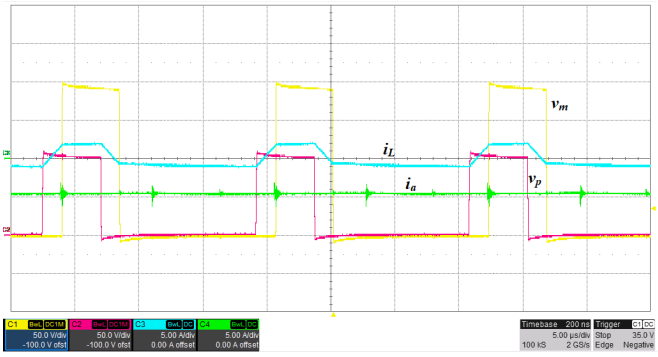

Fig. 20. Measured converter phase waveforms when PMSM phase current is negative and v_{bat}=100 V. Inverter output voltage v_m (50 V/div), inductor current i_L (5 A/div), primary side voltage v_p (50 V/div), current flowing to the PMSM i_a (5 A/div).

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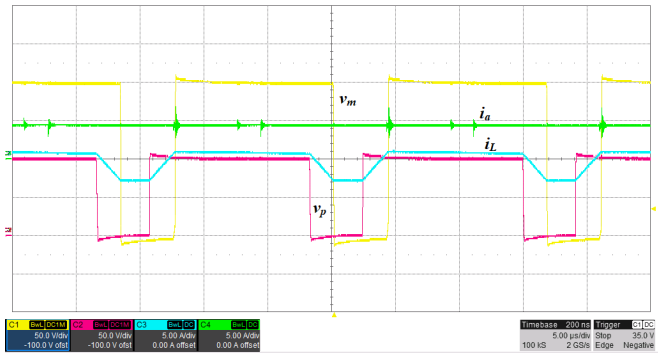

Fig. 21. Measured converter phase waveforms when PMSM phase current is positive and v_{bat}=100 V. Inverter output voltage v_m (50 V/div), inductor current i_L (5 A/div), primary side voltage v_p (50 V/div), current flowing to the PMSM i_a (5 A/div).

VI. Conclusions

Wide range step up and down converter and motor inverter are integrated into one single topology for electrical vehicle powertrain system. Analytical waveforms and loss model are developed. Based on this analysis, converter design procedure to meet main automotive requirements is proposed. From common high voltage automotive battery values, entire inverter voltage operating range is covered. ZVS is maintained in the step up and down stage. Moreover, since part of current generated at primary side flows directly to motor, inverter transistors RMS current results lower than in typical used solutions. Simulated results and experimental results with two prototypes are used to validate the converter proof of concept. As conclusion, a compact solution that merges the inverter and the step up and down stage with less components, and wide voltage range is achieved for electrical vehicles powertrain system.

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