Effects of Thermal Annealing on the Density of States in Low Voltage Operating Range, High Mobility, Hf-In-ZnO/HfO_2 TFTs Fabricated at Temperatures Below 200 °C

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***Abstract*— In this paper, we report the effects of thermal annealing on Poly(methyl methacrylate) (PMMA) passivated, bottom gate thin film transistors, with amorphous hafnium oxide (HfO_2) as gate dielectric and amorphous hafnium-indium-zinc oxide (a-HIZO) as semiconductor, fabricated at temperatures below 200 °C. It is shown that TFTs, with V_{TH} =0.55 V, μ_{FE}>250 cm^2/Vs, *SS*=200 mV/dec corresponding to D_{it}= $1x10^{12}$ $cm^{-2}eV^{-1}$ and $I_{on}/I_{off}>10^7$, can be obtained, using a thermal annealing at 200 °C in N_2, after the semiconductor layer is deposited. The dielectric constant of the HfO_2 layer deposited by RF sputtering was 19.5, allowing devices to work within the operating voltage range of 2 V. An important increase of the field effect mobility is obtained, combining a high-k gate dielectric and a high carrier concentration a-HIZO layer, with a lower density of localized states.**

***Index Terms*—Low temperature AOSTFT process, passivated a-HIZO TFTs, HfO_2 gate dielectric, density of states, interface trap density.**

I. Introduction

Amorphous oxide semiconductor thin film transistors (AOSTFTs) exhibit several important device characteristics that distinguish them from other amorphous TFTs, as hydrogeneted amorphous silicon (a-Si:H) or organic TFTs. The conduction mechanisms are different, allowing high values of field effect mobility (μ_{FET}). Their optical transparency in the visible-light range is above 80 % and their stability under bias and light stress is acceptable for many applications. Their processing temperature is below 450 °C, with lower fabrication costs [1]-[3]. At present, these devices are widely used in active-matrix organic light emitting diode (AMOLED) displays [4]-[6], while other digital and analog applications are appearing [7], [8].

Many amorphous metal oxide semiconductors (AMOS) have been studied as the active layer of AOSTFTs, [1], [9]-[12], but the most commonly used one is the amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) [3,9]. Among other AMOS, amorphous Hafnium-Indium-Zinc-Oxide (a-HIZO) provides more stable devices under bias and light stress compared to a-IGZO, due to a more stable binding of hafnium ions with oxygen, compared to gallium ones, [10]-[12].

Despite the significant performance already obtained for AOSTFTs, efforts to further improve their performance have been focused on increasing mobility [13]-[16], as well as on reducing the voltage operating range, among other aspects.

The reduction of the operating voltage range is obtained by using high-k insulators [13]. Mobility values above 60 cm^2/Vs have been reported for a-IGZO TFTs with hafnium oxide (HfO_2) as dielectric layer, operating in the voltage range up to 2 V [14]. Using a-IZO as the semiconductor layer, mobility values above 116 cm^2/Vs have been reported, even when the gate dielectric was sillicon oxide (SiO_x) [15]. In [16], authors reported mobility values above 300 cm^2/Vs, after a meticuluous selection of the materials and processing conditions.

Another effort to improve device characteristics involves the study of thermal annealing (TA) conditions, since the density of localized states (DOS) in the oxide semiconductor layer and the characteristics of the dielectric/semiconductor interface are sensitive to the annealing temperature and the atmosphere. The effects of the TA also depend on the device structure and materials used [17]-[22].

Thermal annealing processes of a-IGZO TFTs are usually carried out at temperatures ≤300 °C to guarantee the required reduction of the density of localized states at the dielectric/semiconductor interface, as well as in the gap of the semiconductor layer (DOS) [17]-[20]. In [19], the combined effect of plasma and thermal annealing was analized. However, not all flexible substrates can suport these temperatures without damage [18]. For this reason, the study of the effects of annealing at temperatures ≤200 °C is important.

In this paper, we analyze the effects of thermal annealing at 150 °C and 200 °C, performed at different moments of the fabrication process, on the gap density of states (DOS), on the interface trap density, as well as on device performance of the analyzed devices. Devices were bottom gate, passivated, thin film transistors, using amorphous HfO_2 as gate dielectric, a-HIZO as semiconductor and molybdenum (Mo) as gate (G), drain (D) and source (S) contacts. The a-HIZO, HfO_2 and Mo layers were deposited by magnetron sputtering at room temperature (RT). Poly(methyl methacrylate) (PMMA) was used as etch stop and passivation layer (ESL), and deposited by spin coating. The effects of using N_2 or O_2 ambient are also investigated. As far as we know, there are no previous studies on the effects of TA below 200 °C, for magnetron sputtered HfO_2/a-HIZO TFTs.

Limiting the processing temperature is important also for our fabrication process, since the PMMA layer used as ESL, starts to degrade at temperatures above 150 °C.

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II. Experimental Details

The basic fabrication process of the analized AOSTFTs included the following steps: 1) A 150 nm thick (Mo) layer was deposited on glass substrate and patterned to define the gate contact; 2) Deposition of 150 nm of HfO_2 as gate dielectric, by RF magnetron sputtering at RT, using a HfO_2 target (purity 99.999%) at argon (Ar) pressure of 20 mTorr; 3) Deposition of a 36 nm thick a-HIZO layer by RF magnetron sputtering, using a HfO_2:In_2O_3:ZnO target with 99.999% purity and composition of 0.3:1:1 mol%; 4) Photolitography and wet etching of the a-HIZO layer followed by another photolitography and etching to open vias through the gate dielectric, using reactive ion etching (RIE) with a tetrafluoromethane plasma; 5) Deposition of 400 nm of PMMA followed by a photolithographic process and etching in oxygen plasma to open Source/Drain (S/D) vias through the ESL; 6) Deposition of a 250 nm thick Mo layer followed by a photolithographic process and etching, to define S and D contacts and top connection to bottom G contact. The analysis of a similar structure without thermal annealing was reported in [23]. Prior to each deposition process, the vacuum chamber was evacuated to a base pressure lower than $2x10^{-5}$ Torr. The cross section of the device structure is shown in Fig.1.

The analized thermal annealing processes were:

1) Final thermal annealing (FTA) at 150 °C in N_2 for 20 min;
2) Thermal annealing TA1 at 200 °C for 20 min, after depositing the HfO_2 layer;
3) Thermal annealing TA2 at 200 °C for 20 min, after depositing the a-HIZO semiconductor layer.

To analyze the effects of the annealing gas, TA1 and TA2 were done either in nitrogen (N_2) or in oxygen (O_2) atmosphere.

Fabricated devices included Thin Film Transistors (TFTs), as well as Metal-Insulator-Metal (MIM) and Metal-Insulator Semiconductor (MIS) capacitors. MIM and MIS structures were used to obtain the relative dielectric constant of the gate insulator (*ki*) and the carrier concentration (N_D) of the a-HIZO from capacitance-voltage (C-V) measurements:

$$N_D = \frac{2q \cdot \varepsilon_0}{SL \cdot A^2 \cdot k_s}, \tag{1}$$

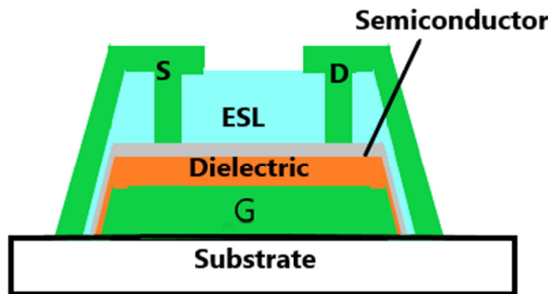


Fig.1 Cross-section of the TFT structure.

where *SL* is the slope of the curve $\frac{d\left(\frac{1}{C}\right)^2}{dV_{GS}}$, *A* is the area of the capacitor, k_s is the relative dielectric constant of the semiconductor layer and ε_o is the dielectric constant of vaccum.

The lateral size of MIM and MIS square capacitors ranged from 100 to 300 µm per side.

The channel width (W) of the TFTs was 150 µm and the channel length (L) was varied from 20 to 60 µm.

The drain current I_{DS} in the above threshold linear regime, can be expressed as:

$$I_{DS} = \frac{\frac{W}{L} C_i \mu_{FE} (V_{GS} - V_{TH}) V_{DS}}{1 + \frac{W}{L} C_i \, \mu_{FE} \, R_s (V_{GS} - V_{TH})}, \tag{2}$$

where R_s is the series resistance, C_i is gate dielectric capacitance per unit area, V_{TH} is the threshold voltage and μ_{FE} is the field effect mobility. Finally, V_{GS} and V_{DS} are the voltages from sorce to gate and drain, respectively.

The values of V_{TH} and μ_{FE} for MOSFETs can be extracted using different methodolgies e.g., from the MOSFET conductance $g_d = \frac{I_{DS}}{V_{DS}}$ using the expression:

$$\mu_{FE} = \frac{g_d}{\frac{W}{L} C_i \, (V_{GS} - V_{TH})} \tag{3}$$

In this work, the values of V_{TH} and μ_{FE} were extracted using the procedure of the Universal Model and Extraction Method (UMEM). The expression for the dependence of μ_{FE} with V_{GS}, specific for amorphous TFTs, is [24]:

$$\mu_{FE} = \mu_1 (V_{GS} - V_{TH})^{\gamma_a}, \tag{4}$$

where μ_1 is the value of mobility when $(V_{GS} - V_{TH}) = 1$ and γ_a is the mobility parameter.

The on resistance (R_{on}) was obtained from the output characteristic for V_{GS}=2 V.

In the subthreshold region of operation, two parameters were extracted, *SS* and D_{it}. The subthreshold slope (*SS*) is determined in the deep subthehold region of the semilog plot of the linear transfer characteristic.

The interface trap density (D_{it}), at the interface between the gate dielectric and the HIZO layer, was determined using the expresion:

$$D_{it} = \left(\frac{SS}{2.3 \frac{k_B T}{q}} - 1 \right) \frac{C_i}{q}, \tag{5}$$

where k_B, q and T are the Boltzmann's constant, electron charge and absolute temperature, respectively.

Capacitance-voltage characteristics of MIM and MIS capacitors were measured with the LCR meter model 4980A, from Agilent. The current-voltage (I-V) curves of the devices were obtained, using a Keithley measurement system. C-V and I-V measurements were done in dark and environmental conditions, inside a shielded box. The thickness of all layers were measured by L2W16S633.830 ellipsometer from Gaerthner Scientific Corporation.

III. Results and discussion

Fig. 2 shows the X-ray diffraction patterns of RF sputtered HfO2 and a-HIZO layers. This confirms that both materials are amorphous because these do not produce sharp diffraction peaks.

Fig. 3 shows the output characteristics and Fig. 4 the linear transfer characteristics of devices with different TA processes. The efffects of these TA processes on device electrical parameters V_{TH}, μ_{FE}, SS, D_{it}, on and off currents ratio (I_{on}/I_{off}), N_D and R_{on} are shown in Table 1, as well as the value of k_i parameter.

First, as seen in Fig. 3 a, b and c, the voltage operating range reduces up to 2 V, as was expected by using a high-k gate dielectric.

The value of V_{TH} was 0.5 V for devices with TA2 or FTA. The value of μ_{FE} increases for all thermally annealed devices regarding to non-annealed, with the maximum values observed after TA2 in N_2. The smallest value of R_{on} was obtained after TA2 in N_2, since the conductivity of the semiconductor layer increased, (see N_D value in Table I) and the density of localized states was the smallest, see Table II.

Table I also shows that the value of the relative dielectric constant of the HfO_2 increased from 14.5 to 19.5, while the value of N_D also experimented a slight increase. It is important to remark that the value of *ki* increased in all devices annealed at 200 °C, except when the TA was done in O_2 before depositing the HIZO layer.

Values of *ki* around 15 for non-annealed devices have been reported, and it varies accordinig to different deposition methods [25]. This also depends on measurement frequency [26]. The increase of *ki* after TA, has been previously observed, and it is related to the reduction of structural and chemical defects in the bulk of the HfO_2 [27]. In [14], a similar value of *ki*=19 for a HfO_2 has also been reported.

We observed an exception in the behavior of k_i after TA1 in O_2. which can be explained by the formation of a thin interfacial layer between the HfO_2 and the HIZO layers. This can occur, because the oxygen atoms that remain adsorbed on the HfO_2 layer, after TA1 in O_2, can interact with the a-HIZO layer at the beginning of its deposition, forming an interfacial layer that does not contribute to improve the HfO_2 quality, therefore, the *ki* value does not increase.

In Table 1, it is also shown that SS, D_{it}, and V_{TH} values practically were the same for devices after FTA and after TA2 in N_2, indicating that a reduction of the localized interface states is already achieved at 150 °C. For non-annealed devices, D_{it} is higher, which is consistent with a smaller value of V_{TH} produced by an increase of negatively charged interface traps. For devices with TA2 in O_2, again D_{it} increase, and V_{TH} is smaller. The I_{on}/I_{off} currents ratio increased after TA2 at 200 °C, but it is high enough, even after FTA at 150 °C.

After different TA processes, the mobility behavior can be explained by considering the behavior of several parame-

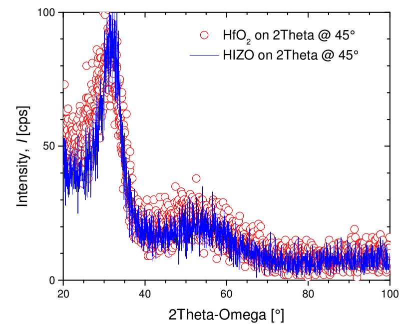
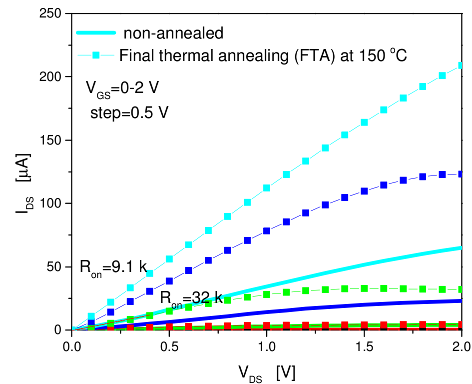
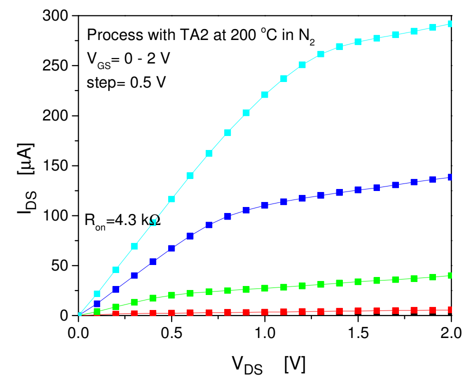


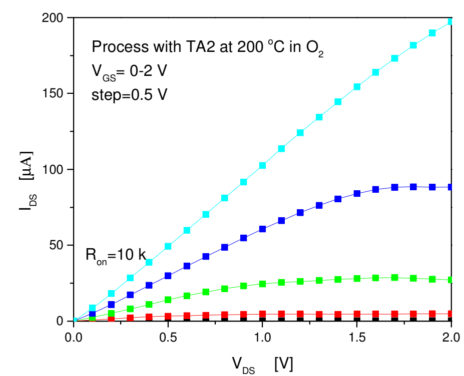
Fig. 2 X-ray diffractogram for deposited HfO_2 and HIZO layers.



(a)



(b)



(c)

Fig. 3 I_{DS}-V_{DS} output characteristics of devices with L=30 and W=150 a) non annealed and with FTA in N_2 at 150 °C; b) with TA2 in N_2 at 200 °C, after depositing the HIZO layer; c) with TA2 in O_2 at 200 °C, after depositing the HIZO layer.

Table I. Main electrical parameters for the different thermal annealing.

Annealing process	ki	V_{TH} [V]	μ_{FE} [cm^2/Vs]	SS [mV/dec]	D_{it} [$cm^{-2}eV^{-1}$]	I_{on}/I_{off}	N_D [cm^{-3}]	R_{on} [kΩ]
Non annealed	14.5	0.33	66	440	$3x10^{12}$	$9x10^6$	$1.2x10^{17}$	32.2
FTA, 150 °C, N_2	14.5	0.5	180	200	$1.7x10^{12}$	$1.5x10^7$	$1.2x10^{17}$	9.1
TA2, 200 °C, N_2	19.5	0.54	279	200	$1x10^{12}$	$3x10^7$	$8.5x10^{17}$	4.3
TA2, 200 °C, O_2	19.5	0.34	134	200	$2.7x10^{12}$	$3x10^5$	$8.5x10^{17}$	18.8

Table II. Calculated parameters for DOS in the semiconductor layer.

TA process	g_{ato} [$cm^{-3}eV^{-1}$]	T_T [K]	Ea [meV]
Non annealed	$2.8x10^{19}$	729	63
FTA, 150 ^oC, N_2	$0.9\ x10^{19}$	394	34
TA2, 200 ^oC, N_2	$0.3\ x10^{19}$	396	34
TA2, 200 ^oC, O_2	$3.2x10^{19}$	675	58

ters shown in Tables I and II. For non-annealed devices, μ_{FE} showed a similar value as that reported in [14] for non-annealed TFTs, using HfO_2 as gate dielectric and IGZO as semiconductor.

After FTA, μ_{FE} increased around 3 times in our fabricated devices. However, comparing the μ_{FE} of TFTs with FTA at 150 °C and those with TA2 at 200 °C in N_2, for the last ones the μ_{FE} still significantly increased. Additionally, the difference between Fig. 3a and 3b indicates that temperature increase in the TA process yields an important effect on this characteristic parameter.

It is well documented that μ_{FE} in AOSTFTs depends on the relative dielectric constant of the gate dielectric, on the density of interface traps, on the carrier concentration of the AMOS, on the series resistance at the D and S contacts, and on the of density of states distributed in the semiconductor gap (DOS) [13]-[16].

Table II shows the three main parameters of this DOS, which are: the value of the localized acceptor trap density at the conduction band energy (g_{ato}), the characteristic temperature of the tail localized states (T_T) and their characteristic energy (E_a), considering a semi-logarithmic dependence with energy of the DOS [29,30].

As shown in Tables I and II, the values of k_i and N_D are the same for non-annealed and after FTA at 150°C devices. However, an important reduction of (g_{ato}) and T_T parameters is observed, which can be the cause of μ_{FE} increase.

After TA2 in N_2, ki and N_D increased. The increase of charge concentration in a-HIZO layers, deposited by RF sputtering and after a TA process, has been reported previously and it can be attributed to the formation of oxygen vacancies that contribute to the carrier conduction in these materials, which occurs at temperatures above 200 ^oC [10].

At the same time, g_{ato} and T_T further reduced and the characteristic temperature T_T or E_a energy also significantly reduced. After TA2 at 200 ^oC, the values of g_{ato} and T_T are below 10^{19} $cm^{-3}eV^{-1}$ and 400 K, respectively, which are lower than those typicaly reported for IGZO TFTs [30]. Moreover, the increase observed in the μ_{FE} of our devices, with respect to devices with FTA, is consistent with the combined effect of these factors.

It is worth to mention, that the drain current of amorphous TFTs can decrease with temperature, when g_{ato} and T_T become less than $6x10^{18}$ $cm^{-3}eV^{-1}$ and 400 K, respectively, [31]. We called this effect a crytalline-like behavior, and it is possible because the conduction mechanisms in AOSTFTs can be multiple trapping, percolation, or even conduction in extended states [32]. If conditions are appropriated for this later to became predominant, the amorphous TFT can show what we call a crystalline-like behavior, which produces an important increase in μ_{FE}.

For devices annealed with TA2 in O_2, the value of g_{ato} is in the same order as for a-HIZO layers non-anealed, while T_T is slightly smaller, so the effect of the DOS, should be similar to that for non-annealed devices. However, R_{on} is smaller than for non-annealed devices, although higher than when TA is done in N_2, probably due to the presence of adsorbed oxygen at the surface of the a-HIZO layer before the metal deposition of D and S. The combination of these effects produces mobility values higher than the μ_{FE} of non-annealed devices, but still smaller than those obtained with other TA, as shown in Table I.

It is worth to remark that, R_{on} is related to the total resistance of the device, which includes channel and series resistance. In our devices, we used the transmission-line method (TLM), to determine their channel and series resistance [28]. First, it was confirmed that the series resistance (R_S) was lesser than the channel resistance (R_{ch}) for all channel lengths. For a device with TA2 in N_2, R_S=689 Ω and the R_{ch} was around 4 kΩ, for V_{GS}=2 V, obtaining a total resistance of 4.7 kΩ, which is consistent with the R_{on} value of 4.3 kΩ for the same V_{GS}=2 V, shown in Table I.

In summary, the important increase obtained for the field effect mobility becomes possible by combining a high-k dielectric, a relatively high carrier concentration in the amorphous semiconductor, a low series resistance at the metal contacts and a low interface trap density, as well as a very low density of localized states with low characteristic energy in the a-HIZO layer. These whole conditions allow that carrier conduction at the conduction band becomes predominant (a cristalline-like behavior), which can be obtained even in fabrication processes, where temperature is below 200 ^oC.

Finally, as can be seen in Fig. 4, the semilog plot of the linear transfer characteristic is shown for devices being measured with a V_{GS} swept from −2 V to +2 V, and viceversa. The values of SS and D_{it} in Table I correspond to the experimental curves swept from −2 to 2 V. It is seen that, the annealing at 150 °C or 200 ^oC produces a similar effect on linear transfer characteristic. The observed hysteresis loop is around 1.1 V and the shift of the curve is toward more negative values of V_{GS}, which indicates that in-

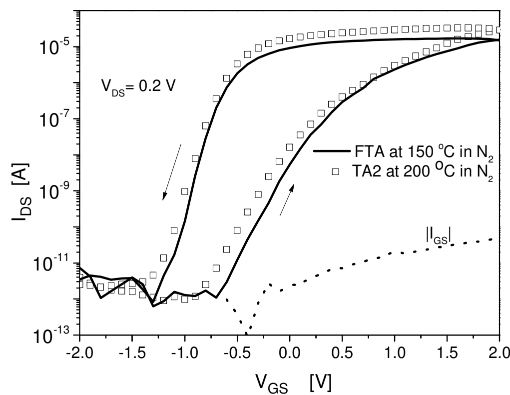


Fig. 4 Linear transfer characteristics and gate current for devices with FTA at 150°C in N_2 and TA2 at 200 °C in N_2.

terface traps are charged negatively, when a positive bias is applied. Moreover, the curve shift is not strictly parallel, when seeping in both votage direction. In non-annealed devices, D_{it} and *SS* were the highest, but the observed IV curve shift practically was parallel, as we reported in [23]. The reduction of *SS* after positive bias stress in devices with FTA or TA2, can be due to the polarizability of the high-k dielectric, since, as the dielectric constant of materials is higher, their polarizability is also higher. In this last case, when a positive gate voltage is applied, the orientation of the dipoles can reduce the effect of the interface charge, which depends on the applied gate voltage.

IV. Conclusions

In this work, we investigated the influence on the density of states and on the device characteristics, of thermal annealing at 150 °C, in N_2, and at 200 °C in N_2 or O_2, at different stages of the AOSTFTs fabrication proces, using HfO_2 as dielectric and amorphous HIZO as semiconductor. It was shown, that PMMA passivated, bottom gate HfO_2/a-HIZO TFTs, can be obtained with V_{TH}=0.55 V, μ_{FE}>250 cm^2/Vs, *SS*=200 mV/dec corresponding to D_{it}=1x10^{12} $cm^{-2}eV^{-1}$ and I_{on}/I_{off} >10^7, using a thermal annealing in N_2 with a temperature as low as 200 °C, after the semiconductor layer deposition. The dielectric constant of the HfO_2 layer deposited by RF sputtering was 19.5, allowing TFTs operate within the voltage range of 2 V. At the same time, a low density of localized states in the a-HIZO layer, in the order of 3x10^{18} $cm^{-3}eV^{-1}$ was obtained, with a low characteristic energy of 34 meV, allowing carrier conduction in the conduction band to become the predominant conduction mechanism. An important increase of the field effect mobility was obtained by combining a high-k dielectric, a relatively high carrier concentration in the amorphous semiconductor, a low series resistance at the metal contacts and a low interface trap density, as well as, a low density of localized states with low characteristic energy in the a-HIZO layer. Results suggest the potential use of these devices in high performance/low voltage applications.

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References

[1] S.Y. Lee, Comprehensive Review on Amorphous Oxide Semiconductor Thin Film Transistor, Trans. Electr. Electron. Mater. 21, (2020) 235–248. doi.org/10.1007/s42341-020-00197-w

[2] J.E. Medvedeva, D.B. Buchholz, R.P.H. Chang, Recent Advances in Understanding the Structure and Properties of Amorphous Oxide Semiconductors, Adv. Electron. Mater. 3 (2017) 1700082. doi.org/10.1002/aelm.201700082

[3] T. Kamiya, K. Nomura, H. Hosono, Present status of amorphous In-Ga-Zn-O thin film transistors, Sci. Technol. Adv. Mater. 11 (2010) 044305, doi.org/10.1088/1468-6996/11/4/044305

[4] G.M. Wan, S.M. Ge, C. Gong, S. Li, X.N. Lin, A stable FHD display device based on BCE IGZO TFTs. IOP Conf. Ser. Mater. Sci. and Eng. 729 (2020) 012099. doi.org/10.1088/1757-899X/729/1/012099

[5] A. Sodhani, K. Kandpal, Design of threshold voltage insensitive pixel driver circuitry using a-IGZO TFT for AMOLED displays. Microelectronics J.101 (2020) 104819. doi.org/10.1016/j.mejo.2020.104819

[6] J-H. Kim, J. Oh, Y-S Kim, Y-S, K. Park, IGZO TFT gate driver circuit with large threshold voltage margin, Displays 53 (2018) 1-7. doi.org/10.1016/j.displa.2018.03.003

[7] Y. He, S. Nie, R. Liu, Y. Shi and Q. Wan, Indium–Gallium–Zinc–Oxide Schottky Synaptic Transistors for Silent Synapse Conversion Emulation. IEEE Electron Device Letters, 40:1 (2019) 139-142 doi.org/10.1109/LED.2018.2883442.

[8] C. Garripoli, J-L.P.J Van der Steen, F. Torricelli, M. Ghittorelli, G.H. Gelinck, A.H.M. Van Roermun, E. Cantatore, Analogue Frontend Amplifiers for Bio-Potential Measurements Manufactured With a-IGZO TFTs on Flexible Substrate. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 7:1 (2017) 60-70. doi.org/10.1109/JETCAS.2016.2616723.

[9] R.Z. Wang, S.L. Wu, X.Y. Li, J.T. Zhang, The electrical performance and gate bias stability of an amorphous InGaZnO thin-film transistor with HfO2 high-k dielectrics. Solid State Electron, 133 (2017) 6-9. doi.org/10.1016/j.sse.2017.04.004.

[10] C-J. Kim, S. Kim, J-H Lee, J-S. Park, S. Kim, J. Park, E. Lee, J. Lee, Y. Park, J-H. Kim, S.T. Shin, U-In Chung, Amorphous hafnium-indium-zinc oxide semiconductor thin film transistors, Appl. Phys. Lett. 95 (2009) 252103. doi.org/10.1063/1.3275801

[11] E. Chong, Y.S. Chun, S.H. Kim, S.Y. Lee, Improvement of bias stability of indium zinc oxide thin film transistors by the incorporation of hafnium fabricated by radio-frequency magnetron sputtering, Thin Solid Films 519 (2011) 519:6881. doi.org/10.1016/j.tsf.2011.04.044.

[12] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, U-I. Chung, J-H. Lee, Instability in threshold voltage and subthreshold behavior in Hf–In–Zn–O thin film transistors induced by bias-and light-stress, Appl. Phys. Lett. 97 (2010) 113504. doi.org/10.1063/1.3480547

[13] J.Y. Choi, S.Y. Lee, Comprehensive Review on the development of High Mobility in oxide thin film transistors, J. Korean Physical Soc. 71:8 (2017) 516-527. doi.org/10.3938/jkps.71.516

[14] H-H. Hsu, C-Y. Chang, C-H. Cheng, P-C. Chen, Y-C. Chiu, P. Chiou, C-P. Cheng, High Mobility Field-Effect Thin Film Transistor Using Room-Temperature High- κ Gate Dielectrics, Journal of. Display Technology 10:10 (2014) 847-853. doi.org/10.1109/JDT.2014.2331351

[15] J.C. Park, C.J. Kim, U-I. Chung, S. Im, High performance self-aligned top-gate amorphous indium zinc oxide thin- film transistors, Twentieth International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD), Kyoto (2013) 247-250. https://ieeexplore.ieee.org/document/6617758

[16] C.W. Shih, A. Chin, Remarkably High Mobility Thin-Film Transistor on Flexible Substrate by Novel Passivation, Material. Sci. Rep. 7:1 (2017). doi.org/10.1038/s41598-017-01231-3

[17] K. Nomura, T. Kamiya, H. Hosono, Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects Appl. Phys. Lett. 99 (2011) 053505. 10.1063/1.3622121

[18] J. Song, X. Huang, C. Han, Y. Yu, Y. Su, P- Lai, Recent Developments of Flexible InGaZnO Thin-Film Transistors Physica Status Solidi (A) Applications and Materials Science, (2021), 218 (7), art. no. 2000527. DOI: 10.1002/pssa.202000527

[19] W-S. Liu, C-H. Hsu, Y. Jiang, Y-C. Lai, H-C. Kuo, Improvement of device characteristics of plasma-treated indium gallium zinc oxide thin-film transistors through thermal annealing, Semiconductor Science and Technology, (2021) 36 (4), art. no. 045007. DOI:10.1088/1361-6641/abe6da

[20] W-F. Chung, T-C. Chang, H-W. Li, S-C. Chen, Y-C. Chen, T-Y. Tseng, Ya H. Tai, Environment-dependent thermal instability of sol-gel derived amorphous indium-gallium-zinc-oxide thin film transistors App. Phys. Lett. 98, (2011) 152109. doi: 10.1063/1.3580614

[21] M. Li, L. Lan ⇑, M. Xu, H. Xu, D. Luo, P. Xiao, J. Peng, Performance improvement of oxide thin-film transistors with a two-step-annealing method, Solid-State Electronics 91 (2014) 9–12

[22] Z. Xu, M. Li, M. Xu, J. Zou, Z. Gao, J. Pang, Y. Guo, L. Zhou, C. Wang, D. Fu, J. Peng, L. Wang, Y. Cao, Flexible amorphous oxide thin-film transistors on polyimide substrate for AMOLED, Proc. of SPIE Vol. 9270 92700A-1 doi: 10.1117/12.2071794.

[23] C.A. Pons-Flores, I. Mejia, I. Hernandez, I. Garduño, M. Estrada, High performance low temperature processed Hf-In-Zn-O/HfO_2 thin film transistors using PMMA as etch-stop and passivation layer, Microelectronic Engineering; 205 (2019) 1-5. doi.org/10.1016/j.mee.2018.11.008

[24] A. Cerdeira, M. Estrada, R. García, A. Ortiz-Conde, F.J. García Sanchez, New Procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions, Solid State Electronics 45 (2001) 1077. doi.org/ 10.1016/s0038-1101(01)00143-5

[25] X. Zou, G. Fang, L. Yuan, X. Tong, X. Zhao, A comparative study of amorphous InGaZnO thin-film transistors with HfO*x*N*y* and HfO2 gate dielectrics, Semicond. Sci. Technol. 25 (2010) 055006. doi:10.1088/0268-1242/25/5/055006

[26] I. Hernandez, C.A. Pons-Flores, I. Garduño, J. Tinoco, I. Mejia, M. Estrada, Characterization of MIS structures and thin film transistors using RF-sputtered HfO_2/HIZO layers, (2017) Microelectronics Reliability, 75, pp. 9-13. doi:10.1016/j.microrel.2017.06.003

[27] R. Yao, Z. Zheng, M. Xiong, X. Zhang, X. Li, H. Ning, Z. Fang, W. Xie, X. Lu, J. Peng, Low-temperature fabrication of sputtered high-k HfO_2 gate dielectric for flexible a-IGZO thin film transistors, Appl. Phys. Lett. 112 (2018) 103503. doi.org/10.1063/1.5022088

[28] A. Cerdeira, M. Estrada, I. F. Marsal, J. Pallares, B. Iñiguez, On the series resistance in staggered amorphous thin film transistors, Microelectron. Rel., 63,325-335, (2016). dx.doi.org/10.1016/j.microrel.2016.05.005

[29] M. Shur, M. Hack, Physics of amorphous silicon based alloy field-effect-transistors, J. Appl Phys 55 (1984) 3831–42. doi.org/10.1063/1.332893

[30] Y. Hernandez-Barrios, A. Cerdeira, M. Estrada, B. Iñiguez, An insight to mobility parameters for AOSTFTs when the effect of both, localized and free carriers, must be considered to describe the device behavior, Solid State Electron 149 (2018) 32. doi.org/10.1016/j.sse.2018.08.006

[31] M. Estrada, Y. Hernandez-Barrios, A. Cerdeira, F. Ávila-Herrera, J. Tinoco, O. Moldovan, F. Lime, B. Iñiguez, Crystalline-like temperature dependence of the electrical characteristics in amorphous Indium-Gallium-Zinc-Oxide thin film transistors, Solid-State Electronics 135 (2017) 43–48.dx.doi.org/10.1016/j.sse.2017.06.030

[32] W. Chr. Germs, W. H. Adriaans, A. K. Tripathi, W. S. C. Roelofs, B. Cobb, R. A. J. Janssen, G. H. Gelinck, M. Kemerink, Charge transport in amorphous InGaZnO thin-film transistors, Physical Review B 86 (2012) 155319. doi.org/10.1103/PhysRevB.86.15531