Operation of the Low-Capacitance Cascaded H-Bridge StatCom under Grid Voltage Swells

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***Abstract*—Grid voltage transients, and in particular grid voltage swells, pose control challenges for static compensators (StatComs). This paper presents an efficient control strategy for changing the dc value of capacitor voltages, that is especially useful for operating a low-capacitance StatCom (LC-StatCom) under grid voltage swells. In the proposed strategy, the capacitor voltages are changed as a function of the grid voltage magnitude in each phase. The paper details all the required control stages for implementing this control strategy. Effectiveness of this strategy to deal with grid voltage swells is compared with other strategies both in conventional StatComs and LC-StatComs using a simulated 36-MVA 11-level cascaded H-bridge converter in MATLAB Simulink. The comparison is based on current transient performance and an analytical model of switching losses. Finally, feasibility of this strategy is confirmed by experiments on a 1-kVA prototype.**

I. Introduction

Installation of static compensators (StatComs) is growing rapidly all over the world, as a result of the transition towards renewables, increasing electricity demand, and improving technology.

The increasing rate of installation of StatComs is a driving force to further reduce converter size, cost, and losses, without compromising the performance. Transitioning from two-level voltage source converters to cascaded H-bridge (CHB) converters was a first stepping stone. However, large capacitors are still used in conventional CHB-StatComs to reduce the capacitor voltage oscillations induced by the second harmonic of power that comes from the ac-side [1]–[4]. On the other hand, low-capacitance StatCom (LC-StatCom) [5]–[9] uses smaller capacitors to absorb the same amount of oscillating power, which results in a nonnegligible oscillation in the capacitor voltages. Nonetheless, both conventional- and LC-StatComs must maintain a sufficiently large dc capacitor voltage to prevent overmodulation [10].

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In conventional StatComs, the capacitors are designed to handle overrated dc voltages, since the IEEE 1159 standard [11] requires the converters to operate safely when the grid voltage increases up to 180% of its nominal RMS value. However, continuously operating with higher capacitor voltages implies that the blocking voltage of the submodule (SM) switches is higher, which increases switching losses. Alternatively, having some redundant SMs that are in an idle state (bypassed by a thyristor) until a voltage swell is detected, is an effective strategy to reduce the switching losses [12]. However, this strategy would require an additional control mechanism to guarantee that the redundant SMs are properly charged at any time instant for their seamless integration at the start of a voltage swell event [13]. Here, it should be noted that implementing a strategy in which the capacitor voltage dc levels increase rapidly when a grid voltage swell occurs, requires a significant amount of active power draw from the grid in conventional StatComs to charge large capacitors rapidly. It is worth noting that the control strategy of changing the capacitor voltage dc levels has been utilized before to achieve other objectives. For instance, [14] uses this control strategy to enhance the modulation indices during grid voltage sags to improve the grid current quality.

The requirements for LC-StatComs are no different than in conventional StatComs when dealing with voltage swells, i.e. they should also be designed to operate with overrated capacitor voltages. Nevertheless, again, keeping the capacitors voltages at their maximum rated value will cause a significant increase in switching losses during normal operating conditions. The alternative approach of having some redundant SMs in idle mode that activate when a voltage swell is detected is even more challenging to implement in LC-StatComs as compared to conventional StatComs, because activating the idle SMs would require accurate tracking of the oscillations in the capacitor voltages, which is not feasible without interfering with the normal operation of the LC-StatCom. On the other hand, as LC-StatComs have reduced electrical inertia, implementing the strategy of fast increasing the capacitor voltage dc levels when the grid voltage swell occurs becomes a feasible solution.

This solution, which is only suitable for the LC-StatComs (owing to its lower inertia), is analyzed in the paper from two perspectives, firstly from the efficiency perspective, as varying the capacitor voltage directly affects switching losses, and secondly from the control point of view because the changes in capacitor voltage dc levels should be fast. The efficiency

perspective allows assessing the increased efficiency of an LC-StatCom that operates effectively even in the presence of voltage swells. The efficiency assessment is carried out using an accurate model of switching losses that does not disregard the capacitor voltage oscillation. The proposed strategy also allows operating with different capacitor voltage dc levels in different phases, thus further reducing the switching losses. Consequently, the main contribution of the paper is the development of a control strategy in LC-StatComs to ride-through grid voltage swells without loosing control of the converter while keeping high operating efficiency during normal operation.

The organization of the rest of the paper is as follows. Section II models the LC-StatCom with delta configuration taking into account grid voltage swells. The proposed strategy to set the capacitor voltage dc levels is discussed in terms of efficiency, and compared with other alternatives in Section III. Section IV presents the control block diagram to steer the system variables to the required set values when a voltage swell occurs. Section V depicts simulation results to demonstrate the effectiveness of the approach. Section VI describes experimental results obtained with a downscaled prototype. Section VII summarises the conclusions of the paper.

II. Modeling of LC-StatComs in Presence of Grid Voltage Swells

This section reviews the topology of the LC-StatCom with delta configuration, its state variables, and its main mathematical relationships. The effect of grid voltage swells is addressed in the model relationships.

A. Topology

Fig. 1 shows a circuit representation of the LC-StatCom with delta configuration. The power converter consists of three identical phase-arms $x \in \{ab,\, bc,\, ca\}$. Each phase-arm includes n H-bridge converters in cascade, and an arm impedance $\{L_{arm},\, R_{arm}\}$. Each H-bridge consists of a floating capacitor C, and two pairs of power switches. The three vertices of the delta connection (a), (b) and (c) are connected to the point of common coupling (PCC) grid voltages $\{e_a,\, e_b,\, e_c\}$.

B. Relationships in CHB Multilevel Converters with Delta Configuration

The dc-side voltage $v_{\Sigma-x}$ is defined as the per-phase sum of individual capacitor voltages, i.e.,

$$v_{\Sigma-x} = \sum_{j=1}^{n} v_{C-xj}. \tag{1}$$

Denoting δ_x as the modulating signals, which lie in the $[-1,\ 1]$ continuous range, the ac-side converter voltages v_x correspond to,

$$v_x = \delta_x v_{\Sigma-x}. \tag{2}$$

The line currents $\{i_a,\, i_b,\, i_c\}$ are linear combinations of the arm currents i_{arm-x}. However, the transformation matrix of

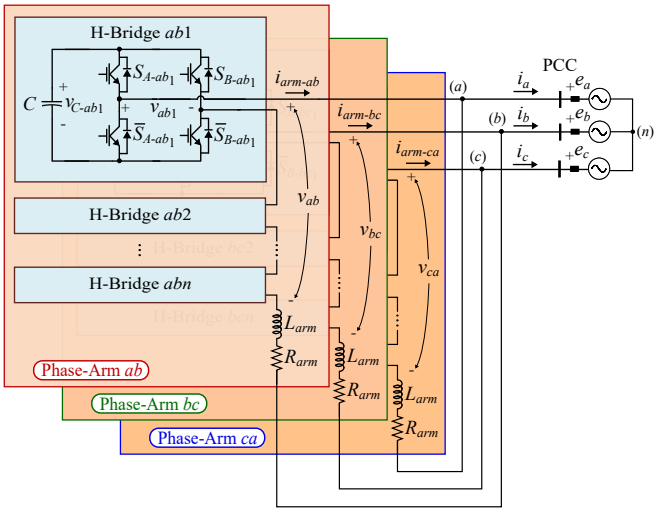

Fig. 1. Circuit diagram of a three-phase CHB power converter with delta configuration.

line currents to arm currents is nonfull rank until introducing the circulating current i_{circ} as a constraint [15],

$$i_{circ} = \frac{1}{3}\left(i_{arm-ab} + i_{arm-bc} + i_{arm-ca}\right). \tag{3}$$

Then, the following relationship for the converter arm currents can be obtained,

$$\begin{bmatrix} i_{arm-ab} \\ i_{arm-bc} \\ i_{arm-ca} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} i_{circ}. \tag{4}$$

Applying circuit analysis, and using (4), the arm current dynamics are found as,

$$\frac{d\, i_{arm-x}}{dt} = -\frac{R_{arm}}{L_{arm}} i_{arm-x} + \frac{1}{L_{arm}}\left(v_x - e_x\right), \tag{5}$$

where e_x refer to the line-to-line PCC grid voltages.

The expression that relates the ac-side power and the dc-side voltage in each phase-arm corresponds to,

$$\frac{1}{2}\frac{C}{n}\frac{d\, v_{\Sigma-x}^2}{dt} = -v_x i_{arm-x}. \tag{6}$$

C. Steady-State Relationships during Grid Voltage Swells

This subsection models grid voltage swells and provides a coherent set of steady-state values for all the converter variables.

A grid voltage swell can be modelled as a temporary increase in one (or more than one) of the line-to-neutral grid voltages [11],

$$\begin{aligned} e_a\left(t\right) &= \lambda_a \hat{E}_n \cos\left(\omega t\right) \\ e_b\left(t\right) &= \lambda_b \hat{E}_n \cos\left(\omega t - \tfrac{2\pi}{3}\right) \\ e_c\left(t\right) &= \lambda_c \hat{E}_n \cos\left(\omega t - \tfrac{4\pi}{3}\right) \end{aligned} \tag{7}$$

where ω is the grid frequency, $\hat{E}_n$ is the nominal amplitude of the line-to-neutral grid voltages, and parameters λ_a, λ_b and λ_c

model the magnitude of grid voltage swells. In a generalized grid voltage swell, the three parameters are expected to be,

$$1 \leq \lambda_{a,\,b,\,c} \leq 1.8. \tag{8}$$

To simplify the analysis, it is assumed that the delta-connected LC-StatCom only provides positive-sequence reactive currents to the grid, then, the line currents in the steady-state can be expressed as,

$$\begin{array}{l} i_a^{ss}(t) = I_d^{ss}\cos(\omega t) - I_q^{ss}\sin(\omega t) \\ i_b^{ss}(t) = I_d^{ss}\cos\left(\omega t - \frac{2\pi}{3}\right) - I_q^{ss}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ i_c^{ss}(t) = I_d^{ss}\cos\left(\omega t - \frac{4\pi}{3}\right) - I_q^{ss}\sin\left(\omega t - \frac{4\pi}{3}\right) \end{array} \tag{9}$$

where I_q^{ss} is the reactive current magnitude, which can be regarded as a known value (superscript ss is used for steady-state signals). Note that (9) considers active current I_d^{ss} for losses compensation.

According to (7), a grid voltage swell can involve an unbalanced set of line-to-line grid voltages when the swell affects each phase differently,

$$\begin{bmatrix} e_{ab}(t) \\ e_{bc}(t) \\ e_{ca}(t) \end{bmatrix} = \hat{E}_n \begin{bmatrix} \lambda_a + \frac{1}{2}\lambda_b \\ -\frac{1}{2}\lambda_b + \frac{1}{2}\lambda_c \\ -\left(\lambda_a + \frac{1}{2}\lambda_c\right) \end{bmatrix} \cos(\omega t) - \hat{E}_n \begin{bmatrix} \frac{\sqrt{3}}{2}\lambda_b \\ -\frac{\sqrt{3}}{2}\lambda_b - \frac{\sqrt{3}}{2}\lambda_c \\ \frac{\sqrt{3}}{2}\lambda_c \end{bmatrix} \sin(\omega t), \tag{10}$$

which can be rewritten as,

$$e_x(t) = E_{d,x}\cos(\omega t) - E_{q,x}\sin(\omega t), \tag{11}$$

where $E_{d,x}$ and $E_{q,x}$ are readily provided in (10). Therefore, the grid voltage amplitudes in each phase-arm correspond to $\hat{E}_x = \sqrt{E_{d,x}^2 + E_{q,x}^2}$, and the phase-angles correspond to $\phi_{e_x} = -\text{atan2}\left(-E_{q,x},\, E_{d,x}\right)$. Note that $\hat{E}_{ab}$, $\hat{E}_{bc}$, and $\hat{E}_{ca}$ can be different if the voltage swell has an unbalanced behaviour, i.e., if λ_a, λ_b and λ_c are not equal.

If the grid voltage amplitudes in each phase-arm are different, then the active power distribution among the converter phase-arms are not equal, and consequently, a circulating current is needed to mantain the capacitor voltage dc level values. Given the converter voltages v_x and arm currents i_{arm-x}, the average ac-side power P_{x-avg} can be obtained:

$$P_{x-avg} = \frac{1}{T}\int_0^T v_x i_{arm-x}\, dt. \tag{12}$$

Note that according to (6), P_{x-avg} charges the dc-capacitors, therefore, it must be zero in the steady-state, i.e., $P_{x-avg}^{ss} = 0$. To fulfill $P_{x-avg}^{ss} = 0$, a suitable steady-state fundamental-frequency circulating current must be injected [1],

$$i_{circ}^{ss}(t) = I_{d0}^{ss}\cos(\omega t) - I_{q0}^{ss}\sin(\omega t), \tag{13}$$

where I_{d0}^{ss} and I_{q0}^{ss} determine the amplitude $\hat{I}_{circ}^{ss} = \sqrt{I_{d0}^{ss\,2} + I_{q0}^{ss\,2}}$ and phase-angle $\phi_{i_{circ}}^{ss} = -\text{atan2}\left(-I_{q0}^{ss},\, I_{d0}^{ss}\right)$.

According to the Appendix, the steady-state current values in the $dq0$ frame $\left\{I_{d0}^{ss},\, I_{q0}^{ss},\, I_d^{ss}\right\}$ are

$$\begin{array}{l} I_{d0}^{ss} = \frac{\sqrt{3}I_q^{ss}}{6}\frac{\lambda_a\lambda_b + \lambda_a\lambda_c - 2\lambda_b\lambda_c}{\lambda_a\lambda_b + \lambda_a\lambda_c + \lambda_b\lambda_c} \\ I_{q0}^{ss} = -\frac{I_q^{ss}}{2}\frac{\lambda_a(\lambda_b - \lambda_c)}{\lambda_a\lambda_b + \lambda_a\lambda_c + \lambda_b\lambda_c} \\ I_d^{ss} = 0. \end{array} \tag{14}$$

The values in (14) correspond to ideal converter current values when no losses are considered, and these ideal current values are used as feedforward terms in the outer control loops in Section IV.

Consequently, substituting the expressions in the Appendix for the arm currents (A.1) and voltages (A.2) in (6), the capacitor voltages in the steady-state can be obtained [16] as follows,

$$v_{\Sigma-x}^{ss}(t) = \sqrt{K_x^{ss} - \frac{\hat{V}_x^{ss}\hat{I}_{arm-x}^{ss}}{2\omega C/n}\sin\left(2\omega t + \phi_{v_x}^{ss} + \phi_{i_{arm-x}}^{ss}\right)}, \tag{15}$$

where K_x^{ss} is a design variable that has to be chosen sufficiently large to avoid overmodulation and sufficiently low to reduce switching losses. Variables $\left\{\hat{V}_x^{ss},\, \phi_{v_x}^{ss}\right\}$ and $\left\{\hat{I}_{arm-x}^{ss},\, \phi_{i_{arm-x}}^{ss}\right\}$ are the amplitude and phase-angle of the steady-state converter voltages v_x^{ss} in (A.2) and arm currents i_{arm-x}^{ss} in (A.1), respectively. Note that $\left|\phi_{v_x}^{ss} - \phi_{i_{arm-x}}^{ss}\right| = \pi/2$ rad is guaranteed due to the circulating current injection (13). Then, as said, a proper setting of design variable K_x^{ss} is of importance both from an efficiency point of view and to prevent overmodulation. Therefore, the next section is devoted to studying different approaches to derive K_x^{ss}.

III. DC Capacitor Voltage Regulation Strategies

A. Strategies

In this section, four control strategies to regulate the dc capacitor voltages are evaluated, two of them for the conventional StatComs (**Strategy C1** and **Strategy C2**) and the other two for the LC-StatComs (**Strategy LC1** and **Strategy LC2**). These strategies involve different capacitor voltage dc levels, which are determined by the design variable K_x^{ss}. Note that K_x^{ss} plays an important role in the converter switching losses (illustrated in the following subsection).

The four strategies considered to establish the design variable K_x^{ss} are explained next. The maximum magnitude of the voltage swell considered in the next analysis is 180% increase of nominal value $\hat{E}_n$, according to the IEEE 1159 [11]; this means that, λ_a, λ_b, or λ_c is equal to 1.8 in (7).

- **Strategy C1**. In this strategy, the conventional StatCom is prepared for a grid voltage swell of up to 180%-magnitude, fixing permanently K_x^{ss} as,

$$K_x^{ss} = \left(h\, 1.8\sqrt{3}\hat{E}_n\right)^2, \tag{16}$$

  where h models a desired margin between dc- and ac-side converter voltages, thus h must be greater than 1 to prevent overmodulation. Note that $\sqrt{3}\hat{E}_n$ is the amplitude of the nominal line-to-line grid voltage.
- **Strategy C2**. In this strategy, the conventional StatCom deals with a grid voltage swell of up to 180% by adding

r redundant SMs. This means that the dc-value of the squared dc-side voltage of the set of active SMs, K_x^{ss}, corresponds to,

$$K_x^{ss} = \left(h \frac{n + r_1}{n} \sqrt{3} \hat{E}_n \right)^2, \tag{17}$$

$r_1 = \{0, 1, \ldots, r\}$ being the number of active redundant SMs. The number of active redundant SMs r_1 must be chosen according to the amplitude $\hat{E}_x$ as $r_1 = \left\lceil \hat{E}_x / \sqrt{3} \hat{E}_n \right\rceil$, where $\lceil x \rceil$ is a function that rounds up x. Note that (17) can be approximated, for a large enough number of redundant SMs, by

$$K_x^{ss} \approx \left(h \hat{E}_x \right)^2. \tag{18}$$

- **Strategy LC1**. In this strategy, the LC-StatCom is prepared for a grid voltage swell of up to 180%-magnitude, fixing permanently K_x^{ss} as,

$$K_x^{ss} = \left(h \, 1.8 \sqrt{3} \hat{E}_n \right)^2 - \frac{\hat{V}_x^{ss} \hat{I}_{arm-x}^{ss}}{2\omega C/n}. \tag{19}$$

- **Strategy LC2**. This is the proposed strategy, and the LC-StatCom is prepared for a grid voltage swell of up to 180%-magnitude, by setting K_x^{ss} as,

$$K_x^{ss} = \left(h \hat{E}_x \right)^2 - \frac{\hat{V}_x^{ss} \hat{I}_{arm-x}^{ss}}{2\omega C/n}. \tag{20}$$

Note that the amplitude $\hat{E}_x$ depends on the magnitude of the voltage swell λ_a, λ_b, or λ_c, according to (10).

In Fig. 2, the typical dc-side voltage waveforms according to (15) are shown for the four strategies, i.e., when K_x^{ss} corresponds to those of (16)-(20). Note that **Strategy C1** and **Strategy LC1** limit the capacitor voltage dc levels in each phase to a fixed value, whereas **Strategy C2** and the proposed **Strategy LC2** allow different capacitor voltage dc levels according to the grid voltage condition. It is important to remark that **Strategy C2** requires maintaining the voltage in the SMs at a pre-established value even if they are inactive for their seamless integration at the start of the swell event. This strategy cannot be directly applied to LC-StatComs since it is not possible to have a seamless integration due to the nonnegligible oscillation in the capacitor voltages. Moreover, **Strategy LC2** would be impractical in conventional StatComs, as significant amount of active power draw from the grid would be required to charge the large capacitors rapidly.

B. Efficiency Analysis and Comparison

In the sequel, for the sake of brevity, given the symmetry between phase-arms, the subscript corresponding to each phase-arm x is dropped. Also, this is a steady-state analysis, and the superscript ss is not explicitly indicated.

The switching losses for any switching event in jth H-bridge of a phase-arm, denoted as p_{sw-j}, is assumed to be proportional to the product between the blocking voltage v_{C-j} and the current i_{arm} at the switching instant, i.e.,

$$p_{sw-j}(t) = \alpha \, v_{C-j}(t) \, |i_{arm}(t)|. \tag{21}$$

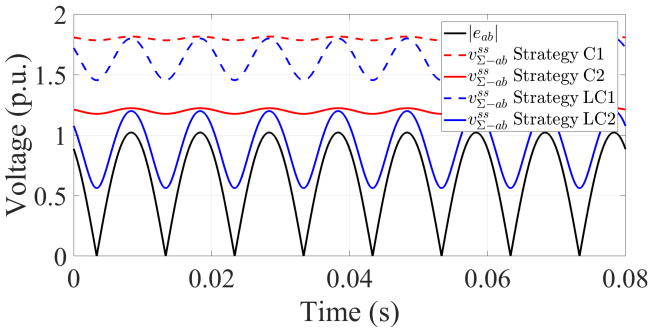

Fig. 2. StatCom voltage waveforms in phase-arm ab for the different capacitor voltage dc level strategies when operating at full-capacitive mode.

Adding together the losses of n H-bridges in the phase-arm yields,

$$p_{sw}(t) = \alpha \, v_{\Sigma}(t) \, |i_{arm}(t)|, \tag{22}$$

where α is a proportionality constant which represents the switching losses at $v_{C-j} = 1$ p.u. and $i_{arm} = 1$ p.u. Note that α depends on the switching rising and falling times and other physical characteristics of switches that are usually provided in datasheet.

The average switching losses over a grid period $T = 2\pi/\omega$ in a phase-arm is, in turn, proportional to $p_{sw}(t)$, and can be modeled as,

$$\langle P_{sw} \rangle = -\frac{\alpha'}{T} \int_{-T/2}^{0} v_{\Sigma}(\tau) \, i_{arm}(\tau) \, d\tau + \frac{\alpha'}{T} \int_{0}^{T/2} v_{\Sigma}(\tau) \, i_{arm}(\tau) \, d\tau, \tag{23}$$

where $\alpha' \neq \alpha$ depends on the ratio between switching rising-falling time and switching period, and also on the switching frequency. For comparison purposes, α' is equal in all the assessed strategies since conclusions will not depend on it.

Given the odd symmetry of the integrand, i.e., $v_{\Sigma} i_{arm}$, along the period T, (23) simplifies as,

$$\langle P_{sw} \rangle = 2\frac{\alpha'}{T} \int_{0}^{T/2} v_{\Sigma}(\tau) \, i_{arm}(\tau) \, d\tau. \tag{24}$$

Substituting $i_{arm} = \hat{I}_{arm} \cos\left(\omega t \pm \frac{\pi}{2}\right)$ and (15) into (24) yields,

$$\langle P_{sw} \rangle = 2\frac{\alpha'}{T} \sqrt{K} \hat{I}_{arm} \frac{1}{\omega} \int_{0}^{\pi} \sqrt{1 - \frac{1}{K} \frac{\hat{V} \hat{I}_{arm}}{2\omega C/n} \sin\left(2\theta \pm \frac{\pi}{2}\right)} \cos\left(\theta \pm \frac{\pi}{2}\right) d\theta, \tag{25}$$

where $d\theta = \omega \, dt$. Assuming capacitive operation and the even symmetry of the integrand, (25) can be rewritten as,

$$\langle P_{sw} \rangle = \frac{2}{\pi} \alpha' \sqrt{K} \hat{I}_{arm} \int_{0}^{\pi/2} \sqrt{1 + \Delta_{LC} \cos(2\theta)} \sin(\theta) \, d\theta, \tag{26}$$

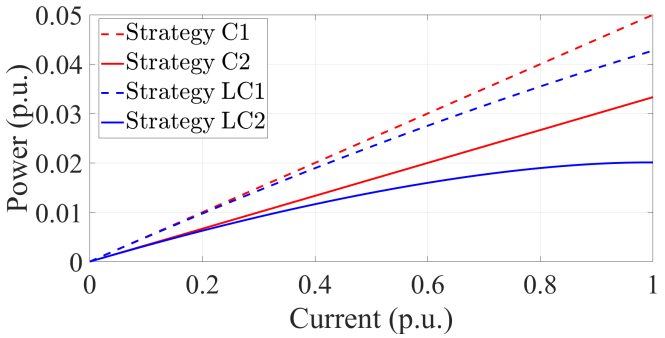

Fig. 3. Average switching losses for the different capacitor voltage dc level control strategies for $\hat{I}_{arm}$ from 0 to 1 p.u.

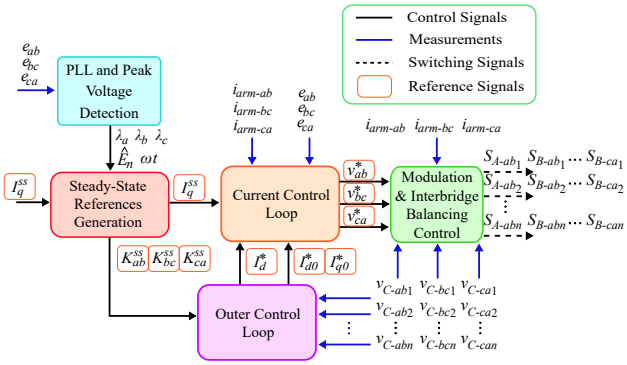

Fig. 4. Control block diagram for the proposed **Strategy LC2**.

where the integration interval is from 0 to $\pi/2$, and Δ_{LC} corresponds to,

$$\Delta_{LC} = \frac{1}{K}\frac{\hat{V}\hat{I}_{arm}}{2\omega C/n}, \tag{27}$$

which stands for the low-capacitance degree. Note that the low-capacitance degree is bounded by $0 < \Delta_{LC} < 1$. Observe that $\Delta_{LC} = 0$ represents the ideal conventional StatCom without capacitor voltage oscillations, and $\Delta_{LC} = 1$ represents the limit of low-capacitance where the capacitor voltage would instantaneously be zero at each multiple of half the grid period.

Using the variable change $v = \cos(\theta)$ in (26), yields,

$$\langle P_{sw} \rangle = \frac{2}{\pi}\alpha' \sqrt{K}\hat{I}_{arm} \int_0^1 \sqrt{(1-\Delta_{LC}) + 2\Delta_{LC}v^2}\, dv, \tag{28}$$

whose solution corresponds to,

$$\langle P_{sw} \rangle = \frac{\alpha'}{\pi}\sqrt{K}\hat{I}_{arm} \left(\sqrt{1+\Delta_{LC}} + \frac{1-\Delta_{LC}}{\sqrt{2\Delta_{LC}}} \sinh^{-1}\left(\sqrt{\frac{2\Delta_{LC}}{1-\Delta_{LC}}} \right) \right), \tag{29}$$

where $\sinh^{-1}(x)$ is the inverse hyperbolic sine function. Note that $\sinh^{-1}(x) = \ln\left(x + \sqrt{x^2+1}\right)$.

For the sake of illustration, the aforementioned strategies are compared next. Specifically, in the example, the α' value is determined considering a case where the switching losses in **Strategy C1** represents 5% of the processed power for the nominal current, i.e., $\hat{I}_{arm} = 1$ p.u., and the corresponding K according to (16). This α' value is maintained along other strategies. An analysis of the power switching losses for each strategy is carried out and the results are depicted in Fig. 3. As it can be observed, the proposed **Strategy LC2** reduces the switching losses from 5% to 2%, which represents a 60% reduction, which is a significant enhancement from an efficiency point of view. In the next section, the control architecture for the LC-StatCom according to **Strategy LC2** is explained.

IV. Control Stages for Implementing the Proposed Strategy LC2

This section provides the details of LC-StatCom control system for the proposed strategy that sets the capacitor voltage dc levels for efficient operation considering possible grid voltage swell occurrences.

The proposed **Strategy LC2**, which allows setting the capacitor voltage dc levels K_x^{ss} to prevent overmodulation, requires the detection of the swell magnitudes of each phase, i.e., $\{\lambda_a, \lambda_b, \lambda_c\}$. The control stages to operate the LC-StatCom based on this strategy are shown in the block diagram of Fig. 4. The first block processes the three-phase grid voltages $\{e_{ab}, e_{bc}, e_{ca}\}$ using a phase-locked loop (PLL) and a peak voltage detector, and obtains the grid angle ωt and the swell magnitudes $\{\lambda_a, \lambda_b, \lambda_c\}$. Once the grid condition is obtained, i.e., the values of $\{\lambda_a, \lambda_b, \lambda_c\}$, and the required reactive current I_q^{ss}, a block named Steady-State References Generation calculates the design variables $\{K_{ab}^{ss}, K_{bc}^{ss}, K_{ca}^{ss}\}$ according to (20). The Outer Control Loop block is in charge of controlling the instantaneous $\{K_{ab}, K_{bc}, K_{ca}\}$ values towards their desired steady-state values $\{K_{ab}^{ss}, K_{bc}^{ss}, K_{ca}^{ss}\}$, being the control output the current references in the $dq0$ frame $\{I_{d0}^*, I_{q0}^*, I_d^*\}$. Finally, the Current Control Loop block and the Modulation & Interbridge Balancing Control block, provide switching signals for the H-bridge switches S_{A-xj}, S_{B-xj}.

The Outer Control Loop block controls the instantaneous dc-value of the squared dc-side voltages $\{K_{ab}, K_{bc}, K_{ca}\}$, compensating for small operational losses. This block is shown in Fig. 5, and consists of two subblocks. The first subblock, named DC Level Extraction, extracts $\{K_{ab}, K_{bc}, K_{ca}\}$ from the measured capacitor voltages using second-order generalised integrators (SOGIs) configured as notch filters at 2ω [17]. Note that the subblock DC-Level Extraction, provides the $\alpha\beta 0$ components, i.e., $\{K_\alpha, K_\beta, K_0\}$, of the instantaneous variables $\{K_{ab}, K_{bc}, K_{ca}\}$. Thus,

$$\begin{bmatrix} K_\alpha \\ K_\beta \\ K_0 \end{bmatrix} = \boldsymbol{T}_{\alpha\beta 0} \begin{bmatrix} K_{ab} \\ K_{bc} \\ K_{ca} \end{bmatrix}, \tag{30}$$

with $\boldsymbol{T}_{\alpha\beta 0}$ as the power-conservative Clarke Transformation

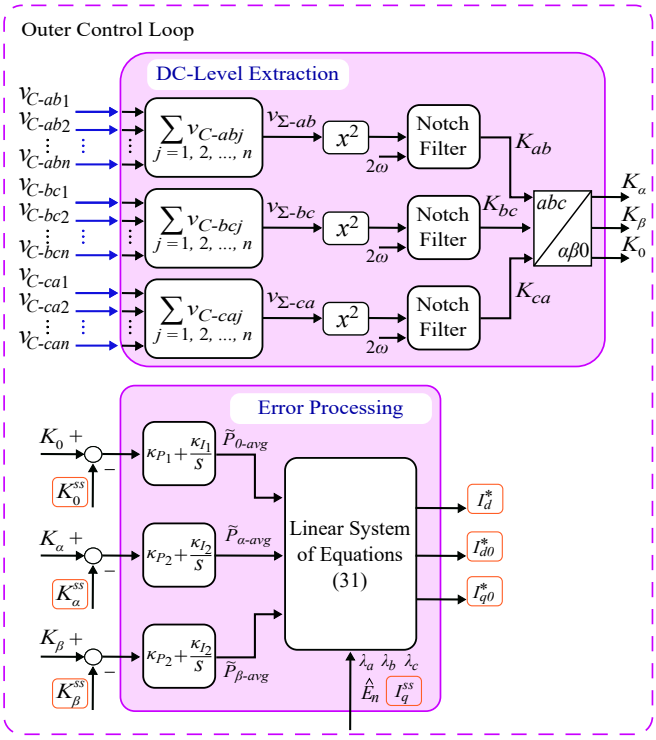

Fig. 5. Block diagram of the Outer Control Loop.

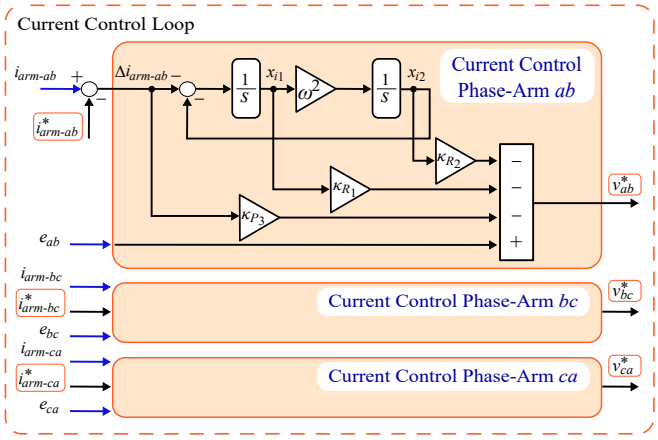

Fig. 6. Block diagram of the Current Control Loop.

Matrix. The $\alpha\beta 0$ components of $\{K_{ab}^{ss},\, K_{bc}^{ss},\, K_{ca}^{ss}\}$ are identically calculated.

The second subblock, named Error Processing, provides $\{I_{d0}^{*},\, I_{q0}^{*},\, I_{d}^{*}\}$ using three proportional-integral (PI) controllers. According to (A.6) in the Appendix, the current references are calculated as,

$$\begin{bmatrix} I_{d0}^{*} \\ I_{q0}^{*} \\ I_{d}^{*} \end{bmatrix} = \boldsymbol{A}^{-1} \left(\begin{bmatrix} P_{\alpha-avg} \\ P_{\beta-avg} \\ P_{0-avg} \end{bmatrix} - \boldsymbol{b} \right), \tag{31}$$

with $\boldsymbol{A}$ and $\boldsymbol{b}$ as in (A.4) and (A.5), respectively. Note that $P_{\alpha-avg} = \tilde{P}_{\alpha-avg}$ since $P_{\alpha-avg}^{ss} = 0$, and similarly for the β and 0 components.

The averaged power $\tilde{P}_{0-avg}$ is calculated by a PI controller, from the error $\tilde{K}_0 = K_0 - K_0^{ss}$,

$$\tilde{P}_{0-avg} = \kappa_{P1}\tilde{K}_0 + \kappa_{I1} \int \tilde{K}_0 \, dt. \tag{32}$$

Note that $\tilde{P}_{0-avg}$ compensates for relatively small losses in the StatCom.

The averaged powers $\tilde{P}_{\alpha-avg}$ and $\tilde{P}_{\beta-avg}$ are calculated using similar PI controllers, i.e.,

$$\tilde{P}_{\alpha-avg} = \kappa_{P2}\tilde{K}_\alpha + \kappa_{I2} \int \tilde{K}_\alpha \, dt, \tag{33}$$

$$\tilde{P}_{\beta-avg} = \kappa_{P2}\tilde{K}_\beta + \kappa_{I2} \int \tilde{K}_\beta \, dt, \tag{34}$$

with the errors $\tilde{K}_\alpha = K_\alpha - K_\alpha^{ss}$ and $\tilde{K}_\beta = K_\beta - K_\beta^{ss}$.

As said, the inner Current Control Loop block, together with the Modulation & Interbridge Balancing Control block, provide switching signals for the H-bridge switches. The Current Control Loop block uses as inputs: (i) the instantaneous arm currents $\{i_{arm-ab},\, i_{arm-bc},\, i_{arm-ca}\}$, (ii) the arm current references $\{i_{arm-ab}^{*},\, i_{arm-bc}^{*},\, i_{arm-ca}^{*}\}$ (according to I_q^{ss}, and $\{I_{d0}^{*},\, I_{q0}^{*},\, I_{d}^{*}\}$ obtained from (31)), and (iii) the instantaneous line-to-line grid voltages $\{e_{ab},\, e_{bc},\, e_{ca}\}$. The Current Control Loop block steers the arm currents towards their references, by adjusting the converter voltage references $\{v_{ab}^{*},\, v_{bc}^{*},\, v_{ca}^{*}\}$. This block is shown in Fig. 6, and consists of three identical and phase-arm-decoupled subblocks. For the sake of completeness, the calculation of v_{ab}^{*} is performed in the subblock Current Control Phase-Arm ab by using a state feedback approach,

$$v_{ab}^{*} = -\begin{bmatrix} \kappa_{P3} & \kappa_{R1} & \kappa_{R2} \end{bmatrix} \begin{bmatrix} \Delta i_{arm-ab} \\ x_{i1} \\ x_{i2} \end{bmatrix} + e_{ab}, \tag{35}$$

with current error $\Delta i_{arm-ab} = i_{arm-ab} - i_{arm-ab}^{*}$, and with two added integral states x_{i1}, x_{i2} to achieve zero steady-state error tracking at grid frequency ω [18], as,

$$\dot{x}_{i1} = -\Delta i_{arm-ab} - x_{i2}, \tag{36}$$

$$\dot{x}_{i2} = \omega^2 x_{i1}. \tag{37}$$

Note that e_{ab} is used as a feedforward term.

$\{v_{ab}^{*},\, v_{bc}^{*},\, v_{ca}^{*}\}$ constitute the input of the block Modulation & Interbridge Balancing Control, which, in turn, generates appropiate signals for the switching devices using phase-shifted carrier pulse-width modulation (PSC-PWM) [2].

V. Simulation Results

In this section, simulation results from a 36-MVA multilevel LC-StatCom with five SMs per phase connected to a 6-kV 50-Hz grid are provided to show the effectiveness of the proposed strategy. A PSC-PWM strategy with 5 kHz carriers has been adopted. The system is simulated in MATLAB/Simulink environment. The selected capacitor size in each SM is $C = 1.43$ mF, which yields 60% voltage oscillation during nominal operating conditions.

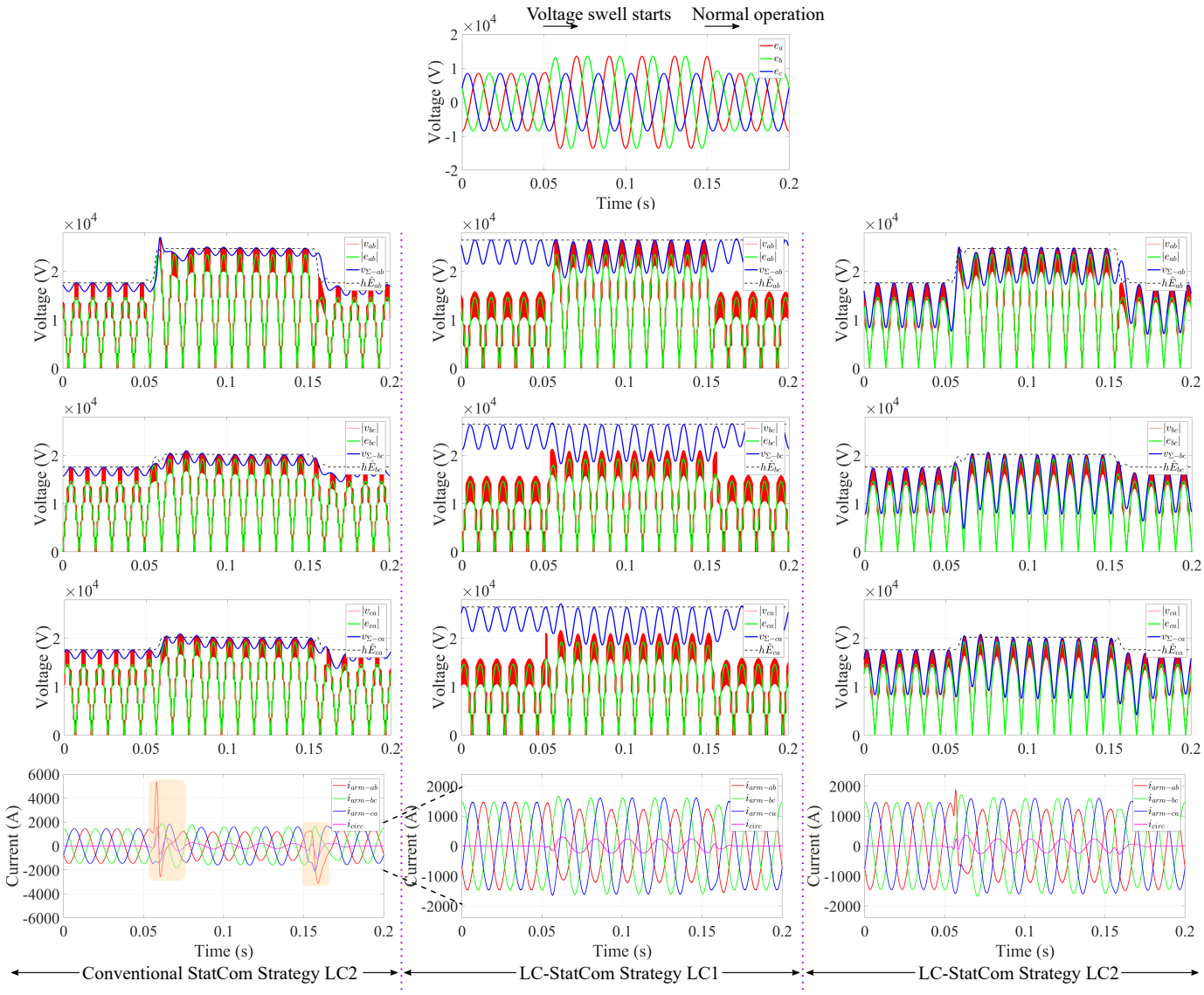

Fig. 7. Simulation waveforms. From top to bottom: Line-to-neutral PCC grid voltages, phase-arm ab voltages $\{v_{ab}, v_{\Sigma-ab}\}$, phase-arm bc voltages $\{v_{bc}, v_{\Sigma-bc}\}$, phase-arm ca voltages $\{v_{ca}, v_{\Sigma-ca}\}$, and arm currents $\{i_{arm-ab}, i_{arm-bc}, i_{arm-ca}\}$.

The waveforms are obtained when the LC-StatCom is providing 100%-rated power capacitive-mode, and a voltage swell of 60% magnitude occurs in phases a and b between $t_1 = 0.05\,\text{s}$ and $t_2 = 0.15\,\text{s}$, as it can be observed in the top plot of Fig. 7. The left column of Fig. 7 depicts the voltage and current waveforms of a conventional StatCom (using a four-times larger capacitor size) when the proposed **Strategy LC2** is applied, where the capacitor voltage dc levels are set according to (20); the middle column of Fig. 7 depicts the LC-StatCom voltage and current waveforms when the **Strategy LC1** is used, where the capacitor voltage dc levels are permanently fixed according to (19); whilst the right column of Fig. 7 depicts the LC-StatCom voltage and current waveforms with the proposed **Strategy LC2**. The proposed strategy can be theoretically applied to any StatCom, however, as can be seen in the arm currents in the bottom plot of the left column, abrupt current transients are produced, approximately four-times the nominal value, to be able to quickly charge/discharge the large capacitors used in the conventional StatCom. This is intolerable in practice since such current levels could trip the StatCom protections. On the other hand, the proposed strategy becomes practical when applied to the LC-StatCom, i.e., the capacitor voltage dc levels can be quickly charged/discharged with lower current requirements according to the grid conditions. In the case depicted in Fig. 7, the phase-arm ab is the most affected by the voltage swell, and thus i_{arm-ab} quickly charges K_{ab} to its reference value. In the **Strategy LC1**, instead, the voltage swell transient is seamless from the arm currents point of view, but at the expense of greater switching losses during normal converter operation.

It can be observed that during normal converter operation, i.e., before $t_1 = 0.05\,\text{s}$ and after $t_2 = 0.15\,\text{s}$, the proposed strategy allows the converter's full-capacity operation using

TABLE I
EXPERIMENTAL SYSTEM PARAMETERS

Parameter	Value
Nominal line-to-line grid voltage amplitude, $\sqrt{3}\hat{E}_n$	$30\sqrt{6}$ V (1 p.u.)
Nominal grid power, S_n	740 VA (1 p.u.)
Nominal arm current amplitude, $\hat{I}_{arm,n}$	6.7 A (1 p.u.)
Grid angular frequency, ω_g	100π rad/s
Carrier frequency, f_c	20 kHz
Nominal upper bound capacitor voltage, $h\sqrt{3}\hat{E}_n$	$1.3\sqrt{3}\hat{E}_n = 95.5$ V
Capacitance per SM, C	210 μF (0.24 p.u.)
Filter inductances, L_{arm}	2 mH (0.06 p.u.)

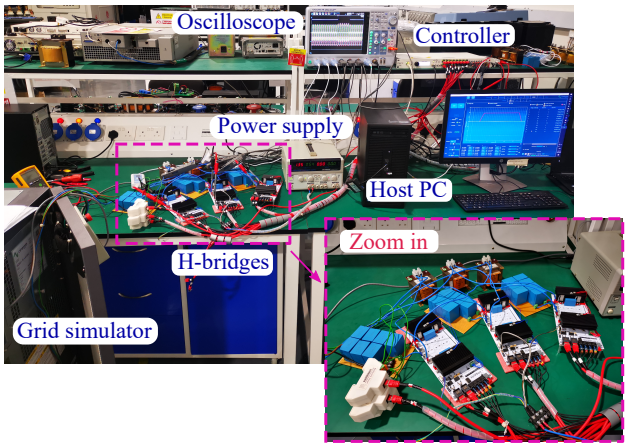

Fig. 8. Experimental setup.

its eleven voltage levels, while the **Strategy LC1** limits the converter operation to only five voltage levels. This results in inferior voltage quality, specifically, the total harmonic distortion (THD) of the LC-StatCom PWM converter voltages $\{v_{ab}, v_{bc}, v_{ca}\}$ is approximately 10% in the proposed strategy, whereas it is 19% when using the **Strategy LC1**. The THD of the conventional StatCom voltages is approximately 13%. Thus, the proposed strategy allows i) fast capacitor dc levels regulation with safe current values, and ii) full-capacity operation with lower THD and switching losses.

VI. EXPERIMENTAL RESULTS

This section presents experimental measurements that illustrate the LC-StatCom behaviour concerning its ability to ride through grid voltage swells while operating at efficient capacitor voltage dc levels. First, the constructed prototype is described and its main parameters are defined. Then, experimental measurements are shown with the purpose of assessing the proposed **Strategy LC2**.

Table I shows the system parameters and Fig. 8 depicts the experimental setup. The prototype has one SM per phase. Note that a margin $h = 1.3$, according to (20), has been selected during normal operation, while h is reduced down to $h = 1.15$ during grid voltage swells. The selected capacitor

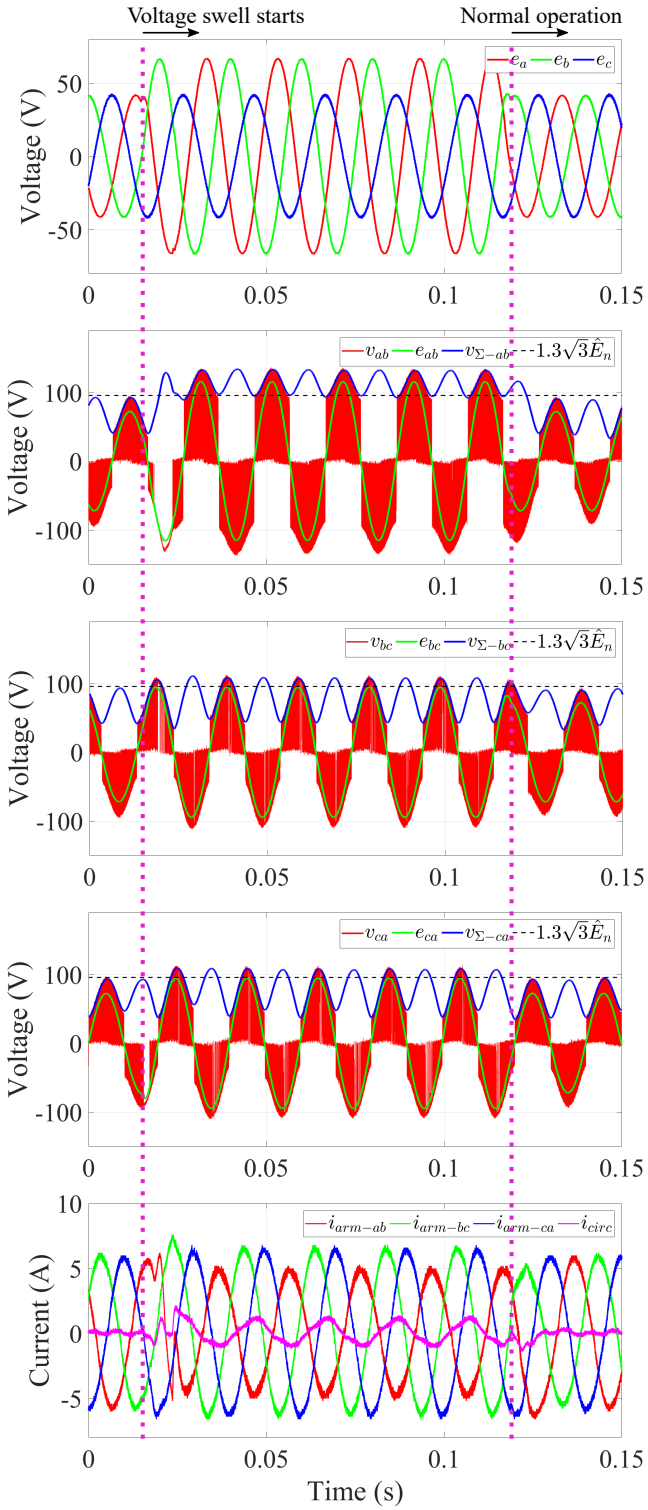

Fig. 9. Experimental waveforms. From top to bottom: Line-to-neutral PCC grid voltages, phase-arm ab voltages $\{v_{ab}, v_{\Sigma-ab}\}$, phase-arm bc voltages $\{v_{bc}, v_{\Sigma-bc}\}$, phase-arm ca voltages $\{v_{ca}, v_{\Sigma-ca}\}$, and arm currents $\{i_{arm-ab}, i_{arm-bc}, i_{arm-ca}\}$.

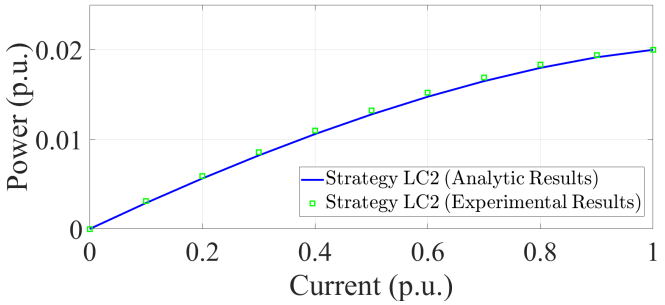

Fig. 10. Experimental measurement and analytical prediction of switching losses for the proposed **Strategy LC2**, for $\hat{I}_{arm}$ from 0 to 1 p.u.

size produces approximately 60% capacitor voltage oscillation during nominal operating conditions.

The PI gains κ_{P1} and κ_{I1} in (32) are chosen such that the closed-loop K_0 frequential response has a bandwidth of 311.49 rad/s, a damping ratio of 1.2, and a settling time of 0.03 s. Similarly, the PI gains κ_{P2} and κ_{I2} in (33)-(34) are chosen such that the closed-loop K_α and K_β frequential responses have a bandwidth of 155.75 rad/s, a damping ratio of 1.2, and a settling time of 0.06 s. Note that the loop in charge of updating the sum of capacitor voltage dc values, i.e., the K_0 control, is faster than the loop in charge of balancing the capacitor voltage dc values among the three phase-arms, i.e., the K_α and K_β control. Also, it is important to remark that the settling time for the inner current loop has been chosen equal to 1.5 ms.

Fig. 9 depicts the experimental waveforms during a voltage swell event. The waveforms are obtained when the LC-StatCom is providing 100%-rated power capacitive-mode, and a voltage swell of 60% magnitude occurs in phases a and b between $t_1 = 0.1$ s and $t_2 = 0.6$ s, which is shown in the top plot of Fig. 9. As it can be observed, the proposed **Strategy LC2** sets the capacitor voltage dc levels in each phase-arm according to the magnitude of the voltage swell, using (20). During regular converter operation, i.e., before $t_1 = 0.1$ s and after $t_2 = 0.6$ s, $\{K_{ab}, K_{bc}, K_{ca}\}$ are set such that the peak voltage across the capacitors in each phase-arm is equal to the prescribed value $1.3\sqrt{3}\hat{E}_n$, shown with a dashed line in the middle plots of Fig. 9. Then, when the grid voltage swell occurs, $\{K_{ab}, K_{bc}, K_{ca}\}$ are modified rapidly such that overmodulation is prevented as much as possible during the transient, and thus the LC-StatCom can still provide the required current. Note that if $\{K_{ab}, K_{bc}, K_{ca}\}$ values were not updated during the voltage swell, the capacitor voltages $\{v_{\Sigma-ab}, v_{\Sigma-bc}, v_{\Sigma-ca}\}$ would overlap with the absolute value of the voltages on the ac-side $\{|e_{ab}|, |e_{bc}|, |e_{ca}|\}$, thus incurring overmodulation. In the swell case depicted in Fig. 9, the phase-arm ab is the most affected by the grid voltage swell, and thus K_{ab} experiences a fast and abrupt transition to its new greater reference value. It is also important to note that a fundamental-frequency circulating current is needed during the voltage swell, and it is shown in the bottom plot of Fig. 9. The circulating current increases the peak value of the arm current in phase-arms bc and ca, while it decreases the peak value of the arm current in phase-arm ab. Consequently, the capacitor voltage oscillations become larger in magnitude in phase-arms bc and ca during the swell event, while smaller in phase-arm ab. Note that the arm currents in the bottom plot of Fig. 9 do not show abrupt changes, which is in accordance with the low-inertia behaviour in LC-StatComs. Consequently, for the depicted swell event, control stages behave in a proper manner, allowing to implement the proposed **Strategy LC2**, thus resulting in an efficient operation of the LC-StatComs under grid voltage swell events.

Moreover, Fig. 10 shows the switching losses obtained from the measured samples of capacitor voltages and arm currents along a period for different output power levels. In the figure, the measured switching losses are compared with those obtained by the analytic model (29), showing a close agreement between them.

VII. Conclusion

An efficient strategy for setting the capacitor voltage dc levels for LC-StatComs with delta configuration in presence of grid voltage swells has been analysed in the paper. The proposed strategy allows different capacitor voltage dc level references in each phase-arm of the LC-StatCom when the grid voltage swell occurs. The proposed strategy has been assessed from an efficiency point of view, and from a control perspective. The efficiency assessment is carried out using an analytical model that takes into account the capacitor voltage oscillation. This analytical model has allowed the comparison among different strategies for the conventional StatCom and the LC-StatCom, and has resulted in an accurate estimation of switching losses in each strategy. It has been shown that the proposed strategy is the most efficient among the considered alternatives. The proposed strategy, which changes the capacitor voltage dc levels when a grid voltage swell occurs, is implementable in LC-StatComs due to their low electrical inertia. The proposed strategy requires control stages that have been described in the paper. Simulation and experimental results show that changing the capacitor voltage dc levels as a function of the grid voltage magnitudes becomes a viable and efficient approach for the LC-StatComs. The proposed strategy reduces the switching losses up to 60%, whereas overmodulation is not compromised. Experimental results corroborate the feasibility of the proposed strategy and its excellent efficiency performance.

Appendix

Circulating Current Calculation for a Balanced Steady-State Behaviour

This Appendix provides the details of required circulating current and active current in the steady-state $\{I_{d0}^{ss}, I_{q0}^{ss}, I_d^{ss}\}$ for mantaining the capacitor voltages bounded. Substituting

(13) and (9) into (4) in the steady-state, yields the desired steady-state arm currents,

$$\begin{bmatrix} i^{ss}_{arm-ab}(t) \\ i^{ss}_{arm-bc}(t) \\ i^{ss}_{arm-ca}(t) \end{bmatrix} = \begin{bmatrix} \frac{I^{ss}_d}{2} - \frac{\sqrt{3}I^{ss}_q}{6} + I^{ss}_{d0} \\ \frac{\sqrt{3}I^{ss}_q}{3} + I^{ss}_{d0} \\ -\frac{I^{ss}_d}{2} - \frac{\sqrt{3}I^{ss}_q}{6} + I^{ss}_{d0} \end{bmatrix} \cos(\omega t) - \begin{bmatrix} \frac{\sqrt{3}I^{ss}_d}{6} + \frac{I^{ss}_q}{2} + I^{ss}_{q0} \\ -\frac{\sqrt{3}I^{ss}_d}{3} + I^{ss}_{q0} \\ \frac{\sqrt{3}I^{ss}_d}{6} - \frac{I^{ss}_q}{2} + I^{ss}_{q0} \end{bmatrix} \sin(\omega t). \quad \text{(A.1)}$$

Substituting (10) and (A.1) into (5) in the steady-state, and neglecting losses in the arm impedance, the desired steady-state converter voltages v^{ss}_x can be calculated,

$$v^{ss}_x(t) = L_{arm}\frac{d}{dt}\left(\hat{I}^{ss}_{arm-x}\cos\left(\omega t + \phi^{ss}_{i_{arm-x}}\right)\right) + \hat{E}_x\cos(\omega t + \phi_{e_x}), \quad \text{(A.2)}$$

where the amplitude of the arm current $\hat{I}^{ss}_{arm-x}$ and its phase angle $\phi^{ss}_{i_{arm-x}}$ are readily obtainable from (A.1). Considering (A.2) and (A.1) in (12), yields the following equation,

$$\boldsymbol{A}\begin{bmatrix} I^{ss}_{d0} \\ I^{ss}_{q0} \\ I^{ss}_d \end{bmatrix} + \boldsymbol{b} = \boldsymbol{T}_{\alpha\beta 0}\begin{bmatrix} P^{ss}_{ab-avg} \\ P^{ss}_{bc-avg} \\ P^{ss}_{ca-avg} \end{bmatrix}, \quad \text{(A.3)}$$

where

$$\boldsymbol{A} = \hat{E}_n\begin{bmatrix} \frac{\sqrt{6}(2\lambda_a+\lambda_b)}{8} & \frac{3\sqrt{2}\lambda_b}{8} & \frac{\sqrt{6}(\lambda_a+\lambda_b-2\lambda_c)}{24} \\ \frac{\sqrt{2}(2\lambda_a-\lambda_b+2\lambda_c)}{8} & -\frac{\sqrt{6}(\lambda_b+2\lambda_c)}{8} & -\frac{\sqrt{2}(\lambda_a-\lambda_b)}{8} \\ 0 & 0 & \frac{\sqrt{3}(\lambda_a+\lambda_b+\lambda_c)}{6} \end{bmatrix} \quad \text{(A.4)}$$

$$\boldsymbol{b} = \hat{E}_n I^{ss}_q\begin{bmatrix} -\frac{\sqrt{2}(\lambda_a-\lambda_b)}{8} \\ -\frac{\sqrt{6}(\lambda_a+\lambda_b-2\lambda_c)}{24} \\ 0 \end{bmatrix}, \quad \text{(A.5)}$$

with $\boldsymbol{T}_{\alpha\beta 0}$ as the power-conservative Clarke Transformation Matrix, and note that in the steady-state the average powers must be zero, i.e., $P^{ss}_{x-avg} = 0$.

Note that the steady-state relationship (A.3) between the average ac-side powers P_{x-avg} and the currents in the $dq0$ frame, can be extended for transient behaviour around the steady-state as (A.6), namely, when the arm currents i_{arm-x} are close enough to their steady-state values,

$$\boldsymbol{A}\begin{bmatrix} I_{d0} \\ I_{q0} \\ I_d \end{bmatrix} + \boldsymbol{b} = \boldsymbol{T}_{\alpha\beta 0}\begin{bmatrix} P_{ab-avg} \\ P_{bc-avg} \\ P_{ca-avg} \end{bmatrix}. \quad \text{(A.6)}$$

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