Improved Model Predictive Current Control of the versatile Buck-Boost Converter for a Photovoltaic Application

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***Abstract*—The digital implementation of all the control loops of a versatile buck-boost (VBB) dc–dc converter used in a stand-alone photovoltaic application is proposed in this paper to improve existing digital-analog sliding-mode-based implementations. All three control loops: maximum power point tracking (MPPT), fast input voltage regulation, and inner high-bandwidth current control, have been programmed in the same digital signal controller (DSC). A Model Predictive Control (MPC) based algorithm has satisfactorily solved the challenge of implementing the nominal 100 kHz switching frequency current loop. The MPC cost function is distributed throughout the algorithm to achieve three specific goals: the tracking of the reference current (G1), a quasi-constant steady-state switching frequency (G2), and the assurance that the duration of an interval is larger than the time required to calculate it (G3). The third goal requires the current control to toggle between peak- and valley-modes depending on the operating point. The correct fulfillment of these control objectives on the proposed MPC-based algorithm has been validated through simulations and experimental tests performed on a purpose built-prototype.**

***Index Terms*—Current-Mode Model Predictive Control, versatile Buck-Boost converter, fast MPPT, Stand-Alone Photovoltaic Application.**

I. Introduction

Maximum power point tracking (MPPT) algorithms are a topic of broad interest in the field of photovoltaic (PV) systems. Power converters carry out the MPPT algorithms implementation and any control action in PV systems [1]. Step-up dc-dc converters (boost converters) are usually used to obtain the maximum power and raise the generated voltage according to the dc-bus imposed by a battery [2]. An alternative converter is a buck-boost topology, which can increase and reduce the PV panel voltage, convenient in applications where a wide variation range of the input and/or output voltage is required [3], [4]. Buck-boost converters allow storing the harvesting power in lower voltage batteries and provide power to loads with a lower voltage than the nominal maximum power point (MPP). In addition, the possible switching between buck and boost modes allows obtaining the maximum power when the bypass diodes of the photovoltaic modules are activated due to partial shading conditions [5].

The simplest buck-boost topology that has been used for MPPT implementation is the classic buck-boost converter [6]. A modified P&O MPPT algorithm extracts the maximum power in this application and supplies a resistive load. The main drawbacks of this unidirectional topology are the voltage gain and the stress in the converter components [7]. More complex buck-boost topologies have been proposed in the literature for PV source applications, batteries, and dc-loads [8]–[10]. The cascade buck-boost converter has emerged in this field for its high efficiency and bidirectional capacity that allows controlling the power flow between sources, energy storage units, and loads [8]. In this topology, the power source and the dc-load share the same port but are not connected simultaneously. In [9], a buck-boost converter that allows the simultaneous connection of a PV source, battery, and load is presented. This topology requires only one inductor, but it uses several semiconductors to provide all the required configurations. Likewise, a buck-boost converter with two inputs (PV source and battery) and three outputs is proposed in [10]. In all the above applications, buck-boost converters use constant-frequency PWM control techniques.

Model predictive control (MPC), and more specifically the finite control set (FCS) MPC, is a variable switching frequency control strategy widely used in power converters [11], powered by the advances in digital processing systems that allow meeting with most demanding control goals. FCS-MPC technique has been presented in the literature in several MPPT applications, but most publications have not addressed the double loop control strategy proposed in this work [12]–[16]. Only two publications have presented FCS-MPC in the current loop in the MPPT algorithm based on a double loop control strategy. On the one hand, in [17], FCS-MPC was integrated into the current-controlled boost converter with a sampling frequency of 36.6 kHz, which generates an equivalent switch-

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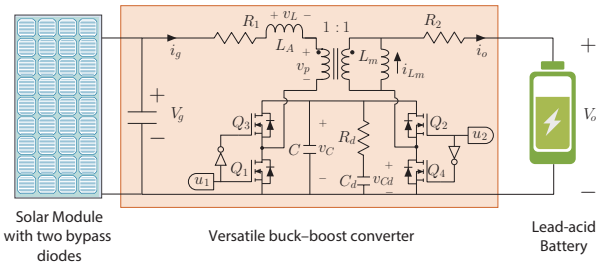

Fig. 1. Schematic circuit diagram of the VBB converter.

ing frequency of around 10 kHz. On the other hand, in [18], an inner current controller of a battery and supercapacitors systems is presented in a stand-alone dc-microgrid. Still, a PWM-based control performs the MPPT tracking. Although details of the system sampling frequencies are not given, it is believed to be low due to IGBT modules. Both works approach the classic FCS-MPC technique, characterized by variable switching frequency, with a steady-state tracking error. Some examples of fixed switching frequency FCS-MPC can be found in the literature on dc-ac applications [19]–[22] but not in the case of dc-dc converters. Some works deepen in the operation at fixed switching frequency of dc-dc converters but using a continuous control set MPC (CCS-MPC) [23] and are limited to low switching frequencies.

This work proposes an inner current loop based on an FCS-MPC of the dc-dc VBB converter [24] for a stand-alone PV application, as shown in Fig. 1. The proposed current control is based on the analog peak current control with variable switching frequency applied to a boost-based power factor corrector pre-regulator [25]. This current strategy was later modified and digitally implemented in [26], taking two current samples per switching cycle. Now a one-sample digital predictive control has been adapted to the two-switch VBB converter that, for efficiency reasons, is mainly operated as a synchronous boost converter with output filter or as a synchronous buck converter with input filter [24].

The main contribution of this paper is the digital implementation of an internal current control with a high dynamic response, based on the FCS-MPC technique, which decides the switching sequence and the duration of states to achieve the following challenging and novel control goals:

- *G1: Reference current tracking without steady-state error*. This goal faces one of the main drawbacks of a classic FCS-MPC characterized by a steady-state error of the controlled variable caused by oscillations around the reference value [27]. This error is due to the discrete nature of the FCS-MPC that does not take into account the system performance between samples. This error is alleviated using intermediate sampling or an integral term in the cost function [27]. However, it will lead to computational overhead in both cases, which increases the processor requirements for its implementation. Therefore, this article proposes a low computational FCS-MPC strategy with a zero steady-state error, which allows its programming in a low-cost microcontroller.
- *G2: Quasi-constant steady-state switching frequency.* This goal approaches one of the significant drawbacks of FCS-MPC, which is the variable switching frequency of the semiconductors [27], [28]. This frequency can vary randomly depending mainly on the operating point of the converter and the control sampling time, which produce a wide distributed voltage and current spectrum, causing audible noise, resonances, and poor steady-state behavior [28]. The proposed FCS-MPC strategy achieves a quasi-constant steady-state switching frequency (f_{sw}) of 100 kHz, overcoming the problems described.
- *G3: Assurance of enough time to compute the control.* With this goal, the proposed control can be programmed in a low-cost microcontroller at a high switching frequency of 100 kHz, unlike other systems presented in the literature operating at lower frequencies (< 30 kHz) and programmed into expensive platforms [23]. Therefore, depending on the operating point, the current control toggle between peak- and valley-modes to provide the maximum calculation time for the control law. In this goal, the proposed algorithm ensures that the duration of an interval is larger than the time required to calculate it.

This paper is organized as follows: Section I provides an introduction and describes precedent works. Section II describes the proposed model predictive digital control. Simulations and experimental results are provided and compared in Section III. Finally, Section IV offers conclusions and some suggestions for future works.

II. Versatile buck-boost converter

A previous publication proposed the use of the topology known as the VBB converter for its comparative advantages for a stand-alone photovoltaic application that benefits from the converter's voltage step-up and step-down static characteristics to extract the maximum available power from an 85 W PV module that, because of its two bypass diodes, has two possible MPPs [29]. When no bypass diode is activated, the nominal MPP voltage will be in the vicinity of 18 V. In the case of the activation of one of the bypass diodes because of partial shadowing, the PV module $p - v$ curve exhibits two local maxima: the PV nominal operating voltage of around 18 V and a lower voltage one around 9 V. To extract the maximum energy from the PV module, an MPPT algorithm [30] must quickly decide which one of the local maxima is the actual MPP and, to obtain a good MPPT efficiency, make the system voltage change rapidly from the vicinity of one of the nominal MPPs to the other and vice versa. In [29], two different fast analog controllers based on sliding mode control were proposed to regulate the converter's input voltage, which was also the output voltage of the PV module, so that the system battery was charged with the maximum available current. A key factor of the reported application was that the voltage range of the system battery should be between the two possible MPP voltages, which justified the need for a two-switch dc–dc converter operating either as a boost converter with output filter or as a buck converter with input filter. Fig. 2 depicts, for a nominal 25°C ambient temperature, the $p - v$ curve under partial shadowing of the PV module (MSP-105W) selected in

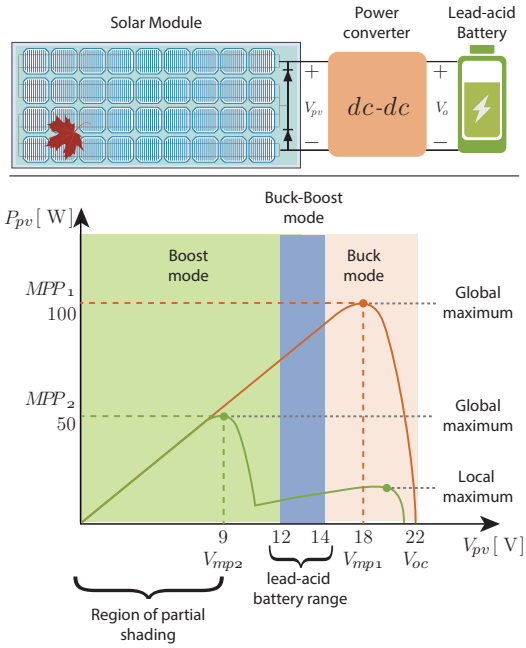

Fig. 2. A stand-alone PV battery-charging system and $p-v$ curves of its PV module without (one power peak) and under partial shadowing (two power peaks).

this work, similar to the BP585 used in the previous works except for delivering 105 W at the nominal MPP. The figure also indicates the approximate voltage range of the considered lead-acid battery. To determine and operate in the vicinity of the system's MPP, a digital algorithm, modified from the well–known perturb and observe type, provided the analog regulator with a fast time-varying voltage reference with large and small amplitude steps. The required fast regulation loop was based on a high bandwidth inner current control loop, which is possible thanks to the converter's minimum-phase behavior obtained by magnetically coupling its two inductors, and by adding an RC damping network in parallel to its intermediate capacitor, as shown in Fig. 1. The voltage regulator bandwidth was about 20 kHz, one fifth of the 100 kHz nominal switching frequency.

To further improve the previous system [29], a logical step is to digitally implement its inner current control loop with the same hardware as the MPPT outer loop.The main difficulties in implementing a fast current control loop for a dc–dc converter operating at a nominal switching frequency of 100 kHz, are the bandwidth of the required current sensor along with the sampling ratio of analog to digital converters such as the provided by the TMS320F28335 digital signal controller (DSC). Minimizing the calculation time required to compute the control algorithm so that the control outputs can be updated in the switching interval that follows the current sampling can be difficult if a multisampling approach digital pulse width modulation (DPWM), such as the one in [31], or predictive strategies requiring more than one sample per switching period [32] are used.

III. Model Predictive Digital Current Control

In this paper, an FCS-MPC for the inner current loop of the VBB converter is proposed. The outer voltage loop is based on a classical PI control capable of tracking the voltage reference imposed by the MPPT algorithm. A common and fundamental P&O MPPT strategy has been used. The proposed current control can be seen as a peak current control for the boost configuration resulting in a valley current control for the buck configuration. Similarly, a valley current control in boost configuration results in a peak current control in a buck configuration.

Since the two-switch converter has three possible switching states (one combination is forbidden), the control algorithm has to decide the sequence and time duration of states so that three goals are achieved. One goal is that, at the end of some states, the current peak or valley value must be at the predicted level (goal G1). The second goal is that, despite being implemented in a variable switching form that provides fast transient responses, the steady-state switching frequency must be ideally at the same specified nominal value of 100 kHz irrespectively of the operating point (goal G2). The third goal is that the calculation times required by the algorithm in each state must not exceed their calculated values so that the delay introduced by the digital implementation is less than the expected stationary switching period (goal G3). To ensure this last goal, the current sampling point can be displaced when the previous duration of some intervals approaches the minimum duration required to perform the algorithm calculations. Any sampling point displacement transforms a peak current control into a valley current control and vice versa. Therefore, the control algorithm is a multi-objective algorithm: it must provide zero peak (or valley) current error, constant stationary switching frequency, and enough calculation time to update the control variables at the switching interval following the current sampling point.

The proposed current control can be seen as a particular case of FCS-MPC with a cost function that is a combination of the error between the input inductor current peak (or valley) and its reference, and the error between the switching cycle duration and its desired steady-state value. In addition, whether the current reference means peak or valley is decided to ensure the in–cycle calculation and update of the two control variables. Because of the reduced number of states, the transitions between them have been optimized offline so that they do not require the computation of the full cost function. As will be explained, there is also an outer voltage regulation loop with a digital proportional-integral PI type compensator that provides the current reference. The voltage reference of the voltage loop is expected to be provided by an MPPT supervising algorithm.

In a simplified description, the algorithm starts by sampling the input inductor current and input and output voltages at the beginning of the first of the two switching subintervals. The current sample, together with the theoretical slope of the inductor (either in boost mode or in buck mode) is used to determine the required duration of the first subinterval, so that, at its end, the current value reaches the reference provided by the voltage loop, of the PI type. The duration of the second

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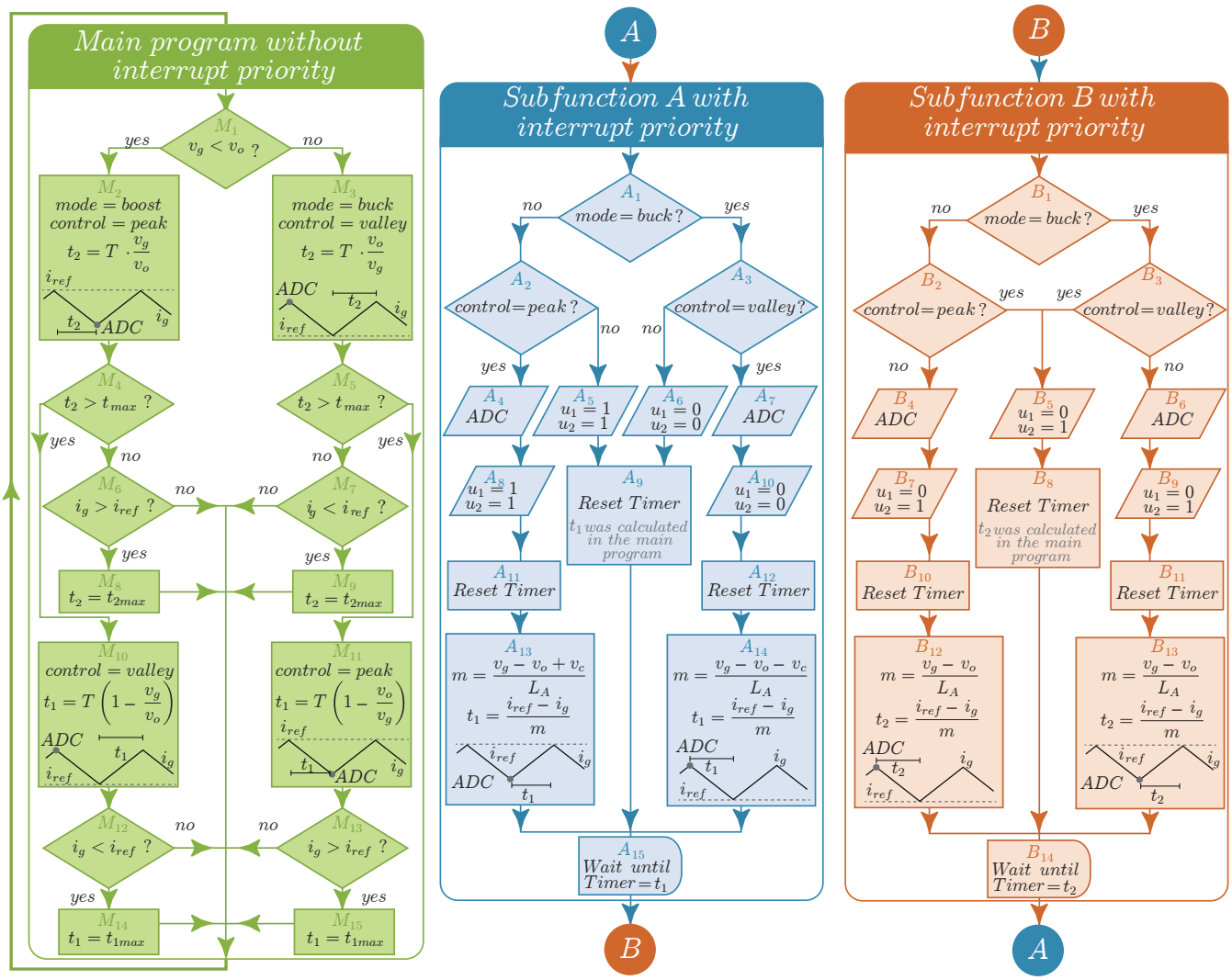

Fig. 3. Main states of the inner current loop.

subinterval can be obtained from the static input/output voltage ratio [25], [26] so that $t_2 = T \cdot v_g/v_o$ in boost mode, where the input voltage (v_g) is smaller than the output voltage (v_o), or $t_2 = T \cdot v_o/v_g$ in buck mode where $v_g > v_o$. In some cases, the slope of the input inductor current also depends on the intermediate capacitor voltage (v_C). To reduce the algorithm execution time, it has been decided that sampling the actual value of the intermediate capacitor voltage is not required and its expected mean value $v_C = max[v_g, v_o]$ is considered instead.

As in the case of the intermediate capacitor, it is also assumed that the input (PV module) and output (battery) voltages are approximately constant in a switching cycle. Therefore their sampling instant does not affect the current slope calculation significantly. Disregarding losses, the switching frequency will be constant only in steady-state and can vary at the transients, fundamentally due to changes in the input voltage. Since the MPPT algorithm will require continuous input voltage changes, the variable switching frequency provides an additional degree of freedom that improves the system response at the voltage transients [25].

As mentioned before, the algorithm requires that the input and output voltages of the converter are also sampled. For example, the MPPT algorithm could require the input voltage to evaluate whether the power extracted (current times voltage) is maximum. Also, the input voltage is compared with the reference provided by the MPPT algorithm in a PI-type voltage controller to provide the current reference for the inner loop.

Fig. 3 shows a more detailed description of the inner current control algorithm. The left column corresponds to the main continuous loop, in which the output voltage (the battery voltage) is compared with the input voltage reference to determine if the converter switches should operate in boost (step-up) mode or in buck (step-down) mode. The default current control in boost mode regulates the peak current (control variable set to peak), which requires the calculation of the negative current slope subinterval duration as $t_2 = T\frac{v_g}{v_o}$. In steady-state peak current operation, the actual sample of the inductor current (i_g) must be under the current reference (i_{ref}). If this is not the case, the calculated duration of the negative slope subinterval is set to a predetermined maximum value ($t_2 = t_{2max}$) so that i_g will have a maximum decrease conducting it below

i_{ref}. The subinterval duration t_2 is subsequently compared with a threshold level t_{max} to decide if the current control has to be changed to valley operation (control variable set to valley). The duration of the positive current slope subinterval is calculated as $t_1 = T\left(1 - \frac{v_g}{v_o}\right)$ instead of t_2. Contrary to the peak control, in valley control the actual sample of the inductor current (i_g) must be above the current reference (i_{ref}) in steady-state. If this is not the case, the positive-slope subinterval duration is set to a predetermined maximum value ($t_1 = t_{1max}$). This ensures that the complementary subinterval duration, t_1 in peak control or t_2 in valley control, can have a value large enough so that it can be calculated and updated at its corresponding timer without overflowing the count. A symmetric branch in the main loop algorithm processes the program flow in buck mode. Note that in buck mode the default current control is the valley one, and the duration of the positive-slope subinterval becomes t_2, while t_1 represents the negative-slope subinterval duration. Note also that in a switching cycle, the input capacitor voltage and the battery voltage can be considered constant ($v_g = V_{in}$) and ($v_o = V_{out}$), so their mean values (low pass filtered) can be used instead of their instantaneous values at the sampling instants.

Discrete control variables u_1 and u_2 (see Fig.1) have three permitted combinations {State 00: (u_1=0, u_2=0), State 01: (u_1=1, u_1=0), State 11: (u_1=1, u_2=1)} and a forbidden one (State 10: (u_1=1, u_1=0)). State 01 is common to both buck and boost modes, while State 11 is exclusive to boost mode and State 00 to buck mode. The direct transition from State 00 to State 11 is not allowed. The permitted States and transitions allowed among them ensure that only one half-bridge switches at high frequency (the left one in boost mode and the right one in buck mode), eliminating unnecessary simultaneous high-frequency switching of both half-bridges and the associated increase in switching losses. Two almost symmetrical subfunctions (A and B) are sequentially executed so that when timer B, representing the common State 01 duration, reaches the count t_2, the execution flow goes to subfunction A. The timer A is reset in subfunction A and, when it reaches the desired duration (t_1) of buck State 00 or boost State 11, the execution flow comes back to subfunction B.

In both subfunctions, the input current sampling instant is triggered, when necessary, before the switching instant in which the control variables are updated. At the algorithm branches where the current is sampled, after updating the control variables, the predictive model is used to determine the corresponding subinterval durations t_1 or t_2 as can be seen in Fig. 3. First of all, the inductor current slope (m) is calculated following the general expression:

$$m = \frac{v_g - v_o + v_C(1 - u_1 - u_2)}{L_A}. \quad (1)$$

To speed up the slope calculation, as in the case of v_g and v_o, the mean value of intermediate capacitor voltage v_C has been considered instead of its instantaneous value at the sampling instant. The mean value of the intermediate capacitor in steady-state is $v_C = max(v_g, v_o)$, $v_C = v_o$ in boost mode and $v_C = v_g$ in buck mode, so there is no need for sampling v_C.

After calculating the slope, the duration of the subinterval, not calculated in the main program, is predicted in subfunction A as (2) or (3) in subfunction B, so that in steady-state the error between the sampled current and its reference ($i_{ref} - i_g$) becomes zero.

$$t_1 = \frac{i_{ref} - i_g}{m}, t_2 \text{ calculated in the main program} \quad (2)$$

$$t_2 = \frac{i_{ref} - i_g}{m}, t_1 \text{ calculated in the main program} \quad (3)$$

To clarify the algorithm in Fig. 3, temporal evolutions which link the converter current waveform and the algorithm flow in four different steady-state conditions, have been depicted in Fig. 4. These conditions are: buck mode with valley current control, buck mode with peak current control, boost mode with valley current control, and boost mode with peak current control. In each diagram in Fig. 4, the flow of the inner current loop algorithm is associated with the typical stages of a predictive controller: measure, apply, predict and evaluate, and optimize. The Appendix includes detailed information about the mathematical model of the VBB converter and the MPC cost function; both are included in the algorithm shown in Fig. 3.

IV. Simulation and Experimental Results

To test the model predictive control based system, in addition to simulations, a prototype has been built considering a lead-acid battery in the 12 V to 14 V range and a solar PV module MSP-105W with two bypass diodes, whose nominal characteristics are: maximum power $P_{max} = 105$ W, maximum power voltage $V_{mp} = 17.7$ V, maximum power current $I_{mp} = 5.94$ A, open-circuit voltage $V_{oc} = 21.6$ V, short circuit current $I_{sc} = 6.34$ A. In normal operation, an MPP is around 18 V and with the activation of one of the bypass diodes, the new MPP is around 9 V. See Fig. 2 for more details. The buck-boost power converter circuit components are listed in Table I. All the required controllers (inner predictive current control, input voltage regulation and MPPT) have been implemented in a Texas Instruments' TMS320F28335 digital signal controller (DSC). The experimental configuration of the power devices is shown in Fig. 5.

A. Inner loop (current loop)

Figs. 6 and 7 show simulated and experimental responses of the inner loop in both buck and boost modes. In all the experiments, a Chroma 62050H-600S power source (see Fig.5) has been connected at the buck-boost converter input, where a Keysight N5748A dc electronic load configured to emulate the 12-V battery has been connected at its output. Assuming perfect regulation, the input voltage has been adjusted to constant levels of 24 V in buck mode experiments and 6 V in boost mode experiments. The steady-state duty-cycle is 50% and there are no valley-peak transitions. Steady-state responses for references of 2 A are shown in Figs. 6(a) and 6(b) in buck mode and Figs. 7(a) and 7(b) in boost modes.

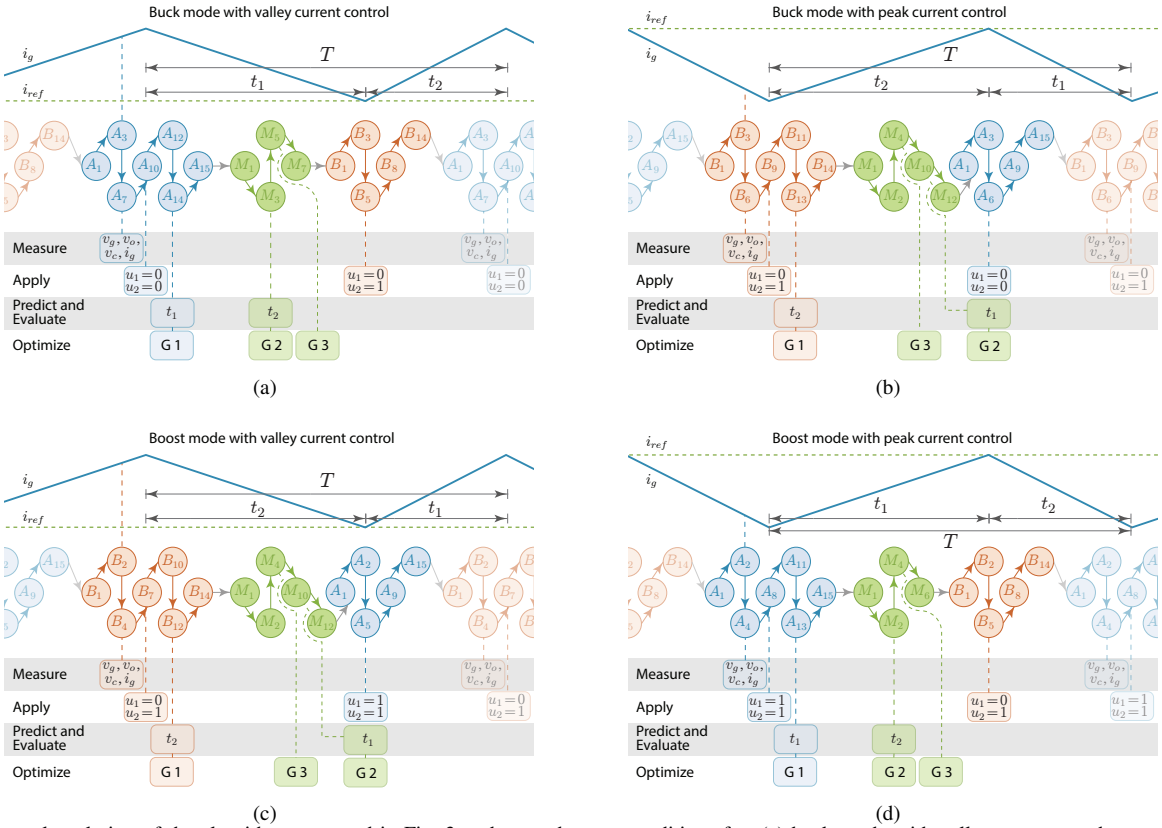

Fig. 4. Temporal evolution of the algorithm presented in Fig. 3 under steady-state conditions for: (a) buck mode with valley current-mode control, (b) buck mode with peak current-mode control, (c) boost mode with valley current-mode control, and (d) boost mode with peak current-mode control.

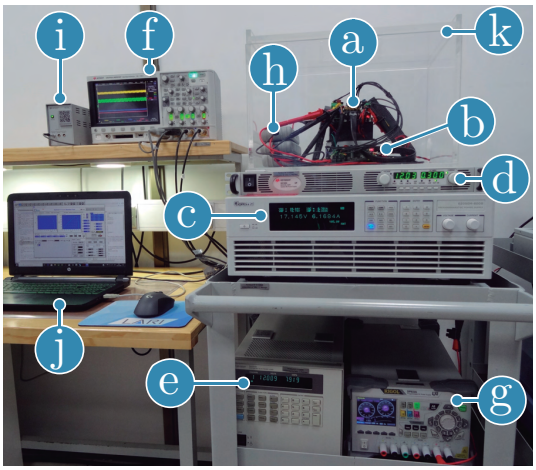

Fig. 5. Experimental configuration for testing the proposed digital current controllers: (a) buck–boost converter, (b) digital signal controller, (c) input dc power supply (Chroma 62050H-600S with programmable solar array simulator), (d) output dc power supply (Keysight N3501A), (e) dc electronic load in constant voltage mode (Keysight N5748A), (f) oscilloscope (Keysight MSOX3104T), (g) auxiliary power supply for DSC, converter current and voltage sensors and MOSFET Drivers, (h) voltage differential probes, (i) power supply for current probe, (j) laptop for programming the DSC, (k) acrylic case for testing circuits.

TABLE I
COMPONENTS OF THE BUCK-BOOST CONVERTER.

Component	Description	Type
Q_1 to Q_4	Power MOSFETs	IRFB4510PBF
L_A	SMD Flat Wire Inductor	74435584700 Wurth Elektronik Inductance: 47 μH DC Resistance: 19.2 $m\Omega$
C	Ceramic Capacitor X7R dielectric	CKG57NX7R2A106M500JH 2 x 10 μF
R_d	Damping Resistor	0.5 Ω, 1 W Vishay WSL2512R5000FEA
C_d	Aluminum Electrolytic Capacitor	100 μF Panasonic EEEFK2A101AM
L	WE-CFWI Coupled Flatwire Inductor	74485540290 Wurth Elektronik Inductance: L_1=L_2=4 x 2.9 μH Turns ratio: 1 : 1 Dc Resistance: R_1=R_2=4 x 5.6 $m\Omega$

Likewise, responses in both modes for a 4-A reference current are depicted in Figs. 6(c), 6(d), 7(c) and 7(d). Also, the response to a step-like current going from 2 A to 4 A is shown in Figs. 6(e), 6(f) in buck mode and Figs. 7(e), 7(f) in boost mode. The traces corresponding to a 4 A to 2 A reference change are shown in Figs. 6(g), 6(h), 7(g) and 7(h). In all cases, there is a good current regulation in steady-state and

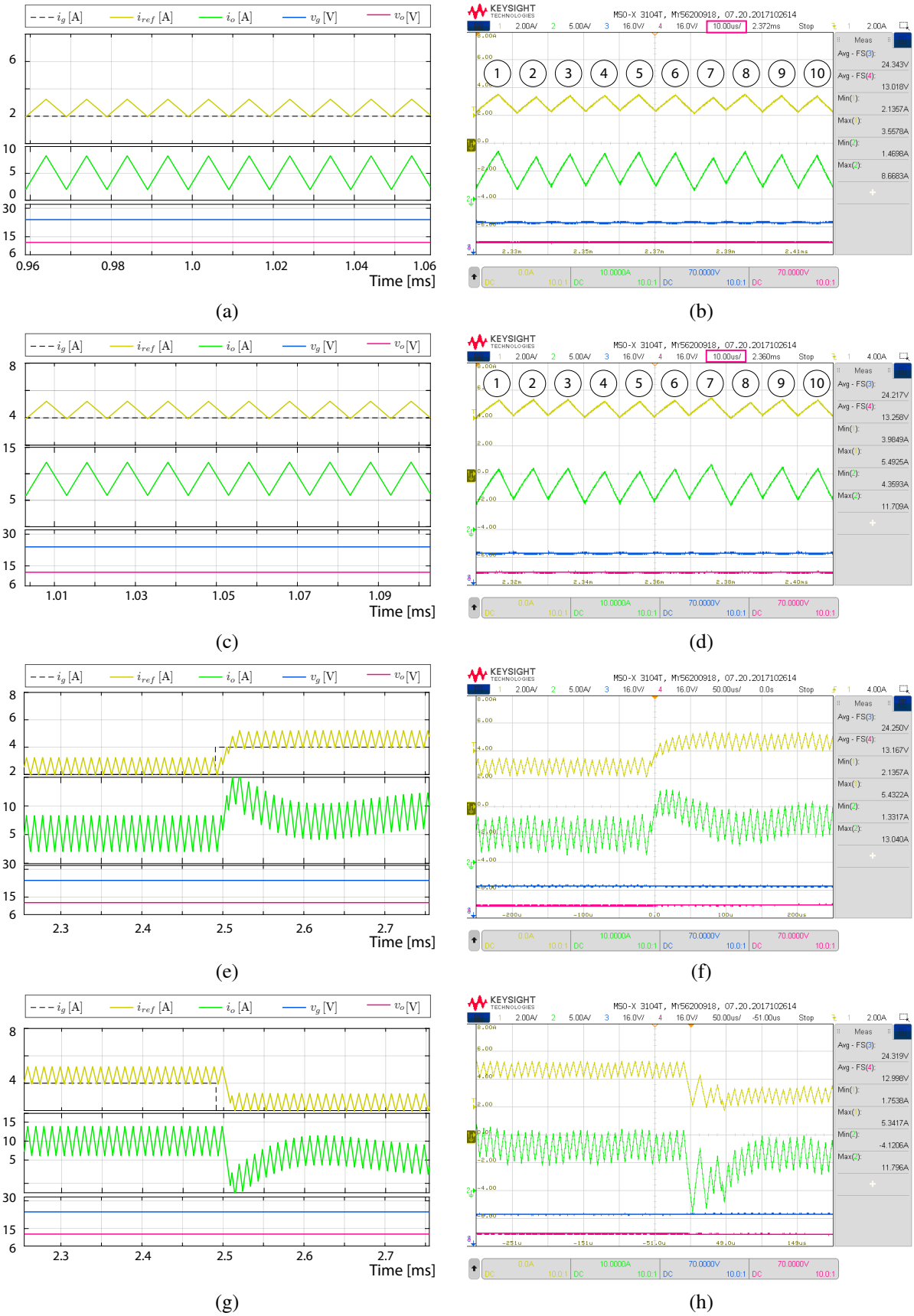

Fig. 6. Simulated (a), (c), (e), (g) and experimental (b), (d), (f), (h) responses of the input current control based on a FCS-MPC strategy when the reference i_{ref}: (a,b) is equal to 2 A, (c,d) is equal to 4 A, (e,f) changes from 2 A to 4 A, and (g,h) from 4 A to 2 A. The converter is operating in buck mode ($V_g = 24$ V and $V_o = 12$ V). CH1: i_g (2 A/div), CH2: i_o (5 A/div), CH3: V_g (16 V/div), CH4: V_o (16 V/div).

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Fig. 7. Simulated (a), (c), (e), (g) and experimental (b), (d), (f), (h) responses of the input current control based on a FCS-MPC strategy when the reference i_{ref}: (a,b) is equal to 2 A, (c,d) is equal to 4 A, (e,f) changes from 2 A to 4 A, and (g,h) from 4 A to 2 A. The converter is operating in boost mode ($V_g = 6$ V and $V_o = 12$ V). CH1: i_g (2 A/div), CH2: i_o (5 A/div), CH3: V_g (16 V/div), CH3: V_o (16 V/div).

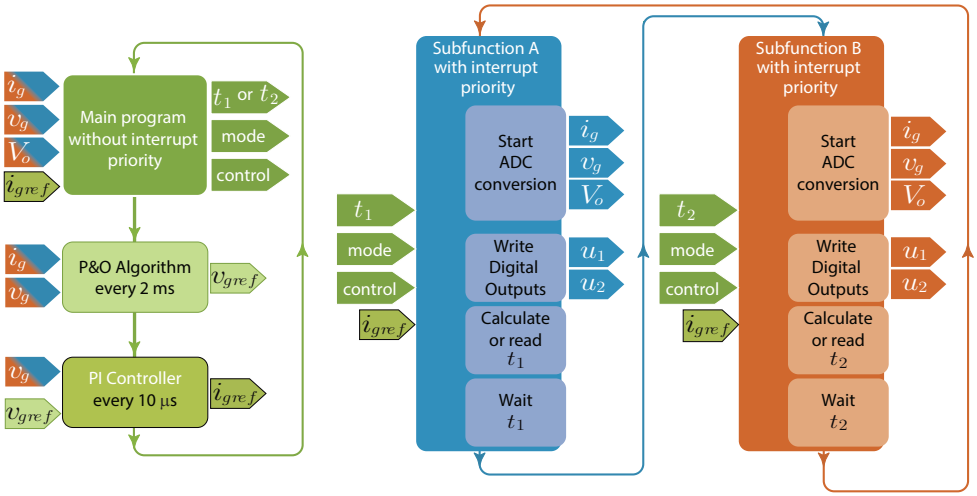

Fig. 8. Main program with the inner current loop states show Fig. 3 with the outer voltage loop and the maximum power point tracking subfunctions.

the new steady-state levels of the input current are achieved quickly and without overshoot. Regarding the output current, there is a slight overshoot during the transitions in buck mode but a much more soft transition in boost mode. In all the results, it is also possible to verify a quasi-constant steady-state switching frequency of 100 kHz as shown in Figs. 6(a), 6(b), 7(a), and 7(b). From these figures, it can be verified that for a total time of 100 μs, a total of 10 current peaks have been recorded, which gives an approximate period of 10 μs per triangular waveform, which is equivalent to a switching frequency of approximately 100 kHz. In addition, Figs. 6 and 7 show a clear valley-mode current control in buck mode and a peak-mode current control in boost-mode. Because of the selected voltage operating points, no operation in valley-mode in boost steady-state operation or peak-mode in buck steady-state operation can be appreciated. Although not shown in the paper, closed-loop PSIM-simulations performed at about the two nominal MPPs candidates (5.8 A at 18 V, and 5.8 A at 9 V) in buck and boost modes have crossover frequencies around 20 kHz (about $1/5$ of the desired steady-state switching frequency of 100 kHz) with phase margins in the 60° to 70° range.

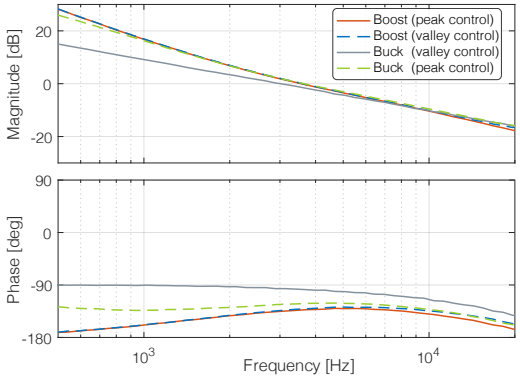

Fig. 9. Outer loop bode plots for buck and boost modes.

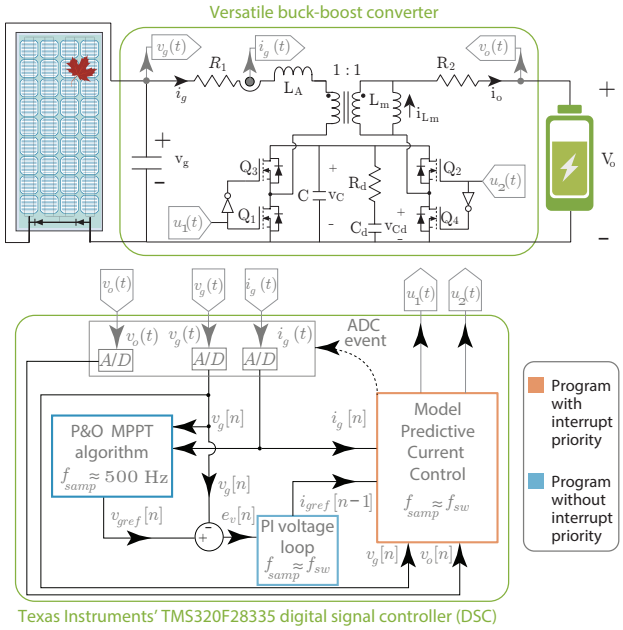

Fig. 10. Block diagram of the digital controller for the MPPT of the VBB converter based on a MPC strategy.

B. Outer loop (voltage loop)

The algorithms to implement the PV module output voltage (input voltage of the power converter), as well as the MPPT have been implemented in the same TMS320F28335 DSC. Fig. 8 shows that both algorithms have been inserted after the main program of the current control. In particular, the voltage regulator has a typical proportional-integral structure whose parameters have been adjusted by simulation. A proportional gain of 2 and a time constant of 80 μs yields crossover frequencies of about 3.5 kHz (about $1/6$ of the inner loop crossover frequency, and about $1/30$ of the switching frequency) with 60° phase margins as can be seen in Fig. 9. See Chapter 9 in [33] for further details on the consequences of these choices. Bode plots shown in this figure have been

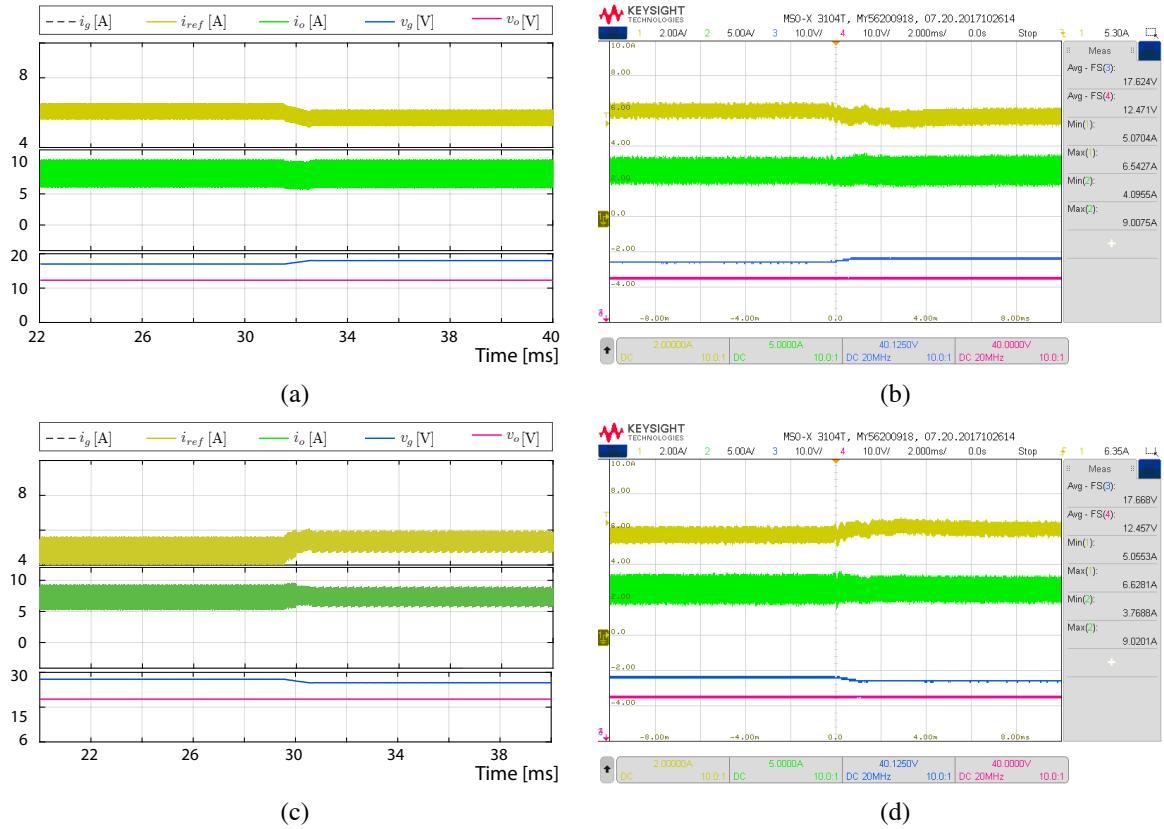

Fig. 11. Simulated (a), (c) and experimental (b), (d) responses of the input current control based on a FCS-MPC strategy when the reference v_{ref}: (a,b) changes from 17 V to 18 V, and (c,d) from 18 V to 17 V. The converter is operating in buck mode ($V_o = 12$ V). CH1: i_g (2 A/div), CH2: i_o (5 A/div), CH3: V_g (10 V/div), CH4: V_o (10 V/div).

simulated in PSIM software. The voltage regulator calculates a new inductor current reference every 10 μs. In addition, Fig. 10 shows a control block diagram that includes an MPPT strategy to obtain the voltage reference for the outer PI control loop, which provides the current reference to the MPC digital current control.

Fig. 11 shows simulated and experimental responses of the voltage loop in buck mode. Responses to voltage variations from 17 V to 18 V are shown in Figs. 11(a) and 11(b), and the transition from 18 V to 17 V are depicted in Figs. 11(c) and 11(d).

Simulated and experimental results in boost mode are shown in Fig. 12. Responses to voltage reference varying from 9 V to 10 V and vice versa are shown in Figs. 12(a), 12(b), 12(c), 12(d). Note that 1-V voltage transitions similar in shape to those of a conventional MPPT algorithm have been selected. As expected, the current transitions caused by the voltage changes are smooth in both buck and boost modes.

C. Maximum power point tracking (MPPT)

Since designing a maximum power point tracking algorithm is not the paper's main goal, a relatively simple non-optimized MPPT algorithm derived from a classical P&O approach has been implemented after the main program of the current loop, as in the case of the voltage regulation loop. Furthermore, it has been configured to provide a new voltage reference for the voltage loop every 2 ms (Fig. 8).

Fig. 13 shows experimental results of the MPP tracking performance under periodic abrupt irradiation changes that result in MPP variations from 50 W to 100 W and vice versa every 5 s. Since the voltage regulation has good bandwidth, the MPPT can have high dynamic performance with an average tracking efficiency of 97 %. Since the voltage coordinates of the MPP are not very sensitive to irradiation changes (they are more sensitive to temperature variations), the output current of the PV module is a square waveform proportional to the power waveform, whose values change between 2.9 A and 5.8 A. As expected, the output voltage at the PV module terminal has an average value of 16.2 V. Note that all waveforms are provided by the PV module emulator Chroma 62050H-600S (Solar Array IV Curve Simulation Softpanel) and are sampled at 500 ms so that the 2 ms MPPT voltage pulses can not be observed because of the undersampling

D. Converter under shading

Fig. 14 shows the experimental performance of the MPPT when an emulated shading that causes the activation of a bypass diode in the PV module is removed. In the interval (40 s $< t <$ 70 s) there is partial shading and, because of the bypass diode activation, the PV module supplies 50 W at about 8 V. The interval is so short that the efficiency provided by

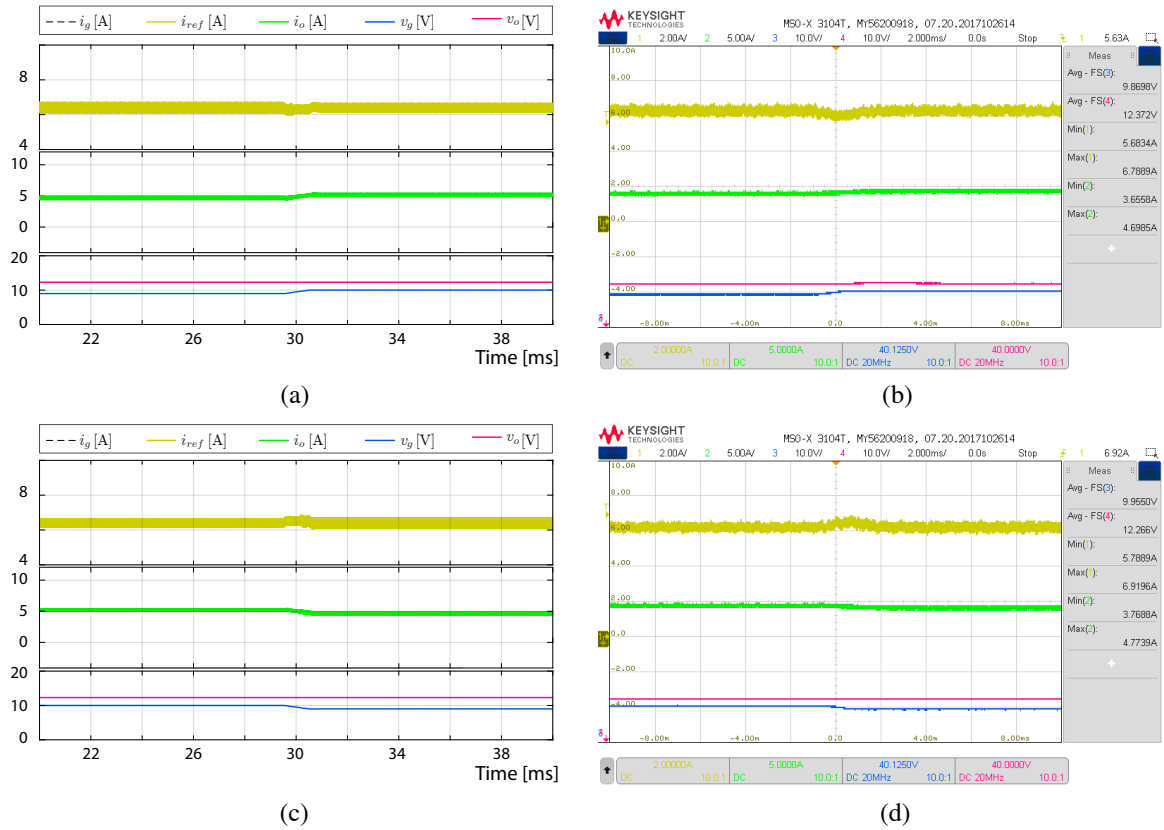

Fig. 12. Simulated (a), (c) and experimental (b), (d) responses of the input current control based on a FCS-MPC strategy when the reference v_{ref}: (a,b) changes from 9 V to 10 V, and (c,d) from 10 V to 9 V. The converter is operating in boost mode ($V_o = 12$ V). CH1: i_g (2 A/div), CH2: i_o (5 A/div), CH3: V_g (10 V/div), CH4: V_o (10 V/div).

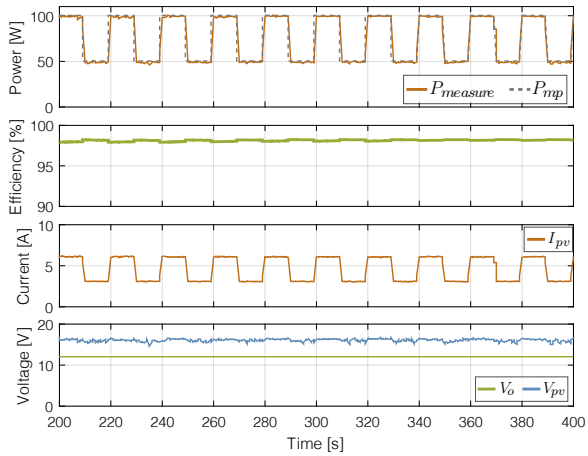

Fig. 13. MPP tracking under irradiance changes. The converter is operating in buck mode.

the PV emulator has not yet arrived at its steady-state value when, at instant $t = 70$ s, the shading disappears. After an intermediate transition of about 4 s, in which the input and output voltages are close, and there are some simultaneous high frequency switching of both buck-boost half-bridges, the converters enter in buck mode ($t > 74$ s). The emulator indicates that the PV module provides about 100 W at an average voltage of 17 V and a current of about 6.1 A (again with undersampled waveforms). Finally, the MPPT efficiency stabilizes at the 96 % level.

V. Conclusions and Future Works

A Model Predictive Control based algorithm has been applied to the inner input current loop of a VBB converter in a stand-alone PV battery charger system. The control algorithm has been implemented so that the three goals of the cost function have been achieved: the current is well regulated, the steady-state switching frequency is the same in buck and boost modes, and despite the small time intervals, the DSC has been able to correctly update the control signals within each switching cycle. A comprehensive set of simulations and experiments have been carried out to verify the correct behavior and performance of all the current loops of the complete PV system: the fast inner current MPC based loop, the PI regulation loop of the PV module voltage, and the slower P&O-based MPPT outer loop. It has been demonstrated that the PV system operates correctly in nominal buck conditions and partial shadow conditions when the activation of the PV module's bypass diodes results in a maximum power point under the battery voltage range and the converter has to operate in boost mode.

Future works will study the application of the designed MPC current strategy to other demanding applications using buck-boost power stages such as single-phase rectifier.

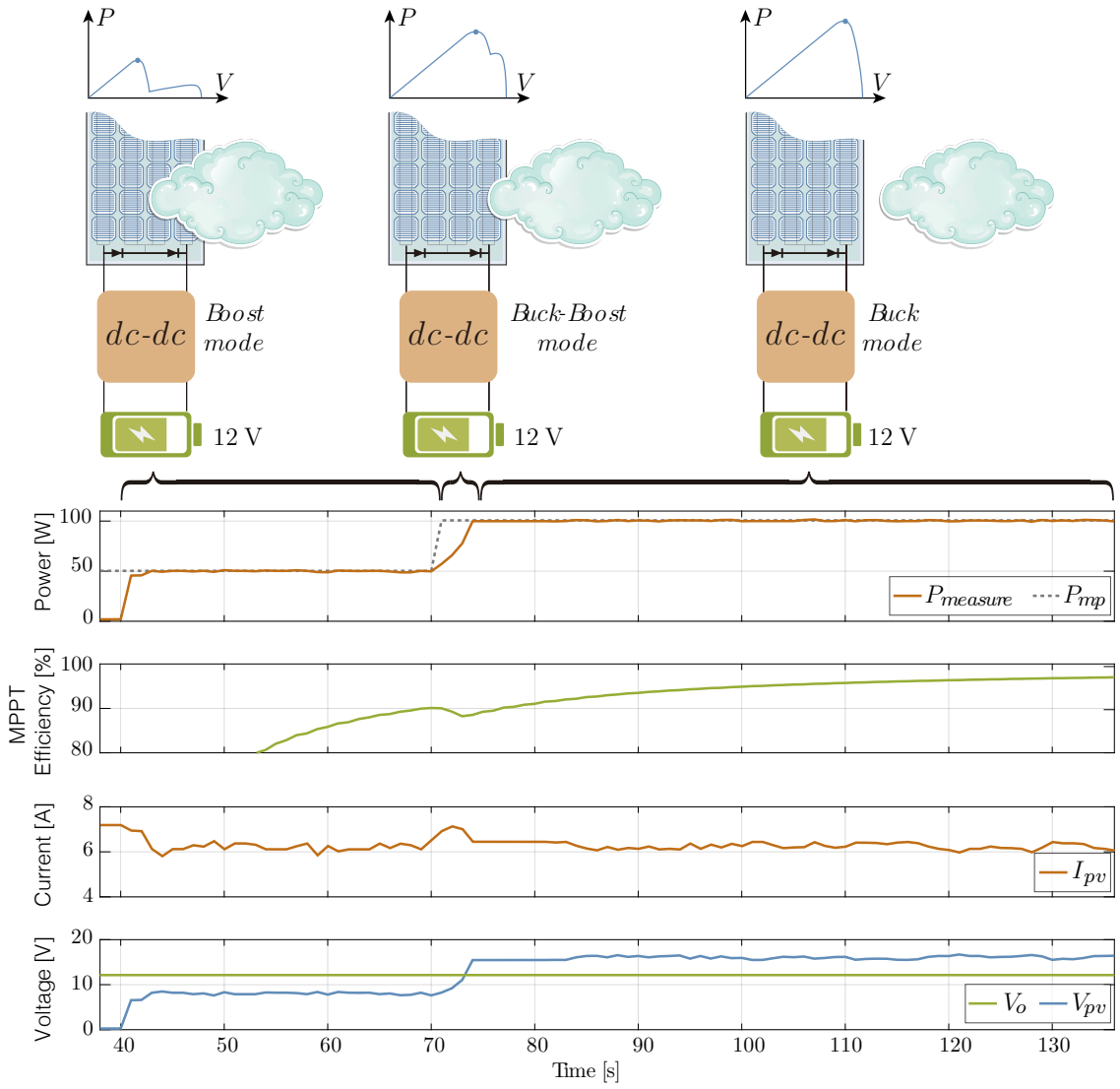

Fig. 14. Converter's performance under shading.

APPENDIX
MODEL PREDICTIVE CURRENT CONTROL OF THE VBB CONVERTER

In this Appendix the MPC current control mathematical formulation is presented based on the works [34], [35]. Let us consider the VBB converter shown in Fig. 1. Applying the fundamental Kirchhoff laws assuming negligible ohmic losses in the inductors, we obtain

$$\frac{di_{L_m}}{dt} = \frac{-v_o + u_2 v_C}{L_m} \tag{A.1}$$

$$\frac{dv_C}{dt} = \frac{-(i_g + i_{L_m})u_2}{C} - \frac{v_C - v_{C_d}}{CR_d} + \frac{(1-u_1)i_g}{C} \tag{A.2}$$

$$\frac{dv_{C_d}}{dt} = \frac{v_C - v_{C_d}}{C_d R_d} \tag{A.3}$$

$$\frac{di_g}{dt} = \frac{v_g - v_p - (1-u_1)v_C}{L_A} \tag{A.4}$$

$$0 = v_o - u_2 v_C - v_p \tag{A.5}$$

where $(u_1, u_2) \in \{0,1\}^2$. In boost mode $u_2 = 1$, while u_1 periodically switches between 0 and 1, whereas in buck mode $u_1 = 0$ and u_2 switches. Assuming that the converter is in steady-state with constant duty cycles U1 and U2, input voltage $v_g(t) = V_g$, and output voltage $v_o(t) = V_o$, equating the right-hand side expressions in (A.1) to (A.4) to zero yields the steady-state conditions in the converter.

$$0 = -V_o + U_2 V_C \tag{A.6}$$

$$0 = -(I_g + I_{L_m})U_2 - \frac{V_C - V_{C_d}}{R_d} + (1-U_1)I_g \tag{A.7}$$

$$0 = V_C - V_{C_d} \tag{A.8}$$

$$0 = V_g - V_p - (1-U_1)V_C \tag{A.9}$$

$$0 = V_o - U_2 V_C - V_p \tag{A.10}$$

Substituting V_p in (A.11) into (A.9) yields:

$$V_o - U_2 V_C = V_g - V_p - (1-U_1)V_C. \tag{A.11}$$

Substituting the steady-state expression of the capacitor voltage V_C of (A.6) into (A.11), the following voltage conversion ratio $M(U1, U2)$ is obtained:

$$M(U_1, U_2) \equiv \frac{V_o}{V_g} = \frac{U_2}{1 - U_1} \tag{A.12}$$

From the voltage conversion ratio (A.12) is possible to calculate the duration of the ON state and the duration of the OFF state of each operation mode as they are listed in Table II.

TABLE II
ON STATE AND OFF STATE DURATIONS OF THE VBB CONVERTER

Operation mode	t_{on}	t_{off}
Buck ($U_1 = 0$)	$T\left(1 - \frac{V_o}{V_g}\right)$	$T\left(\frac{V_o}{V_g}\right)$
Boost ($U_2 = 1$)	$T\left(1 - \frac{V_g}{V_o}\right)$	$T\left(\frac{V_g}{V_o}\right)$

where T is the quasi-constant steady-state switching period and it must be fulfilled that $T \approx t_{on} + t_{off}$. Therefore, from Table II is possible to calculate the required time duration of t_{on} or t_{off} to keep a quasi-constant steady-state switching frequency. These time durations correspond with the variables t_1 and t_2 presented in the main program shown in Fig. 3.

On the other hand, substituting (A.5) into (A.4) the expression for the inductor current slope can be isolated as:

$$\frac{di_g}{dt} = \frac{v_g - (1 - u_1)v_C - v_o + u_2 v_C}{L_A}. \tag{A.13}$$

This inductor current slope serves as the basis for designing predictive control and matches the general expression (1). This inductor current has a triangular waveform with two subintervals within which the current is rising with a slope m_1 as well as one within which the current is falling with a slope $-m_2$. The current slope for each converter operation mode and subinterval are listed in Table III.

TABLE III
SLOPE OF THE INDUCTOR CURRENT WAVEFORM VBB CONVERTER

Operation mode	m_1 (during t_{on})	$-m_2$ (during t_{off})
Buck ($u_1 = 0$)	$\frac{V_g - V_o}{L_A}$	$\frac{V_g - v_C - V_o}{L_A}$
Boost ($u_2 = 1$)	$\frac{V_g + v_C - V_o}{L_A}$	$\frac{V_g - V_o}{L_A}$

The objective is to control the input current i_g without steady-state error (control goal G1) but considering additional operation requirements, which are quasi-constant steady-state switching frequency while ensuring high switching frequency. A way to accomplish these objectives is to solve at each step, the following optimization problem:

$$\begin{aligned}
\underset{t_1, t_2}{\text{minimize}} \quad & (\mid i_g + t_1 m_1 - i_{ref} \mid + \mid t_2 m_2 - t_{off} m_2 \mid) \cdot \\
& \quad min(t_2 \leq t_{max}, 1) \; + \\
& (\mid i_g + t_2 m_2 - i_{ref} \mid + \mid t_1 m_1 - t_{on} m_1 \mid) \cdot \\
& \quad min(t_2 > t_{max}, 1) \\
\text{subject to} \quad & T \approx t_1 + t_2, \\
& t_1 \in \{0, T\}, \\
& t_2 \in \{0, T\}
\end{aligned}$$

where, depending on the converter operation mode, buck or boost, current slopes m_1 and m_2 corresponds with the listed in Table III and the ON and OFF durations (t_1 and t_2) are listed in Table II. In addition, parameter t_{max} allows deciding to toggle between peak-mode or valley-mode current control to ensure maximum calculation time for the control law (control goal G3). Finally, the optimization constraint ensures a quasi-constant steady-state switching period T of 10 μs corresponding with a switching frequency of 100 kHz (control goal G2).

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