Discretized Discontinuous Modulation Strategy for Cascaded H-Bridge StatCom

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***Abstract*—This paper proposes a discontinuous modulation (DM) scheme for cascaded H-bridge (CHB) static compensators (StatComs) with star configuration. The proposed DM scheme guarantees zero steady-state active power in each converter phase-arm, even in the presence of severe grid imbalance conditions, thus remaining decoupled from the inter-phase capacitor voltage balancing controller. Moreover, the proposed DM scheme exploits the possibility of clamping to the zero-voltage level, thus providing a more flexible discontinuous operation than conventional DM methods. This involves lower zero-sequence-voltage injection requirements and lower switching losses. The proposed modulation scheme is experimentally corroborated and its performance under different grid voltage conditions is compared with traditional modulation schemes.**

***Index Terms*—Cascaded H-bridge (CHB), discontinuous modulation (DPWM), inter-phase balancing, static compensator (STATCOM), voltage sag, zero-sequence voltage.**

I. Introduction

Static synchronous compensators (StatComs) are well-known devices for grid voltage regulation [1]-[4]. Among different circuit topologies to implement StatComs, the cascaded H-bridge (CHB) converter has been widely adopted due to its modularity, which allows direct connection to a high-voltage electrical network even though the power semiconductors are sized for relatively low blocking voltages [5]-[8]. The aim of obtaining converters with high-efficiency levels is a strong driving force to develop modulation strategies that minimize the number of switching events. In particular, discontinuous modulation (DM) schemes represent an attractive solution where the converter is operated by intentionally clamping the ac-side voltages to their respective dc-rails [9]-[11].

In three-phase systems with star configuration, DM is achieved by injecting a zero-sequence voltage (ZSV). Determining the clamping phase-arm at any time instant is done based on desired control objectives (normally to minimize the switching losses). The clamped converter phase-arm ceases switching and, consequently, the average switching frequency of the converter can be reduced by a third. The DMs discussed in [9]-[11] consider two-level three-phase voltage source inverters (VSIs) with a common dc-link voltage. Therefore, the instantaneous power generated in each phase-arm by the injected ZSV cancels out in the converter dc-side, thus it remains decoupled from the rest of the control system.

Unlike in VSIs with a common dc-link, the dc-side of each phase-arm in CHB StatComs is implemented with multiple floating capacitors that are regulated and balanced via a closed-loop controller to guarantee stable operation [12], [13]. In the CHB converters, as the dc-link is distributed, the instantaneous power generated in each phase-arm by the injected ZSV is directly transferred to the respective dc-sides. Thus, during unbalanced grid conditions, the injected ZSV affects the capacitor voltages and, in turn, interferes with the inter-phase balancing controller. This phenomenon is particularly noteworthy under strong unbalanced grid voltage conditions, since the required ZSV for DM contains a significant fundamental-frequency component. The DMs in [9]-[11] do not consider inter-phase balancing effects since they are developed for VSIs with a common dc-link, and hence they are not suitable for CHB StatComs. In [14], a DM strategy for CHB StatComs is reported. Several advantages of using DM in CHB StatComs are discussed, but the coupling effects with inter-phase balancing control while operating under unbalanced grid voltage conditions is overlooked.

A problem with a similar nature appears in neutral-point-clamped (NPC) converters as the dc-side consists of two capacitors that have to be balanced [15]-[16]. A DM strategy that selects positive- or negative-ZSV depending on the sign of the neutral-point current and the difference between the two capacitor voltages is proposed in [15]. Approaches in [16] and [17] improve the conventional 60° DM (named as DPWM1 in [9]-[11], and referred to as conventional DM henceforth) for its application in the NPC converter. Particularly, the width of the injected positive- and negative-ZSV pulses is inversely adjusted by processing the difference between the

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two capacitor voltages with a proportional controller [16] or by a hysteresis controller [17]. The above methods are not directly applicable to CHB StatComs because of their topological differences, specifically, CHB StatComs have floating capacitors on three individual phase-arms that need to be balanced. Nevertheless, the applied concept to simultaneously achieve voltage balancing and DM in the NPC converters inspires to develop a similar concept for the CHB converters.

This paper identifies and studies the effect of DM on the inter-phase voltage balance of CHB StatComs. The paper proposes a DM scheme for the CHB StatComs that, unlike the conventional DM, does not affect the inter-phase capacitor voltage balance, thus enhancing the converter operation, particularly in the presence of severe grid voltage imbalances. Furthermore, the proposed DM allows clamping to the zero-voltage level, which helps to reduce the root mean square (rms) value of the injected ZSV, and therefore, the capacitor voltage waveforms are less affected. Besides, as clamping to the zero-voltage level occurs when the corresponding phase-arm current is at its peak value, lower switching losses are achieved compared to the conventional DM.

The rest of the paper is organized as follows. Section II revisits the background of CHB StatComs with star configuration, and introduces the proposed control technique. Section III discusses the drawbacks of the conventional DM in CHB StatComs. Then, the proposed DM is introduced as a solution. Experimental results in Section IV compare the performance of the proposed DM with the conventional CM and DM strategies under different unbalanced grid voltage conditions. Section V compares switching losses of the proposed DM with the conventional CM and DM strategies. Finally, Section VI concludes the paper.

II. CHB StatComs with Star Configuration

This section revisits the main circuit relationships in CHB StatComs and introduces the proposed control technique.

A. Main Circuit Relationships

The star-connected CHB StatCom topology is presented in Fig. 1. Each phase-arm of the CHB converter consists of n H-bridge submodules (SMs). The positive ac-side terminals of the converter phase-arms, (a), (b) and (c), are connected to the point of common coupling (PCC) grid voltages $v_{g,a}$, $v_{g,b}$ and $v_{g,c}$ through filtering impedances (L_g, R_g). The dc-side of each H-bridge SM consists of a capacitor with capacitance C. In the star configuration, a ZSV v_Z appears between the ground (neutral point of the grid) and the neutral point of the converter, as Fig. 1 shows.

In the averaged model, the dc- and ac-side SM voltages are related by the modulating signals $\delta_{xj} \in [-1, 1]$ as:

$$\delta_{xj} = \frac{v_{xj}}{v_{dc,xj}}, \tag{1}$$

where $v_{dc,xj}$ and v_{xj} are the dc- and ac-side SM voltages, respectively ($x \in \{a, b, c\}$ refers to the phase-arm index, and $j \in \{1, \cdots, n\}$ refers to the SM index within the phase-arm).

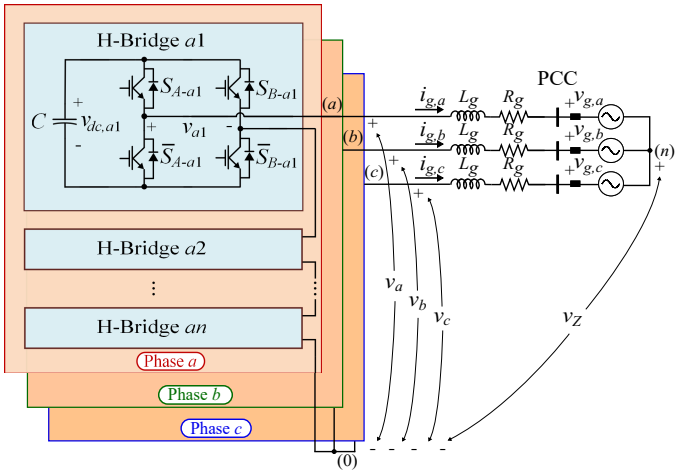

Fig. 1. Circuit diagram of a three-phase CHB StatCom with star configuration.

The total dc- and ac-side converter voltages are defined as the per-phase-arm sum of the respective individual voltages, i.e., $v_{dc,x} = \sum_{j=1}^{n} v_{dc,xj}$ and $v_x = \sum_{j=1}^{n} v_{xj}$, respectively.

In this paper, the ZSV is defined as follows:

$$v_Z = v_{Zb} + v_{Zd}. \tag{2}$$

where v_{Zb} is a continuous component for inter-phase balancing [12], [13], and v_{Zd} is a piecewise continuous component for discontinuous operation.

Similarly, the total ac-side converter voltages v_x can be decomposed as follows:

$$v_x = v'_x + v_{Zd}, \tag{3}$$

where, according to Fig. 1,

$$v'_x = v_{g,x} + L_g \frac{di_{g,x}}{dt} + R_g i_{g,x} + v_{Zb}, \tag{4}$$

is a continuous voltage waveform since the grid voltages $v_{g,x}$ and grid currents $i_{g,x}$ are sinusoidal.

Note that when using a continuous modulation (CM), $v_{Zd} = 0$. Also, note that v_{Zb} is negligible under balanced grid conditions. However, when grid imbalances occur, v_{Zb} is a fundamental-frequency voltage that guarantees zero active power in each converter phase-arm [12], [13].

Assuming inter-SM capacitor voltage balance, i.e., $v_{dc,xj} = v_{dc,x}/n$ for every j, the dc-link voltages dynamics correspond to:

$$\frac{C}{2n} \frac{dv_{dc,x}^2}{dt} = -v_x i_{g,x}, \tag{5}$$

where it can be observed that v_{Zd} directly affects the dc-link voltages, according to (3).

The modulation index of each converter phase-arm is defined as

$$M_{a,x} = \frac{V'_x}{V_{dc,x,max}}, \tag{6}$$

where V'_x and $V_{dc,x,max}$ represent the amplitude of v'_x and the peak of $v_{dc,x}$, respectively.

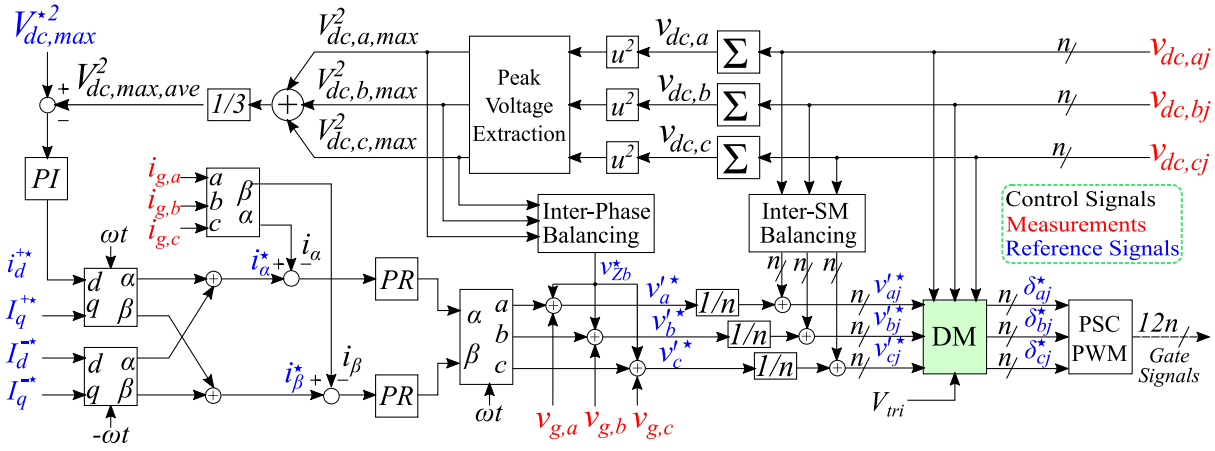

Fig. 2. Overview of the CHB StatCom control scheme with peak capacitor voltage regulation.

B. Control Implementation

Fig. 2 shows the closed-loop control block diagram adopted in this paper. It is based on a conventional hierarchical approach where the grid currents are regulated in α-β frame, using two proportional-resonant (PR) controllers, and grid voltage feedforward loops [18]. This controller allows the StatCom to operate in the event of unbalanced grid conditions. Superscripts $+$ and $-$ represent the positive- and negative-sequence components, and subscripts d and q stand for the d- and q-components, respectively (the amplitude conservative dqz-transformation is used in this paper).

The current references $I_q^{+\star}$, $I_d^{-\star}$, $I_q^{-\star}$ are given by an upper level controller, while reference $i_d^{+\star}$ is calculated to compensate for system losses by processing the error between the average peak square dc-link voltages, i.e., $V^2_{dc,max,ave} = 1/3 \sum_{x=a,b,c} V^2_{dc,x,max}$, and the reference $V^{\star 2}_{dc,max}$, using a proportional-integral (PI) controller [19], [20]. $V_{dc,x,max}$ is obtained in the Peak Voltage Extraction block using a second-order generalized integrator (SOGI) filter [19].

The Inter-Phase Balancing block in Fig. 2 calculates $v^{\star}_{Zb}$ by processing the differences between the per-phase-arm peak square dc-link voltages ($V^2_{dc,a,max}$ and $V^2_{dc,b,max}$) and the average value $V^2_{dc,max,ave}$ using two PI controllers [12]. Reference $v^{\star}_{Zb}$ is then added to the current controller outputs.

The Inter-SM Balancing block calculates incremental voltages that are added to the references $v'^{\star}_x/n$ [21] to achieve capacitor voltage balance within a phase-arm. Each incremental voltage is calculated by multiplying the output of a PI with the respective current $i_{g,x}$. Each PI processes the difference between individual capacitor voltage $v_{dc,xj}$ and the average value $v_{dc,x}/n$.

The DM block calculates $v^{\star}_{Zd}$ for discontinuous operation according to the controller outputs and measured capacitor voltages. The design and implementation of this block is the main contribution of this paper and is described in the next section.

III. ZSV Injection for DM

A. DM Principle

According to (3), at any time instant, the converter voltage v_x can be clamped to either its positive ($v_{dc,x}$) or negative ($-v_{dc,x}$) dc-link voltage by injecting a positive-ZSV (PZSV) or a negative-ZSV (NZSV), respectively. The PZSV and NZSV for phase-arm x are denoted as $v_{Zd,xp}$ and $v_{Zd,xn}$, respectively, and correspond to

$$\begin{cases} v_{Zd,xp} & = v_{dc,x} - v'_x, \\ v_{Zd,xn} & = -v_{dc,x} - v'_x. \end{cases} \tag{7}$$

Note that according to (1), when the converter phase-arm x is clamped, $|v_x/v_{dc,x}| = 1$.

To prevent the injected ZSV from causing overmodulation in other phase-arms, the selection of PZSV and NZSV must agree with the following criterion:

$$\begin{cases} v_{Zd,p} & = \min\{v_{Zd,xp}\}, \\ v_{Zd,n} & = \max\{v_{Zd,xn}\}. \end{cases} \tag{8}$$

B. Conventional DM

Under the conventional DM, v_{Zd} is chosen as the minimum magnitude clamping bound, i.e.,

$$v_{Zd} = \begin{cases} v_{Zd,p} & \text{if } v_{Zd,p} < -v_{Zd,n}, \\ v_{Zd,n} & \text{otherwise.} \end{cases} \tag{9}$$

According to (9), the converter phase-arms are clamped by only comparing the magnitudes of $v_{Zd,p}$ and $v_{Zd,n}$.

Fig. 3 shows the waveform and frequency spectrum of v_{Zd} when (9) is implemented. A sampling frequency of 10 kHz and a frequency spacing of 0.5 Hz have been considered to perform the fast Fourier transform (FFT) analysis of v_{Zd}. Using lower sampling frequencies does not significantly affect the harmonic amplitudes within the baseband region of v_{Zd}. Different grid voltage conditions are considered. Particularly, Fig. 3(a) shows a nominal grid condition with converter modulation indices $M_a = 0.9$. Figs. 3(b), (c) and (d) show cases of one-phase,

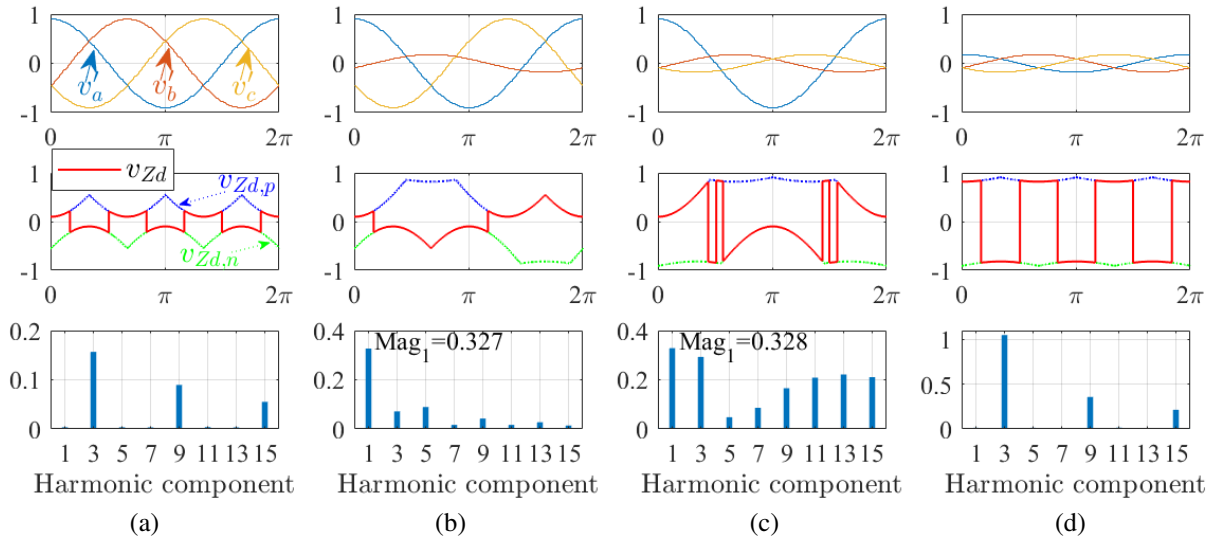

Fig. 3. Waveforms when using a conventional DM under different grid conditions. (a) Balanced and rated PCC grid voltages with $M_a = 0.9$, (b) grid voltage $v_{g,b}$ drops to 20%, (c) grid voltages $v_{g,b}$ and $v_{g,c}$ drop to 20%, and (d) three-phase grid voltages drop to 20%.

two-phase and three-phase grid voltage drops, respectively. For the sake of illustration, voltage drops in the inductors are neglected, and the three-phase capacitor voltages are regarded as constant and balanced. In Figs. 3 and 4, all the voltages are normalized with respect to the capacitor voltages.

As it can be observed in Figs. 3(a) and (d), under balanced grid voltage conditions, the injected v_{Zd} only contains triplen harmonics (the odd multiples of third harmonics), due to the three-phase symmetry among converter voltages, and thus it does not create any net power during a fundamental period T_g, i.e.,

$$\frac{1}{T_g}\int_0^{T_g} v_{Zd} i_{g,x} dt = 0, \tag{10}$$

for every converter phase-arm. Consequently, the capacitor voltages will not diverge due to v_{Zd} and, hence, the Inter-Phase Balancing block is not affected.

On the other hand, when asymmetric grid voltage conditions emerge, as in Figs. 3(b) and (c), v_a', v_b' and v_c' are unbalanced and, as a result, the clamping periods are no longer 60° each. This involves that v_{Zd} could contain a significant fundamental-frequency component, as the frequency spectra in Figs. 3(b) and (c) show, which affects the inter-phase balancing, since (10) does not hold. Specifically, the magnitude of the fundamental-frequency component in Figs. 3(b) and (c) is approximately one-third of the nominal value. This unwanted nonnegligible coupling between the Inter-Phase Balancing block and the DM block in Fig. 2 is a drawback of the conventional DM and should be minimized to improve the DM performance.

One more important drawback of the conventional DM is the relatively large magnitude of v_{Zd} needed when the grid voltages are low, as Figs. 3(b), (c) and (d) show. This is because the conventional DM was proposed for two-level VSIs where the converter voltages can only be clamped to {+1, -1}. However, in the CHB StatCom, the converter voltages can also be clamped to zero, thus adding an extra degree of freedom to minimize v_{Zd} injection. Note that large v_{Zd} magnitudes significantly affect the capacitor voltage waveforms according to (5), which is not desirable.

C. Proposed Discretized DM

The proposed discretized DM (DDM) addresses the two aforementioned drawbacks of the conventional DM by i) mitigating the interaction with the Inter-Phase Balancing loop and ii) reducing the magnitude of v_{Zd}.

According to (3), the converter voltages can be clamped to zero by injecting a ZSV $v_{Zd} = -v_x'$. Note that this clamping option becomes practical as v_x' amplitude decreases, or equivalently, when the grid voltage v_{gx} amplitude decreases, according to (4). Considering the zero-voltage level involves modifying $v_{Zd,p}$ and $v_{Zd,n}$ in (8) as follows:

$$\begin{cases} v_{Zd,p} & = \min\left\{ v_{Zd,xp}, v_{Zd,x0p} \right\}, \\ v_{Zd,n} & = \max\left\{ v_{Zd,xn}, v_{Zd,x0n} \right\}. \end{cases} \tag{11}$$

where the two virtual states $v_{Zd,x0p}$ and $v_{Zd,x0n}$ correspond to:

$$\begin{cases} v_{Zd,x0p} = \infty, \ v_{Zd,x0n} = -v_x' & \text{if } v_x' \geq 0, \\ v_{Zd,x0p} = -v_x', \ v_{Zd,x0n} = -\infty & \text{otherwise.} \end{cases} \tag{12}$$

The proposed DDM uses the two clamping candidates given by (11), i.e., $v_{Zd,p}$ and $v_{Zd,n}$, to generate a v_{Zd} with average zero within a small discretization interval T_d. Specifically, during T_d, the time fraction $D_d T_d$ corresponds to the injection of PZSV $v_{Zd,p}$, while the complementary time fraction $(1 - D_d) T_d$ corresponds to the injection of NZSV $v_{Zd,n}$, i.e.,

$$\begin{aligned} &\int_0^{T_d} v_{Zd} i_{g,x} dt \\ &= \int_0^{D_d T_d} v_{Zd,p} i_{g,x} dt + \int_{D_d T_d}^{T_d} v_{Zd,n} i_{g,x} dt = 0, \end{aligned} \tag{13}$$

where $D_d \in [0, 1]$ denotes duty cycle.

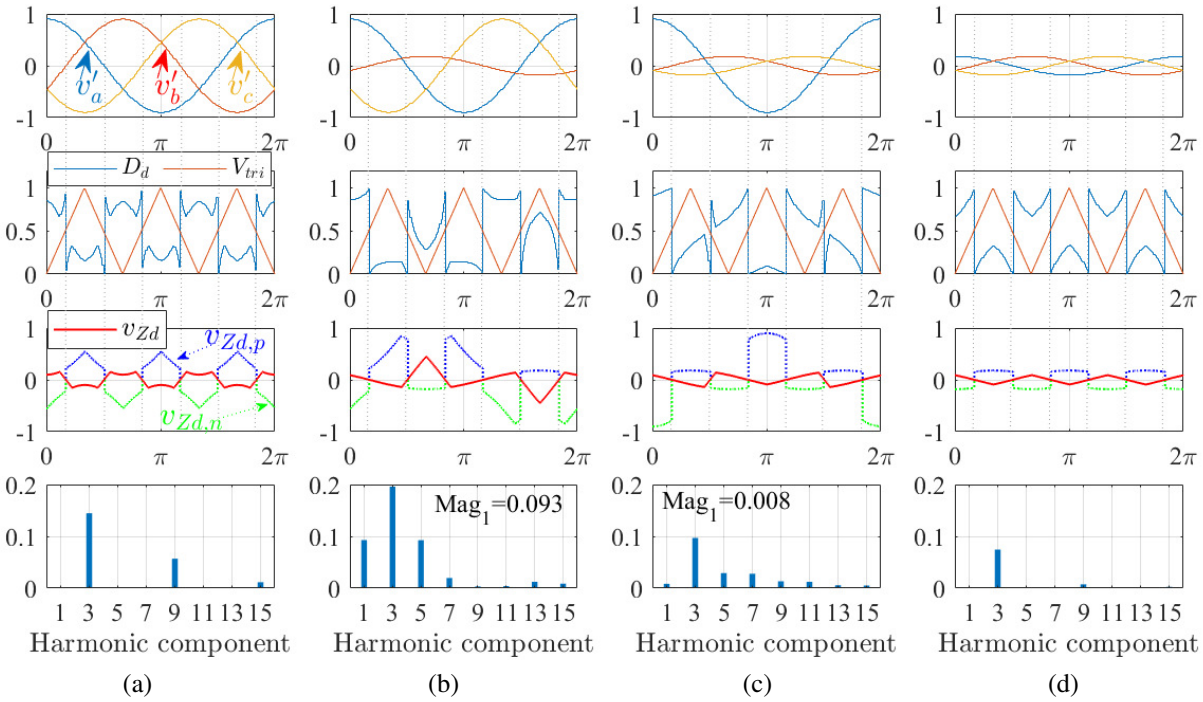

Fig. 4. Waveforms when using the proposed DDM under different grid conditions. (a) Balanced and rated PCC grid voltages with modulation index $M_a = 0.9$, (b) grid voltage $v_{g,b}$ drops to 20%, (c) grid voltages $v_{g,b}$ and $v_{g,c}$ drop to 20%, and (d) three-phase grid voltages drop to 20%.

Note that for small enough T_d, (13) can be approximated as:

$$D_d v_{Zd,p} + (1 - D_d)\, v_{Zd,n} = 0. \tag{14}$$

Obviously, the smaller T_d is, the more accurate (14) becomes. However, small T_d implies more switching events. To have a relatively fair comparison between the proposed DDM and the conventional DM in terms of the number of switching events, $T_d = T_g/3$ is used in this paper.

According to (14), D_d corresponds to,

$$D_d = \frac{v_{Zd,n}}{v_{Zd,n} - v_{Zd,p}}. \tag{15}$$

Comparing D_d with a triangular carrier waveform, V_{tri}, of frequency $1/T_d$ and range $[0, 1]$, the following definition for v_{Zd} is proposed:

$$v_{Zd} = \begin{cases} v_{Zd,p} & \text{if } D_d > V_{tri}, \\ v_{Zd,n} & \text{otherwise.} \end{cases} \tag{16}$$

Fig. 4 illustrates the main waveforms of the CHB StatCom when the proposed DDM is implemented. The same grid conditions as in Fig. 3 are considered for the sake of comparison. As shown in Fig. 4(a), under nominal grid condition, the frequency spectrum of v_{Zd} under DDM and the conventional DM are very similar. However, when grid voltage imbalances occur, as Figs. 4(b) and (c) depict, the proposed DDM strategy creates a v_{Zd} dominated by a third-harmonic component (since the frequency of V_{tri} has been chosen according to $T_d = T_g/3$), with fundamental component magnitudes well below 10% of the nominal value. Note that

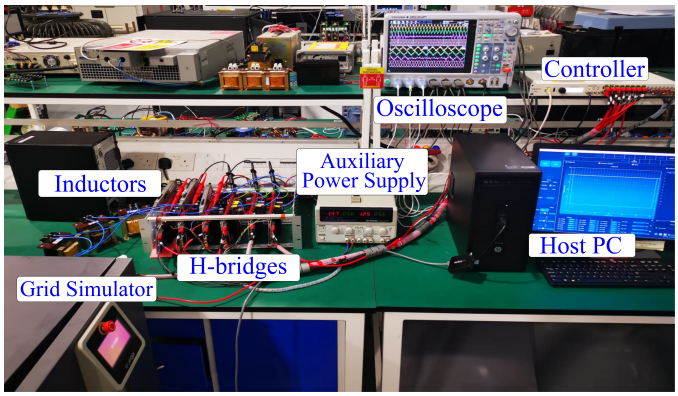

Fig. 5. Experimental setup.

$T_d < T_g/3$ would lead to even lower fundamental voltage magnitudes. In comparison with the conventional DM results in Fig. 3, the fundamental component of v_{Zd} is reduced by more than 70% when the grid voltage of one phase drops, and by more than 95% when two phases experience voltage drops. Moreover, other harmonic magnitudes of v_{Zd} under DDM are also reduced due to the zero-voltage level clamping. For example, the magnitude of the third harmonic of v_{Zd} is reduced by more than 65% when two grid voltages drop, and by more than 90% when three grid voltages drop.

IV. Experimental Results

In this section, experimental results are presented to show the effectiveness of the proposed DDM under various grid voltage conditions. The CHB StatCom prototype used for

TABLE I
EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
PCC grid voltage nominal amplitude, V_g	$100\sqrt{2}$ V
Nominal reactive power, Q	2.5 kVAr
Grid angular frequency, ω	100π rad/s
Carrier frequency, f_{sw}	5 kHz
SMs in each phase-arm, n	2
Peak dc-link voltage, $V_{dc,max}$	$1.3V_g$
Capacitance per H-bridge, C	1 mF
Filter inductance, L_g	2 mH

experimental validation consists of two IMPERIX PEH2015 H-bridge converters on each phase-arm. The PCC grid voltages are provided by a GL&EL 15-kVA CINERGIA grid emulator. A B-Box RCP 3.0 from IMPERIX has been used to implement the control shown in Fig. 2. The experimental setup is shown in Fig. 5, and the system parameters are given in Table I. The capacitors have been sized to provide approximately 15% twice-fundamental-frequency capacitor voltage oscillations at the rated operating condition (considering a CM strategy).

Four different cases are studied to evaluate features of the proposed DDM. ***Case I***: Transient operation under balanced PCC grid voltages, ***Case II***: Single-phase 100% grid voltage sag, ***Case III***: Two-phase 100% grid voltage sag, and ***Case IV***: Three-phase 80% grid voltage sag.

Case I: Balanced PCC Grid Voltages

Fig. 6 presents the capacitor voltage and grid current waveforms under the proposed DDM for different current transitions. Particularly, Fig. 6(a) presents a transition from $1/3$ p.u. to 1 p.u. positive-sequence capacitive current, Fig. 6(b) depicts a transition from 1 p.u. positive-sequence capacitive current to 1 p.u. positive-sequence inductive current, and Fig. 6(c) shows a transition from balanced current operation to unbalanced current operation ($I_d^- = 0.1$ p.u. and $I_q^- = 0.1$ p.u.) when the StatCom is delivering 1 p.u. positive-sequence capacitive current.

As it can be observed, the proposed DDM is able to keep the capacitor voltages well regulated and balanced. Moreover, the different current transitions show fast current responses with settling times below 5 ms. These results demonstrate the effectiveness of the proposed DDM to cope with different grid current requirements.

Case II: One-Phase 100% Voltage Sag

Fig. 7 presents the capacitor voltage and grid current waveforms under the CM, the conventional DM and the proposed DDM, when the grid voltage $v_{g,b}$ experiences a 100% sag, from $t = 0.025$ s to $t = 0.325$ s. As shown, the grid current waveforms are barely affected under these modulation strategies both during the voltage sag occurrence and its restoration. Furthermore, balanced sinusoidal grid currents are delivered during the whole voltage sag period. Despite the similar current waveforms, it is important to point out the noticeable differences in the capacitor voltages evolution. Specifically,

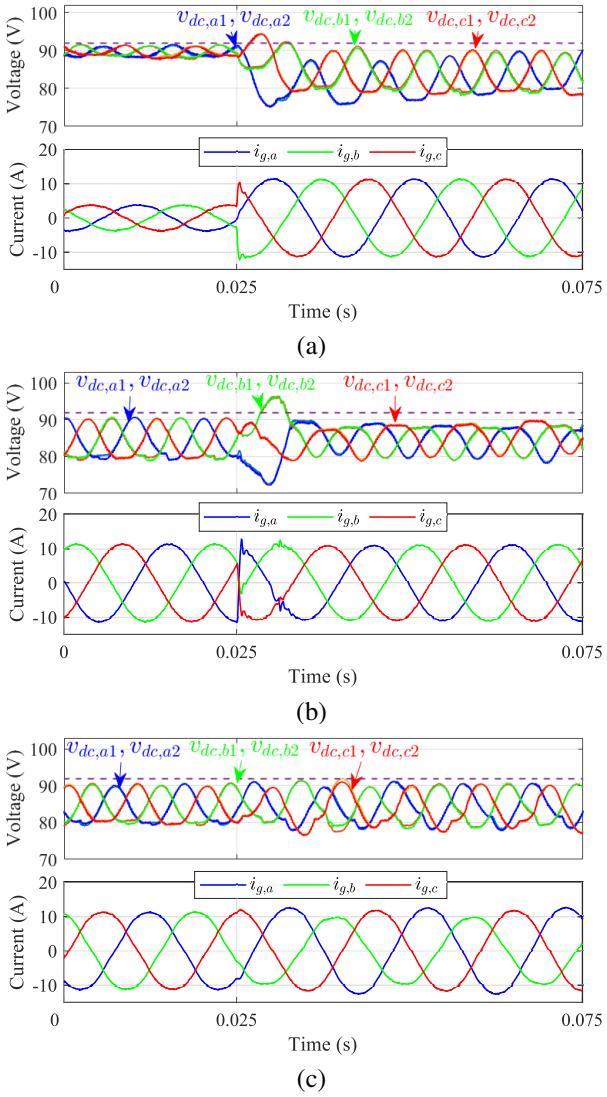

Fig. 6. ***Case I***: DDM experimental waveforms for different current transitions at $t = 0.025$ s under balanced grid voltages: (a) $1/3$ p.u. to 1 p.u. capacitive current, (b) 1 p.u. capacitive current to 1 p.u. inductive current, and (c) balanced current to unbalanced current.

the capacitor voltages with the conventional DM are highly affected during the transient stages of the voltage sag, and this is because the Inter-Phase Balancing loop is trying to reject the active power disturbance introduced by the fundamental component in v_{Zd}. On the other hand, the proposed DDM yields stable capacitor voltages with fast and damped transient response, similar to that achieved with the CM. The proposed DDM is able to keep the individual SM capacitor voltages well balanced during the whole voltage sag event. Regarding the steady-state behavior, it can be observed that the proposed DDM results in lower twice-fundamental-frequency capacitor voltage oscillation on the capacitor voltages than the CM.

Case III: Two-Phase 100% Voltage Sag

Fig. 8 shows the capacitor voltage and grid current waveforms under the CM, the conventional DM, and the proposed DDM, when the grid voltages $v_{g,b}$ and $v_{g,c}$ experience a 100%

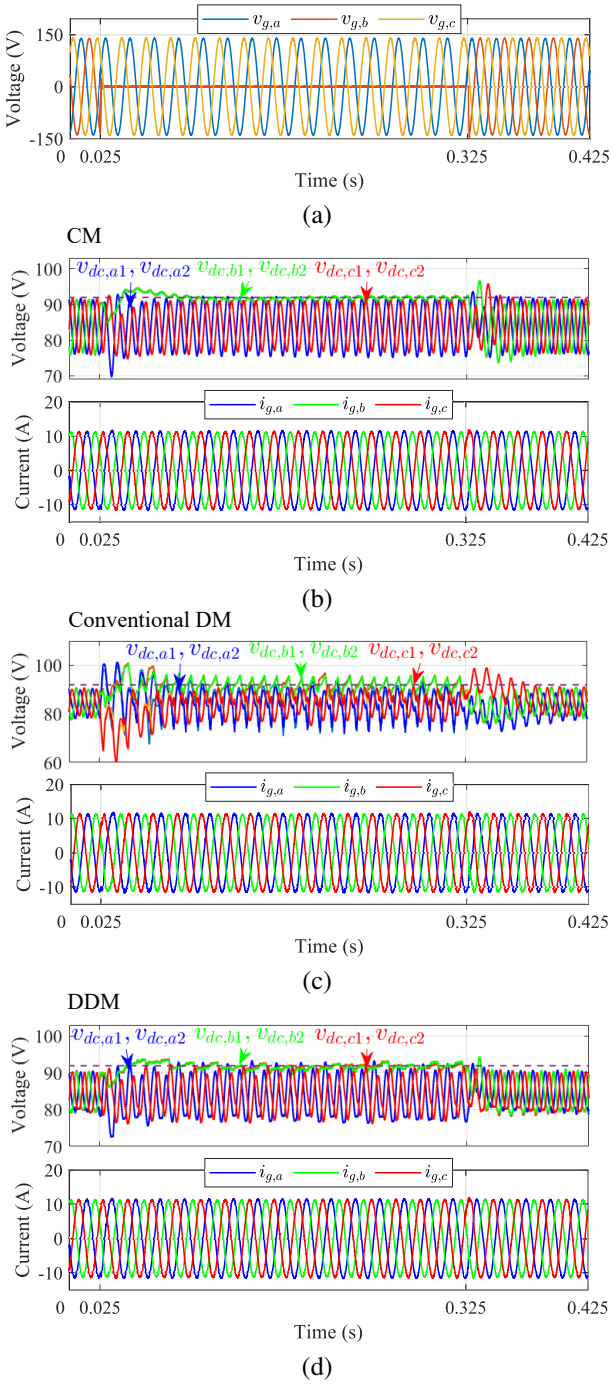

Fig. 7. ***Case II***: Experimental waveforms when the grid voltage in phase b drops to zero from $t = 0.025$ s to $t = 0.325$ s. (a) PCC grid voltages, (b)-(d) capacitor voltages and grid currents under the CM, the conventional DM, and the proposed DDM, respectively.

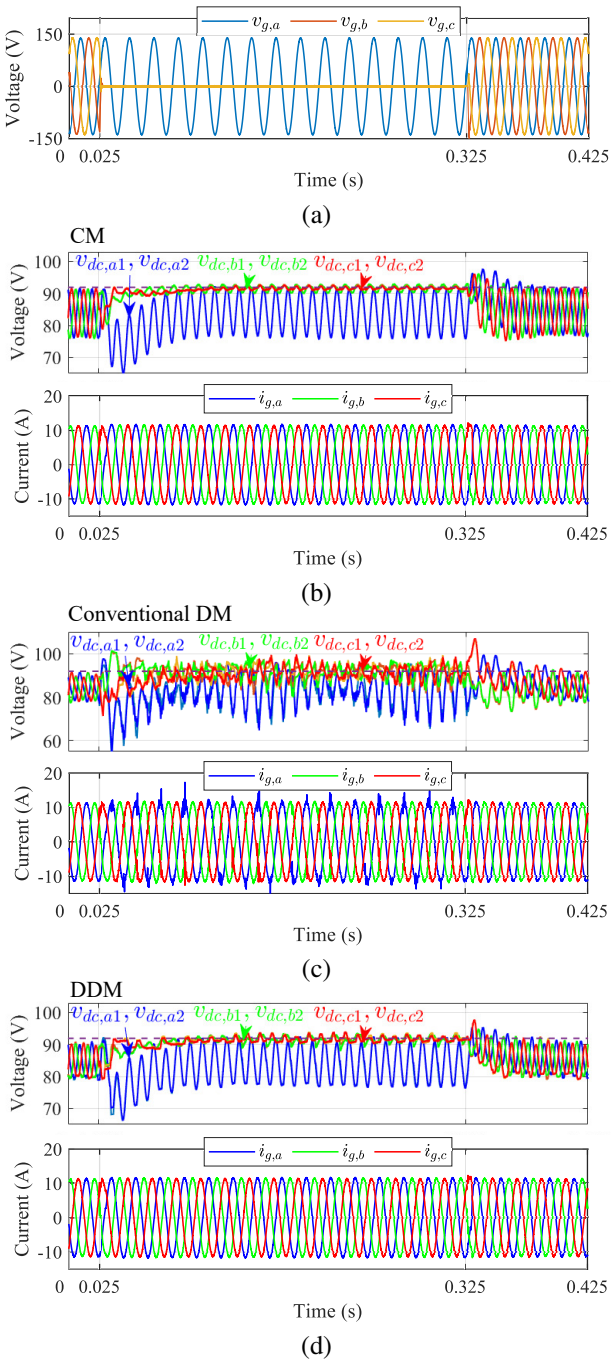

Fig. 8. ***Case III***: Experimental waveforms when the grid voltages in phases b and c drop to zero from $t = 0.025$ s to $t = 0.325$ s. (a) PCC grid voltages, (b)-(d) capacitor voltages and grid currents under the CM, the conventional DM, and the proposed DDM, respectively.

sag, from $t = 0.025$ s to $t = 0.325$ s. As it can be observed, when the voltage sag occurs, the conventional DM yields an unstable behavior where the capacitor voltages are not properly controlled and the grid currents are distorted. On the other hand, the proposed DDM exhibits a good transient response and steady-state behavior, both in the capacitor voltages and in the grid currents. It is important to remark that the proposed DDM again achieves a similar transient performance to that of the classic CM, but with the added benefit of lower switching losses inherent to the discontinuous operation, as it will be shown in the next section.

With the intention of emphasizing the advantages of the proposed DDM with respect to the conventional DM, a transient between both modulation strategies has been carried out, during a grid voltage sag. Specifically, a transition at $t = 0.225$ s from the conventional DM to the proposed DDM,

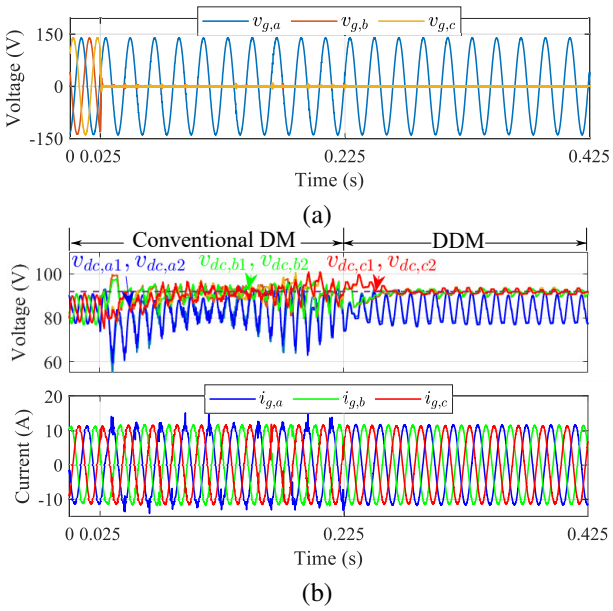

Fig. 9. ***Case III***: Experimental waveforms showing a transition from the conventional DM to the proposed DDM when grid voltages in phases b and c are zero, and when the StatCom is processing full capacitive current. (a) PCC grid voltages and, (b) capacitor voltages and grid currents.

when $v_{g,b}$ and $v_{g,c}$ are zero, is presented in Fig. 9. As it can be observed, with the conventional DM, as soon as the grid voltage sag takes place the capacitor voltages become unstable and the grid currents are distorted. After switching to the proposed DDM in the middle of the grid voltage sag, the StatCom quickly recovers its stable operation with balanced capacitor voltages and sinusoidal currents.

Case IV: Three-Phase 80% Voltage Sag

Fig. 10 shows the capacitor voltage and grid current waveforms when the three grid voltages drop to 20% of the nominal value, from $t = 0.025$ s to $t = 0.325$ s. Similarly as in ***Case III***, the conventional DM results in an undesirable behavior during the grid voltage sag with distorted grid currents and excessive twice-fundamental-frequency capacitor voltage oscillations. On the other hand, the proposed DDM rides through the three-phase grid voltage sag smoothly, while providing the required balanced sinusoidal grid currents. This is because the proposed DDM has the capability to clamp to the zero-voltage level, while the conventional DM does not.

The above experimental results in Figs. 7-10 demonstrate the effectiveness and superiority of the proposed DDM for CHB StatComs during severe grid voltage sags. Oscilloscope captured results, showing multilevel PWM converter voltages and grid currents, corresponding to Figs. 7(d), 8(d) and 10(d), are given in Figs. 13, 14 and 15, respectively, in the Appendix section.

V. Switching Loss Comparison

This section provides a comparison between the classic CM, the conventional DM, and the proposed DDM, in terms of switching losses.

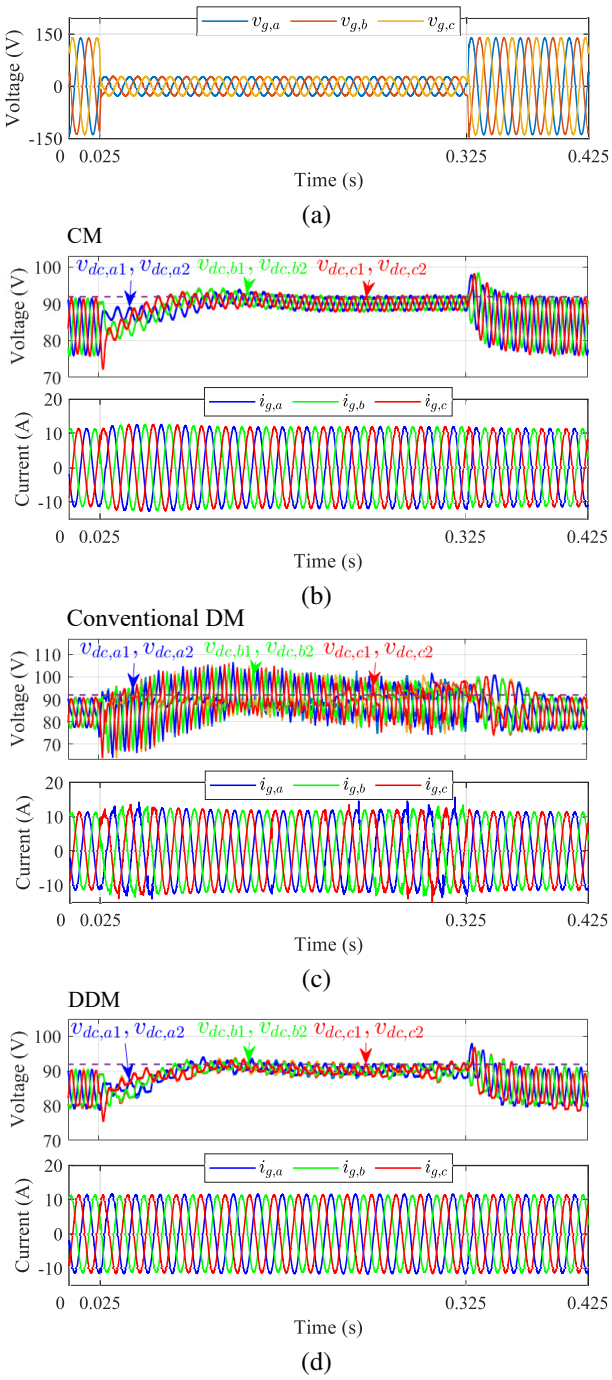

Fig. 10. ***Case IV***: Experimental waveforms when the grid voltages in phases a, b and c drop to 20% of nominal PCC grid voltages. (a) PCC grid voltages, (b)-(d) capacitor voltages and grid currents under the CM, the conventional DM, and the proposed DDM, respectively.

Fig. 11 shows typical StatCom waveforms, under rated positive-sequence inductive current and nominal PCC grid voltages, for the three modulation schemes. The capability of the proposed DDM to use the zero-voltage level is clear from the individual modulating signal (δ_{xj}) waveforms, and it has been highlighted with a red shading in the figure. Note that when the converter voltages are clamped to the zero-voltage level, their corresponding capacitor voltages remain constant

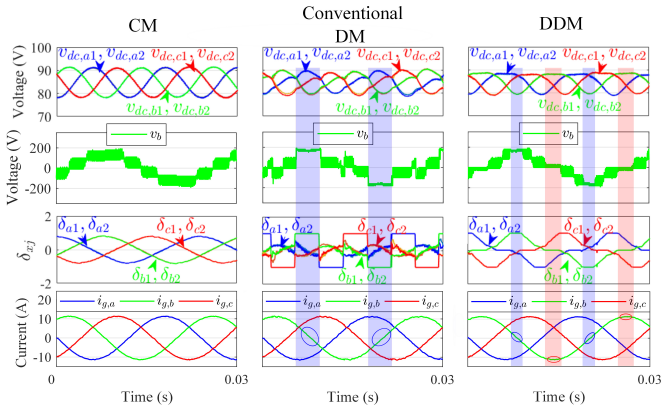

Fig. 11. Steady-state experimental waveforms under the CM, the conventional DM, and the proposed DDM, under full inductive current and nominal PCC grid voltages.

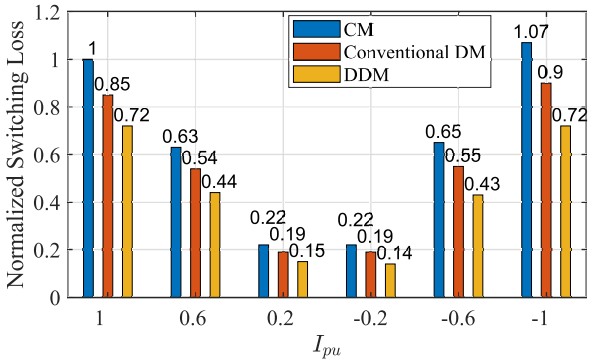

Fig. 12. Normalized experimental switching loss comparison under nominal PCC grid voltages.

since they are bypassed. The clamping periods to the positive and negative dc-link voltages have been highlighted using a blue shading. Remarkably, the proposed DDM has two more clamping periods than the conventional DM. However, each phase-arm under both the conventional DM and the proposed DDM are clamped a total of $2\pi/3$ rad within a fundamental period. More importantly, the conventional DM clamps the phase-arm with the highest absolute value of converter voltage, which coincides with low absolute value of current, as highlighted with a blue circle in Fig. 11. On the other hand, the proposed DDM can clamp to the zero-voltage level, which coincides with maximum absolute value of current, as highlighted with a red circle in Fig. 11. Significantly, this involves that the phase-arm does not switch when its respective current is at its maximum value, which is a desirable behavior in terms of switching loss reduction.

Fig. 12 shows switching losses comparison results for the three modulation strategies, considering nominal grid voltages, and for different current values from rated capacitive ($I_{pu} = 1$) to rated inductive ($I_{pu} = -1$). Note that switching losses have been calculated according to the expressions given in [22]. The switching losses of CM at $I_{pu} = 1$ have been considered as the base value for comparison purpose. As it can be observed from Fig. 12, the conventional DM and the proposed DDM

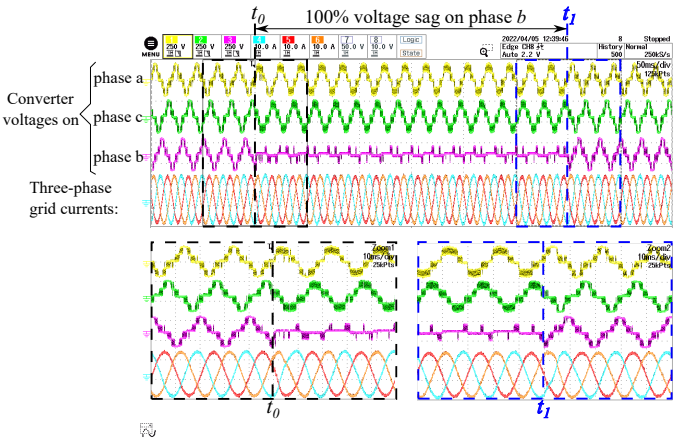

Fig. 13. 100% grid voltage sag in phase b when the StatCom is operating at full capacitive current and using the proposed DDM. Channels CH1, 2, and 3 are the PWM converter voltages, and Channels CH4, 5, and 6 are the grid currents.

have less switching losses than the CM, which is expected due to the discontinuous operation. Besides, the proposed DDM has the lowest switching losses, as could be expected, since the phase-arm does not switch when its respective current is around its maximum.

VI. Conclusion

This paper has proposed a DDM strategy for CHB StatComs. The proposed DDM combines the benefits of a classic CM and the conventional DM. Specifically, it presents a transient performance as good as the CM offers while reducing the average switching losses. The proposed DDM outperforms the conventional DM, especially in the event of unbalanced grid voltage occurrences, such as grid voltage sags. Moreover, the proposed DDM yields lower switching losses compared to the CM and the conventional DM. The experimental results show that the proposed DDM reduces the twice-fundamental-frequency capacitor voltage oscillations in comparison to the conventional CM, thus allowing to reduce the capacitor size. Furthermore, the experimental results verify excellent performance of the proposed DDM strategy under various grid voltage and current conditions.

Appendix

This appendix shows experimental results obtained from the oscilloscope which recorded data have been used to plot Figs. 7, 8, and 10 of this paper.

Fig. 13 shows the oscilloscope captured results corresponding to the experimental results presented in Fig. 7(d). The grid voltage sag lasts for 0.3 s, from t_0 to t_1. The instants in which the transient occurs is shown zoomed in at the bottom of the figure. Note that the current transient is very fast, and the converter voltage on phase b presents longer zero-voltage level clamping intervals during the grid voltage sag, as expected.

Fig. 14 shows the oscilloscope captured results corresponding to the experimental results presented in Fig. 8(d). Note that again the current transient is very fast and the converter

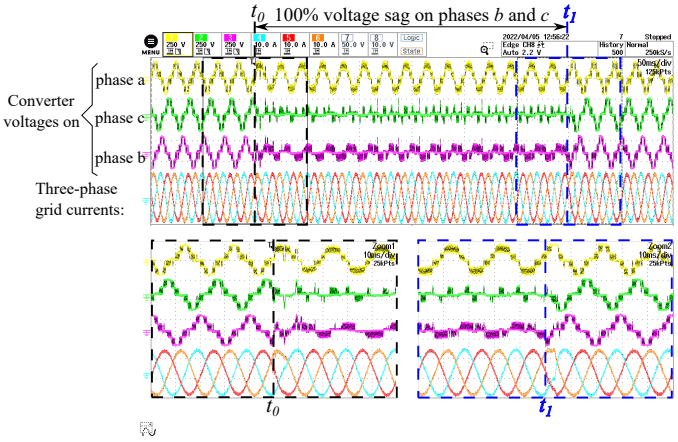

Fig. 14. 100% grid voltage sag in phases b and c when the StatCom is operating at full capacitive current and using the proposed DDM. Channels CH1, 2, and 3 are the PWM converter voltages, and Channels CH4, 5, and 6 are the grid currents.

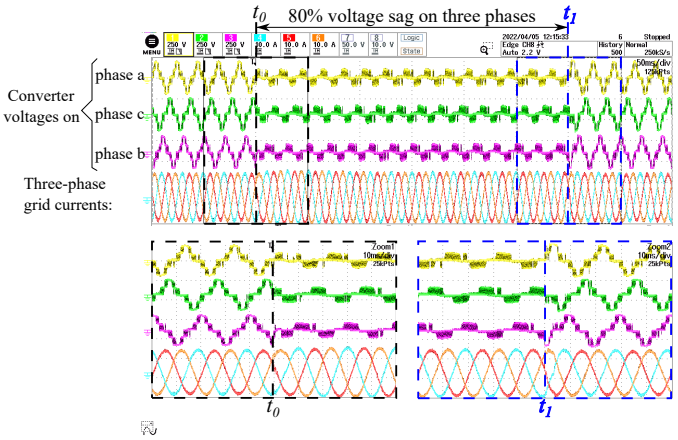

Fig. 15. 80% grid voltage sag in the three phases when the StatCom is operating at full capacitive current and using the proposed DDM. Channels CH1, 2, and 3 are the PWM converter voltages, and Channels CH4, 5, and 6 are the grid currents.

voltages on phases b and c are consecutively clamped to the zero-voltage level during the grid voltage sag to keep a small magnitude of the zero-sequence voltage.

Fig. 15 shows the oscilloscope captured results corresponding to the experimental results presented in Fig. 10(d). Note that the current transition is very fast, and during the grid voltage sag, the converter voltages are only clamped to the zero-voltage level.

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