Prediction of Subharmonic Oscillation in Switching Converters Under Different Control Strategies

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***Abstract*—Subharmonic oscillation is an undesired phenomenon in switching converters. In past studies, its prediction has been mainly tackled by explicitly deriving a discrete time model and then linearizing it in the vicinity of the operating point. However, the results obtained from such an approach cannot be applied for design purpose except for simple cases such as peak or valley current mode control. Alternatively, in this paper, this phenomenon is analyzed by using a unified formal symbolic approach which can be applied for different control strategies. This approach is based on expressing the condition for subharmonic oscillation occurrence using Fourier series and then converting the result into a matrix form expression which depends explicitly on the system parameters making the results directly applicable for design purpose. Under certain practical conditions concerning these parameters, the matrix form expression can be approximated by standard polynomial functions depending on the operating duty cycle. The results presented in this work clearly generalize the well known stability condition of peak/valley current mode control.**

***Index Terms*—DC-DC Converters, Voltage Mode Control, Current Mode Control, V^2 Control, Subharmonic Oscillation.**

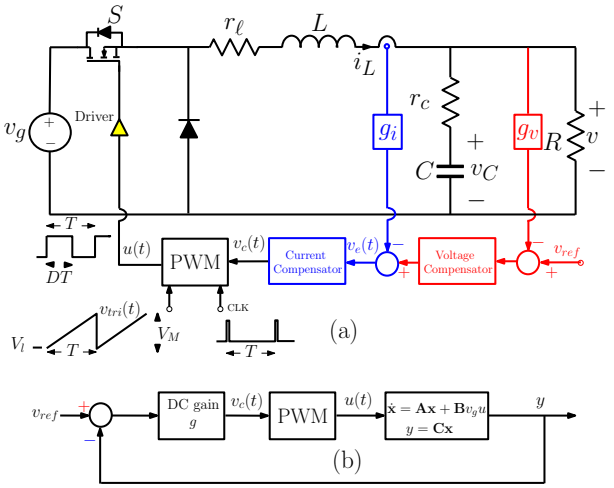

Fig. 1. (a) Block circuit diagram of a DC-DC buck converter under generic CMC. (b) Equivalent block diagram.

I. Introduction

Switching converters are integral elements to modern power electronics. Despite their widespread use, they can pose serious challenges to power-supply designers because almost all of the *rules of thumb* governing their design are only applicable to the linearized averaged system even though the system works in switched mode [1], [2]. Switch mode operation is carried out by means of Pulse Width Modulation (PWM) action on the switches. In the traditional PWM control, the duty cycle of the pulse driving signal $u(t)$ is varied according to the error $v_e(t)$ between the output variable (voltage or current) and its desired reference v_{ref}. This error is processed through an error amplifier to provide the control voltage $v_c(t)$. In Voltage Mode Control (VMC) or duty cycle control, the simplest analog form of generating a fixed frequency PWM is by comparing the control voltage with a ramp periodic signal $v_{tri}(t)$ in such a way that the pulse signal $u(t)$ goes high/low when the control signal $v_c(t)$ is higher/lower than the triangular signal $v_{tri}(t)$. In peak (resp. valley) Current Mode Control (CMC), the switch is turned ON (resp. OFF) periodically while it is turned OFF (resp. ON) whenever the peak (resp. valley) inductor current reaches a reference signal dictated by the output voltage error signal and a ramp compensator. Figure 1(a) shows a schematic circuit DC-DC buck converter under a general control scheme encompassing both VMC and CMC. It can be recognized that the voltage at the input of the RLC circuit (diode voltage) is essentially a square wave with amplitude v_g (input voltage). This fact justify the equivalent block diagram in Fig. 1(b). It is worth to note that a CMC converter generally uses the inductor current, as well as the output voltage error signal, as input signals to the PWM modulator. According to Fig. 1(b), the state equations of the system can be written as follows

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}v_g u(t) \quad (1)$$

$$v_c(t) = g(v_{ref} - y(t)) \quad (2)$$

$$y(t) = \mathbf{C}\mathbf{x}(t) \quad (3)$$

where $\mathbf{x}(t)$ is the vector of the state variables corresponding to the power stage (capacitor voltage v_C and inductor current i_L) and probably to the controller. v_{ref} is the reference signal and g is an appropriate gain. $u(t)$ is the square wave driving signal with steady state duty cycle D defined as the ratio between the ON time duration ($u(t) = 1$) and the entire switching period T. $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$ are system matrices to be specified later. It is important to point out that the mathematical description (1)-(3) is, in general, valid for both VMC and CMC strategies but the dimension and the expression of the system matrices will depend on the controller used. In practice, it is desirable that the system operates periodically with a constant switching frequency $f_s = 1/T$ equal to that of the external sawtooth

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ramp signal which is the same frequency of the external clock signal. However, under parameter changes, the stability of this operating mode may be lost resulting in different kinds of instabilities and dynamical behaviors [3]. There have been hitherto many research efforts devoted to predict the border of occurrence of such instabilities. In the past studies, the prediction of subharmonic oscillation has been mainly based on deriving an accurate discrete time model and then linearizing it in the vicinity of the operating point [4], [5], [6]. Recently, Filippov's method and the monodromy matrix has been used to predict these instabilities in DC-DC converters and similar results to those obtained from the discrete time approach were derived [7], [8]. However, the results obtained from both approaches, although very accurate, are not suited to obtain clear design-oriented criteria in the parametric design space. Exceptionally, the subharmonic oscillation can be perfectly predicted in the peak/valley CMC system examining mainly the slopes of the inductor current during the ON and the OFF time durations [1]. For example, from the well known slope-based criterion in [1], it can be shown that in order to guarantee the stability of a peak CMC DC-DC buck converter with a compensating ramp and with voltage loop open, the following inequality, in terms of the duty cycle D and the system parameters, must hold

$$\frac{1}{V_M}\frac{v_g T}{L}(D-\frac{1}{2})<1 \tag{4}$$

where L is the inductance of the inductor, V_M is the amplitude of the triangular signal $v_{tri}(t)$, and T its period (See Fig. 1). For a valley CMC buck converter, the same inequality holds by changing D with $\overline{D}=1-D$. A similar inequality can also be obtained for other control schemes with triangular waveforms of the control signal v_c like for example ripple-based V^2 control [9] where the Equivalent Series Resistance (ESR) of the output capacitor makes the waveform of the output voltage practically triangular similarly to the case of CMC. However, in situations where the control voltage has not a triangular shape, the slope-based criterion (4) can not be applied. This is the case of control schemes like type II and III VMC [10] or Type II average CMC [11]. A ripple-based approach has been suggested in [12]-[13] as a design-oriented approach for locating the boundary of subharmonic oscillation in a VMC buck converter demonstrating that effectively (4) can not be applied in this case.

An equivalent expression to (4), in the case of a generic control scheme, will be extremely helpful in designing switching converters free from subharmonic oscillation. This paper tries to develop a similar expression as (4) for different control strategies. The rest of this paper is organized as follows: Section II presents a Fourier-analysis-based condition from [14], written as a Fourier series in the frequency domain, for subharmonic oscillation occurrence in the DC-DC buck converter. In Section III, a closed form expression for this series is obtained. This expression is then simplified and specified in Section IV for different control strategies. A widely studied VMC DC-DC buck converter is used as an example to illustrate the theoretical results derived in this paper. Finally, in the last section, some concluding remarks of this work are summarized.

II. Fourier-analysis-based condition for subharmonic oscillation occurrence

This section is an overview of the results derived in a quite interesting but overlooked work [14]. Expanding the square wave diode voltage in a Fourier series and operating on each term of the u-to-v_c open loop transfer function $H(s)$, equating the resulting expression to the ramp signal at the switching instants defined by the crossing between $v_c(t)$ and $v_{tri}(t)$, conditions for different periodicities can be obtained. In [14] it has been shown that at the boundary of the first subharmonic oscillation, an equality in the form $\mathcal{S}(D)=V_M$ holds, where $\mathcal{S}(D)$ is the series given by

$$\mathcal{S}(D)=\sum_{k=-\infty}^{\infty}(1-e^{2\pi jkD})H(jk\omega_s)-H(j(k-\frac{1}{2})\omega_s) \tag{5}$$

$\omega_s=2\pi/T$ being the angular switching frequency. Therefore the system will be free from subharmonic oscillation whenever the following inequality holds

$$\frac{1}{V_M}\mathcal{S}(D)<1 \tag{6}$$

Note that inequality (6) looks like the well known condition (4) but it is more general.

III. A Generic analytical matrix form expression for predicting subharmonic oscillation

In [14], the series $\mathcal{S}(D)$ in (5) has been approximated by the term that involves the transfer function $H(s)$ with the smallest argument or solved graphically by truncating the series to an arbitrarily large number of harmonics. In this work, a closed form expression will be given for the series $\mathcal{S}(D)$ defined in (5). It will also be shown later that by considering practical operating conditions, this series can even be approximated by polynomial functions depending on the power stage and controller parameters and more importantly on the steady state value of the duty cycle D. Differently to [14], let us express $H(s)$ as follows (See Fig. 1(b))

$$H(s)=g\mathbf{C}\mathcal{R}_A(s)\mathbf{B}v_g \tag{7}$$

where $\mathcal{R}_A(s)$ is known in matrix theory as the resolvent of the matrix $\mathbf{A}$ which is given by [15]

$$\mathcal{R}_A(s)=(s\mathbf{I}-\mathbf{A})^{-1} \tag{8}$$

$\mathbf{I}$ is a unity matrix with appropriate dimensions. Then, from (8), the series $\mathcal{S}(D)$ in (5) becomes

$$\begin{aligned}\mathcal{S}(D) &= g\mathbf{C}\sum_{k=-\infty}^{\infty}(1-e^{2\pi jkD})\mathcal{R}_A(jk\omega_s)\mathbf{B}v_g \\ &- g\mathbf{C}\sum_{k=-\infty}^{\infty}\mathcal{R}_A(j(k-\frac{1}{2})\omega_s)\mathbf{B}v_g\end{aligned} \tag{9}$$

By using the Poisson sum formulae one can write [16]

$$\sum_{k=-\infty}^{\infty}H(jk\omega_s)=T\sum_{n=-\infty}^{\infty}h(nT) \tag{10}$$

where $h(t)$ is the impulse response which for the loop gain of the system described in (1)-(3), with input $u(t)$ and output $v_c(t)$, is given by

$$h(t) = \begin{cases} g\mathbf{C}e^{\mathbf{A}t}\mathbf{B}v_g & \text{if} \quad t \geq 0 \\ 0 & \text{if} \quad t < 0 \end{cases} \tag{11}$$

Using (11) and (10), one obtains

$$\sum_{k=-\infty}^{\infty} H(jk\omega_s) = gT\sum_{n=0}^{\infty} \mathbf{C}e^{n\mathbf{A}T}\mathbf{B}v_g = gT\mathbf{C}(\mathbf{I}-e^{\mathbf{A}T})^{-1}\mathbf{B}v_g \tag{12}$$

Using the Poisson sum formulae together with the modulation and the delay properties of the Fourier series, one obtains

$$\sum_{k=-\infty}^{\infty} H(jk\omega_s)e^{j2\pi kD} = gT\mathbf{C}e^{\mathbf{A}DT}(e^{\mathbf{A}T}-\mathbf{I})^{-1}\mathbf{B}v_g \tag{13}$$

$$\sum_{k=-\infty}^{\infty} H(j(k-\frac{1}{2})\omega_s) = gT\mathbf{C}(\mathbf{I}+e^{\mathbf{A}T})^{-1}\mathbf{B}v_g \tag{14}$$

Equations (12)-(14), when substituted in (5), give the following closed form expression for the series $\mathcal{S}(D)$

$$\mathcal{S}(D) = gT\mathbf{C}[(e^{\mathbf{A}DT}-\mathbf{I})(\mathbf{I}-e^{\mathbf{A}T})^{-1} + (\mathbf{I}+e^{\mathbf{A}T})^{-1}]\mathbf{B}v_g \tag{15}$$

Therefore, the condition (6) for the system to be free from subharmonic oscillation can be written as follows

$$\frac{gv_gT}{V_M}\mathbf{C}[(e^{\mathbf{A}DT}-\mathbf{I})(\mathbf{I}-e^{\mathbf{A}T})^{-1} + (\mathbf{I}+e^{\mathbf{A}T})^{-1}]\mathbf{B} < 1 \tag{16}$$

The inequality (16) can be considered as a generalized expression of (4) for different control schemes. This inequality can be solved in closed form for some design parameters like v_g, V_M, T and g to locate the boundary between the desired stable periodic behavior and subharmonic oscillation. For instance, from (16), an expression for the input voltage $v_g^*(D)$ in terms of the circuit parameters and the duty cycle D at the boundary of subharmonic oscillation is

$$v_g^*(D) = \frac{V_M}{gT\mathbf{C}[(e^{\mathbf{A}DT}-\mathbf{I})(\mathbf{I}-e^{\mathbf{A}T})^{-1} + (\mathbf{I}+e^{\mathbf{A}T})^{-1}]\mathbf{B}} \tag{17}$$

IV. Approximate expression for predicting subharmonic oscillation

It is instructive to apply the previous results to a buck converter with a simple but representative proportional controller (CMC or VMC) with static gain g although the results can be extended for the case of a dynamic controller. With a simple proportional control, the expressions of the matrix $\mathbf{A}$ and vector $\mathbf{B}$ are given by

$$\mathbf{A} = \begin{pmatrix} -\frac{\kappa_c}{RC} & \frac{\kappa_c}{C} \\ -\frac{\kappa_c}{L} & -\frac{R_L}{L}-\frac{\kappa_c R_c}{L} \end{pmatrix}, \quad \mathbf{B} = \begin{pmatrix} 0 \\ \frac{1}{L} \end{pmatrix} \tag{18}$$

where $\kappa_c = R/(R+R_c)$. The vector of the state variables is $\mathbf{x}(t) = (v_C, \ i_L)'$. The resolvent matrix can be written in the following formal geometric series expansion [15]

$$\mathcal{R}_A(s) = \sum_{m=1}^{\infty} \frac{\mathbf{A}^{m-1}}{s^m} \tag{19}$$

TABLE I
Polynomial functions $\mathcal{S}_m(D)$ for different values of m.

m	$\mathcal{S}_m(D)$
1	$\frac{1}{2} - D$
2	$\frac{1}{2}(\frac{1}{2} - D + D^2)$
3	$\frac{1}{4}(\frac{1}{3}D - D^2 + \frac{2}{3}D^3)$

Therefore, from (9) and (19), the series $\mathcal{S}(D)$ can be expressed as follows

$$\mathcal{S}(D) \quad = \quad \sum_{m=1}^{\infty} \mathcal{S}_m(D) gT^m\mathbf{C}\mathbf{A}^{m-1}\mathbf{B}v_g \tag{20}$$

where $\mathcal{S}_m(D)$ is the series given by

$$\mathcal{S}_m(D) = \sum_{k=-\infty}^{\infty} \frac{1-e^{2\pi jkD}}{(jk)^m} - \frac{1}{(j(k-\frac{1}{2}))^m} \tag{21}$$

The expression of $\mathcal{S}_m(D)$ can be obtained in closed form in terms of the duty cycle D for each value of m. In fact, $\mathcal{S}_m(D)$ is an m-th polynomial function of D. Table I shows the expressions of $\mathcal{S}_m(D)$ for $m = 1 \ldots 3$. To have a flexibility to deal with both VMC and peak CMC, let us consider a signal $y(t)$ (See Fig. 1) that can be expressed as a linear combination of the output voltage and the inductor current, *i.e*, $y(t) = g_v v(t) + g_i i_L(t)$. Therefore, the row vector $\mathbf{C}$ can be written as as follows: $\mathbf{C} = (\kappa_c g_v, \quad \kappa_c g_v R_c + g_i)$, where g_v and g_i represent the voltage and the current sensor gains respectively. Note for example, that for VMC $g_i = 0$, $g_v \neq 0$ while for CMC with voltage loop open, $g_v = 0$ and $g_i \neq 0$. For CMC with voltage loop closed, $g_v \neq 0$ and $g_i \neq 0$. It is to be pointed out that the previous expression of $\mathbf{C}$ is valid only for the case of static controllers. For the case of a dynamic controller, this vector must be adapted to include the terms corresponding to the state variables of the controller. The expressions of $gT^m\mathbf{C}\mathbf{A}^{m-1}\mathbf{B}$ in (20) for the first two values of m are given below for a general static control scheme encompassing both VMC and CMC.

$$gT\mathbf{C}\mathbf{B} = \frac{gT(R_c\kappa_c g_v + g_i)}{L} \tag{22}$$

$$gT^2\mathbf{C}\mathbf{A}\mathbf{B} = gT^2(\frac{\kappa_c^2 g_v}{LC} - \frac{(R_c\kappa_c g_v + g_i)(R_L + \kappa_c R_c)}{L^2}) \tag{23}$$

The high order terms are omitted to save space. However, these terms can be ignored for practical values of circuit parameters as it will be shown later. This is because for large enough $|s|$ with respect of the magnitude of the eigenvalues of the matrix $\mathbf{A}$, as it is the case in DC-DC converters, one can approximate $\mathcal{R}_A(s)$ by the two first terms in (19) and therefore in most cases, these terms are necessary and sufficient to predict subharmonic oscillation. Ignoring terms for $m \geq 3$, and after some algebra, the following expression for the critical input voltage is obtained

$$v_g^*(D) \approx \frac{V_M L}{gTc_2\mathcal{S}_1(D) + gT^2(\frac{c_1}{C} + \frac{c_2}{L}(-R_L - R_c\kappa_c))\mathcal{S}_2(D)} \tag{24}$$

where $c_1 = \kappa_c g_v$, $c_2 = \kappa_c g_v R_c + g_i$ and $\mathcal{S}_1(D)$ and $\mathcal{S}_2(D)$ are given in Table I. Note that (4) corresponds to (24) only if $R_c = 0$ and $g_v = 0$.

A. Current mode control

It can be noted from (24) that with voltage loop open ($g_v = 0, g_i = 1, g = 1$), and with ideal elements ($R_L = R_c = 0$), only the first term $gT\mathbf{CB} = T/L$ in the dominator is dominant in (20) and therefore (16) becomes (4). Note however, that parasitic elements can alter the subharmonic oscillation condition with respect to the ideal system in CMC. With voltage loop closed, in addition to the first term $gT\mathbf{CB}$, the second term $gT^2\mathbf{CAB}$ is also significant and it has to be taken into account. Otherwise, it may happen that the ramp compensation does not guarantee the avoidance of subharmonic oscillation if the slope of the ramp is designed based on the approximate condition (4). Therefore, a more accurate expression is (24).

B. Voltage mode control

In VMC, (24) is also valid if one makes $g_i = 0$. With an ideal output capacitor ($R_c = 0$), the first term $gT\mathbf{CB}$ in (20) is zero and the second term $gT^2\mathbf{CAB}$ is necessary to predict the subharmonic oscillation occurrence. The first term will be also zero for the case of a pole-zero cancelation between a controller pole (in the case of a dynamic controller) and the zero of the power stage due to the ESR of the output capacitor. In this case, the following expression is obtained for the source voltage at the boundary of subharmonic oscillations

$$v_g^*(D) \approx \frac{V_M L}{gT^2(\frac{c_1}{C} + \frac{c_2}{L}(-R_L - R_c\kappa_c))\mathcal{S}_2(D)} \tag{25}$$

Eq (25) is the same expression obtained in [12] for the case of ideal components ($R_c = R_L = 0$) by using a quite different approach. Without pole-zero cancelation, and with a significant value of the ESR R_c, $gT\mathbf{CB}$ becomes also significant making, generally, very similar the conditions for subharmonic oscillation occurrence in VMC and CMC. It is worth noting that based on (17) a very similar expression than (25) is obtained for Type II CMC and VMC. Details will be reported in a further study.

C. V^2 ripple-based control

Consider the constant-frequency peak voltage regulator (CF-PVR) (with V^2 control) [9]. By rearranging terms in (24), one has the same stability condition as in [9] with $R_L = 0$.

$$\frac{V_M L}{g v_g T} > c_2\mathcal{S}_1(D) + T(\frac{c_1}{C} + \frac{c_2}{L}(-R_L - R_c\kappa_c))\mathcal{S}_2(D) \tag{26}$$

D. Dependence on the load resistance

In the previous expressions, the dependence of the stability boundary on the load resistance is through the parasitic elements R_c and R_L. This dependence disappears if these parasitic parameters vanish. The actual dependence of the boundary on the load resistance R requires the consideration of the terms $T^3\mathbf{CA}^{m-1}\mathbf{B}$ for $m \geq 3$. It can be shown that all these terms are negligible if

$$\frac{LC(R + R_c)}{(RR_c + RR_L + R_cR_L)C + L} \approx RC << T \tag{27}$$

However, if (27) is violated some discrepancies exist between the results obtained from the exact expression (16) and the approximated expressions based on the truncation of the geometric series (20) as it will be shown in the next example.

Example: Consider the well known and widely studied example of buck converter considered first in [3] and later by other researchers in [4], [5], [7]. For this example, the input voltage v_g and the duty cycle D in the nominal T_s-periodic regime are related approximately by the following expression which can be obtained from a simple averaged model

$$v_g(D) = \frac{gv_{ref} + V_l + V_M(1 - D)}{g\kappa_L D} \tag{28}$$

where, $\kappa_L = R/(R+R_L)$ and V_l is the lower value of the ramp modulator signal. With a dynamic controller containing a pole at the origin, the error between v_{ref} and the output voltage v is zero and then (28) becomes simply $v_g(D) = v_{ref}/D$. The same set of parameter values used in [4], [5], [7] will be considered so that the readers can make the comparison easily. Namely, $L = 20$ mH, $C = 47$ μF, $V_l = 3.8$ V, $V_M = 4.4$ V, $T = 400$ μs, $v_{ref} = 11.3$ V and $g_v = 1$, $g_i = 0$, $g = 8.4$, $R_L = R_c = 0$. Numerical simulations are not repeated here to save space. Interested readers can see [3], [7] and [8] for both numerical simulations and experimental measurements. Traditionally the dynamic behavior of the system in this example has been studied in terms of the input voltage v_g [3], [7], [8], [4]. In Fig. 2, the exact mesh plot of $v_g^*(D)$ from (17) is shown together with the approximated plot from (25).

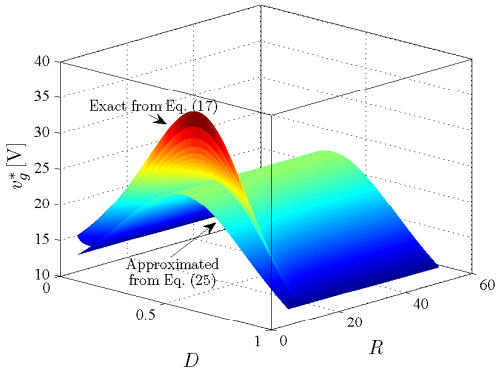

Fig. 2. Exact and approximated stability surface $v_g^*(D)$ in terms of the duty cycle $D \in (0, 1)$ and the load resistance $R \in (5, 50)$ Ω showing that for high values of $T/(RC)$, (25) is not enough accurate.

From Fig. 2, it can be observed that for sufficiently large values of R ($T/(RC) << 1$), a good concordance is obtained, while a discrepancy exists between the exact and the approximated plots for relatively low values of R . This discrepancy becomes significant for time constant RC approaching the switching period T. For $RC \geq T$, (25) will give inaccurate results. Figure 3 shows the plots of $v_g^*(D)$ from (17) and

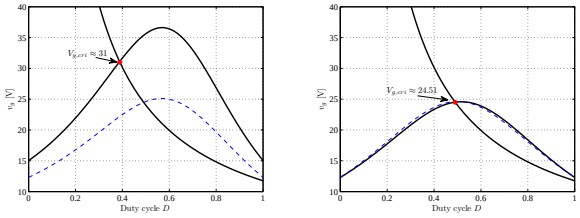

Fig. 3. Stability boundaries of the buck converter with VMC in terms of the input voltage v_g and the duty cycle D for teo different values of the load resistance R. Solid: exact curve. Dashed: approximated curve. Left: $R = 5\,\Omega$. Right: $R = 22\ \Omega$.

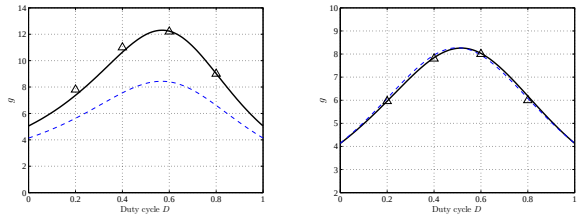

Fig. 4. Theoretical stability boundaries in terms of g and D together with corresponding experimental boundary points marked by $\triangle$. Solid: exact curve. Dashed: approximated curve. Left: $R = 5\ \Omega$. Right: $R = 22\ \Omega$.

its approximation in (25) for two different values of the load resistance R together with (28) in terms of the duty cycles D. The critical value of the input voltage $V_{g,\mathrm{cri}}$ is the intersection of the curves $v_g(D)$ from (28) and $v_g^*(D)$ from (17) or (25). This critical value can be determined approximately by subtracting (28) from (25), equating the resulting expression to zero and solving for D and then substituting in (28) or in (25). For instance, for $R = 22$ (Fig. 3-(b)), the critical value of the input voltage $V_{g,\mathrm{cri}} \approx 24.51$ V (for $D \approx 0.47$) which is in perfect agreement with [4], [7], [8]. For this value of the load resistance, $T/(RC) \approx 0.38$ is relatively small and the critical value can be also obtained accurately from the approximated expression (25). As R decreases, the value of the intersection point $V_{g,\mathrm{cri}}$ increases as predicted in [7] by using a numerical approach based on Fillipov method and the associated monodromy matrix. For example, for $R = 5\ \Omega$, the critical value of the input voltage is approximately 31 V which is in perfect agreement with [7] (See Fig. 7 in [7]). From the approximated expression of $v_g(D)$ one still obtains $V_{g,\mathrm{cri}} \approx 24.51$ V. This discrepancy is mainly due to the violation of (27) because, in this case, $T/(RC) \approx 1.7 > 1$. Some boundary points for the gain g in terms of the duty cycle D for $v_g = 25$ V, obtained from an experimental prototype, are depicted in Fig. 4, together with the theoretical boundary curves, showing an excellent agreement. □

CONCLUSIONS

Subharmonic oscillation in peak/valley CMC converters is well documented by different analytical methods by considering the voltage loop open. However, with voltage loop closed and for VMC, this phenomenon has been only characterized by using numerical simulations or mainly based on abstract mathematical analysis using a discrete time model or the Fillipov method. Explicit expressions for conditions of subharmonic oscillations occurrence in VMC and average CMC have been unavailable for many years. For peak CMC, it is widely believed that without ramp compensation, for example, the stability condition is $D < 1/2$ while with a compensating ramp the stability condition is (4). This expression is shown to be a special case of the general results presented in this paper. Based on the general unified approach used in this study, critical values of the system parameters can be located accurately for different control schemes. The results have been illustrated for a DC-DC buck converter with a simple proportional VMC widely considered in the literature. Works are in progress using the approach developed in this study to deal with dynamic control schemes as well as to extend it to different switching converter topologies. The results will be reported in a further study.

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