Direct digital design of a sliding mode-based control of a PWM synchronous buck converter

Enric Vidal-Idiarte[1*], Adria Marcos-Pastor[1], Roberto Giral[1], Javier Calvente[1], Luis Martinez-Salamero[1]

[1]Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Tarragona, SPAIN.
*enric.vidal@urv.cat

Abstract: A discrete-time sliding mode approach allowing direct digital design of a PWM control of a synchronous buck converter is presented in this paper. Without the need of a compensating ramp, a nonlinear difference equation representing the output voltage dynamic behavior is employed to demonstrate the global stability of the internal control loop of the inductor current. Discrete-time small-signal model is derived from the linearization of the ideal sliding-mode equations, which facilitates the design of the output voltage controller. This model exhibits a zero whose value depends on the operating point coordinates and explains the duty cycle delay associated to digitally PWM controlled converters. The validity of the transfer function is demonstrated through simulation by comparing its frequency behavior with that obtained from the more accurate switched model of the converter. Experimental results for start-up, load and line perturbations, current and voltage reference variations in a 25 W prototype switching at 100 kHz are in good agreement with the theoretical predictions.

Note: The paper has not been presented at a conference nor submitted elsewhere previously.

1. Introduction

Digital control of power converters emerged almost twenty years ago as a new topic in power electronics aiming to reconcile the continuous increase of switching frequency in power devices operation and the inherent advantages of digital computation, which were also undergoing an uninterrupted growth in power computation capabilities.

Compatibility between new power devices and modern digital processors implies a trade-off between converter switching frequency and controller sampling frequency, so that, as a rule of thumb, it can be stated that the higher the sampling frequency is, the larger is the computation capability of the digital device.

A key element in the search of the trade-off is the modelling approach because it can eventually determine the final configuration of the regulator, which includes using or disregarding certain sensors as well as employing ancillary circuitry for stability or start-up. There are several approaches in modelling power converters for digital control that can be grouped in two main categories: Digital Redesign Technique and Direct Digital Design.

Digital Redesign Technique (DRT) is based on the use of an analogue model of the converter, which is expanded with the digital delays of the numerical processing [2-3] in order to design an analogue controller in the frequency domain by means of linear techniques. Then, a digital representation of the analogue controller is obtained via continuous to discrete transformations such a Tustin's or backward Euler's methods [4-5].

Direct Digital Design (D^3), in turn, features an implementation of the digital controller using a discrete-time model of the converter for either voltage-mode [6-8] or current –mode control [9-20]. Although most cases employ an analytical model, a few exceptions [8,10] derive a discrete-time numerical model by applying Tustin's transformation to a continuous small- signal model of the converter for a particular set of parameters.

In digital current-mode control, the bottleneck is the availability of the inductor current for numerical processing because it implies a very high sampling frequency. This drawback is counteracted by the use of predictive digital techniques instead of current sampling in order to obtain sufficient inductor current information for the required digital processing. This is the case of reports [9-16], wherein an inductor current difference equation was used to digitally reproduce the classical current-mode control analogue schemes. As a result, equivalent stability conditions to those of analogue current-mode control were found, the main difference being that an appropriate choice of the modulation technique could preclude the use of a compensating ramp [10]. Besides, it can be observed that most reports on inductor current prediction are based on constant switching frequency through the use of pulse width modulation (PWM) and only few cases deal with variable switching frequency [17-19].

It has to be pointed out that the goal of processing the inductor current is to compute the expression of the control action in an internal fast loop of a two-loop control scheme whose ultimate objective is regulating the converter output voltage. Thus, to give two representative examples in the context of the inner loop, the control action is derived in [13]

through measuring the inductor current slope, i.e. using a partial information on the current behaviour, while it is obtained in reference [14] through slope estimation. Also, it is worth mentioning that most current-loop control actions suffer from one cycle delay, which was eliminated by the techniques reported in [12-13].

Another difficult issue is the design of the outer control loop establishing the reference for the current inner loop and providing output voltage regulation. The design is based on deriving an accurate transfer function in the z-domain relating the current reference variations to the output voltage variations. However, formulating analytically the different predictive current descriptions by means of well-posed models is a difficult task in certain approaches and ,for that reason, some authors have obtained first an equivalent continuous-time model of the current prediction and then have derived the mentioned transfer function by applying DRT [13-17]. To illustrate the degree of difficulty when dealing with discrete-time models of power converters, it is worth mentioning that the well-known general recurrence model described in [21] has been satisfactorily used in [7,20] after having been approximated by a first-order difference equation. Nonetheless, it can be demonstrated that the resulting approximated model can lead to unstable behaviour in some cases in the buck converter. Moreover, a more refined discrete-time model than the previous approximation has shown the existence of a zero in both duty cycle to output voltage and duty cycle to inductor current discrete-transfer functions, whose value depends on the intrinsic digital delay related to the duty cycle.

Regarding the most investigated power stages under digital control; they are mainly of boost or buck type. The interest in the digital control of the buck converter stems from the well-known fact that this converter is extensively applied in industry in applications ranging from few watts to several kilowatts showing a very high efficiency in all cases. Besides, improving the digital control performances in the buck converter is still a hot topic as evidenced by the recent publications [24-26].

A Labview-based implementation of a digital control for a buck converter has been recently reported in [24]. The control strategy is of PWM type and is based on processing a linear combination of the output voltage error and the output of a reduced-order observer. The latter provides an estimation of a linear combination of the derivative of the output voltage error and the output voltage error itself. The complexity of the resulting algorithm for real-

time operation leads to a very low switching frequency (3.6 kHz), which is far below the normal standard requirements. In [25], a nonlinear discrete-time representation of the buck converter dynamics is linearized to derive three digital controllers for output voltage regulation. They process respectively the variations of the output voltage, input voltage and reference voltage to provide a control action that is the sum of their outputs. An excellent performance is obtained for load resistance variations of 33% and input voltage changes of 20% at the expense of a complex tuning. Finally, a variable hysteresis control strategy based on a digital PLL to operate at constant switching frequency and requiring a compensating ramp for stability is reported in [26]. A good agreement between theoretical predictions and experiments are obtained for small variations around the desired switching frequency.

In this work we propose the design of a nonlinear digital current control of a synchronous buck converter, based on the discrete-time approach of the sliding-mode control theory [23] that was previously applied in the boost converter [20] . The novelties of this work are (i) obtaining a more accurate description of the converter dynamics by means of an analytical nonlinear model, (ii) designing a current control loop based on sliding-mode control (iii) proving analytically the resulting closed-loop stability, and (iv) designing analytically the voltage control loop for output voltage regulation.

The paper is organized in five sections. A nonlinear discrete-time representation of the buck converter dynamics is derived in section 2. The inner control loop strategy of the inductor current is designed in section 3. The stability issues are also analysed in this section besides the derivation of the discrete transfer function relating the current reference and the output voltage. In section 4, a PI compensator for output voltage regulation is designed and its performance illustrated by means of simulations and experiments. Finally, section 5 shows the conclusions of the proposed work.

2. Discrete-time model of the buck converter

The block diagram of a PWM digital control application to a synchronous buck converter is represented in Fig. 1. The duty cycle $d(n)=T_{on}(n)/T_s$ in the n^{th} switching period T_s is computed using the sampled values of the input voltage ($V_g(n)$), the output voltage($v(n)$)

and the inductor current ($i_L(n)$), where $T_{on}(n)$ represents the time in which the high-side MOSFET is ON.

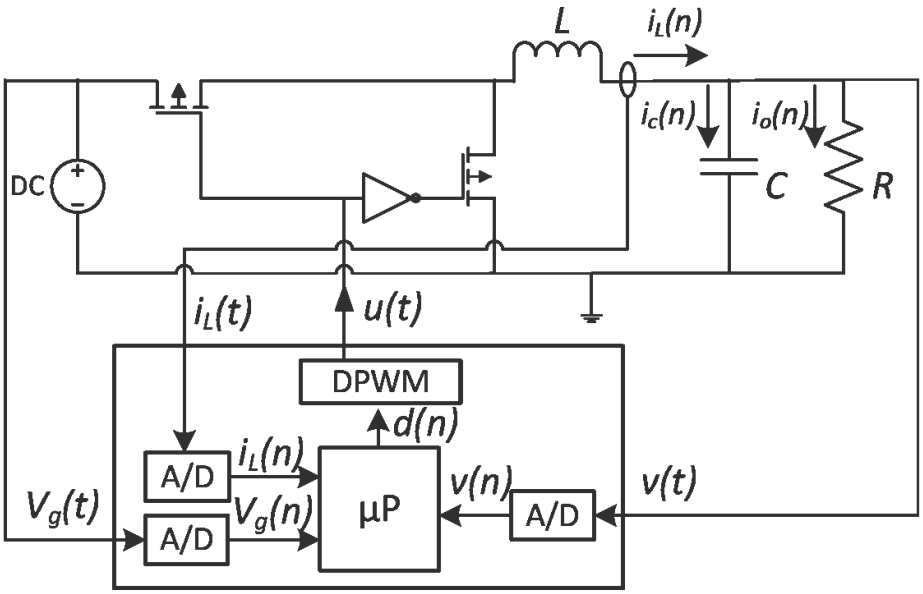


Fig.1. *Digital control of a synchronous buck converter*

Assuming $v_g(n)=V_g$ is constant during the nth switching cycle and observing the inductor current waveform of Fig.2 , the following representation of the inductor current dynamics can be obtained:

$$i_L(n+1) = i_L(n) + \frac{V_g}{L} T_{on} - \frac{v(n)}{L} T_S \tag{1}$$

Under the same assumptions, the value of the voltage capacitor at the end of the nth switching cycle can be represented as

$$v(n+1) = v(n) + \frac{1}{C} \int_{nT_S}^{(n+1)T_S} i_c(t)dt \tag{2}$$

where $i_c(t)$ is the current output capacitor and $i_o(t)$ represents the load current

$$i_c(t) = i_L(t) - i_o(t) \tag{3}$$

From (3), it is derived

$$\int_{nT_s}^{(n+1)T_s} i_c(t)dt = \int_{nT_s}^{nT_s+Ton} i_L(t)dt + \int_{nT_s+Ton}^{(n+1)T_s} i_L(t)dt - \int_{nT_s}^{(n+1)T_s} i_o(t)dt \tag{4}$$

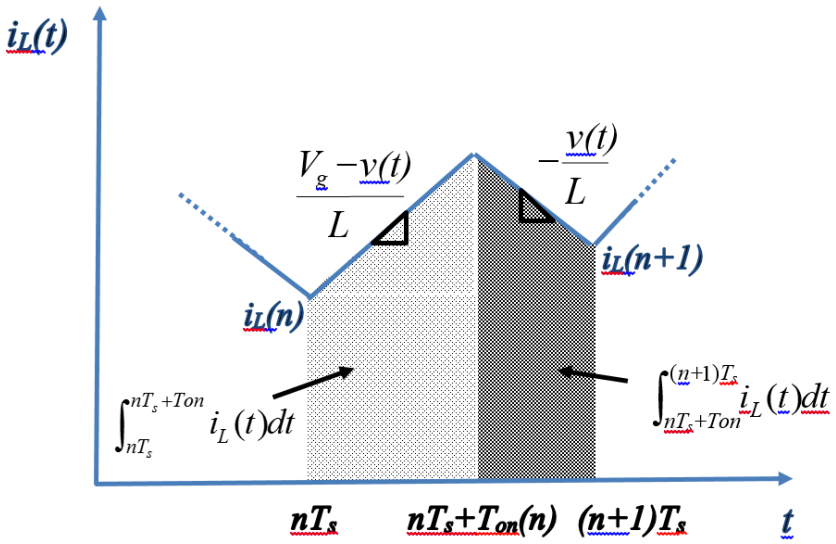


Fig 2. *Inductor current waveform in a synchronous buck converter*

Under small-ripple assumption for output capacitor voltage *v(t)*, the following relations from Fig. 2 are obtained

$$\int_{nT_s}^{nT_s+Ton} i_L(t)dt = i_L(n)T_{on} + \frac{V_g - v(n)}{2L}T_{on}^2 \tag{5}$$

$$\int_{nT_s+Ton}^{(n+1)T_s} i_L(t)dt = i_L(n+1)(T_s - T_{on}) + \frac{v(n)}{2L}(T_s - T_{on})^2 \tag{6}$$

Besides, from Fig.1 it can be written

$$\int_{nT_s}^{(n+1)T_s} i_o(t)dt = \frac{v(n)}{R}T_s \tag{7}$$

Therefore, the following nonlinear dynamics representation of the output capacitor voltage is derived

$$v(n+1) = \left(1 - \frac{T_s}{RC} - \frac{T_s^2}{2LC}\right)v(n) - \frac{V_g}{2LC}T_{on}^2 + \frac{T_s V_g}{LC}T_{on} + \frac{T_s}{C}i_L(n) \tag{8}$$

3. Sliding mode approach in discrete-time

3.1. Sliding motions in the discrete-time inductor current representation.

A discrete-time representation of the constant current sliding mode control surface is defined as

$$s(n) = I_{ref} - i_L(n) \tag{9}$$

where I_{ref} represents the inductor current reference value.

Then, we obtain the corresponding control action at n^{th} switching cycle that induce the system to satisfy

$$s(n+1)=0 \tag{10}$$

which implies computing the $T_{on}(n)$ value that equals the reference and the $(n+1)^{th}$ sampled inductor current value. This is an extension of the equivalent control notion in continuous–time systems to a discrete-time context [24]

$$T_{eq}(n) = \frac{\left(I_{ref} - i_L(n)\right)L + v(n)T_s}{V_g} \tag{11}$$

whose value must be restricted according the following inequality

$$0 \le T_{eq}(n) \le T_s \tag{12}$$

From (12), the existence conditions ensuring discrete-time sliding mode operation are given by

$$v(n) < V_g \tag{13}$$

$$v(n) > 0 \tag{14}$$

During start-up or in case of large variations of I_{ref}, it is necessary to saturate the control value $T_{on}(n)$ to avoid overpassing the range defined in (12), thus becoming

$$T_{on}(n) = \begin{cases} 0 & T_{eq}(n) < 0 \\ T_{eq}(n) & 0 \le T_{eq}(n) \le T_s \\ T_s & T_{eq}(n) > T_s \end{cases} \tag{15}$$

When $T_{on}(n)$ is saturated to either its upper or its lower limit value, then equation (10) will not be satisfied. In order to reach again the discrete-time sliding behaviour we must guarantee that $|s(n)|$ diminishes continuously in the subsequent switching cycles. The reachability conditions will be fulfilled if the following inequality is accomplished:

$$s(n+1)\Delta s(n+1)<0 \tag{16}$$

where

$$\Delta s(n+1) = s(n+1) - s(n) = \frac{1}{L}\left(T_s v(n) - T_{on}(n)V_g\right) \tag{17}$$

When $T_{on}(n)$ is saturated to 0, then s(n+1)<0 and (17) results in

$$\Delta s(n+1) = \frac{T_s}{L} v(s) > 0 \tag{18}$$

When $T_{on}(n)$ is saturated to the highest control value, i.e. $T_{on}(n)=T_s$, then $s(n+1)>0$ and, hence (17) becomes

$$\Delta s(n+1) = \frac{T_s}{L} (v(n) - V_g) < 0 \tag{19}$$

By ensuring existence conditions (13) and (14), conditions (18) and (19) are fulfilled and hence the system will always evolve towards the switching surface.

Therefore, it has been proved that the sliding-mode regime exists in discrete-time when a switching surface based on a constant current reference (9) is used and the control action applied is the previously shown in (15).

3.1.1 Ideal sliding-modes in discrete-time:

Using the expression of $T_{eq}(n)$ given by (11) in (1) and (8), with the assumption of sliding-mode behaviour, results in

$$i_L(n+1) = I_{ref} \tag{20}$$

$$v(n+1) = \left(1 - \frac{T_s}{RC} + \frac{T_s^2}{2LC}\right) v(n) - \frac{T_s^2 v(n)^2}{2LCV_g} + \frac{T_s}{C} I_{ref} \tag{21}$$

where (20) and (21) respectively describe the ideal sliding dynamics of the inductor current and the capacitor voltage in discrete-time. It has to be pointed out that the recurrence in (21) is a non-linear function of the capacitor voltage, and that the order of the converter dynamics has been reduced by one.

Assuming $i_L(n+1) = i_L(n)$ and $v(n+1) = v(n)$ in (20) and (21), the equilibrium point is obtained

$$x^* = \begin{pmatrix} I_e \\ V_e \end{pmatrix} = \begin{pmatrix} I_{ref} \\ \frac{V_g}{2}\left(1 - \frac{2L}{RT_s} + \sqrt{\left(1 - \frac{2L}{RT_s}\right)^2 + \frac{8L}{T_s V_g} I_e}\right) \end{pmatrix} \tag{22}$$

where I_e and V_e represents the corresponding inductor current and output voltage equilibrium point coordinates.

3.1.2 Equilibrium point stability

Considering

$$\Delta v(n) = v(n) - v(n-1) \tag{23}$$

the following identity is derived

$$\Delta v(n)^2 - \Delta v(n-1)^2 = \left(v(n) + v(n-1)\right)\Delta v(n) \tag{24}$$

and then, from (21) and (24) we can obtain

$$\Delta v(n+1) = \left(1 - \frac{T_s}{RC} + \frac{T_s^{\,2}}{2LC} - \frac{T_s^{\,2}\left(v(n) + v(n-1)\right)}{2LCV_g}\right)\Delta v(n) = \gamma\,\Delta v(n) \tag{25}$$

which represents the dynamic behaviour of the error.

Hence, a sufficient stability condition of the difference equation is

$$|\gamma| < 1 \tag{26}$$

In accordance with equations (13) and (14), the minimum and maximum values of γ are related to the corresponding maximum and minimum values of *v(n)*, thus leading to the following inequality

$$\frac{T_s^{\,2}\left(v(n) + v(n-1)\right)}{2LCV_g} < \frac{T_s^{\,2}}{LC} \tag{27}$$

Hence, when *v(n)* equals *Vg* it is derived

$$1 - \frac{T_s}{RC} + \frac{T_s^{\,2}}{2LC} - \frac{T_s^{\,2}\left(v(n) + v(n-1)\right)}{2LCV_g} = 1 - \frac{T_s}{RC} - \frac{T_s^{\,2}}{2LC} \tag{28}$$

Similarly, *v(n)* =0 implies

$$1 - \frac{T_s}{RC} + \frac{T_s^{\,2}}{2LC} - \frac{T_s^{\,2}\left(v(n) + v(n-1)\right)}{2LCV_g} = 1 - \frac{T_s}{RC} + \frac{T_s^{\,2}}{2LC} \tag{29}$$

Therefore, imposing the constraint (26) to (28) leads to the following two restrictions:

$$T_s < RC \tag{30}$$

$$T_s < \sqrt{2LC} \tag{31}$$

Similarly, from (26) and (29) we obtain

$$T_s < \frac{2L}{R} \tag{32}$$

Satisfying equations (30) and (32) automatically ensures fulfilling (31) and, in consequence, (26) is accomplished, thus guaranteeing the global stability of the corresponding equilibrium point.

3.2. Inner loop transfer function

Now, an external control loop is included with the aim of indirectly regulating the output voltage by introducing appropriate changes in the internal control loop reference. This is carried out by the discrete transfer function $Gi_{ref}v(z)$, which relates the changes in the current reference to the changes in the output voltage. This transfer function is derived assuming small-signal variations in the vicinity of the operating point (v_{ref}), so that expression (9) can be written now as follows

$$s(n) = i_{ref}(n-1) - i_L(n) \tag{30}$$

Taking into account (10) and (30) modifies (11) as follows

$$T_{eq}(n) = \frac{\left(i_{ref}(n) - i_L(n)\right)L + v(n)T_s}{V_g} \tag{31}$$

Assuming sliding-mode operation in discrete-time results in

$$i_L(n) = i_{ref}(n-1) \tag{32}$$

Hence, from (30), (31) and (8) it can be derived the reduced order dynamic behaviour of v(n)

$$v(n+1) = \left(1 - \frac{T_s}{RC} + \frac{T_s^2}{2LC} - \frac{T_s}{CV_g}\left(i_{ref}(n) - i_{ref}(n-1)\right)\right)v(n) - \frac{T_s^2}{2LCV_g}v(n)^2 - \frac{L}{2CV_g}\left(i_{ref}(n) - i_{ref}(n-1)\right)^2 + \frac{T_s}{C}i_{ref}(n) \tag{33}$$

Linearizing (33) around the equilibrium point $x^*=[I_e, V_{ref}]^T$ and employing (22) yield the internal loop transfer function

$$Gi_{ref}v(z) = \frac{V_{ref}T_s}{V_g C} \frac{\left(1-\frac{V_g}{V_{ref}}\right)z-1}{z\left(z+\left(\frac{T_s^{\,2}}{LC}\left(\frac{V_{ref}}{V_g}-\frac{1}{2}\right)-\left(1+\frac{T_s}{RC}\right)\right)\right)} \tag{34}$$

It is worth mentioning that, as in the case of the small-signal model presented in [22], the poles and zeros of (34) are related to the operating point, i.e., to the specified output voltage (V_{ref}). To analyse the validity of the discrete-time small-signal model presented in (34) the small-signal frequency representation of the switched converter for different output voltages by means of PSim simulations is obtained. In Fig. 3 the results of these simulations are compared with those calculated from (34) for the same set of output voltage values V_{ref}. It can be observed that the model given by (34) represents accurately the gain and phase values up to half of the switching frequency for different operating points including the corresponding digital delays showed in [22].

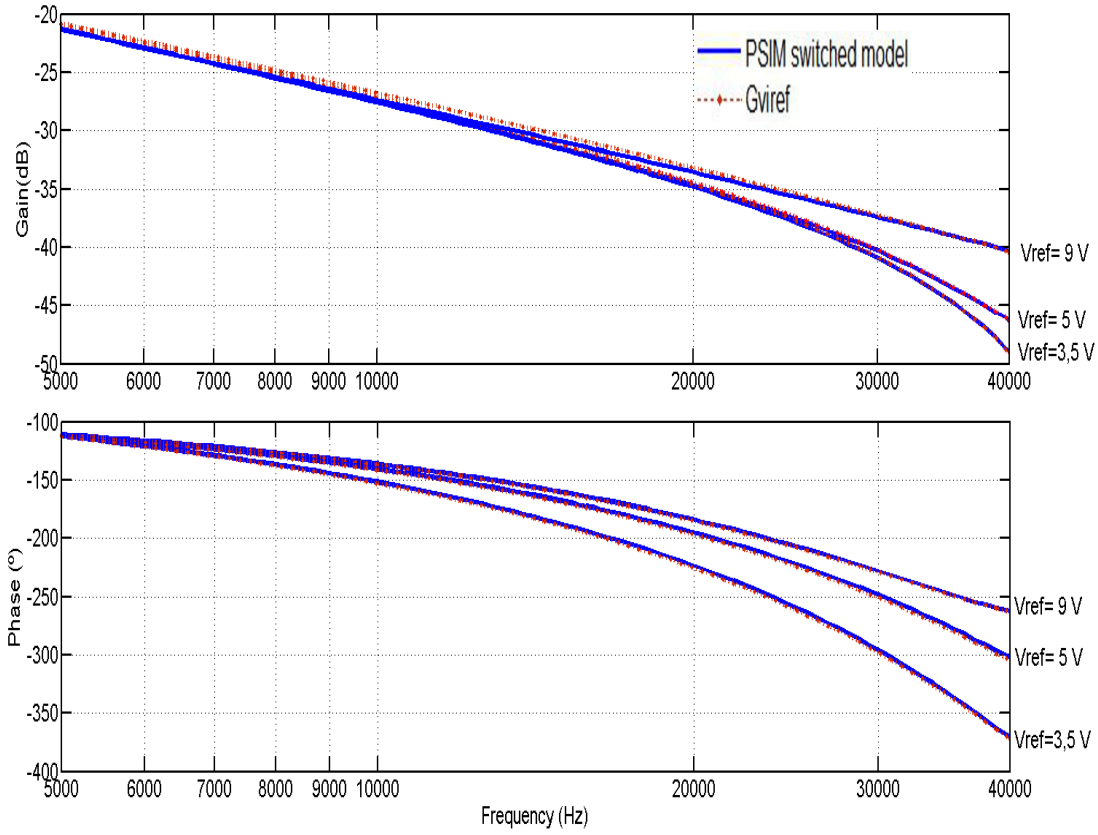


Fig 3. Frequency response of $Gi_{ref}v(z)$

4. Control strategy validation

The goal of this section is to prove the validity of the proposed control strategy. With this aim, PSim simulations are performed using the converter parameters: Vref= 5 V, Vg= 10 V $T_s=10^{-5}$ s, L=6.6 mH, C=350 μF, and R= 1 Ω. The experimental setup in Fig. 4 shows a prototype of the buck converter for the same set of parameters, an electronic load, a power supply and a Digital Signal Controller (TMS20F28335) to implement the corresponding discrete-time control law.

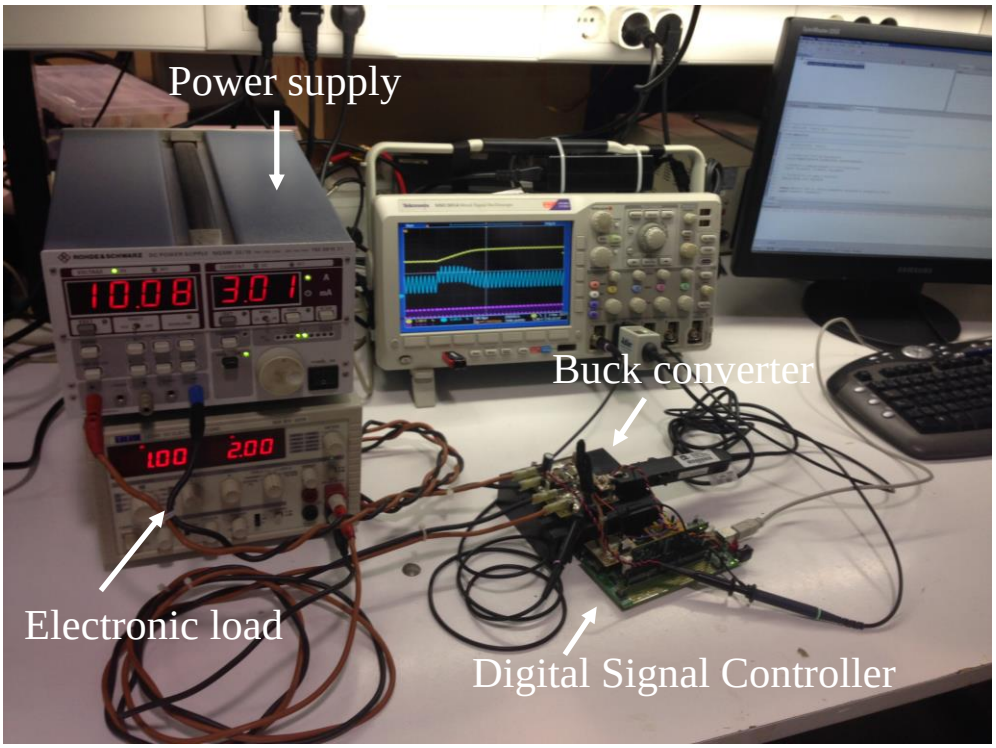


Fig 4. Experimental setup

The diagram of the experimental power stage is represented in Fig. 5 showing the elements for the variables measurement and the MOSFET driver. Both N-Channel MOSFETs are IRF3708s (V_{DDS} = 30 V, $R_{DS(on)\_max}$= 12 mΩ) while the 3.3 μH inductor is a WE-HCC SMD High Current Cube Inductor (Ref. 7443320330). The output capacitor bank is made of eleven 47 μF X7R-dielectric multilayer ceramic capacitors (Ref. TDK-CKG57KX7R1C476M). Although the nominal capacitance of the bank is about 500 μF, the actual total capacitance at 5 V estimated from ripple measurements is 350 μF.

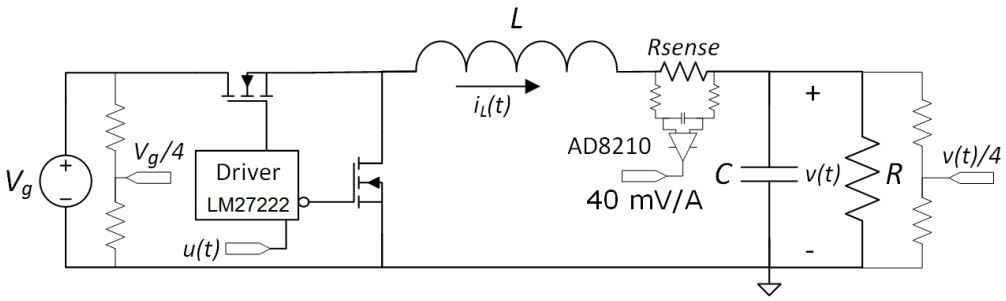


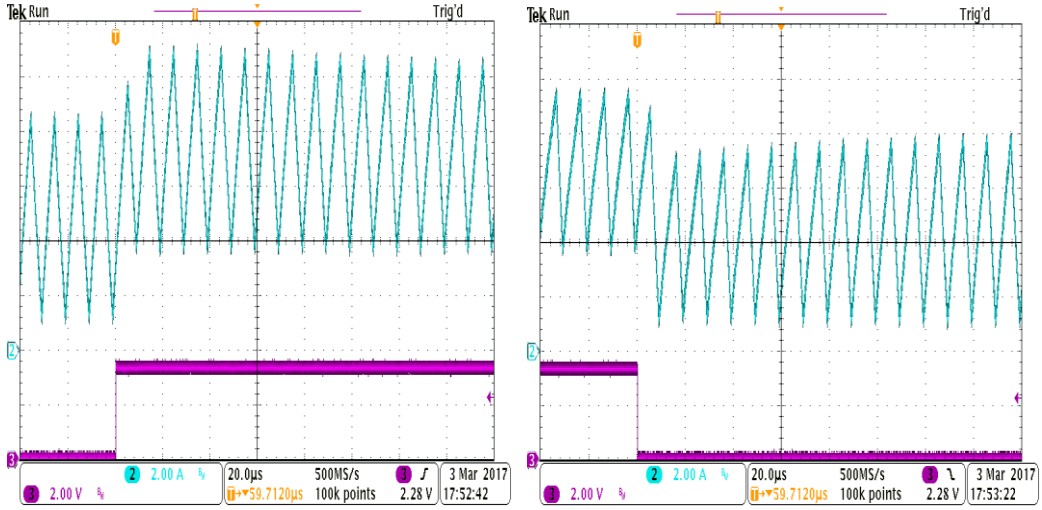
Fig 5. Diagram of the experimental power stage

In order to validate the theoretical predictions and to obtain output voltage regulation, a proportional-integral (PI)-based controller is designed with a phase margin of 45 º and gain margin of 8 dB:

$$G_{PI}(z) = 25\frac{z-0.83}{z-1} \qquad (35)$$

It can be observed the existence of an integrator which ensures zero steady-state error, a multiplicative constant and a zero placed before the loop gain crossover frequency. Both zero and gain values have been adjusted to ensure the desired phase margin using the SISO tool of Matlab[28].

Fig 6 illustrates the experimental results for a step variation in the current reference value. As expected, equation (19) is accomplished and the system achieves the new current reference value in the next switching period either in the step-up (Fig 6a) or in the step-down (Fig. 6b) transient.



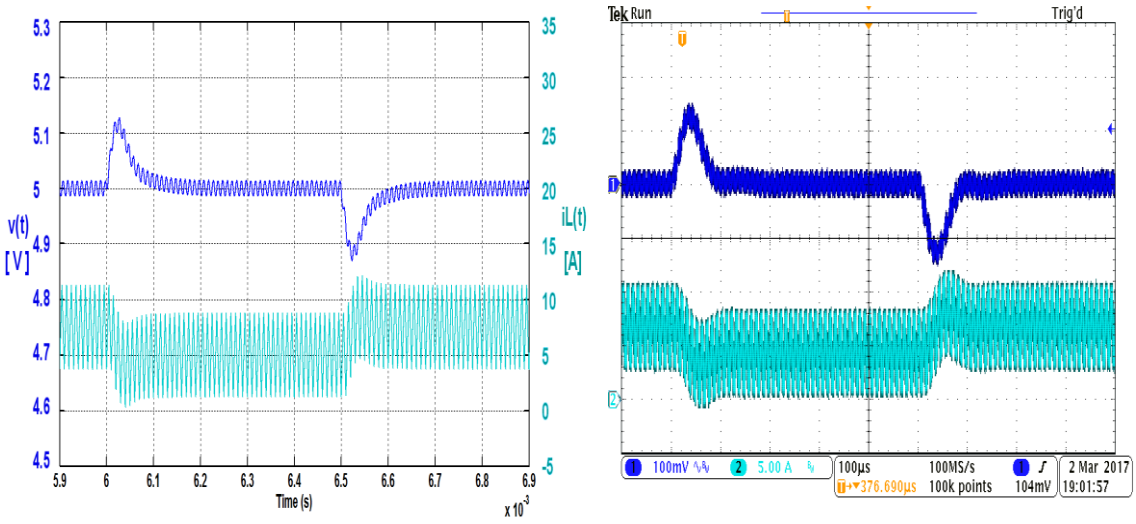
a ***b***

Fig. 6*: Time response of inductor current for current reference step change*

a Step-up current reference change

b Step-down current reference change.

Time responses of both output voltage and inductor current for step-type load perturbations of 50 % are illustrated in Fig. 7, i.e., the simulated results are presented in Fig4a while experimental results are shown in Fig. 7b. A good agreement is observed between both figures. Note that the desired output voltage of 5 V is recovered after a relatively fast transient regime for both positive and negative transitions.



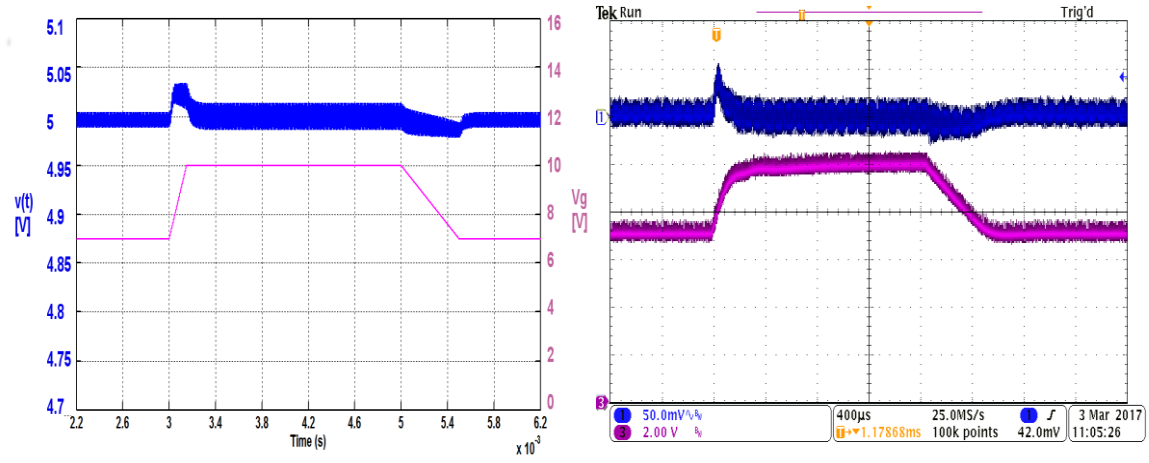
a ***b***

Fig. 7*: State variables response for step-type load perturbations of 50 %.*

a Simulated

b Experimental.

Similarly, a good agreement is observed between simulated and experimental results for input voltage variations as depicted in Fig. 8. Note that an increment of 3 V is applied first to Vg at instant 3 ms and the initial value of Vg is again established after 2 ms.



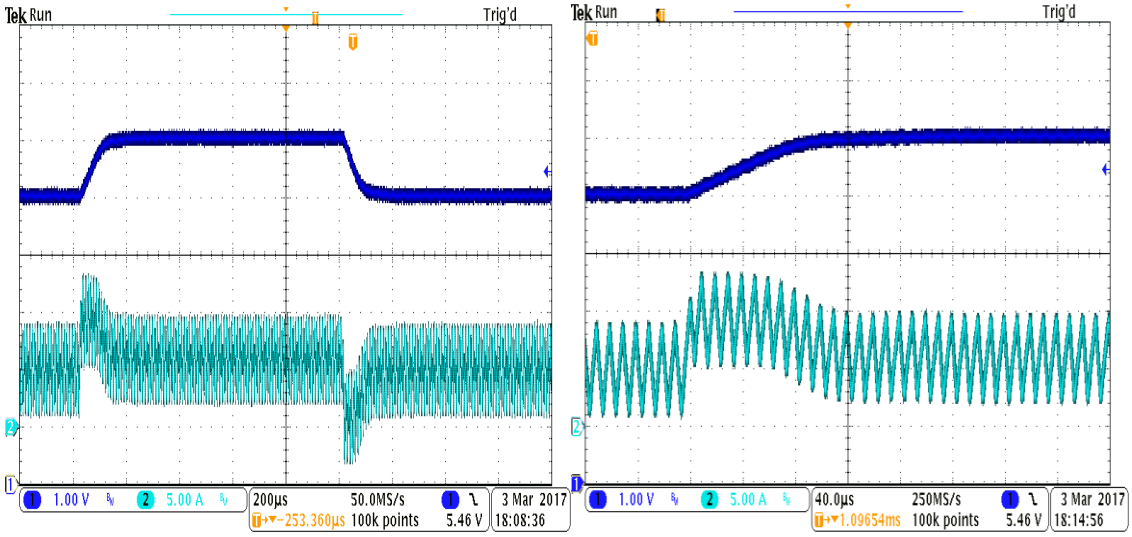
a ***b***

Fig. 8: *Output voltage response to input voltage variations*

a Simulated

b Experimental.

The output voltage response to a voltage reference change of step type from 5 V to 6 V and vice-versa is shown in Fig. 9a, where a perfect tracking is observed. Fig. 9b is a zoom of Fig. 9a detailing the step up output voltage change behaviour. Note that the output voltage reaches its new steady-state in around 13 cycles (130 µs). This time is the expected one since the closed -loop dominant pole of the system is located at z=0.7768, or equivalently in a continuous-time system at s=-2.5252e+004, which would result in an approximate settling time t_s= 4/2.5252e+004 = 15e-5 s.



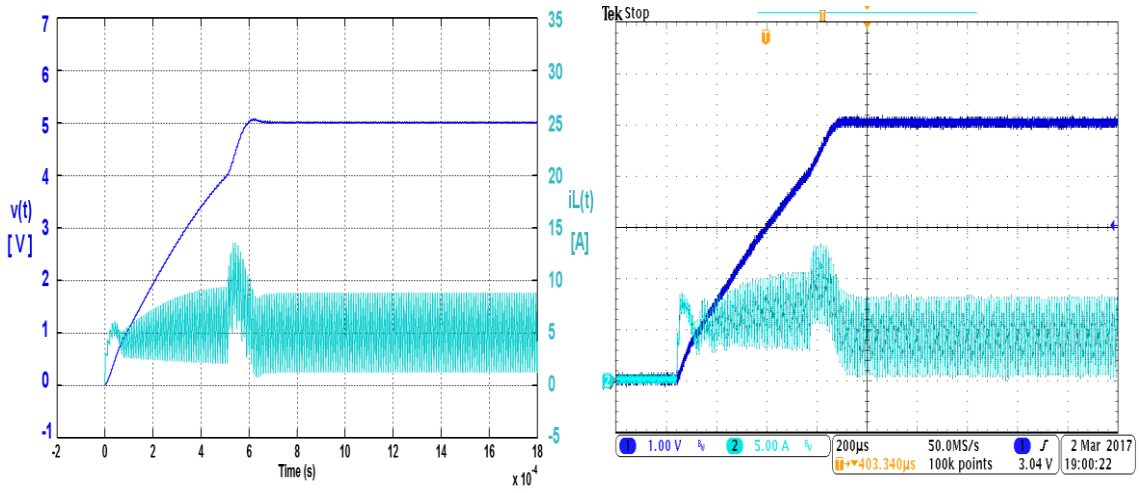
a ***b***

Fig. 9: *Output voltage response to voltage reference step variation*

a step up and step down change

b step up change.

Also, it is worth mentioning that the proposed discrete-time control strategy also provides an appropriate start-up of the system leading the converter dynamics to the desired output voltage with no overcurrent or overvoltage. The versatility of the digital implementation allows mitigating the inrush current [28] by means of a software controlled start-up procedure whose result is illustrated in Fig 10.



a ***b***

Fig. 10 *Soft start-up of the buck converter*

a Simulated

b Experimental.

5. Conclusions

This work has presented a new two-loop Direct Digital Design procedure to control the output voltage of a synchronous buck converter by combining an analytical approach based on the sliding mode control theory in discrete-time and its subsequent implementation with constant switching frequency by means of pulse-width modulation.

The controller consists in an inner nonlinear control loop applied to the inductor current, and an external PI-based voltage regulation loop. The discrete-time sliding-mode approach has been used to design the internal loop, which has led to a parametric equation for the inner current control loop. Global stability of the system has been analytically demonstrated using a nonlinear model of the output voltage.

The external loop is derived by means of a Direct Digital Design technique, which is based on a discrete transfer function of the inner loop. As expected, the intrinsic digital delay is included in the obtained model and is represented by the zero and pole dependence on the working point coordinates.

Validation of this model has been done through frequency behaviour comparison with the switched controlled buck converter by means of simulation. The analytically obtained transfer function has facilitated the design of a PI compensator for output voltage regulation. The simulation and experimental results have validated the theoretical predictions and proved the feasibility and good performance of the proposed direct digital design procedure.

Compared to other predictive digital current control methods for high switching controlled power converters, the proposed controller does not require the implementation of a compensating ramp to ensure the stability.

Besides, the versatility of the algorithm implementation has allowed the inclusion of a soft-start strategy to avoid the high peak of the inrush current.

Finally, it has to be pointed out that the converter directly operates in PWM, which could allow interleaving operation in future applications as in the case of a boost converter for PFC applications [20].

6. Acknowledgments

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7.References

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