Boundaries of Subharmonic Oscillations Associated to Filtering Effects of Controllers and Current Sensors in Switched Converters Under CMC

A. El Aroudi, *Senior Member, IEEE*, J. Calvente, *Member, IEEE*, R. Giral, *Senior Member, IEEE*, M. Al-Numay, *Member, IEEE*, and L. Martínez-Salamero, *Senior Member, IEEE*

***Abstract*—Subharmonic oscillation is widely studied in switching converters under current mode control (CMC). Its boundary of occurrence in the design parameter space is well known in the case of an infinite bandwidth current sensor. However, in a practical implementation, either a limited bandwidth current sensor or an additional filter is used. This could have an effect on the system dynamics especially for relatively high switching frequencies. This paper discusses the effect of the additional dynamics due to finite bandwidth current sensor or additional filter on the stability and subharmonic oscillation boundaries in switching converters under CMC. It is shown that a simplified model taking into account the dynamics of the inductor current and the sensor/filter is enough to obtain accurate results concerning the prediction of the occurrence of subharmonic instabilities in switched converters. Design-oriented equations describing the occurrence of subharmonic oscillations are used to show some problems related to the additional dynamics on the ramp compensator design in single-switch dc-dc converter working in continuous conduction mode. Some proposed solutions are also discussed. Numerical simulations and experimental measurements corroborate the theoretical predictions.**

I. Introduction

SWITCHING power converters are widely used in many applications due to their high efficiency, small size and light weight [1]–[4]. Two main control modes exist for these converters, namely Voltage Mode Control (VMC) and Current Mode Control (CMC) [1]. The last one has been considered the best choice for high performance switched mode power supplies due to significant advantages over the more conventional VMC strategy. For instance, since instantaneous changes in the input voltage are immediately reflected in the inductor current, CMC provides excellent line transient response. In addition, the current mode operation also eases loop stabilization, cycle-by-cycle current limitation and thermal shutdown protection [5].

Manuscript received November 5, 2014; revised February 2, 2015; April 13, 2015; May 21, 2015 and June 25, 2015; accepted June 27, 2015.

This work was supported by the Spanish *Ministerio de Economía y Competitividad* under the projects DPI2013-47293-R, CSD2009-00046 and TEC2012-30952. A. El Aroudi and M. Al-Numay also acknowledges the support of VPP of the King Saud University, Riyadh, KSA.

A. El Aroudi, J. Calvente, R. Giral and L. Martínez-Salamero are with the GAEI research group, Dept. d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, 43007, Tarragona, Spain. Email address: {abdelali.elaroudi, javier.calvente, roberto.giral, luis.martinez}@urv.cat.

M. Al-Numay is with Electrical Engineering Department, King Saud University, Riyadh, KSA, alnumay@ksu.edu.sa.

On the other hand, it is well-known in the power electronics community that without ramp compensation, constant frequency converters under CMC exhibit subharmonic oscillation for half of the range of the duty cycle. Switching converters may present a variety of complex dynamics that linear analysis tools from averaging theory generally fail to describe even when the control loop is considered ideal (See for example [6]–[12]).

For peak CMC, it is believed that the system is stable for low duty cycles range ($D < 50\%$) and that the stability range is inverted when changing between peak CMC and valley CMC [4], [13], [14]. The use of slope compensation ramp can increase the stability range of the desired periodic behavior, but as a penalty, it reduces some of the benefits of CMC by lengthening the closed loop system response since a ramp slope increase makes it approaching to that of complex conjugate poles characterizing converters under VMC [15], [16]. The ramp compensator can either be added to the sensed current or subtracted from the reference signal. Another drawback with traditional compensation schemes is that the inductor current deviates from its desired reference introducing harmonic distortion in the current waveforms near the zero crossing area [14], [17], [18].

There are many applications where the duty ratio changes from cycle to cycle and the stability must be ensured for its entire range. For instance in power factor correction (PFC) ac-dc applications, the input voltage is sinusoidal while the output voltage is regulated to a practically constant value and therefore the duty ratio varies between 1 and a minimum value depending on the relation between the peak input voltage and the averaged value of the output voltage [13]. In grid connected dc-ac inverters, the opposite occurs, i.e., the average value of the input voltage is constant while the output voltage is a time varying sinusoidal signal making the duty ratio also time varying [19]. In particular, there exists a significant degradation of the performance for low conversion gain buck converters [20] and high conversion gain boost converters [21]–[23]. Low conversion gains are needed in dc-dc buck converter applications such as in Voltage Regulator Modules (VRMs) [24] and high conversion gains are required in dc-dc boost converters applications such as in fuel cell and photovoltaic energy processing. The difficulty of design for low values of duty cycles prompted many researchers to seek for alternative variable frequency CMC such as ripple-based control [24] and constant ON time control [25] or by using

TABLE I
THE EXPRESSIONS OF m_1 AND m_2 FOR THE DIFFERENT ELEMENTARY SWITCHING CONVERTERS [1].

	Buck	**Boost**	**Buck-Boost**
m_1	$\frac{v_g - v_o}{L}$	$\frac{v_g}{L}$	$\frac{v_g}{L}$
m_2	$\frac{v_o}{L}$	$\frac{v_o - v_g}{L}$	$-\frac{v_o}{L}$

some converter topologies avoiding very small and very large duty ratio operation [21], [22], [26].

Based on the analysis of the perturbed waveform of the inductor current, a slope-based criterion can be obtained establishing that a switching converter under a peak CMC will be stable provided that the following inequality holds [1]:

$$-1 < -\frac{m_2 - m_a}{m_1 + m_a}, \tag{1}$$

where m_1 and $-m_2$ are the positive and negative slopes of the inductor current during a switching period and m_a is the slope of the T-periodic artificial ramp compensator. If the input and the output voltages are well regulated or slowly varying, the above slopes will be practically constant. Using the fact that in steady-state one has $m_1 D = m_2(1-D)$, the following four different but equivalent stability conditions are obtained:

$$\frac{m_2}{D}(D - \frac{1}{2}) < m_a, \tag{2a}$$

$$\frac{m_1}{1-D}(D - \frac{1}{2}) < m_a, \tag{2b}$$

$$m_s(D - \frac{1}{2}) < m_a, \tag{2c}$$

$$\frac{m_d}{2} < m_a, \tag{2d}$$

where $m_s = m_1 + m_2$ and $m_d = m_1 - m_2$. Table I gives the expressions of the slopes m_1 and m_2 for the three different elementary switching converters buck, boost and buck-boost.

The expressions in (2a)-(2d) establish that the converter is stable if the ramp compensator slope must be greater than a certain critical value that depends on the operating duty cycle D. The criteria in (1) and (2a)-(2d) are obtained by assuming that a perfect sensing of the inductor current can be performed. If either a limited bandwidth current sensor is used or an additional filter is added to the feedback loop, the waveforms and the harmonics content of the signal obtained at the output of the current sensor/filter will be different from those of the real inductor current without any filtering effects [27], [28]. In some industrial applications, the current sensor bandwidth ranges from few tens [29], [30] to several hundreds of kHz [28], which can pose some problems if the switching frequency is in the same range or higher. In such cases the criteria in (1) or (2a)-(2d) cannot be applied as the shape of the control signal is no more triangular and its slope is not constant within a complete switching cycle. It should be noted that even when the bandwidth is supposed to be infinite, there are also other control strategies which uses CMC with a suitable filtering of the current signal such as type II average CMC [31].

A procedure has been presented in [32] to theoretically study the effects of current sensor bandwidth limitation. The results have been validated by numerical simulations in a boost converter. There, it has been shown that this critical non-ideality influences significantly the dynamic behavior of the system and leads to subharmonic oscillation for parameter values different than those of the ideal case. In this paper, we thoroughly study and expand the results presented in [32] and we validate the reported phenomena using experimental measurements. Some problems due to the influence of the limited bandwidth of the current sensor on the ramp compensator design and system dynamics are discussed along with some proposed solutions.

The outline of the paper is as follows. A motivating example of switched converter that can work in both buck-mode and boost-mode from [13] is presented in Section II and studied with a limited bandwidth current sensor or with an equivalent filtering effect in the feedback loop. In Section III, a simplified model is proposed for the elementary switching converters: buck, boost and buck-boost under CMC with current filtering or finite bandwidth limitation. From this model, an accurate expression for predicting subharmonic oscillation occurrence is presented in Section IV for the three elementary switching converters. The expression takes into account the above mentioned current sensor bandwidth limitation. In Section V, it is shown by numerical simulations using different examples that this phenomenon still occurs even in cases where the expression given in (1) predicts a stable behavior. Some new design-oriented expressions for subharmonic oscillation boundaries are proposed in the same section. Experimental validation of the theoretical predictions and the numerical simulations are presented in Section VI. Finally, discussions, conclusions and contributions of this study are summarized in the last section.

II. A MOTIVATING EXAMPLE

A two-switch cascaded buck-boost rectifier shown in Fig. 1 for single-phase PFC applications is selected for study in this section. The used parameter values are the same of [13] and are as follows: inductance $L = 600$ μH, input voltage $v_g(t) = 230\sqrt{2}|\sin(2\pi 50t)|$ V, switching frequency $f_s = 1/T = 28$ kHz, desired output voltage $V_{\rm ref} = 250$ V, output capacitance $C = 400$ μF, load resistance $R = 100$ Ω, input filter parameters L_f =400 μH and $C_f = 4$ μF. The converter has two operating modes: a buck mode and a boost mode. Buck mode takes place when the rectified input voltage v_g is higher than the output voltage v_o, and boost mode occurs when the rectified voltage is lower than the output voltage. The boost switch ($S_{\rm boost}$) is turned OFF permanently in buck mode, and only the buck switch ($S_{\rm buck}$) is switched. The buck switch is constantly in the ON state in the boost mode and only the boost switch is commutating. For details on the system operation, see [13]. In [13] no ramp compensation was used and the sensor was supposed to be ideal. Theoretically, the system should exhibit subharmonic oscillation during a certain interval within the line period in the boost mode when the duty cycle is greater than 0.5. Such behavior cannot be observed

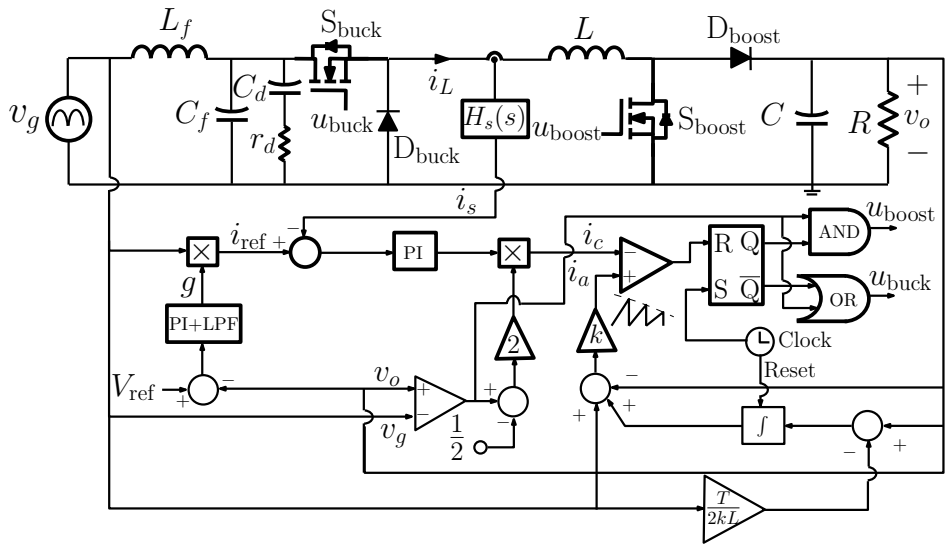
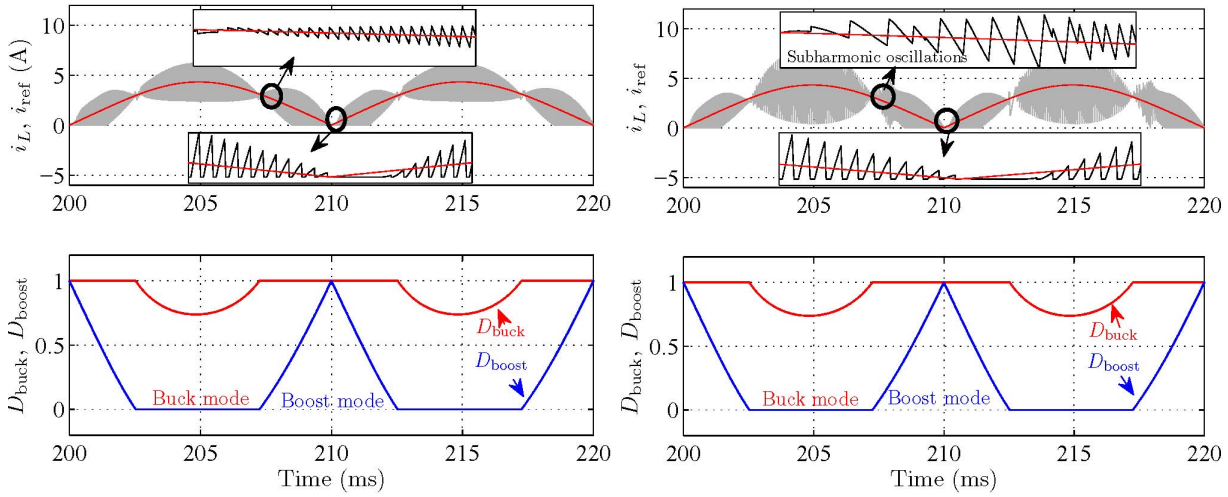


Fig. 1. Circuit diagram of the two-switch cascaded buck-boost switching converter for PFC applications [13].



(a) Ideal sensor

(b) Limited sensor bandwidth

Fig. 2. Time-domain waveforms of the two-switch cascaded buck-boost converter under CMC.

in [13] because the control strategy used and the choice of the parameter values correspond to discontinuous conduction mode (DCM) in the boost mode when $D > 0.5$ (see Figs. 4 and 7 in [13]). Ideally, ramp compensation is not needed for stabilization in DCM because the current loop is naturally stable. In order to force the system to operate in CCM, we make the current reference proportional to the input voltage ($i_{\text{ref}} = gv_g$) as it is the case in PFC applications, where g is a conductance dictated by the outer voltage loop. In [13], the system is operated under peak CMC in the boost mode and in the buck mode it works under valley CMC. Controlling the peak value in the boost mode and the valley value in the buck mode may decrease the system power factor. To avoid this effect, the reference current is shifted up in the boost mode under peak CMC and shifted down in the buck mode under valley CMC by using a PI controller in the current loop and a hybrid dynamic compensation scheme [18]. This strategy can ensure that the average inductor current tracks the desired sinusoidal reference without steady-state error and without input current distortion near the zero crossing. With the used scheme, the ramp compensator slope in the boost mode is time varying according to the following expression:

$$m_a = \frac{kv_o}{T} - \frac{v_g}{2L}, \tag{3}$$

where k is a feedback gain to be chosen to avoid subharmonic oscillation (see [18] for more details). In the buck mode under valley current control, a constant ramp slope $m_a = 28$ kA/s is used guaranteeing a stable response for all the duty cycles. The pulse width modulation is carried out as follows: the error between the reference current i_{ref} and the sensed current i_s is processed by a PI controller whose input i_c is compared with a ramp compensator i_a. In the boost mode under peak CMC, the switch is turned ON periodically every switching (ramp) period while it is turned OFF whenever $i_c = i_a$, where

$i_a = m_a t \mod T$. In the buck mode under valley CMC, the contrary occurs, i.e., the switch is turned OFF periodically every switching period while it is turned ON whenever $i_c = i_a$. The scheme in Fig. 1 includes the logic circuit for transition from peak CMC to valley CMC [13]. Ideally, in the boost mode under peak CMC, according to (1) or (2a)-(2d), the minimum value of k for avoiding subharmonic oscillation is:

$$k_{\min} = \frac{T}{L}(D - \frac{1}{2}) + \frac{Tv_g}{2Lv_o}, \tag{4}$$

which becomes $k_{\min,1} = T/(2L) = 0.0298$ s/H for $D = 1$ [18]. The outer voltage loop is closed to regulate the output voltage v_o. For this purpose, a compensator, in the form of a PI corrector and an additional first order low pass filter (LPF), is used with a proportional gain $\kappa_p = 0.001$. The corner frequencies of the LPF real pole and the PI real zero are 10 rad/s and 1 rad/s respectively. The output of this controller gives the conductance g for the inner current loop. For completeness, a passive damping is also inserted in the input filter by adding a capacitor $C_d = 44$ μF with an equivalent series resistance $r_d = 5\ \Omega$. Numerical simulations are performed using PSIM to show the effect of the current sensor bandwidth limitation on the dynamical behavior of the system. Fig. 2 shows the waveforms of the system under two different conditions. In the first case, an ideal current sensor is used. In the second case, the current sensor is selected to have a limited bandwidth equal to the switching frequency. To show the effect of this limited bandwidth, a low pass filter is deliberately inserted in the current loop. Note that this filter is also added in practice to remove the switching noise and it is also present in average CMC [31] and in sensorless predictive CMC [33]. While the system with ideal current sensor exhibits stable behavior during the entire line cycle, it exhibits subharmonic oscillation within a large window inside the line period when a limited bandwidth sensor is used. In the following sections a study of this phenomenon is performed and an analytical expression for its occurrence is presented.

III. A GENERAL SIMPLIFIED MODEL FOR THE ELEMENTARY SWITCHING CONVERTERS UNDER CMC WITH FINITE BANDWIDTH

A. Unified modeling of the converter power stage

The tendency in many emerging fields such as in the example of the previous section, in microgrids [34] or distributed power system applications [5] is to interconnect many converters to form high dimensional networked systems more complex than the one considered in the previous section [35]. However, the appropriate operation of the whole network can only be assured by a well design of each individual part. Moreover, under practical conditions, complex networked systems can still be represented by simple models [34]. Although a full-order model can be used, the output voltage of the switching converter is supposed constant for simplicity. This is a practical assumption where the switching period is sufficiently smaller than the time constant corresponding to the load and the filtering capacitor. It is also a representative case in battery charging/discharging and photovoltaic applications [36], [37]. Subharmonic oscillation has been widely addressed in elementary switching converters under current mode control by using the previous approach and considering a first order model representing the dynamics of the inductor current [1]. This approach has also been used for other high order converters such as the current mode controlled single-phase cascaded two-switch buck-boost power factor correction circuit with a time varying input considered in Section II [13]. The equation describing the dynamics of the inductor current is:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = m(t), \tag{5}$$

where $m(t) = v_L/L$, v_L being the inductor voltage supposed to be piecewise constant and L is its inductance. The signal $m(t)$ can be expressed for any switching converter as follows:

$$m(t) = m_s\delta(t) - m_2, \tag{6}$$

where δ is the driving binary signal, with duty cycle D applied to the switch, which is generated by the PWM process. In practice, the control reference i_{ref} is very slowly varying and can be assumed constant within a switching cycle. Also, the inductor current can be considered as a triangular signal and accordingly, the signal m is a square-wave signal with upper value Lm_1 and lower value Lm_2. This square-wave signal is generated by the PWM process.

B. Modeling the current sensor or filter

Consider a current sensor/filter with first order dynamics whose i_L-to-i_s transfer function $H_s(s)$ can be expressed as follows:

$$H_s(s) = \frac{i_s(s)}{i_L(s)} = \frac{\omega_b}{s + \omega_b}. \tag{7}$$

For simplicity, we have selected a sensor static gain equal to 1. If this sensor has a certain amplifying or attenuating factor, it can be easily included in the analysis. Other non-ideal effects, such as propagation delay, can also be included without a significant difficulty. Let $\rho = \omega_b/\omega_s$ be the ratio between the current sensor bandwidth and the angular switching frequency. Therefore, (7) can be expressed by the following differential equation:

$$\frac{\mathrm{d}i_s(t)}{\mathrm{d}t} = \rho\omega_s(i_L(t) - i_s(t)). \tag{8}$$

C. A simplified model with finite bandwidth current sensor

Putting together (5) and (8) and taking into account the above mentioned switching decision, the dynamical behavior of the system can be described by a state-space model that can be expressed as follows:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}m(t) \tag{9}$$

$$i_s(t) = \mathbf{C}\mathbf{x}(t), \tag{10}$$

where $\mathbf{x}(t) = (i_L(t), i_s(t))^\intercal$ is the vector of the state variables and $^\top$ stands for vector transpose. If the output voltage is supposed to be constant or slowly varying, the expressions of matrices $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$ are the same for all elementary converters and only the signal m must be specified for each converter.

IV. Prediction of subharmonic oscillation taking into account limited current sensing bandwidth

A. Critical condition for subharmonic instability

It has been shown in [32] that the critical compensating slope at which subharmonic oscillation takes place in elementary switching converters is given by:

$$m_{a,\mathrm{cri}}(D) = m_s \rho_m(D), \tag{11}$$

where the function $\rho_m(D)$ is given by the following expression:

$$\rho_m(D) = \mathbf{C}[(\mathbf{I} - e^{\mathbf{A}DT})(\mathbf{I} - e^{\mathbf{A}T})^{-1} - (\mathbf{I} + e^{\mathbf{A}T})^{-1}]\mathbf{B} \tag{12}$$

and the system will be stable if the following condition holds:

$$\rho_m(D) < \rho_a(D), \tag{13}$$

where $\rho_a(D) = m_a/m_s$. Note that without ramp compensator, $\rho_a(D) = 0 \ \forall \ D \in (0,1)$ and the system will be stable if $\rho_m(D)$ is negative. The same result is valid for valley CMC by replacing D by $\overline{D} = 1 - D$. The inequality (13) can be considered as a generalized expression of (1) when a finite bandwidth of the current sensor is taken into account. It is interesting to remark that (13) becomes (1) when $\rho = \omega_b/\omega_s$ becomes infinite as it will be shown later.

B. Design-oriented criteria for prediction of subharmonic oscillation occurrence

With CMC and limited-bandwidth current sensor, the dynamics of the inductor current and the limited bandwidth sensor can be described by the following state matrix $\mathbf{A}$ and input and feedback vectors $\mathbf{B}$ and $\mathbf{C}$ respectively:

$$\mathbf{A} = \rho \begin{pmatrix} 0 & 0 \\ \omega_s & -\omega_s \end{pmatrix}, \quad \mathbf{B} = \begin{pmatrix} 1 \\ 0 \end{pmatrix}, \quad \mathbf{C} = (0 \quad 1). \tag{14}$$

The matrix exponential $e^{\mathbf{A}t}$ can be written as follows:

$$e^{\mathbf{A}t} = \begin{pmatrix} 1 & 0 \\ 1 - e^{-t\rho\omega_s} & e^{-t\rho\omega_s} \end{pmatrix}. \tag{15}$$

By substituting the expression of the involved matrices in (12), one obtains:

$$\rho_m(D) = D - \frac{1}{2} + \frac{e^{-2\pi\rho D}(e^{2\pi\rho} + e^{4\pi\rho}) - 2e^{2\pi\rho}}{e^{4\pi\rho} - 1}. \tag{16}$$

From (16), the extremal critical slopes at $D = 0$ and $D = 1$ are given by $m_{a,0} = m_s\rho_m(0)$ and $m_{a,1} = m_s\rho_m(1)$ respectively, where, according to (16), $\rho_m(0)$ and $\rho_m(1)$ can be expressed as follows:

$$\rho_m(0) = \rho_m(1) = \frac{1}{2}\frac{e^{2\pi\rho} - 1}{e^{2\pi\rho} + 1} = \frac{1}{2}\tanh(\pi\rho). \tag{17}$$

The function $\rho_m(D)$ presents a single minimum at a certain duty cycle D_m that can be obtained by taking its derivative with respect to D, equating the result to zero and solving for D. This gives:

$$D_m = 1 + \frac{1}{2\pi\rho}\ln\left(\frac{2\pi\rho}{e^{2\pi\rho} - 1}\right). \tag{18}$$

A careful examination of the expression of D_m reveals that it is a monotonically decreasing function of ρ and that:

$$\lim_{\rho\to\infty} D_m = 0, \quad \lim_{\rho\to 0} D_m = \frac{1}{2}. \tag{19}$$

The second derivative of $\rho_m(D)$ is:

$$\frac{\mathrm{d}^2\rho_m}{\mathrm{d}^2 D} = \frac{4\pi^2\rho^2 e^{-2\pi\rho D}(e^{2\pi\rho} - e^{4\pi\rho})}{e^{2\pi\rho} - 1}. \tag{20}$$

It can be observed that this second derivative is positive and therefore $\rho_m(D)$ is a convex function and its maximum is located at $D = 0$ and $D = 1$. Moreover, one has that:

$$\rho_m(0) = \rho_m(1) = \frac{1}{2}\tanh(\pi\rho) \leq \frac{1}{2}. \tag{21}$$

Therefore one concludes that $\rho_m(D) \leq 1/2 \ \forall D \in (0,1)$ and hence, from (13), by choosing the ramp compensator as follows:

$$m_a = \frac{m_s}{2} = \frac{m_1 + m_2}{2}, \tag{22}$$

the stability of the system will be ensured within all the interval $D \in (0,1)$ and it will not present subharmonic oscillation.

The ideal case of an infinite bandwidth current sensor and without additional filtering effect in the feedback loop can be recovered from the limit of $\rho_m(D)$ when $\rho \to \infty$, i.e.,

$$\lim_{\rho\to\infty} \rho_m(D) \quad = \quad D - \frac{1}{2}. \tag{23}$$

It should be noted that in this case as shown in [1], the critical value of the ramp compensator slope for avoiding subharmonic oscillation for all duty cycles is $m_2/2 \neq m_s/2$. If no slope compensation is used ($\rho_a = 0$), (11) becomes $\rho_m(D) = 0$. By solving this equation in terms of the duty cycle D, the stability limits in terms of this variable can be obtained. By doing so, two different critical values of the duty cycle D can be obtained in general. Both solutions can be expressed by the following expression.

$$D_c = \frac{1}{2}\frac{\mathcal{L}(\rho)\rho(4\pi - 1) + \rho\pi(e^{4\rho\pi} + 4e^{2\rho\pi} - 1)}{\rho\pi(e^{4\rho\pi} - 1)} \tag{24}$$

where $\mathcal{L}(\rho)$ is given by:

$$\mathcal{L}(\rho) = \mathcal{W}\left(\frac{2\rho\pi m_s}{1 - e^{2\rho\pi}} e^{\frac{\rho\pi(e^{4\rho\pi} - 4e^{2\rho\pi})}{e^{4\rho\pi} - 1}}\right) \tag{25}$$

and $\mathcal{W}$ is the Lambert-w function [38]. In the ideal case ($\rho \to \infty$) only one critical value exists which is $D_c = 1/2$ for $m_a = 0$. A similar expression can be derived in the presence of a ramp compensator ($m_a > 0$) and in this case the upper critical value of D_c increases with m_a. In Table II, the expressions for the stability boundary are summarized for different cases.

Fig.3 shows a mesh plot of the function ρ_m in terms of the parameters D and ρ together with the function $D - 0.5$ which corresponds to the ideal case. It can be noticed that the error increases as the parameter ρ decreases. In the low duty cycle range, which has been considered always a *safe* region for peak CMC, the discrepancies between the ideal case and

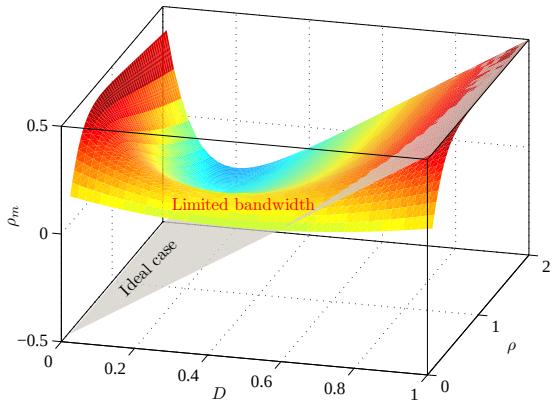


Fig. 3. Mesh plot of the function ρ_m and $D - \frac{1}{2}$ in terms of D and ρ.

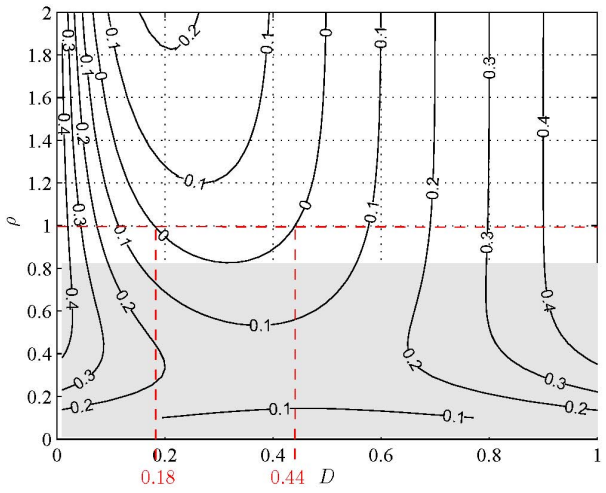


Fig. 4. Contour plot of the function ρ_m in terms of D and ρ showing the values of the contour levels. Within the dashed area the system is unstable for all values of D if no ramp compensator is used.

the case corresponding to a limited bandwidth current sensor are apparent.

Fig. 4 shows a contour plot of the function ρ_m in terms of the parameters D and ρ. It should be noted that in this study we deliberately consider low values of ρ (less than 2) to clearly show the effect of the current sensor bandwidth limitation or filtering in the current loop on the dynamics of the system. The window where the system is free from subharmonic oscillation can be obtained from Fig. 4 by drawing a horizontal line corresponding to a value of ρ and determining its intersections with the contour level numbered by 0. This figure shows that the length of such a window decreases with ρ and becomes zero at $\rho = 0.82$ and the system will be unstable for all values of the duty cycle if no slope compensation is used. For $\rho = 1$, the intersection occurs at the two values of D, $D_{\min} = 0.18$ and $D_{\max} = 0.44$ (shown as vertical lines in Fig. 4). As ρ increases, the minimum value of the duty cycle $D_{\min}$ goes to zero while the maximum value $D_{\max}$ tends to 0.5. The contour plot of Fig. 4 is also useful for selecting the minimum ramp slope to avoid subharmonic oscillation for specific values of D and ρ by using the expression given in (11). According to this expression, the minimum ramp compensator for avoiding subharmonic oscillation for a particular point (D_p, ρ_p) can be obtained by multiplying the value of $\rho_m(D_p, \rho_p)$ (the value numbering the contour) by the value of m_s corresponding to the converter under consideration.

TABLE II
THE CRITICAL STABILITY CONDITIONS FOR DIFFERENT CASES.

Compensation	**Ideal sensor** ($\rho = \infty$)	**Filtering effect** ($\rho < \infty$)
$m_a = 0$	$D = \frac{1}{2}$	$\rho_m(D) = 0$
$m_a \neq 0$	$D = \frac{1}{2} + \frac{m_a}{m_1+m_2}$	$\rho_m(D) = \rho_a, \rho_a = \frac{m_a}{m_s}$

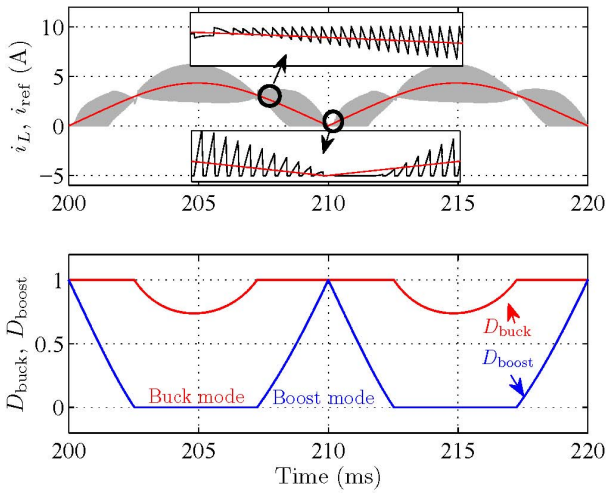


Fig. 5. Time-domain waveforms of the two-switch cascaded buck-boost converter under a CMC and limited bandwidth current sensor showing stable behavior during the entire line period.

V. EXAMPLES

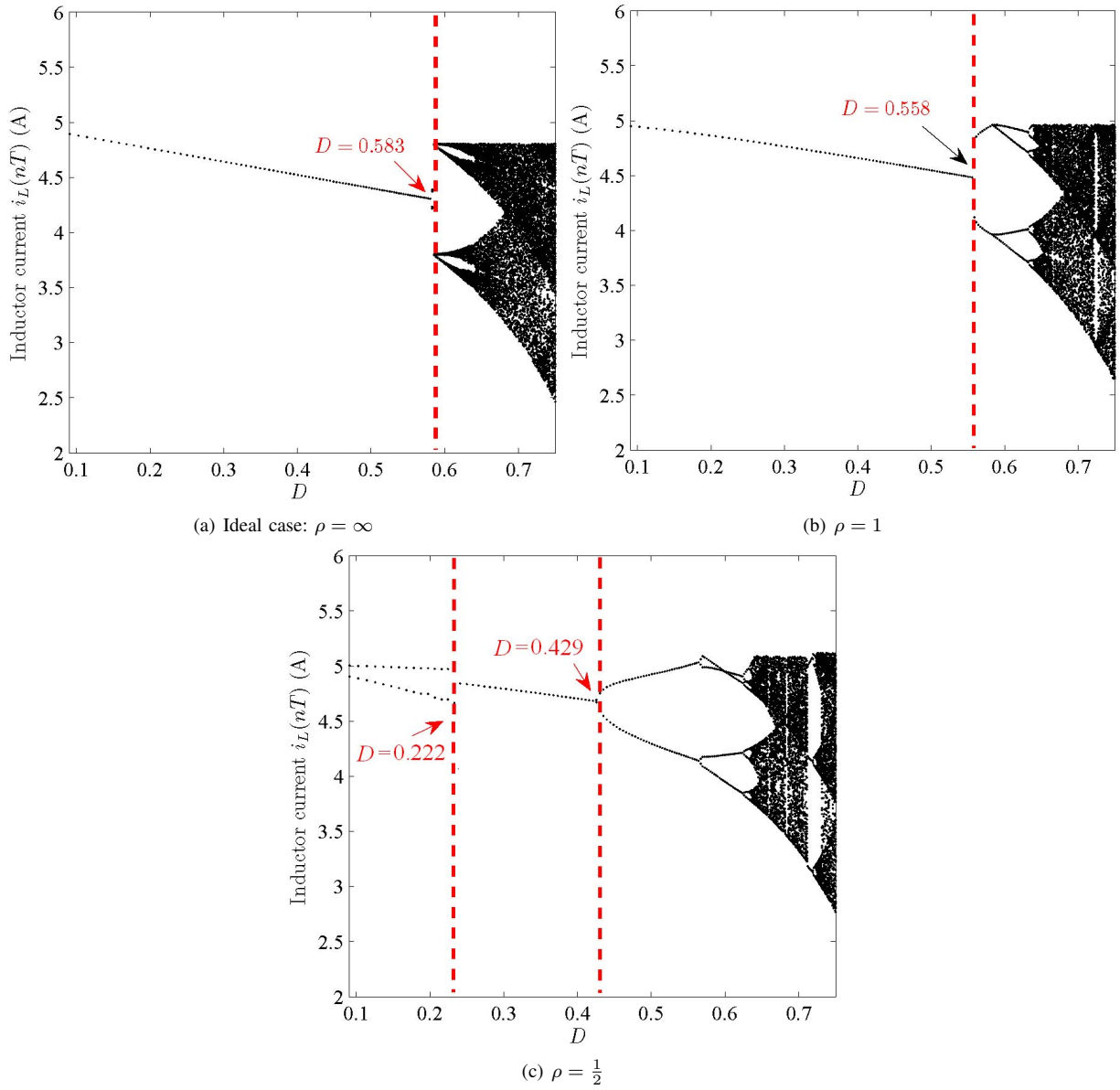
In order to validate the previous theoretical results, different examples of switching converters under CMC are considered in this section.

Example 1: Let us consider the cascaded buck-boost converter in Section II. In the boost mode, the system will exhibit subharmonic oscillation with duty cycle values for which $m_a < v_o \rho_m(D)/L$. Using the expression of m_a in (3) and according to the analysis in the previous section, the minimum value of the parameter k for avoiding subharmonic oscillation is:

$$k_{\min} = \frac{m_s T}{v_o}\rho_m(D) + \frac{T v_g}{2 L v_o}. \tag{26}$$

To guarantee stability at low duty cycle range in the presence of current sensor bandwidth limitation or due to the existence of additional filtering in the feedback loop, the minimum required value of $k_{\min}$ must be derived by imposing $\rho_m(D) = 1/2$ and $D = 0$ (input voltage = output voltage in (26) hence obtaining:

$$k_{\min,0} = k_{\min}|_{D=0} = \frac{T}{L} = 2k_{\min,1}. \tag{27}$$



(a) Ideal case: $\rho = \infty$

(b) $\rho = 1$

(c) $\rho = \frac{1}{2}$

Fig. 6. Bifurcation diagrams for a boost converter under a CMC in terms of D with (a) an ideal current sensor ($\rho = \infty$), (b) with a finite-bandwidth current sensor ($\rho = 1$) and (c) with a finite-bandwidth current sensor with $\rho = 1/2$.

Because the used value of $k_{\min}$ in Section II was $k_{\min,1} < k_{\min,0}$, the system presents subharmonic oscillation near $D = 0$. In the buck mode under valley CMC without ramp compensator and with current sensor bandwidth limited to the switching frequency, the system will present subharmonic oscillation for values of $\overline{D} \in (0.18, 0.44)$, i.e., $D \in (0.56, 0.82)$. In our example, D in the buck mode is varying in the range $(0.77, 1)$ whose subset $(0.77, 0.82)$ corresponds to an instability interval and therefore we observe subharmonic oscillation in the range of the duty cycle $D \in (0.77, 0.82)$ in the buck mode when the current sensor has a limited bandwidth (Fig. 2-b). In order to avoid subharmonic oscillation, the critical ramp compensator slope must be re-calculated by using (11) which for $D = 1$ becomes $m_{a,\text{cri}} = v_o/(2L)$. To validate the previous analysis, time-domain numerical simulations using PSIM are performed for the same system of Section II but with the values of $m_{a,\text{cri}}$ and $k_{\min}$ calculated taking into account current sensor bandwidth limitation. The value of the compensator slope m_a used in the buck mode is $m_{a,\text{cri}} = v_o/(2L) = 208$ kA/s and the gain k used in the boost mode is $k_{\min} = T/L = 0.0595$ s/H. The resulting waveforms are shown in Fig. 5. It can be observed that the subharmonic oscillation have been successfully avoided and that the system exhibits stable behavior within the entire line cycle.

Example 2: Consider a boost converter under CMC with the following parameter values: inductance $L = 500$ μH, input voltage $v_g = 10$ V, switching frequency $f_s = 20$ kHz, peak reference current $i_{\text{ref}} = 5$ A and ramp compensator slope $m_a = 4$ kA/s. The duty cycle is varied in the range (0.1, 0.75) by changing the output voltage in the range (11, 40) V and the bifurcation diagrams of the system are obtained for an ideal current sensor and for a system with a limited bandwidth

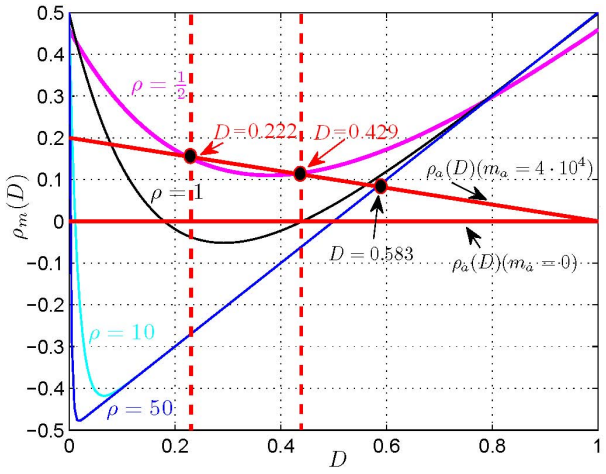


Fig. 7. The function $\rho_m(D)$ in terms of the duty cycle D for different values of ρ together with $\rho_a(D)$ and some critical points from Example 1.

current sensor. The results are shown in Fig. 6 for $\rho=\infty$, $\rho=1$ and $\rho=1/2$. For the above values of parameters, the system with an ideal current sensor ($\rho=\infty$) is stable within the range $(0, 0.583)$ of the duty cycle as it is depicted in Fig. 6-a which is in perfect agreement with (1) and (2a)-(2d) or Table II. Note that in this case a ramp compensator is used and the upper limit of the duty cycle for stability is greater than 0.5. However, with a limited bandwidth (finite ρ), this upper limit of the duty cycle decreases with ρ as shown in Fig. 6-b and Fig. 6-c. For instance, for $v_o=22$ V ($D\approx0.55$), the system with an ideal current sensor would be stable according to (1). However, for $\rho=1/2$ the bifurcation diagram of Fig. 6-c shows that the system is free from subharmonic oscillation only within the interval $D\in(0.24, 0.43)$ whose limits are indicated as vertical dashed lines and that at $D=0.55$ it already exhibits subharmonic oscillation in agreement with the previous analysis. In conclusion, the required ramp for stabilizing the system is different from that predicted by (1).

Fig. 7 shows the function $\rho_m(D)$ in terms of the duty cycle D for different values of ρ together with $\rho_a(D)$. The vertical dashed lines in this figure indicate the stable interval of the duty cycle for $\rho=1/2$. For very large values of ρ ($\rho=50$ for example), the critical value of the duty cycle is $D=0.583$ in good agreement with the bifurcation diagram of Fig. 6-a. A remarkable matching can be observed comparing Fig. 7 and Fig. 6 in all the cases.

Let us now fix $\rho=1/2$ and check the stability of the system in terms of the compensating slope. According to (13), for $v_o=15$ V ($D=0.33$), subharmonic oscillation can be avoided by selecting $m_a>3\cdot10^4\rho_m(0.33)$, i.e., $m_a>3.42$ kA/s. Fig. 8 shows the time-domain waveforms of the system before and after the occurrence of subharmonic instability for $m_a=3.6$ kA/s and $m_a=3.4$ kA/s respectively.

For $v_o=12$ V ($D\approx0.17$), subharmonic oscillation can be avoided by selecting a compensating slope $m_a>24\cdot10^3\rho_m(0.17)=4.77$ kA/s which is *larger* than the one needed for the *larger* duty cycle $D=0.33$. For the boost converter $m_s=v_o/L$. The system will not present subharmonic oscillation if the ramp slope is selected to be $m_a>v_o/(2L)$. For instance for $v_o=22$ V, $m_s=44$ kA/s so that the slope of the artificial ramp should be selected larger than 22 kA/s.

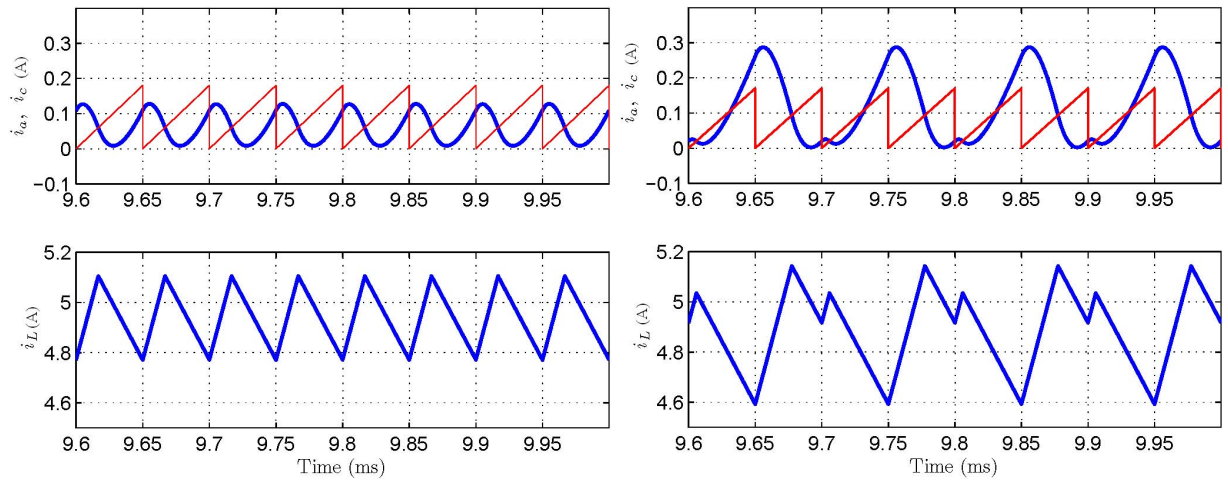
Finally, it should be noted that an independent small-signal analysis for $\rho=0.5$ based on Floquet theory shows that the system has one stable discrete-time eigenvalue for the entire range of the duty cycle and another one which is stable only within the window $D\in(0.222, 0.423)$. This is in perfect agreement with the results shown in Fig. 6-c and Fig. 7.

Example 3: Now, consider a buck converter under CMC with the following parameter values: peak current reference $i_c=5$ A, inductance $L=3.3$ μH, input voltage $v_g=15$ V, switching frequency $f_s=100$ kHz and $m_a=60$ kA/s. The duty cycle is varied in the range (0.1, 0.6) by varying the output voltage in the range (2.5, 9) V. The function $\rho_m(D)$ is plotted for three different values of current sensor bandwidth corresponding to $\rho=1/2$, $\rho=1$ and $\rho=2$. The resulting curves are shown in Fig. 9. In this figure, the horizontal lines stand for the values of ρ_a with and without ramp compensation. Similar effects of the finite bandwidth as in the previous examples of the boost converter can be observed. In particular, the system will only be stable within an interval of duty cycles whose minimum value D_{cm} and maximum value D_{cM} are given by the crossing points between ρ_m and ρ_a and the following remarks can be drawn:

- With finite bandwidth of the current sensor, the lower stability limit of the duty cycle D decreases when the bandwidth of the sensor increases and $D_{cm}\to0$ when $\rho\to\infty$. Concerning the upper limit D_{cM} it increases when the bandwidth of the sensor increases and $D_{cM}\to0.5$ when $\rho\to\infty$.
- The stability window in terms of the duty cycle D gets wider by increasing the compensator slope m_a for a fixed value of ρ. Note however that while in the ideal case no slope compensation is needed for $D<0.5$, with current sensor bandwidth limitation, a slope compensation is needed even for $D<0.5$ and that a good design using a traditional approach could be damaged by an inappropriate current sensor or by inserting filters in the current loop.

VI. Experimental Validation

In order to verify the theoretical and simulation results presented previously, a laboratory prototype of a buck converter has been built and several experimental tests have been performed on this converter. Fig. 10 shows the circuit diagram of the implemented system. The parameter values are those of Example 3 in the previous section and the used output capacitance is $C=500$ μF and the load resistance is $R=1$ Ω. The output voltage loop is closed by using a typical type II controller $H_v(s)=W_v(s+\omega_z)/(s(s+\omega_p))$. The corner frequencies of the pole and the zero are $\omega_p=21.27$ krad/s and $\omega_z=10$ krad/s respectively and the gain of the controller is $W_v=\omega_p$. The duty cycle is varied by changing the reference voltage of the outer voltage loop. The current sensor used is the IC commercial chip AD8210 whose bandwidth is



(a) $m_a = 3.6$ kA/s. (b) $m_a = 3.4$ kA/s.

Fig. 8. Time-domain waveforms of a boost converter under a CMC with a finite-bandwidth current sensor ($\rho = 1/2$) and $D = 0.33$ for different values ramp compensator slopes.

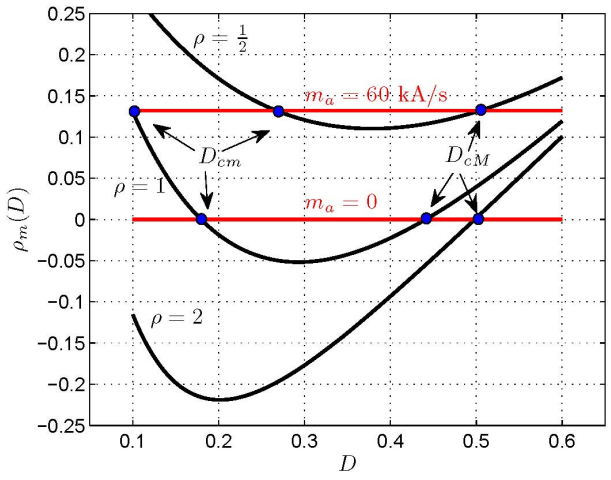


Fig. 9. The function $\rho_m(D)$ together with $\rho_a(D)$ corresponding to Example 3 in terms of the duty cycle D for three different values of ρ.

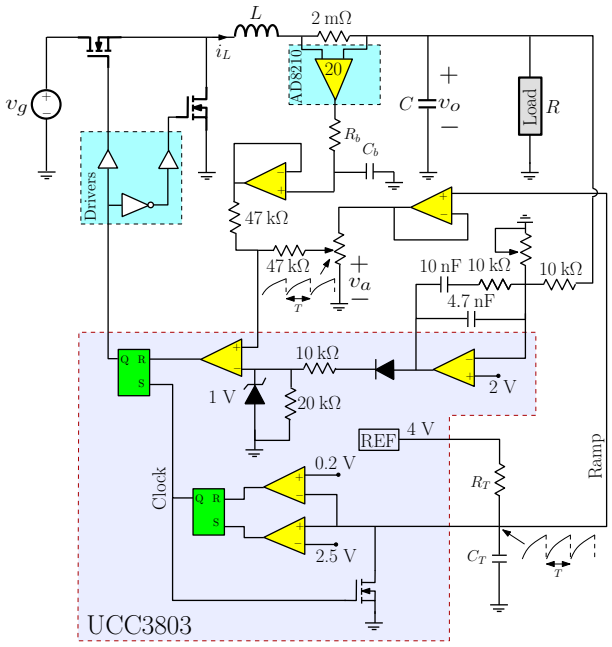
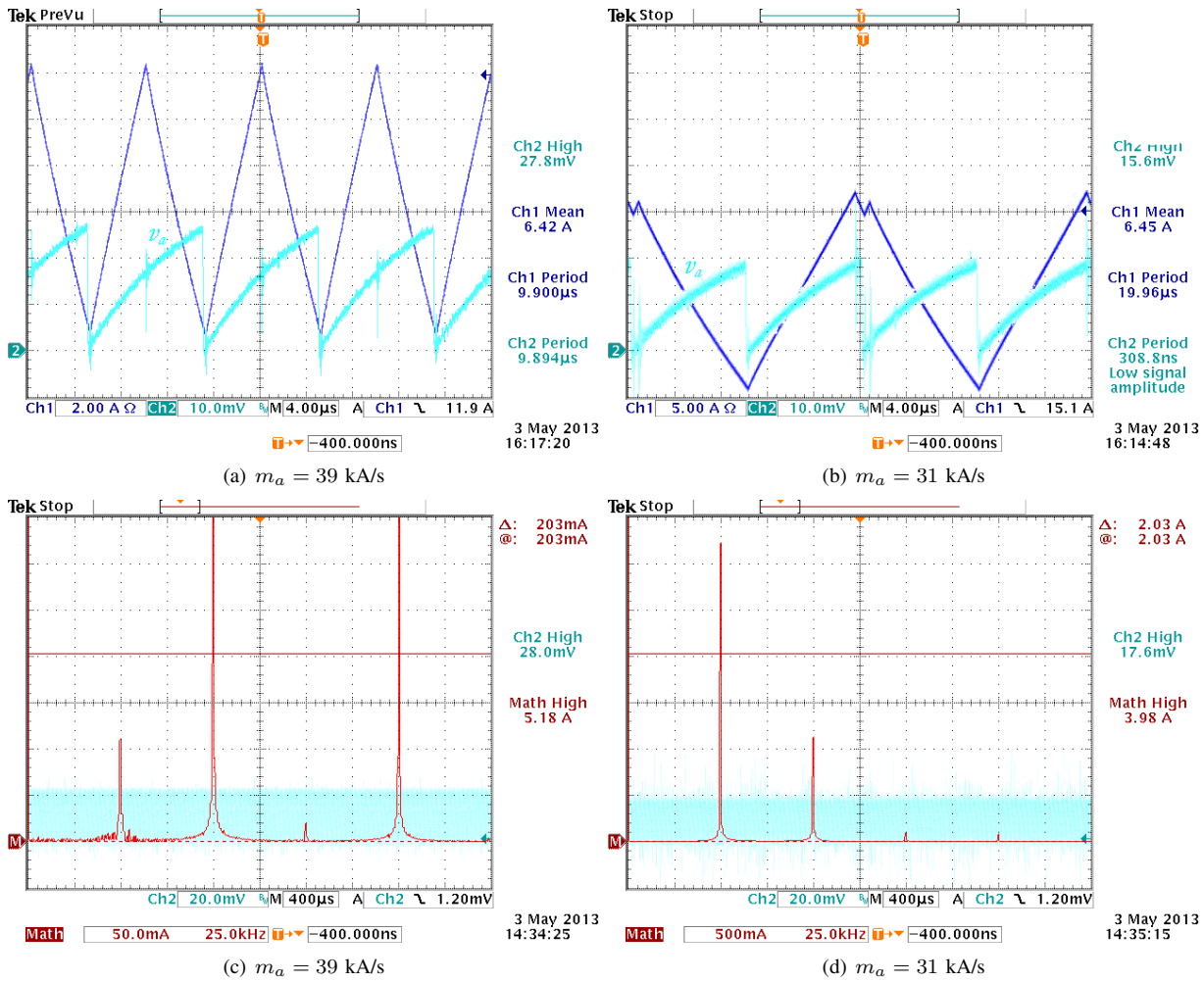


Fig. 10. Schematic circuit diagram of the implemented buck converter prototype under CMC.

$\omega_{\rm bw}$ =450 kHz. To study the effect of the current sensor on the system dynamics, we can use a switching frequency close $\omega_{\rm bw}$ or to place a filter at the output of the current sensor. In order to avoid switching noise and to have clean waveforms, the second option was preferred. A first order RC filter is added at the output of this sensor. The resistance R_b of this filter is fixed at $R_b = 16.5$ kΩ while the capacitor C_b is changed to provide three different values of sensor bandwidth corresponding to $\rho = 1/2$, $\rho = 1$, and $\rho = 2$ by choosing $C_b = 200$ pF, $C_b = 100$ pF, and $C_b = 50$ pF respectively. The ramp compensator has been implemented by using the UCC3803 device and the switching frequency has been fixed to $f_s = 100$ kHz by choosing $R_T = 100$ kΩ and $C_T = 100$ pF. The ramp can either be subtracted from the reference current $i_{\rm ref}$ or added to the sensed current i_s. In the first case, the inductor current i_s is compared with $i_{\rm ref} - i_a$. In the second case the signal $i_{\rm ref} - i_s$ is compared with i_a. Since in our implementation all the controller signals must be between 0 and 5 V we have selected the second option.

Several tests were made with the three different values of the sensor bandwidth. To detect the occurrence of the first subharmonic appearance, the ratio of the harmonic at $\omega_s/2$ and that at ω_s was used. The threshold value for this ratio used for the experimental detection of subharmonic occurrence has been selected to 5%. It is worth mentioning that in the time-domain this detection is more inaccurate because noise would significantly affect the measurements. Our tests proved that the results from the FFT measurements provided by a Tektronix oscilloscope allow more easily to discriminate the previously established threshold amplitude. The duty cycle



(a) $m_a = 39$ kA/s (b) $m_a = 31$ kA/s

(c) $m_a = 39$ kA/s (d) $m_a = 31$ kA/s

Fig. 11. Experimental time-domain waveforms (a,b) and the corresponding FFT spectra (c,d) just when the established harmonics threshold is reached (a,c) and just after the subharmonic oscillations is visible in the time-domain waveforms (b,d). $\rho = 1$. v_o=6.82 V ($D \approx 0.455$).

corresponding to these figures is $D \approx 0.455$. From Fig. 9, the minimum ramp slope needed for this value of the duty cycle is $m_a \approx 36$ kA/s. Fig. 11 shows the time-domain waveforms and the corresponding FFT spectra just when the established harmonics threshold is reached and just after when the subharmonic oscillations are visible in the time-domain waveforms. The boundaries of subharmonic oscillation have been detected by decreasing the ramp compensator amplitude till the threshold value of the harmonics ratio is reached. Fig. 12 shows the experimentally obtained values of $\rho_m(D)$ in terms of some values of the duty cycle and for the three values of ρ. The theoretical curves are also plotted for comparison. Although a good matching can be observed if the shape of the curves are compared, there are many other parasitic elements that cause the results to mismatch. This mismatching can mainly be attributed to the losses in the components, small delays in the MOSFETs response and non modeled dynamics of the current sensor. Another source of error could be the curved shape of the compensator ramp but its effect has been taken into account for plotting Fig. 12 by multiplying the function $\rho_m(D)$ obtained experimentally by a term proportional to e^{-D}. The values of $\rho_m(D)$ obtained by considering the dynamics of the output voltage and its controller [39] are also shown in the same figure for values of output capacitance $C = 47$ μF, 100 μF and 500 μF showing a remarkable agreement with the results obtained from the simplified model. As the output capacitance is increased, the results from the full-order model approaches the ones corresponding to the reduced-order model. In particular, when $C = 500$ μF, the results are almost coincident.

VII. Conclusions

Subharmonic oscillation in switching converters is investigated in this paper by taking into account current sensor bandwidth limitation. An extended expression for predicting this phenomenon is proposed. After introducing the imperfection due to the current sensor bandwidth limitation, a simplified reduced-order model is proposed for the three elementary switching converters. Despite the apparent simplicity of the model, the theoretical results show a satisfactory agreement with the bifurcation diagrams obtained from time-domain numerical simulations. The current sensor bandwidth limitation is included in the study and its effects on stability boundary are examined. Although, the study was focused on

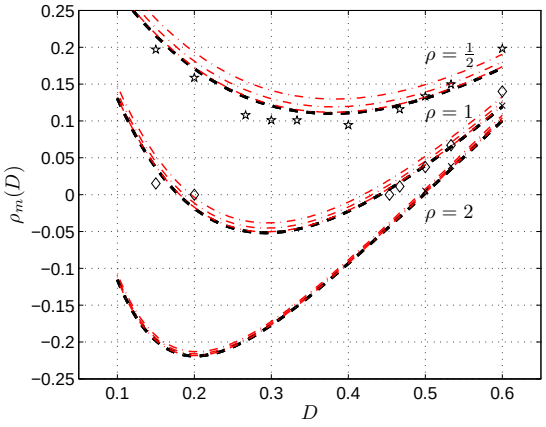


Fig. 12. The function $\rho_m(D)$ in terms of the duty cycle D obtained from theoretical analysis and experimentally ($\star$ for $\rho = 1/2$, $\diamond$ for $\rho = 1$ and $\times$ for $\rho = 2$). Dashed lines correspond to the values of $\rho_m(D)$ obtained by considering the dynamics of the output voltage and its controller for different values of output capacitance.

peak and valley current mode control, the results are also useful for the case of average current mode control where a filter is placed near the switching frequency to limit noise injection. This is also the case of buck converters under PID voltage mode control where the ideal derivative action is modified by inserting in the loop a low-pass filter and that of sensorless CMC where the estimation of the current also involves a bandwidth limitation. The proposed expression for the stability boundary is able to catch properly and accurately the subharmonic oscillation occurrence in switching converters both at high and low values of the duty cycle in peak, valley and average current mode control. While it is broadly believed that subharmonic oscillation can be avoided by a limited bandwidth filtering in the practical circuit, it is demonstrated in this study that these filtering effects could be responsible for this phenomenon. Experimental results obtained from a laboratory prototype corroborate the theoretical predictions and the numerical simulations. Further studies will also deal with the effect of more complex models of the current sensor on the stability boundaries of switching converters.

REFERENCES

[1] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed, Springer, 2001.

[2] F. D. Tan, R. D. Middlebrook, "A Unified Model for Current-Programmed Converters," *IEEE Trans. Power Electron.,* vol. 10, no. 4, pp. 397-408, 1995.

[3] D. J. Perreault, G. C. Verghese, "Time-Varying Effects and Averaging Issues in Models of Current-Mode Control," *IEEE Trans. Power Electron.,* vol. 12, no. 3, pp. 453-461, 1997.

[4] S. C. Smithson, S. S. Williamson, "A Unified State-Space Model of Constant-Frequency Current-Mode-Controlled Power Converters in Continuous Conduction Mode," *IEEE Trans. Ind. Electron.,* vol. 62, no. 7, pp. 4514-4524, 2015.

[5] B. Choi, B. H. Cho, and S.-S. Hong, "Dynamics and Control of DC-to-DC Converters Driving Other Converters Downstream," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 10, pp. 1240-1248, 1999.

[6] B. Lehman and R. M. Bass, "Switching Frequency Dependent Averaged Models for PWM DC-DC Converters," *IEEE Trans. Power Electron.,* vol. 11, no. 1, pp. 89-98, 1996.

[7] R. Redl and J. Sun, "Ripple-Based Control of Switching Regulators - An Overview," *IEEE Trans. Power Electron.,* vol. 24, no. 12, pp. 2669–2680, 2009.

[8] G. Zhou; J. Xu and Y. Jin, "Elimination of Subharmonic Oscillation of Digital-Average-Current-Controlled Switching DC-DC Converters," *IEEE Trans. Ind. Electron.,*, vol. 57, no. 8, pp. 2904-2907, 2010.

[9] H. Li, Y. Liu, J. Lu. T. Zheng, X. Yu, "Suppressing EMI in Power Converters via Chaotic SPWM Control Based on Spectrum Analysis Approach," *IEEE Trans. Ind. Electron,* vol. 61, no. 11, pp. 6128-6137, 2014.

[10] F. Xie, B. Zhang, R. Yang, H.C. Iu, "Detecting Bifurcation Types and Characterizing Stability in DC-DC Switching Converters by Duplicate Symbolic Sequence and Weight Complexity," *IEEE Trans. Ind. Electron.,* vol. 60, no. 8, pp. 3145-3156, 2013.

[11] K. Mandal, S. Banerjee, C. Chakraborty, "A New Algorithm for Small-Signal Analysis of DC-DC Converters," *IEEE Trans. Ind. Informat,* vol. 10, no. 1, pp. 628-636, 2014.

[12] O. Dranga, B. Buti, and I. Nagy, "Stability Analysis of a Feedback Controlled Resonant DC-DC Converter," *IEEE Trans. Ind. Electron.,* vol. 50, no. 1, pp. 141-152, 2003.

[13] G. K. Andersen and F. Blaabjerg, "Current Programmed Control of a Single-Phase Two-Switch Buck-Boost Power Factor Correction Circuit," *IEEE Trans. Ind. Electron.,*, vol. 53, no. 1, pp. 263-271, 2006.

[14] W. Cheng, J. Song, H. Li; Y. Guo, "Time-Varying Compensation for Peak Current-Controlled PFC Boost Converter," *IEEE Trans. Power Electron.,* vol. 30, no. 6, pp. 3431-3437, 2015.

[15] C. K. Tse and M. Lai, "Controlling Bifurcations in Power Electron.. A Conventional Approach Re-visited," *Latin American Applied Research,* vol. 31, pp. 177-184, 2001.

[16] B. Holland, "Modelling, Analysis and Compensation of the Current-Mode Converter," *Proc. Powercon,* vol. 11, no. I2-1-I-2-6, 1984.

[17] W.-G Lu, S. Lang, A. Li and H. H-C. Iu, "Limit-Cycle Stable Control of Current-Mode DC-DC Converter with Zero-Perturbation Dynamical Compensation," *Int. Journal of Circuit Theory and Applications*, early view, 2014.

[18] W.-G Lu, S. Lang ; L. Zhou, H. H-C Iu, T. Fernando, "Improvement of Stability and Power Factor in PCM Controlled Boost PFC Converter with Hybrid Dynamic Compensation," *IEEE Trans. Circuits and Systems I: Regular Papers,* vol. 62, no. 1, pp. 320-328, 2015.

[19] Z. Qin-Chang Zhong, T. Hornik, "Cascaded Current-Voltage Control to Improve the Power Quality for a Grid-Connected Inverter With a Local Load," *IEEE Trans. Ind. Electron.,* vol. 60, no. 4, pp. 1344,1355, 2013.

[20] J. Ejea-Marti, E. Sanchis-Kilders, E. Maset, A. Ferreres, J. Manuel Blanes, A. Jordan, and V. Esteve, "Phase Margin Degradation of a Peak Current Controlled Converter at Reduced Duty Cycle," *IEEE Trans. Power Electron.,* vol. 25, no. 4, pp. 863-874, 2010.

[21] Y.-P. Hsieh, J.-F. Chen, L.-S Yang, C.-Y. Wu; W.-S Liu, "High-Conversion-Ratio Bidirectional DC-DC Converter With Coupled Inductor," *IEEE Trans. Ind. Electron.,* vol. 61, no. 1, pp.210-222, 2014.

[22] A. Shahin, M. Hinaje, J.-P. Martin, S. Pierfederici, S. Raël B. Davat, "High Voltage Ratio DC-DC Converter for Fuel-Cell Applications," *IEEE Trans. Ind. Electron.,* vol. 57, no. 12. pp. 3944-3955, 2010.

[23] A. Leon-Masich, H. Valderrama-Blavi, J. M. Bosque-Moncusi, J. Maixe-Altes and L. Martinez-Salamero, "Sliding-Mode-Control-Based Boost Converter for High-Voltage-Low-Power Applications," *IEEE Trans. Ind. Electron.,* vol. 62, no. 1, pp. 229-237, 2015.

[24] J. Sun, "Characterization and Performance Comparison of Ripple-Based Control for Voltage Regulator Modules," *IEEE Trans. Power Electron.*, no. 2, vol. 21, pp. 346-353, 2006.

[25] T. Qian, "Subharmonic Analysis for Buck Converters With Constant On-Time Control and Ramp Compensation," *IEEE Trans. Industrial Electronics,* vol.60, no.5, pp. 1780-1786, 2013.

[26] K. Yao, Yang Qiu, M. Xu, and F. C. Lee, "A Novel Winding-Coupled Buck Converter for High-Frequency, High-Step-Down DC-DC Conversion," *IEEE Trans. Power Electron.,* vol. 20, no. 5, pp. 1017-1024, 2005.

[27] H. Pooya Forghani-Zadeh, and G. A. Rincón-Mora, "Current-Sensing Techniques for DC-DC Converters," *The 2002 45th Midwest Symposium on Circuits and Systems,* 2002, MWSCAS-2002. vol. 2 pp:II-577 - II-580.

[28] F. Grecki, G. Iwanski, W. Koczara, J. Lastowiecki, "Technologies of Current Sensors Suitable for Hot High Density Power Electron.," *2008 13th Power Electron. and Motion Control Conference,* EPE-PEMC 2008. pp. 1440-1445, Sept. 2008.

[29] http://www.ti.com/lit/ds/symlink/ina286

[30] http://www.farnell.com/datasheets/51640.

[31] W. Tang, F. Lee, and R. Ridley, "Small-Signal Modeling of Average Current-Mode Control," *IEEE Trans. Power Electron.,* vol. 8, no. 2, pp. 112-119, 1993.

[32] A. El Aroudi, J. Calvente, R. Giral and L. Martínez-Salamero, "Effects of Non-ideal Current Sensing on Subharmonic Oscillation Boundary in DC-DC Switching Converters Under CMC," *IEEE Ind. Electron. Conference (IECON'2013)*, pp. 8367-8372, Nov. 2013.
[33] Q. Zhang, R. Min, Q. Tong, X. Zou, Z. Liu, A. Shen, "Sensorless Predictive Current Controlled DC-DC Converter With a Self-Correction Differential Current Observer," *IEEE Trans. Ind. Electron.,* vol. 61, no. 12, pp. 6747-6757, 2014.
[34] T. B. Pavlovič, T. Bjažić, Z. Ban, "Simplified Averaged Models of DC-DC Power Converters Suitable for Controller Design and Microgrid Simulation," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3266-3257, 2013.
[35] J. Lu, G. Chen, "A Time-Varying Complex Dynamical Network Model and its Controlled Synchronization Criteria," *IEEE Transactions on Automatic Control,* vol. 50, no. 6, pp.841-846, 2005.
[36] M. Yilmaz and P. T. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," *IEEE Trans. Power Electron.,* vol. 28, no. 5, 2013.
[37] T. Maeda and T. Saito, "Analysis of Stability and Bifurcation in a Simple Model of Power Converters with Solar Cell Input," *IEEE Ind. Electron. Conference,* pp. 356-362, Nov. 2010.
[38] D. Veberič, "Lambert W Function for Applications in Physics," 2012, available at http://arxiv.org/pdf/1209.0735v1.pdf http://mathworld.wolfram.com/LambertW-Function.html.
[39] A. El Aroudi, "Prediction of Subharmonic Oscillation in Switching Converters Under Different Control Strategies," *IEEE Trans. Circuits and Systems II: Express Briefs,* vol. 62, no. 11, pp. 910-914, 2014.

Abdelali El Aroudi (M'00-SM'13) was born in Tangier, Morocco, in 1973. He received the graduate degree in physical science from Facultt'e des sciences, Université Abdelmalek Essaadi, Tetouan, Morocco, in 1995, and the Ph.D. degree (hons) from Universitat Polit'ecnica de Catalunya, Barcelona, Spain in 2000. During the period 1999-2001 he was a Visiting Professor at the Department of Electronics, Electrical Engineering and Automatic Control, Technical School of Universitat Rovira i Virgili (URV), Tarragona, Spain, where he became an associate professor in 2001 and a full-time tenure Associate Professor in 2005. From September 2007 to January 2008 he was holding a visiting scholarship at the Department of Mathematics and Statistics, Universidad Nacional de Colombia, Manizales, conducting research on modeling of power Electronics circuits for energy management. From February 2008 to July 2008, he was a visiting scholar at the Centre de Recherche en Sciences et Technologies de Communications et de lt'Informations (CReSTIC), Reims, France. From September 2014 to December 2014, he was a visiting scholar at Institut National des Sciences Appliquées (INSA), Université of Toulouse, France and the Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS) of the Centre National de la Recherche Scientifique (CNRS), Toulouse, France. From January 2015 to July 2015, he was a visiting professor at The Petroleum Institute, Abu Dhabi, UAE. His research interests are in the field of structure and control of power conditioning systems for autonomous systems, power factor correction, stability problems, nonlinear phenomena, chaotic dynamics, bifurcations and control. He was a Guest Editor of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems Special Issue on Design of Energy-Efficient Distributed Power Generation Systems (September 2015). He is also serving as Associate Editor in *IEE IET Power Electronics.*

Javier Calvente (S'94-M'04) received the Ingeniero de Telecomunicación degree and the Ph.D. degree from the Universitat Politècnica de Catalunya, Barcelona, Spain, in 1994 and 2001, respectively. He was a visiting scholar with Alcatel Space Industries, Toulouse, France, in 1998. He is currently an Associate Professor with the Departamento d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Tarragona, Spain, where he is working in the fields of power electronics and control systems.

Roberto Giral (S'94-M'02-SM'10) received the B.S. degree in ingeniería técnica de telecomunicación, the M.S. degree in ingeniería de telecomunicación, and the Ph.D. (Hons.) degree from the Universitat Politècnica de Catalunya, Barcelona, Spain, in 1991, 1994, and 1999, respectively. He is currently an Associate Professor at the Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Escola Tècnica Superior d'Enginyeria, Universitat Rovira i Virgili, Tarragona, Spain, where he is working in the field of power electronics.

Mohammed S. Al-Numay (M'04) was born in Riyadh, Saudi Arabia. He received the B.S. degree (with honors) from King Saud University, Riyadh, Saudi Arabia, in 1986, the M.S. degree from Michigan State University, East Lansing, MI, in 1990, and the Ph.D. degree from Georgia Institute of Technology, Atlanta, GA, in 1997, all in electrical engineering. During the period 2002-2006, he was the Dean of Admissions and Registration at King Saud University. From 2008, he is a Senior Consultant of Student Information Systems (SIS) to many governmental and private universities and colleges. Since 1998, he has been with the Electrical Engineering Department at King Saud University, where he is now an Associate Professor. His research interests include discrete-time modeling, nonlinear dynamics, modelling and control of PWM systems, and digital control of non-minimum phase systems.

Luis Martínez-Salamero (S'86-M'88-SM'12) received the Ingeniero de Telecomunicacit'on degree in 1978 and the Ph.D. degree in 1984, both from the Universidad Politt'ecnica de CataluŸna, Barcelona, Spain. From 1978 to 1992, he taught circuit theory, analog electronics and power processing at the Escuela Tt'ecnica Superior de Ingenieros de Telecomunicacit'on de Barcelona, Barcelona. From 1992 to 1993, he was a Visiting Professor in the Center for Solid State Power Conditioning and Control, Department of Electrical Engineering, Duke University, Durham, NC, USA. From 2003 to 2004 and 2010 to 2011, he was a Visiting Scholar in the Division of Power Devices and Power Integration of the Laboratory of Architecture and Systems Analysis, National Agency for Scientific Research, Toulouse, France. Since 1995, he has been a Full Professor in the Department of Electrical Electronic and Automatic Control Engineering, School of Electrical and Computer Engineering, Rovira i Virgili University, Tarragona, Spain, where he is the Director of the Research Group in Industrial Electronics and Automatic Control. His research interests include structure and control of power conditioning systems, namely, electrical architecture of satellites and electric vehicles, as well as nonlinear control of converters and drives, and power conditioning for renewable energy. Dr. Martínez-Salamero has published a large number of papers in scientific journals and conference proceedings in the fields of modeling, simulation, and control of power converters, and holds a U.S. patent on dual voltage electrical distribution in vehicles. He was a Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS SPECIAL ISSUE ON SIMULATION, THEORY AND DESIGN OF SWITCHED-ANALOG NETWORKS (August 1997). He organized in cooperation with the European Space Agency the 5th European Space Power Conference (ESPC-98) in Tarragona and served during two terms (1996-2002) as a Dean of the School of Electrical and Computer Engineering. He was the President of Spanish Joint Chapter of the IEEE Power Electronics and Industrial Electronics Societies from 2005 to 2008, and Distinguished Lecturer of the IEEE Circuits and Systems Society in the period 2001-2002. He is currently a Distinguished Professor of Rovira i Virgili University.