Optimal Decoupled Discontinuous Modulation for StatComs Based on the Cascaded H-Bridge Converter

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***Abstract*—Conventional discontinuous pulse width modulation (DPWM) strategies for cascaded H-bridge static compensators suffer from poor inter-phase capacitor voltage balance control during unbalanced grid voltage conditions. Specifically, the logic-based algorithm that calculates the zero-sequence voltage (ZSV) for discontinuous operation interacts with the closed-loop capacitor voltage control. This paper proposes an optimal DPWM strategy based on a finite-set optimization that chooses the best ZSV candidate that minimizes the control interactions while clamping a converter voltage. Furthermore, the effect of the different ZSV candidates on the switching loss is also considered within the optimization. Extensive experimental study is provided to demonstrate the effectiveness of the proposed approach.**

***Index Terms*—Cascaded H-Bridge (CHB), discontinuous pulse width modulation (DPWM), finite-set optimization, static compensator (StatCom)**

I. Introduction

Static synchronous compensators (StatComs) are well-known grid voltage regulation devices in transmission and distribution systems [1]–[4]. Cascaded H-bridge (CHB) converter is considered a promising topology for StatComs due to its modularity and relatively low component count [1]–[4].

Discontinuous pulse width modulation (DPWM) techniques have attracted interest for their effectiveness in reducing switching loss, enhancing converter reliability and improving power quality [5]–[12]. Particularly, in a three-phase CHB converter with star configuration, DPWM can be achieved by injecting a specific zero-sequence voltage (ZSV) that ceases the switching action of a converter leg for a period of time. Various DPWM methods have been reported for three-phase inverters, such as the two-level voltage source inverter (VSI), the CHB based VSI and the neutral-point-clamped (NPC) inverter [7]–[16]. Particularly, [7] and [8] analytically evaluate the harmonic distortion and switching loss of different DPWM methods in a two-level VSI, and propose a generalized method for improving DPWM performance in high modulation range. Reference [16] compares different DPWMs analyzed in [8] for the CHB StatCom application, and concludes that the one called "DPWM3" presents the best performance in terms of switching loss reduction. References [9] and [10] apply the conventional 60° DPWM (referred as convention DPWM henceforth) to reduce the switching loss in the CHB based VSI. Approaches in [12] and [13] improve the conventional DPWM for its application in the three-level NPC converter considering capacitor voltage balance. However, the DPWM strategies in [7]-[16] cannot be straightforwardly applied to the CHB StatComs because of the different natures of encountered problems. Particularly, the applications in [9]-[10] assume constant voltage sources instead of floating capacitor voltages as in the CHB StatCom, thus the DPWM implementation does not cause capacitor voltage balance problem. The study in [16] only considers balanced grid conditions, and due to the three-phase symmetry characteristics, the negative effects of DPWM implementation on capacitor voltage balance in CHB StatComs are not highlighted. The DPWM methods in [11]-[14] are proposed for balancing the two capacitor voltages that constitute the dc-link of a three-level NPC inverter. However, similar to the two-level VSI, the three legs in the NPC inverter share a common dc-link, whereas the CHB StatComs have floating capacitors on three individual legs that need to be balanced (both inter- and intra-leg), which is especially intricate in unbalanced grid conditions. In fact, each individual submodule (SM) in a CHB StatCom has a floating capacitor at its dc-side, and all the capacitor voltages must be controlled through a feedback loop for a correct operation of the CHB StatCom [17], [18]. Particularly, the capacitor voltage control task is usually subdivided into three main controllers, viz., a

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total energy control, an inter-phase balancing control, and an inter-SM balancing control [17], [18].

In the conventional DPWM approach for CHB StatComs reported in [19], the ZSV is calculated by two different control modules. Specifically, i) the inter-phase balancing control calculates a fundamental-frequency ZSV (FFZSV), while ii) a logic-based algorithm calculates a piecewise continuous ZSV to enable the discontinuous operation of the CHB StatCom. The two control modules present a nonnegligible coupling when operating under unbalanced grid voltage conditions, as the logic-based algorithm introduces an unwanted FFZSV that interacts with the inter-phase balancing control. The inter-phase balancing control tries to compensate for this unwanted FFZSV, which translates into a compromised system stability and poor performance, especially during abrupt transients such as grid voltage sags/swells. To overcome the interaction between the two control modules, a DPWM strategy is proposed in [20], [21]. Despite the fact that the strategy has similar hierarchical control scheme as in [19], it eliminates the fundamental-frequency component in the ZSV for DPWM by introducing an extra degree of freedom in the ZSV generation in the form of an additional switching event. Despite successfully decoupling control, the performance of the DPWM in [20] and [21] highly depends on the phase-angle and frequency of the triangular carrier used to introduce the extra switching event. The challenge of finding the optimal carrier parameters renders the DPWM in [20], [21] less attractive in practice.

This paper proposes a unified ZSV generator for discontinuous operation of CHB StatComs that guarantees effective capacitor voltage control regardless of the grid voltage and current conditions. The proposed method uses a finite-set optimization to choose the most suitable ZSV candidate that clamps a converter output voltage, as there is a finite number of ZSV at any time instant to achieve DPWM. The optimization explicitly uses the FFZSV calculated by the inter-phase balancing control as a reference signal to be tracked on average by the generated piecewise ZSV, thus effectively decoupling the two control modules. In addition, the optimization problem provides the flexibility of minimizing the switching loss. Furthermore, unlike the conventional DPWM methods where only clamping to positive and negative cluster voltages are considered, the proposed DPWM method introduces the possibility of clamping to the zero-voltage level, which unlocks more ZSV candidates and thus, further degrees of freedom to attain multiple control objectives.

The rest of the paper is organized as follows. In Section II, mathematical expressions of the CHB StatComs are revisited. The conventional DPWM strategy is reviewed in Section III and the proposed DPWM strategy is introduced in Section IV. Experimental results in Section V compare the proposed and conventional modulation techniques regarding their steady-state and dynamic performances. Finally, Section VI concludes this paper.

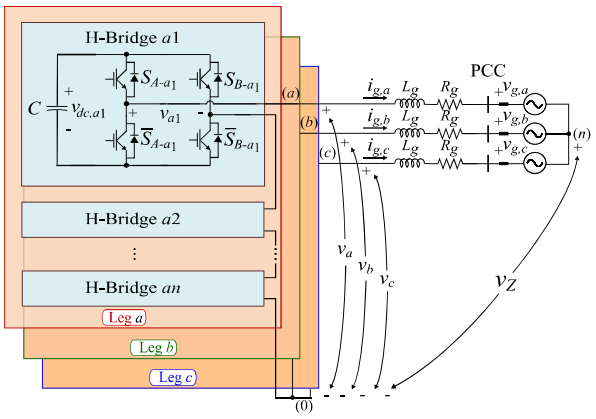

Fig. 1. Circuit diagram of a three-phase CHB StatCom with star configuration.

II. Background of CHB StatComs with Star Configuration

The star-connected CHB StatCom circuit diagram is presented in Fig. 1. Each leg of the CHB converter consists of n H-bridge SMs, with $j \in \{1, \cdots, n\}$ referring to the SM index within a leg. The converter ac-side positive terminals, i.e., terminals (a), (b), and (c) in Fig. 1, are connected to the point of common coupling (PCC) grid voltages $v_{g,a}$, $v_{g,b}$ and $v_{g,c}$, through filtering inductors (L_g, R_g). The dc-side of each H-bridge SM consists of a capacitor C. In the star configuration, a ZSV can be injected between the system ground (n) and the neutral of the converter (0), as indicated in Fig. 1 [19].

In the averaged model [22], the dc- and ac-side SM voltages, $v_{dc,xj}$ and v_{xj}, respectively, are related by the modulating signals δ_{xj} as,

$$\delta_{xj} = \frac{v_{xj}}{v_{dc,xj}}, \tag{1}$$

where $x \in \{a, b, c\}$ refers to the phase index. Note that $\delta_{xj} \in [-1,\ 1]$. During DPWM, clamping the leg x means that all the n δ_{xj} are saturated to $\{-1, 0, 1\}$.

The total converter dc- and ac-side voltages, referred to as cluster voltages and converter voltages henceforth, are defined as the per-leg sum of the respective individual voltages, i.e., $v_{dc,x} = \sum_{j=1}^{n} v_{dc,xj}$ and $v_x = \sum_{j=1}^{n} v_{xj}$, respectively.

The converter voltages v_x can be expressed as

$$v_x = v'_x + v_Z, \tag{2}$$

where, according to Fig. 1, v_Z is a ZSV between the neutral of the converter and the system ground, and v'_x is the postive- and negtaive-sequence converter voltage reference. Particularly, v_Z consists of two components, a fundamental-frequency component for inter-phase balance, denoted as v_{Zb}, and a piecewise continuous component for DPWM, denoted as v_{Zd}, i.e.,

$$v_Z = v_{Zb} + v_{Zd}. \tag{3}$$

Note that $v_{Zd} = 0$ under continuous pulse width modulation (CPWM).

Assuming inter-SM capacitor voltage balance, i.e., $v_{dc,xj} = v_{dc,x}/n$ for every j, the instantaneous power relationship

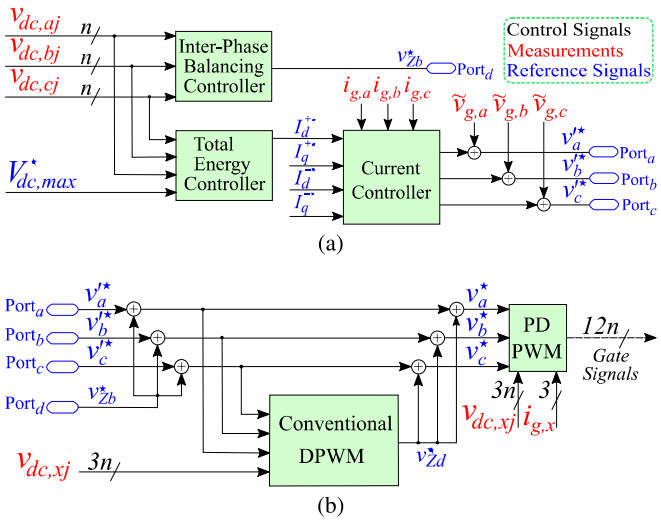

Fig. 2. Overview of the CHB StatCom control scheme. (a) Outer and inner control loops and (b) conventional DPWM implementation scheme.

between the ac- and dc-side in each converter leg corresponds to:

$$\frac{C}{2n}\frac{dv_{dc,x}^2}{dt} = -v_x i_{g,x}. \tag{4}$$

Note that according to (2) and (4), v_{Zd} directly affects the cluster voltages $v_{dc,x}$.

III. Review of Conventional DPWM Strategy

A. ZSV Injection Method

Under the conventional DPWM [19], at any time instant, there is a converter voltage v_x clamped to either its respective cluster voltage with positive polarity, i.e., $v_x = v_{dc,x}$, which is achieved by injecting a positive ZSV $v_Z = v_{Z,xp}$, or with negative polarity, i.e., $v_x = -v_{dc,x}$, by injecting a negative ZSV $v_Z = v_{Z,xn}$. According to (2), $v_{Z,xp}$ and $v_{Z,xn}$ correspond to,

$$\begin{cases} v_{Z,xp} &= v_{dc,x} - v'_x, \\ v_{Z,xn} &= -v_{dc,x} - v'_x. \end{cases} \tag{5}$$

Note that $v_{dc,x}$ can be measured, while v'_x is known within the CHB StatCom control. To avoid overmodulation, i.e., ensure $|\delta_{xj}| \leq 1$ in (1), the following criterion is applied for each leg,

$$|v_x| \leq v_{dc,x}. \tag{6}$$

Substituting (2) into (6) yields the following constraint for v_Z:

$$v_{Z,xn} \leq v_Z \leq v_{Z,xp}, \tag{7}$$

Considering the three converter legs $x \in \{a, b, c\}$, a maximum and a minimum bound for v_Z, i.e., $v_{Z,\max}$ and $v_{Z,\min}$, can be defined as:

$$\begin{aligned} v_{Z,\max} &= \min\left\{v_{Z,ap}, v_{Z,bp}, v_{Z,cp}\right\}, \\ v_{Z,\min} &= \max\left\{v_{Z,an}, v_{Z,bn}, v_{Z,cn}\right\}. \end{aligned} \tag{8}$$

As mentioned, the ZSV v_Z under the conventional DPWM is calculated by two control modules, i.e., one calculates v_{Zb} for inter-phase capacitor voltage balance, and another calculates v_{Zd} for DPWM. Therefore, according to (3) and (8), the maximum and minimum bounds for v_{Zd}, i.e., $v_{Zd,\max}$ and $v_{Zd,\min}$, can be calculated as,

$$\begin{aligned} v_{Zd,\max} &= v_{Z,\max} - v_{Zb}, \\ v_{Zd,\min} &= v_{Z,\min} - v_{Zb}. \end{aligned} \tag{9}$$

Eventually, the conventional DPWM logic selects v_{Zd} as the candidate with the smallest absolute value, i.e.,

$$v_{Zd} = \begin{cases} v_{Zd,\max} & \text{if } |v_{Zd,\max}| < |v_{Zd,\min}|, \\ v_{Zd,\min} & \text{otherwise.} \end{cases} \tag{10}$$

Note that, according to (5)-(10), the selected v_{Zd} based on (10) will clamp a converter voltage to its corresponding positive or negative cluster voltage without creating overmodulation in the rest of converter legs.

B. Control Diagram

Fig. 2(a) shows the hierarchical control approach considered in this paper for the CHB StatCom. The Inter-Phase Balancing Controller block calculates the FFZSV reference $v^\star_{Zb}$ that maintains the energy balance among the converter legs [17]. The Total Energy Controller block calculates the positive-sequence active current reference $I_d^{+\star}$ that compensates for the system loss. The current references $I_q^{+\star}$, $I_d^{-\star}$ and $I_q^{-\star}$ are given by an upper level controller according to the grid conditions, where the superscripts $+$ and $-$ represent the positive- and negative-sequence components, and the subscripts d and q stand for the d- and q-components, respectively. The amplitude conservative dqz-transformation is used in this paper. Note that the Inter-Phase Balancing Controller and the Total Energy Controller blocks constitute the outer control loop, which controls the peak values of the cluster voltages $v_{dc,x}$ to the reference $V^\star_{dc,max}$ [23], [24]. The Current Controller outputs are added to $\widetilde{v}_{g,x}$, which are the measured grid voltage feedforward terms [25], to generate the converter voltage references $v'^\star_x$, i.e., signals in Port_a, Port_b and Port_c.

Fig. 2(b) depicts the conventional DPWM implementation scheme. The FFZSV reference $v^\star_{Zb}$ from the Inter-Phase Balancing Controller is added to $v'^\star_x$, and then, it enters together with the measured $v_{dc,xj}$ into the Conventional DPWM block that calculates $v^\star_{Zd}$ according to (5)-(10).

Inter-SM balancing is achieved by sorting the capacitor voltages and implementing a phase disposition (PD) pulsewidth modulation (PWM) scheme [26].

C. Drawbacks

Waveforms of the conventional DPWM for different grid voltage conditions are illustrated in Fig. 3 (assuming constant capacitor voltages and neglecting ac-side impedances). Particularly, Fig. 3(a) corresponds to balanced grid voltages, Fig. 3(b) considers one grid voltage dropping to 20%, and Fig. 3(c) illustrates two grid voltages dropping to 20%. Note that

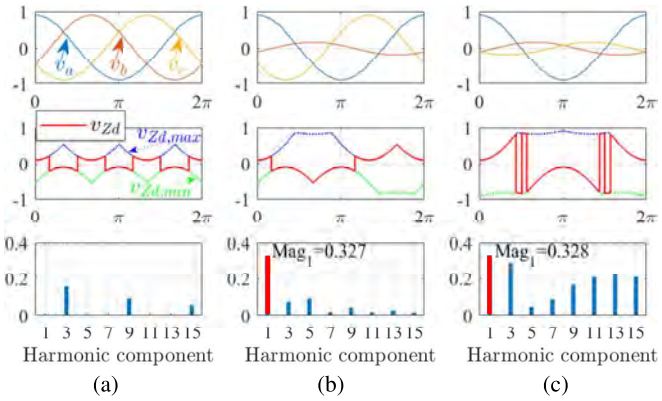

Fig. 3. Main waveforms of the conventional DPWM. (a) Balanced PCC grid voltages with modulation indices 0.9; (b) Grid voltage on phase b drops to 0.2 p.u.; (c) Grid voltage on phases b and c drop to 0.2 p.u. Top plots: PCC voltages; Middle plots: ZSV v_{Zd}; Bottom plots: frequency spectrum of v_{Zd} (in p.u.) normalized with respect to cluster voltage.

the middle row plots of Fig. 3 show how v_{Zd} is selected as the smallest magnitude candidate according to (10).

As it can be observed from Fig. 3(a), the injected v_{Zd} for discontinuous operation composed of triplen harmonics under balanced grid voltage conditions, and thus it does not create any active power, i.e.,

$$\frac{1}{T_g}\int_0^{T_g} v_{Zd} i_{g,x} dt = 0, \tag{11}$$

where T_g is the fundamental-frequency period. Consequently, the inter-phase balance is not affected by v_{Zd}.

However, when grid voltage imbalances occur, v_{Zd} has a nonnegligible fundamental-frequency component, as the frequency spectra of v_{Zd} on the bottom plots of Figs. 3(b) and (c) depict, which has been highlighted using a red color bar for the sake of illustration. Consequently, (11) is not satisfied, and the nonzero active powers per leg due to v_{Zd} interact with v_{Zb}, and thus the capacitor voltage control is deteriorated.

IV. Proposed DPWM Strategy

A. ZSV Candidates

In (8), a maximum and a minimum bounds for the ZSV have been defined. The two bounds, i.e., $v_{Z,\max}$ and $v_{Z,\min}$, only clamp a converter voltage v_x to either $v_{dc,x}$ or $-v_{dc,x}$. However, v_x can also be clamped to zero-voltage level in a CHB StatCom, i.e., $v_x = 0$, by injecting a ZSV equal to $v_{Z,x0}$. Specifically, according to (2),

$$v_{Z,x0} = -v'_x. \tag{12}$$

Clamping v_x to zero means bypassing the dc-side capacitors in the leg x, i.e., $\delta_{xj} = 0$ according to (1). Note that this is a specific characteristic of the CHB converter, which endows the proposed DPWM algorithm with greater degrees of freedom. Specifically, this clamping option offers three new ZSV candidates (one per phase), namely $v_{Z,a0}$, $v_{Z,b0}$ and $v_{Z,c0}$. Considering the ZSV bounds $v_{Z,\max}$ and $v_{Z,\min}$ in (8), $v_{Z,x0}$ in (12) can then be modified as

$$v_{Z,x0} = \begin{cases} -v'_x & \text{if } v_{Z,\min} \le -v'_x \le v_{Z,\max}, \\ \infty & \text{otherwise.} \end{cases} \tag{13}$$

Note that (13) assigns values to the three new ZSV candidates introduced in (12) to rule out those that lead to overmodulation. This is achieved by giving a value of infinity to those ZSV candidates that lie outside of the defined ZSV bounds $[v_{Z,\min}, v_{Z,\max}]$.

Consequently, at the sampling step k, where k is an integer value, there is a total of five ZSV candidates $v_{Z,h}(k)$ available to achieve DPWM, i.e.,

$$v_{Z,h}(k) \in \left\{ \begin{array}{c} v_{Z,\max}(k), v_{Z,\min}(k), \\ v_{Z,a0}(k), v_{Z,b0}(k), v_{Z,c0}(k) \end{array} \right\}, \tag{14}$$

where $h \in \{1, 2, ..., 5\}$ is an index used to refer to the different ZSV candidates in (14) ($v_{Z,1} = v_{Z,\max}$, $v_{Z,2} = v_{Z,\min}$, ..., and $v_{Z,5} = v_{Z,c0}$).

B. Cost Function

A cost function J is proposed to evaluate which ZSV candidate $v_{Z,h}(k)$ in (14) better meets the control objectives: (i) tracking the FFZSV for inter-phase balance $v^\star_{Zb}$, and (ii) minimizing the switching loss. Specifically, the proposed cost function J consists of three terms,

$$J = J_1 + \alpha_2 J_2 + \alpha_3 J_3, \tag{15}$$

where α_2 and α_3 are positive weighting factors to tradeoff the different objectives.

The proposed DPWM strategy finds the optimal ZSV candidate $v^\star_Z$ at each sampling step that minimizes J, i.e.,

$$\begin{aligned} v^\star_Z(k) = \quad & \underset{v_{Z,h}}{\text{arg minimize}}\ J, \\ & \text{subject to (14).} \end{aligned} \tag{16}$$

The first cost function in (15), J_1, penalizes the difference between the ZSV candidates $v_{Z,h}(k)$ and the FFZSV for inter-phase balance $v^\star_{Zb}(k)$, thus steering $v^\star_Z$ to $v^\star_{Zb}$ on average. Specifically, J_1 corresponds to

$$J_1 = \left(v^\star_{Zb}(k) - v_{Z,h}(k)\right)^2. \tag{17}$$

If multiple ZSV candidates have a similar distance to $v^\star_{Zb}$, for example $|v^\star_{Zb} - v_{Z,2}| \approx |v^\star_{Zb} - v_{Z,3}|$, the optimization needs extra information from the previous control step to avoid unwanted glitches in the ZSV and modulation signals that could trigger undesired switching events. For this purpose, cost function J_2 is considered in the optimization,

$$J_2 = \left(v^\star_Z(k-1) - v_{Z,h}(k)\right)^2, \tag{18}$$

where $v^\star_Z(k-1)$ stands for the optimal $v^\star_Z$ value applied in the previous sampling step. Returning to the aforementioned example in which choosing either $v_{Z,2}$ or $v_{Z,3}$ yields a similar J_1 cost value, the addition of J_2 in the optimization

will prioritize the ZSV candidate that maintains the previous control instant.

As it is discussed, the main cost function J_1 guarantees the fundamental-frequency component in the ZSV for inter-phase balance by tracking $v_{Zb}^{\star}$, which implies that all the other harmonics in the ZSV can be manipulated and optimized to achieve the least switching loss. Particularly, the cost of switching leg x, in terms of resultant switching loss, can be considered proportional to the following voltage-current product [27],

$$P_x = v_{dc,x} \left| i_{g,x} \right| . \tag{19}$$

Consequently, it is preferable to choose the ZSV candidate that clamps the leg with the highest P_x value such that no switching is incurred in that leg. Therefore, in order to prioritize the ZSV candidate that minimizes the switching loss, the following cost J_3 is added,

$$J_3 = \zeta \begin{bmatrix} D_a(k) \\ D_b(k) \\ D_c(k) \end{bmatrix}^T \begin{bmatrix} P_a(k) \\ P_b(k) \\ P_c(k) \end{bmatrix}, \tag{20}$$

where the notation T stands for the vector transpose. The binary terms D_x are defined as,

$$D_x(k) = \begin{cases} 0 & \text{if } v_{Z,h}(k) \in \left\{ \begin{matrix} v_{Z,xp}(k), v_{Z,xn}(k), \\ v_{Z,x0}(k) \end{matrix} \right\} \\ 1 & \text{otherwise.} \end{cases}, \tag{21}$$

D_x aims at disregarding the incurred loss in the leg that the candidate $v_{Z,h}$ that is being evaluated, would clamp. For instance, if $v_{Z,a0}$ is being evaluated, which involves clamping v_a to zero-voltage level, then P_a must be set to zero since the leg a will not be switching.

The nonlinear weighting factor ζ in (20) is defined as,

$$\zeta(k) = \begin{cases} \frac{1}{\max\left\{\left|I_{q,pu}^{+}\right|, 0.1\right\}} & \text{if } \frac{V^{-}(k)}{V^{+}(k)} \leq 5\%, \\ 0 & \text{otherwise.} \end{cases} \tag{22}$$

This adaptive weighting factor modifies J_3. $I_{q,pu}^{+}$ is the per-unit value of the positive-sequence reactive current I_q^{+}, and V^{-} and V^{+} are the amplitudes of the negative- and positive-sequence components of the grid voltages, respectively. Note that $I_{q,pu}^{+}$, V^{-} and V^{+} are available signals within the CHB StatCom controller. Also note that ratio V^{-}/V^{+} measures the degree of grid voltage imbalance, and the higher the ratio, the more imbalance the grid.

With the aid of the grid voltage imbalance indicator, (22) can be understood as a switch that either activates ($\zeta(k) > 0$) or deactivates ($\zeta(k) = 0$) the cost function J_3 from the optimization. This is useful since switching loss minimization is not a priority during transient periods. In fact, (22) removes J_3 from the optimization when a severe grid voltage unbalance is detected, i.e., when the negative-sequence grid voltage is nonnegligible, specifically $V^{-}/V^{+} > 5\%$ according to (22). Unlike unbalanced grid voltages, unbalanced grid currents normally represent a steady-state operation in StatCom applications, hence, J_3 is activated ($\zeta(k) > 0$) for unbalanced grid current cases. When J_3 is active, ζ is inversely proportional to $I_{q,pu}^{+}$, i.e., $\zeta = 1/\left|I_{q,pu}^{+}\right|$. This allows to preserve the priority of J_3 within the optimization regardless the processed current amplitude in P_x. Considering $\left|I_{q,pu}^{+}\right| \in [0,1]$, ζ varies from 1 to infinity according to the definition $\zeta = 1/\left|I_{q,pu}^{+}\right|$, hence, to avoid unnecessary large values, ζ is limited to 10 for current amplitudes below 0.1 p.u., i.e., $\zeta = 1/\max\left\{\left|I_{q,pu}^{+}\right|, 0.1\right\}$.

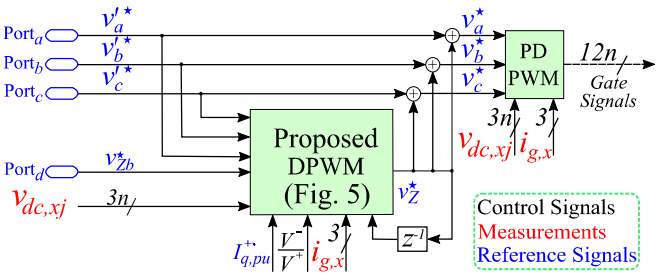

Fig. 4. Proposed DPWM implementation scheme.

As a conclusion, this finite-set optimization produces a unique ZSV $v_Z^{\star}$, which can be considered as consisting of two components, a fundamental-frequency term for inter-phase capacitor voltage balance, and a non-fundamental-frequency term for DPWM. Particularly, the fundamental-frequency term is guaranteed by the cost function J_1, which prioritizes the ZSV candidate closest to the FFZSV for inter-phase balance, i.e., $v_{Zb}^{\star}$, at each control step. The non-fundamental-frequency term, which does not affect inter-phase balance, is shaped by cost functions J_2 and J_3 to create the optimal clamping pattern for switching loss reduction. In this way, the decoupling of inter-phase balance and DPWM implementation is achieved.

Since cost function J_1 is the most important term in the proposed optimization problem, namely it guarantees the DPWM operation with negligible interaction with the inter-phase capacitor voltage controller, weighting factors α_2 and α_3 can be independently chosen without affecting the system performance for a wide range of values. Specifically, α_2 is chosen low enough to smoothen the modulation signals while not compromising the bandwidth. With respect to α_3, it is chosen large enough such that the clamping actions occur when the switching power P_x takes large values in order to minimize switching loss.

C. Controller Diagram

The proposed DPWM implementation scheme is presented in Fig. 4. Note that Port$_a$, Port$_b$, Port$_c$ and Port$_d$ are marked in Fig. 2(a). Unlike in Fig. 2(b), the FFZSV reference $v_{Zb}^{\star}$ from the Inter-Phase Balancing Controller is not directly added to the converter voltage references $v_x'^{\star}$. Instead, $v_{Zb}^{\star}$ is used as a reference to be tracked by the Proposed DPWM block. As a consequence, the Proposed DPWM block produces $v_Z^{\star}$ which simultaneously guarantees inter-phase balance and DPWM.

Fig. 5 illustrates a flow chart for finding $v_Z^{\star}$, which simply requires five iterations.

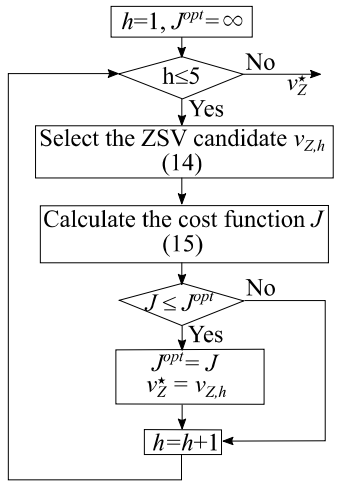

Fig. 5. Flow chart for finding the optimal ZSV candidate.

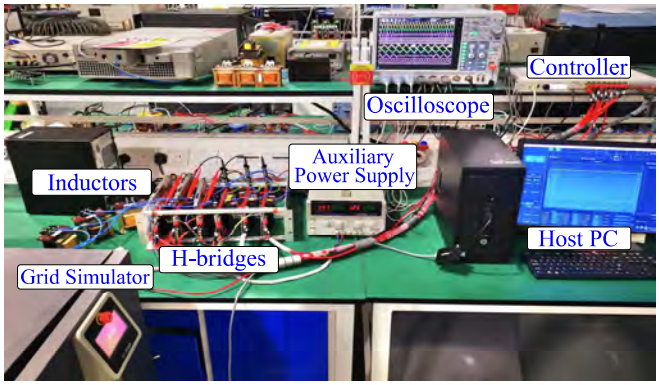

Fig. 6. Experimental setup.

V. Experimental Results

This section experimentally compares the proposed DPWM scheme with both CPWM and the conventional DPWM revisited in Section III. The comparison includes steady-state and transient waveforms. The steady-state results show the clamping behavior of the proposed DPWM and the switching loss of the different modulations. The transient results show the dynamic behavior of the proposed DPWM during grid voltage sags and when the current set-point changes. Experimental results are obtained using a CHB StatCom prototype with two IMPERIX PEH2015 H-bridge converters per leg. The PCC grid voltages are provided by a GL&EL 15-kVA CINERGIA grid emulator. A B-Box RCP 3.0 from IMPERIX has been used to implement the control shown in Figs. 2 and 4. The experimental setup is shown in Fig. 6, and the system parameters are given in Table I.

TABLE I
Experimental System Parameters

Parameters	Value
PCC grid voltage nominal amplitude, V_g	$100\sqrt{2}$ V
Nominal reactive power, Q	2.5 kVAr
Grid angular frequency, ω_g	100π rad/s
Carrier frequency, f_{sw}	9 kHz
Control/sampling frequency, f_s	25 kHz
SMs in each leg, n	2
Peak cluster voltage, $V_{dc,max}$	$1.3V_g$
Capacitance per H-bridge, C	1 mF
Filter inductance, L_g	2 mH

A. Steady-State Results

1) Steady-State Waveforms: Fig. 7 presents the main converter waveforms when using different modulation schemes and considering balanced grid conditions. The proposed DPWM scheme is tested for two different values of α_3 in (15), namely, $\alpha_3 = 0$ (*Case I*), and $\alpha_3 = 10$ (*Case II*), while $\alpha_2 = 0.05$ in both cases. Specifically, *Case II* prioritizes switching loss reduction.

Fig. 7(a) shows the converter waveforms under CPWM. As it can be observed, the resultant ZSV, i.e., $v_Z = 1/3\,(v_a + v_b + v_c)$ is almost zero given the balanced grid conditions. Differently, v_Z contains mainly triplen harmonics under the DPWM schemes, as shown in Figs. 7(b)-(d). The time periods in which leg a is clamped are highlighted with blue shadings for the sake of illustration. As it can be observed, different clamping patterns are achieved depending on the DPWM strategy. However, the total time a leg is clamped within a fundamental grid period is the same for all DPWM schemes, i.e., $2\pi/3$ rad. Note that this is due to the balanced grid conditions. It can be observed that in the conventional DPWM, the clamping intervals of any leg are primarily located near very low switching power P_x values, which is not optimal in terms of switching loss reduction. Specifically, clamping occurs when the converter voltages $v'_x + v_{Zb}$ are at their highest and lowest positions, as in those periods the required ZSV for clamping converter voltages to their corresponding cluster voltages, i.e., v_{Zd}, is minimum, according to (10). Differently, the proposed DPWM allows clamping a converter voltage to the zero-voltage level, which is highlighted in the modulating signals corresponding to Figs. 7(c) and (d). The consideration of the zero-voltage level provides higher degrees of freedom to effectively shift the clamping intervals. For instance, in *Case I* of the proposed DPWM, the clamping intervals at $\delta_{aj} = \pm 1$ are reduced to approximately half compared to the conventional DPWM, and the zero-voltage levels are used instead, which coincide with large P_x values and thus yields advantages in terms of switching loss reduction. When considering the J_3 term in the optimization, namely in *Case II* of the proposed DPWM, the clamping periods at low P_x values are completely removed compared to the conventional DPWM and *Case I*, thus rendering greater switching loss reduction.

As a conclusion, the main difference between the conventional and the proposed DPWM methods, in the steady-state and balanced grid operation, is in the clamping pattern. Specifically, the conventional DPWM clamps the converter voltages only in the vicinity of their peaks. Note that this corresponds to the zero-crossing periods of the corresponding

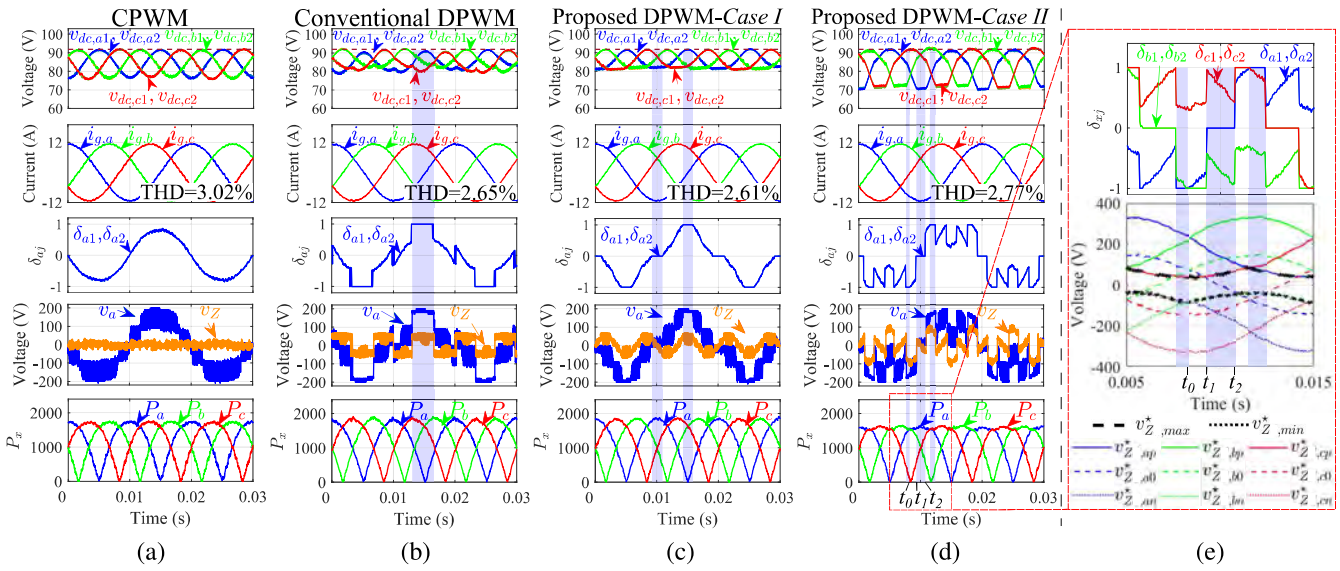

Fig. 7. Steady-state waveforms under nominal operating conditions, when implementing (a) a CPWM scheme, (b) the conventional DPWM, (c) the proposed DPWM with $\alpha_3 = 0$ (*Case I*), and (d) the proposed DPWM with $\alpha_3 = 10$ (*Case II*). Top plots: SM capacitor voltages (6 signals); Middle upper plots: grid currents; Middle plots: SM modulating signals of leg a (2 signals); Middle lower plots: the PWM voltage waveform of leg a and the injected zero-sequence voltage v_Z; Bottom plots: the metric for instantaneous switching loss P_x in (19). (e) Detail of the SM modulating signals (6 signals) and the zero-sequence voltage candidates (11 signals) for *Case II*.

grid currents given the StatCom operation (grid voltage and grid current waveforms in quadrature). Consequently, such clamping pattern does not significantly contribute to improve the switching losses, as the current is near zero. The proposed DPWM method (both *Case I* and *Case II*) optimally distributes the clamping intervals, according to the weighting factor α_3 in the cost function (15), in a way that converter voltages are also clamped when the corresponding current is large in absolute value, which is advantageous in terms of switching loss reduction.

The clamping nature of *Case II* is zoomed-in in Fig. 7(e). Comparing Figs. 7(d) and (e), it can be observed that leg a is clamped from t_1 to t_2, viz. $\delta_{a1} = 0$ and $\delta_{a2} = 0$, where P_a is the largest. However, leg a is not being clamped from t_0 to t_1 despite that P_a is still the largest. The reason for this is that all the ZSV candidates for clamping leg a, i.e., $v_{Z,ap}$, $v_{Z,a0}$ and $v_{Z,an}$, are outside of the feasible range $[v_{Z,\min}, v_{Z,\max}]$ from t_0 to t_1, as it is shown in Fig. 7(e). Consequently, leg b, which has the second largest P_b, is clamped instead from t_0 to t_1 since $v_{Z,bn}$ is within the feasible range $[v_{Z,\min}, v_{Z,\max}]$, viz. $\delta_{b1} = -1$ and $\delta_{b2} = -1$.

It is important to note that minimizing the switching loss (the proposed DPWM-*Case II*) can render higher capacitor current rms value as it clamps the converter voltage to its cluster voltage at large grid current values, where the capacitor current has the same magnitude as the grid current. Consequently, if switching loss minimization (*Case II*) is applied in practice, either low equivalent series resistance capacitors with negligible ohmic losses should be used or the optimization cost function, along with the switching loss, needs to take the dc-side losses into consideration.

2) Switching Loss Comparison: Switching loss reduction is the most valued feature of DPWM strategies. For this reason,

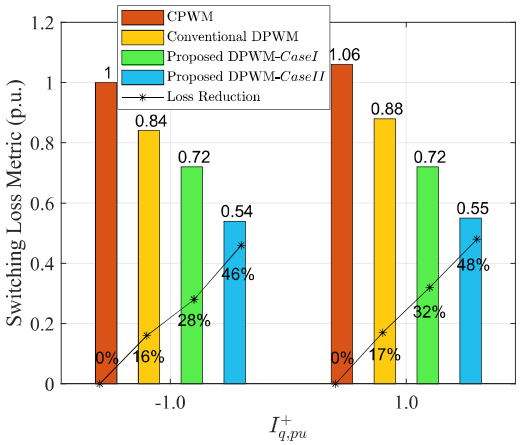

Fig. 8. Average normalized values of switching loss under nominal PCC grid voltages. The base value for the normalization corresponds to the average switching loss of CPWM at full capacitive current given by (23).

the switching loss of the studied modulations are compared next. Expressions (23)-(25) are used to evaluate the average switching loss of an individual switch P_{sw} [27],

$$P_{sw} = \frac{1}{12n} \sum_{x\in\{a,b,c\}} \sum_{j=1}^{n} \sum_{l\in\{A,B\}} P^{l}_{sw,xj}, \tag{23}$$

with

$$P^{l}_{sw,xj} = \frac{e_s}{T_e} \sum_{k=1}^{T_e f_s} \Delta S^{l}_{xj}(k)\, v_{dc,xj}(k)\, |i_{g,x}(k)|, \tag{24}$$

and

$$\Delta S^{l}_{xj}(k) = \left| S^{l}_{xj}(k) - S^{l}_{xj}(k-1) \right|. \tag{25}$$

$P^l_{sw,xj}$ is the average switching loss associated to the l^{th} switch pair in the j^{th} SM of the x^{th} leg along an evaluation time T_e>T_g ($T_e f_s$ samples). e_s is a constant value that models the turning on and off time of the switches. Since (23) is used as a metric for comparison purposes, $e_s = 1$ has been considered. $S^l_{xj}(k) \in \{0,1\}$ is the switching state of the switch pair, and thus ΔS^l_{xj} is equal to one at the switching events, and zero otherwise. The innermost sum in (23) considers the loss in the two switch pairs of each SM, the second innermost sum groups loss in the n SMs of the leg, and the outermost sum groups loss in the three legs. Note that the factor $1/(12n)$ averages overall loss of $12n$ switches.

Fig. 8 shows the experimental measurements of P_{sw} in (23) for the different modulation schemes. Nominal grid voltages are considered, and two current conditions have been evaluated, i.e., rated capacitive current ($I^+_{q,pu} = -1$) and rated inductive current ($I^+_{q,pu} = 1$). The switching loss of CPWM at $I^+_{q,pu} = -1$ has been considered as the base value for the sake of comparison. As it can be observed, *Case I* and *Case II* of the proposed DPWM present lower switching loss than the conventional DPWM. This is in agreement with the time-domain waveforms in Fig. 7, where it was highlighted that the conventional DPWM clamping occurs at time periods in which switching loss in the corresponding leg are low. *Case II* of the proposed DPWM has the lowest switching loss among the investigated modulation techniques due to the usage of J_3 in the cost function, which explicitly penalizes those ZSV candidates that contribute less to minimizing switching loss. Specifically, when compared to CPWM, *Case II* of the proposed DPWM provides approximately 46% (48%) switching loss reduction for rated capacitive (inductive) operation, whilst only 16% (17%) reduction is achieved when the conventional DPWM is implemented.

B. Dynamic Performance

In this subsection, the dynamic performance of the proposed DPWM with $\alpha_3 = 10$ and $\alpha_2 = 0.05$ is studied.

1) Current Transitions: Fig. 9 presents individual capacitor voltages, grid currents, and modulating signals, for three different current transients, and considering balanced grid voltages. Fig. 9(a) presents a transition from 1 p.u positive-sequence capacitive current to 0.3 p.u. positive-sequence capacitive current, Fig. 9(b) shows a transition from 1 p.u positive-sequence capacitive current to 1 p.u. positive-sequence inductive current, and Fig. 9(c) depicts a transition from balanced current operation ($I^+_{q,pu} = -1$, $I^-_{d,pu} = 0$ and $I^-_{q,pu} = 0$) to unbalanced current operation ($I^+_{q,pu} = -1$, $I^-_{d,pu} = -0.2$ and $I^-_{q,pu} = 0.2$).

As it can be observed, the current and capacitor voltage transients are very fast in all the cases, and the individual capacitor voltages are well balanced with their peak values well regulated. Note that the pattern of the modulation signals is similar in all the current operating conditions. This is achieved due to the ζ parameter considered in J_3, which aims at preserving the importance of J_3 within the optimization regardless of the processed current magnitude. The results

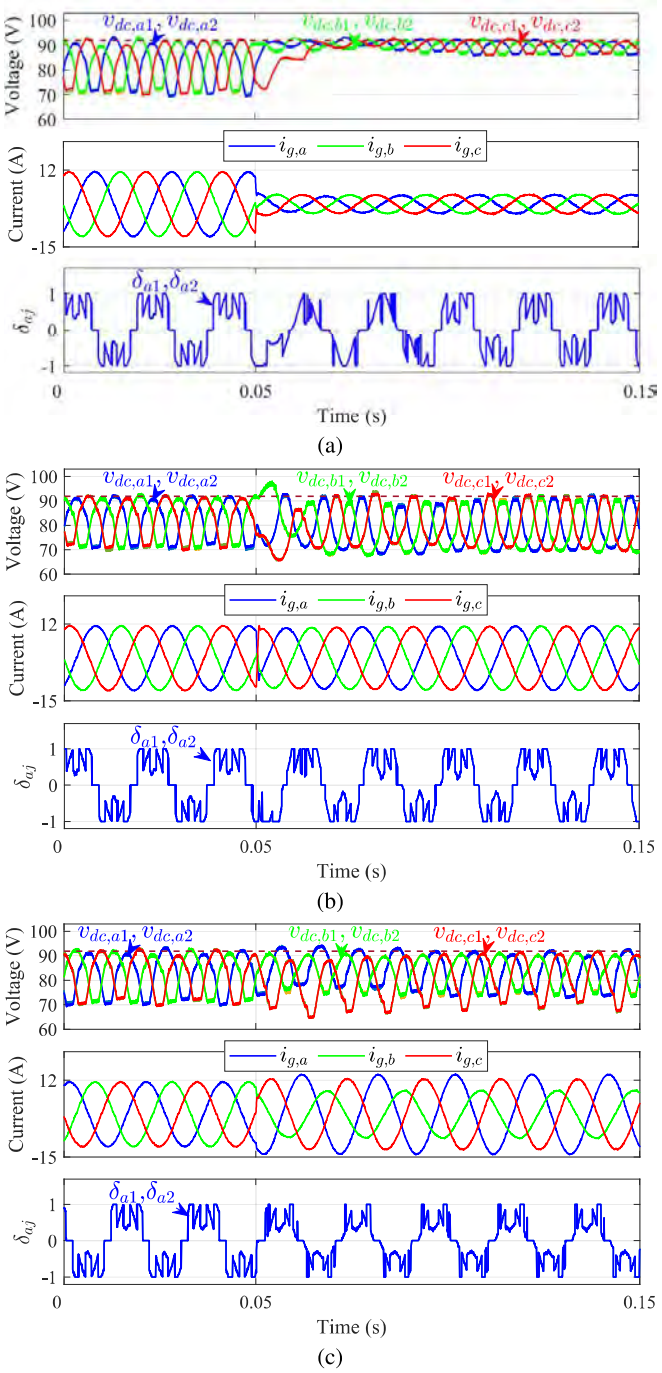

Fig. 9. Experimental waveforms during (a) a transition from rated capacitive current to 30%-rated capacitive current, (b) a transition from rated capacitive current to rated inductive current, (c) a transition from balanced to unbalanced currents.

demonstrate the feasibility of the proposed DPWM to cope with different grid current requirements and its effectiveness in maintaining a low switching loss profile.

2) Grid Voltage Sag: Inter-phase capacitor voltage balance is critical during grid voltage sags, since an FFZSV for maintaining the energy balance among the CHB legs is needed [19].

Fig. 10 compares the performance of the conventional

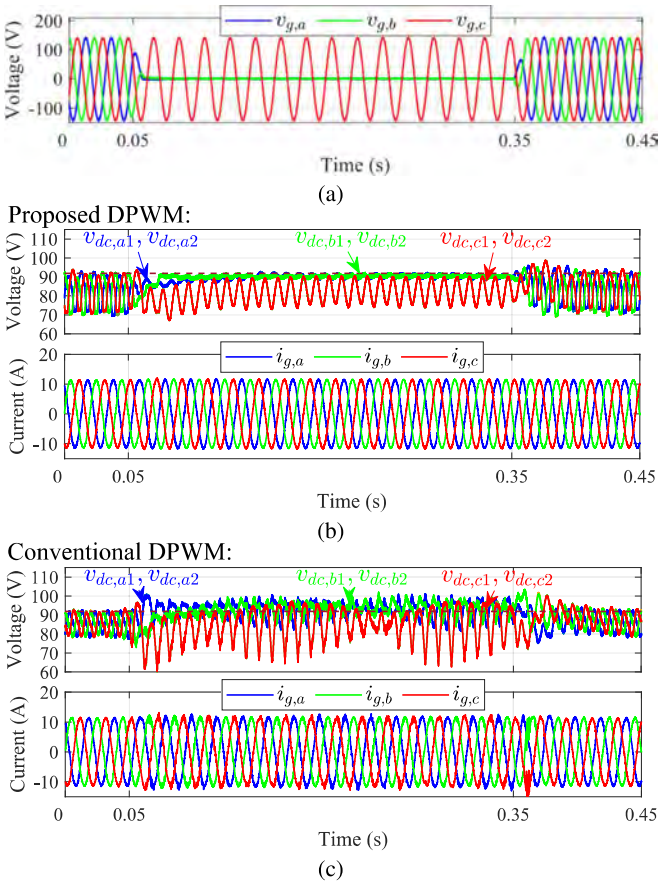

Fig. 10. Experimental waveforms during a grid voltage sag in phases a and b. (a) PCC grid voltages, and (b) and (c) are the capacitor voltages and the StatCom currents under the proposed DPWM and the conventional DPWM, respectively.

DPWM and the proposed DPWM under a grid voltage sag. Specifically, individual capacitor voltage and grid current waveforms of the CHB StatCom are presented, when the grid voltages in phases a and b drop to zero from $t = 0.05$ s to $t = 0.35$ s. As it can be observed, when the voltage sag occurs, the conventional DPWM yields an unstable behavior in which the capacitor voltages are not properly controlled and the grid currents are distorted. This result is in agreement with Fig. 3, where it was shown that the conventional DPWM generates unwanted active powers in the converter legs under unbalanced grid conditions, which interact with the inter-phase capacitor voltage balance control. Differently, the proposed DPWM renders stable capacitor voltages and good quality grid currents thanks to its capability to achieve multiple control objectives simultaneously with only one ZSV. Note that $\zeta = 0$ from $t = 0.05$ s to $t = 0.35$ s since $V^-/V^+ > 5\%$ (unbalanced grid voltage condition detected), while $\zeta = 1$ before $t = 0.05$ s and after $t = 0.35$ s, according to (22). Therefore, switching loss optimization is disregarded during the grid voltage sag, prioritizing $v^\star_{Zb}$ tracking for inter-phase capacitor voltage balance.

VI. Conclusion

A DPWM strategy based on finite-set optimization for CHB StatComs with star configuration has been proposed in this paper. Different from the conventional DPWM, the proposed DPWM strategy decouples the discontinuous operation from the capacitor voltage control loop, thus rendering a great transient performance during grid voltage sags. Furthermore, the proposed DPWM allows for switching loss optimization by a proper cost function design. Specifically, the proposed DPWM achieves up to 45% switching loss reduction compared to the CPWM at rated capacitive and inductive current operation. The cost function is designed in such a way that it provides variable objective prioritizing based on the operating conditions, offering a tradeoff between steady-state and transient behavior.

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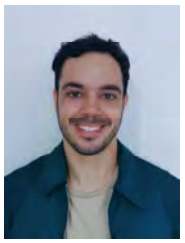

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