

Capacitor Condition Monitoring Method for Low-Capacitance StatComs: An Online Approach Using the Inherent Second-Harmonic Oscillations

Ezequiel Rodriguez, *Member, IEEE*, Ramon Leyva, *Senior Member, IEEE*,

Liu Qingxiang, *Student Member, IEEE*, Glen G. Farivar, *Senior Member, IEEE*, and Josep Pou, *Fellow, IEEE*

Abstract—The cascaded H-bridge low-capacitance static compensator (LC-StatCom) deliberately reduces the capacitor size while allowing large oscillations in capacitor voltages. When a capacitor deteriorates, its capacitance decreases or/and its equivalent series resistance (ESR) increases, compromising StatCom performance and safety. For this reason, the condition monitoring of the capacitors is important to schedule maintenance before failure. This letter introduces a cost-effective and nonintrusive method to monitor the condition of capacitors online. The proposed method offers real-time monitoring without requiring additional hardware or signal injection. The method uses averaged low-frequency signals instead of instantaneous high-frequency signals that can be corrupted by undesired high-frequency noise. Specifically, the method takes advantage of the inherent twice-fundamental-frequency oscillations on the capacitor voltage and current to identify the ESR and capacitance values. The method takes into account the influence of antialiasing filters required for sampling process. The letter shows experimental results that validate the fast and accurate performance of the proposed capacitor condition monitoring.

I. INTRODUCTION

The cascaded H-bridge (CHB) static compensator (StatCom) is a well-known technology for reactive power compensation. A CHB StatCom is composed of several submodules (SMs), each of them with its corresponding capacitor on the dc side. Capacitors are one of the failure prone components in power electronic converters and given the number of capacitors in a CHB converter, monitoring their condition is important to improve the StatCom's reliability. In low-capacitance StatComs (LC-StatComs), the capacitor voltages have significant oscillations [1]. The capacitor voltage and current oscillations in low-frequency ranges are significantly affected by the capacitor parameters, specifically by the capacitance (C) and equivalent series resistor (ESR). These oscillations provide valuable information to determine the capacitor parameters, which serve as indicators of the state of health.

It is widely accepted that the end-of-life criterion for aluminum electrolytic capacitors is a 20% capacitance reduction or 100% increase of the ESR, whereas for film capacitors, a 2% – 5% capacitance reduction indicates the capacitor's end of life [2].

Online capacitor condition monitoring (CCM) methods estimate the C, or C and ESR simultaneously, during operation in real time. Online monitoring methods, which have attracted

special attention in recent years [3]–[7], are more suitable in practice than offline methods [8], [9]. Among the online methods, some use the information contained in the high-frequency range of the capacitor waveforms [3], [4], [7]. Others use the averaged dynamic relationships among converter signals to estimate the capacitor parameters [5], [6]. In most cases, estimation using high-frequency waveforms necessitates the use of advanced filtering stages such as Kalman filters [3]. Nonetheless, recovering signal information is difficult when noise, such as switching ripples or sensor response, contaminates the frequency range of interest. Contrarily, low-frequency approaches do not suffer from the aforementioned high-frequency effects.

An interesting contribution belonging to the low-frequency-range category, but with offline implementation, is found in [9], where the input-to-output transfer function of an LRC network is used to obtain the capacitor parameters. Specifically, [9] evaluates the magnitude and phase of the transfer function employing a Fast-Fourier Transform, which would require a significant amount of computational power in a real-time version.

The proposed online CCM approach in this letter, also uses a transfer function relating low-frequency signals. Specifically, it uses the inherent twice-fundamental-frequency oscillations on the measured dc-side voltage and a reconstructed form of the dc-side current of the LC-StatCom to estimate parameters C and ESR, requiring no additional hardware. These oscillations are obtained using a high-selective second order generalized integrator configured as quadrature signal generator (SOGI-QSG) [10]. Furthermore, the effects of antialiasing filters used in the sampling process are taken into account as well.

The organization of the rest of the letter is the following. Section II reviews the CHB StatCom topology, its standard control modules, and the proposed capacitor parameters estimation approach. Section III depicts experimental results to demonstrate the effectiveness of the approach. Finally, Section IV summarizes the letter.

II. PROPOSED CAPACITOR CONDITION MONITORING METHOD

Fig. 1 shows the LC-StatCom converter. It consists of n submodules (SMs), each with its corresponding capacitance C_k and ESR R_{C_k} , k being the SM index.

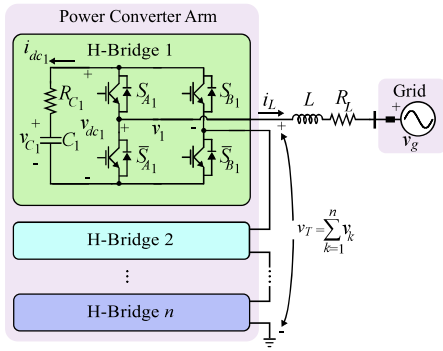


Fig. 1. Circuit diagram of a single-phase multilevel CHB StatCom.

A. LC-StatCom Modeling and Control

The dynamic behaviour of the LC-StatCom is given by

$$C_k \dot{v}_{C_k} = -S_k i_L, \quad (1)$$

$$L \dot{i}_L = -R_L i_L + \sum_{k=1}^n S_k v_{dc_k} - v_g, \quad (2)$$

where S_k is the switching state of the k th SM ($S_k \in \{-1, 0, 1\}$), i_L is the grid current, v_g is the grid voltage, and L and R_L are the inductance and resistance of the filter, respectively. Note that the capacitor voltage v_{C_k} is not measurable or available for feedback purposes, and instead the dc-side voltage v_{dc_k} is measured. The relationship between the dc-side voltage, v_{dc_k} , and the dc-side current, i_{dc_k} , corresponds to

$$v_{dc_k} = R_{C_k} i_{dc_k} + \frac{1}{C_k} \int_{t_0}^t i_{dc_k} d\tau, \quad (3)$$

or alternatively, in the frequency domain,

$$V_{dc_k}(s) = \left(R_{C_k} + \frac{1}{sC_k} \right) I_{dc_k}(s), \quad (4)$$

with s as the Laplace variable, and $V_{dc_k}(s)$ and $I_{dc_k}(s)$ as the Laplace transforms of v_{dc_k} and i_{dc_k} , respectively. Note that (4) defines a transfer function for the capacitor impedance, $Z_{C_k}(s) = R_{C_k} + 1/(sC_k)$.

A conventional LC-StatCom control approach is shown in Fig. 2, and it uses multiple nested loops as in [11]. The control consists of three layers, namely: outer loop, inner loop, and inter-SM balancing loop. Note that i_q^* and $\langle v_{dc_k}^* \rangle$ refer to the prescribed reference signals for the reactive current and the average dc-side voltages, respectively. The active current reference i_d^* , which together with i_q^* constitute the grid current reference for the inner loop, is calculated by the outer loop that processes the error (proportional and integral) of the sum of average voltages with respect to its reference, i.e., $\sum (\langle v_{dc_k} \rangle - \langle v_{dc_k}^* \rangle)$ [11]. The simulation model and control implementation corresponding to [11] is available in [12].

Note that the capacitor current i_{dc_k} is not available without an additional sensor. However, it can be reconstructed via (1). Fig. 2 shows signals involved in the proposed CCM scheme. The proposed CCM uses as input S_k , i_L , v_{dc_k} , and ωt , which

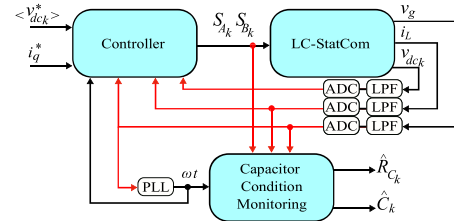


Fig. 2. General control block diagram for the LC-StatCom with the proposed CCM method.

are obtained from the control loops. Nevertheless, i_L and v_{dc_k} used within the CCM scheme are processed by an analog-to-digital converter (ADC) (sampling process) and a lowpass filter (LPF) as antialiasing filter, which add a nonnegligible delay in the time scale of the capacitor impedance time constant, $R_{C_k} C_k$. For this reason, the switching signals S_k used within the proposed CCM loop should be accordingly delayed.

B. Capacitor Parameters Estimation

The ESR and C of the capacitor in each SM can be obtained from its impedance, $Z_{C_k}(j\omega) = R_{C_k} - j/(\omega C_k)$. In the sequel, for the sake of brevity, given the similarity between SMs, the subscript corresponding to each SM_k is dropped. In order to characterize the impedance parameters, only the second-harmonic of the dc-side voltage, v_{dc-2} , and current, i_{dc-2} , is considered,

$$Z_C(j2\omega) = \frac{V_{dc-2} e^{j(2\omega t + \phi_{v_{dc-2}})}}{I_{dc-2} e^{j(2\omega t + \phi_{i_{dc-2}})}}, \quad (5)$$

where V_{dc-2} and $\phi_{v_{dc-2}}$ are the amplitude and phase of v_{dc-2} , and similarly, I_{dc-2} and $\phi_{i_{dc-2}}$ are the amplitude and phase of i_{dc-2} . Therefore,

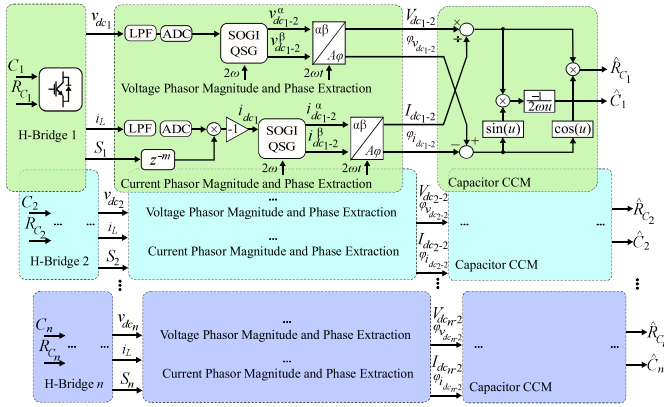
$$\text{Re}\{Z_C(j2\omega)\} = \frac{V_{dc-2}}{I_{dc-2}} \cos(\phi_{v_{dc-2}} - \phi_{i_{dc-2}}) = R_C, \quad (6)$$

$$\text{Im}\{Z_C(j2\omega)\} = \frac{V_{dc-2}}{I_{dc-2}} \sin(\phi_{v_{dc-2}} - \phi_{i_{dc-2}}) = -\frac{1}{2\omega C}. \quad (7)$$

The second-harmonic components have large enough magnitudes to ensure that after the calculation the noise levels are very low, thus avoiding the drawbacks of the high-frequency methods.

Real-time acquisition of these second-harmonic components can be accomplished by using a high-selective SOGI-QSG [10] for both the voltage and current measurements. The outputs of the two SOGIs correspond to the $\alpha\beta$ components of the second-harmonic voltage and current, respectively. Specifically, v_{dc-2}^α and v_{dc-2}^β for the voltage, and i_{dc-2}^α and i_{dc-2}^β for the current. It is important to highlight that the SOGI-QSG processing the voltage waveform must compensate for the dc component [10], thus resulting in the following transfer functions,

$$\frac{V_{dc-2}^\alpha(s)}{V_{dc}(s)} = \frac{2\zeta(2\omega)s}{s^2 + 2\zeta(2\omega)s + (2\omega)^2}, \quad (8)$$


 Fig. 3. Proposed CCM method for n SMs.

$$\frac{V_{dc-2}^\beta(s)}{V_{dc}(s)} = \frac{-2\zeta s^2}{s^2 + 2\zeta(2\omega)s + (2\omega)^2}, \quad (9)$$

whereas for the current,

$$\frac{I_{dc-2}^\alpha(s)}{I_{dc}(s)} = \frac{2\zeta(2\omega)s}{s^2 + 2\zeta(2\omega)s + (2\omega)^2}, \quad (10)$$

$$\frac{I_{dc-2}^\beta(s)}{I_{dc}(s)} = \frac{2\zeta(2\omega)^2}{s^2 + 2\zeta(2\omega)s + (2\omega)^2}, \quad (11)$$

where 2ζ corresponds to the SOGI gain (ζ is the damping ratio), and the actual center frequency 2ω is available as an input signal from the phase-locked loop (PLL). High-selective behaviour involves a value of $\zeta < 0.1$, and it is worth to note that a value of $\zeta < 0.02$ for the parameters in Table I implies that the corresponding filter settling-time is greater than 0.32 s.

Using these $\alpha\beta$ components, the amplitude and phase of the voltage are obtained in real-time as

$$V_{dc-2} = \sqrt{(v_{dc-2}^\alpha)^2 + (v_{dc-2}^\beta)^2}, \quad (12)$$

$$\phi_{v_{dc-2}} = \text{atan2}(v_{dc-2}^\beta, v_{dc-2}^\alpha) - 2\omega t, \quad (13)$$

and similarly for the current. The ESR and C are calculated from these amplitudes and phases according to (6) and (7), respectively. Fig. 3 shows the detailed block diagram of the proposed CCM method for n SMs, where \hat{R}_{Ck} and \hat{C}_k are the outputs of the CCM and refer to the estimated capacitor parameters ESR and C of the k th SM, respectively.

The capacitor impedance, $Z_C(s) = R_C + 1/(sC)$, has a zero at $s_z = -1/(R_C C)$ that causes a phase shift $\phi_{dz} = \arctan(2\omega R_C C)$ between the second-harmonic voltage and current signals. For a small R_C value, ϕ_{dz} can be approximated as $\phi_{dz} \approx 2\omega R_C C$ rad, which results in an advance time of $t_{dz} = R_C C$. The delay caused by the antialiasing filter and ADC can be in the range of t_{dz} . Then, this delay must be taken into account in the CCM method. Details on this delay magnitude are given in the experimental results section.

 TABLE I
 EXPERIMENTAL SYSTEM PARAMETERS

Parameter	Value
Grid voltage nominal amplitude, V_g	$200\sqrt{2}$ V (1 p.u.)
Grid nominal power, S_g	2 kVA (1 p.u.)
Number of SMs per phase-arm, n	3
Grid angular frequency, ω	100π rad/s
Average capacitor voltage reference, $\langle v_{dc}^* \rangle$	110 V
Nominal capacitance per SM, C_k	1.27 mF
Filter inductance, L	5 mH
Sampling frequency, f_s	60 kHz
Cutoff frequency antialiasing filter, f_{af}	20 kHz
Carrier frequency, f_c	10 kHz
SOGI-QSG damping ratio, ζ	0.02

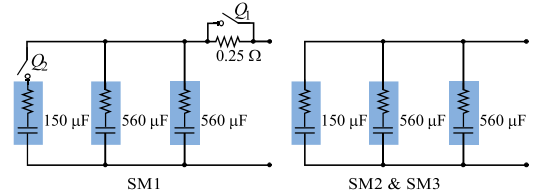


Fig. 4. DC-side circuit diagram for emulating different operating conditions in SM1, and a healthy situation of the dc-side in SM2 and SM3.

III. EXPERIMENTAL RESULTS

An experimental LC-StatCom prototype has been developed and connected to a 200-Vrms grid supplied by a GE&EL 15kVA CINERGIA grid emulator. Table I provides the prototype system parameters. The prototype has three IMPERIX PEH2015 full-bridge modules, each of them with two 560- μ F electrolytic capacitors and one 150- μ F electrolytic capacitor connected in parallel. Disconnecting the 150- μ F electrolytic capacitor enables the emulation of sudden capacitance variations, in particular a 11.8% drop in this case. Furthermore, a 0.25- Ω switch-bypassed-resistor is connected in series with the capacitor of SM1 to emulate sudden resistance variations. A detail of the connection scheme is provided in Fig. 4. The control block diagram and the proposed CCM depicted in Figs. 2 and 3, respectively, have been implemented in a B-Box RCP 3.0 board from IMPERIX. The sampling rate f_s is chosen about three times larger than the antialiasing filter frequency f_{af} , thus satisfying the Nyquist–Shannon Sampling Theorem with slack. The antialiasing filter frequency f_{af} is twice the carrier frequency f_c . The antialiasing filter is a 5th-order Bessel filter with a cutoff frequency $f_{af} = 20$ kHz, hence with a practically flat group/phase delay of 20 μ s, which is taken into account in the proposed CCM. Specifically, the switching signals S_k used to reconstruct the capacitor currents i_{dc_k} are accordingly delayed.

Experimental results are shown in Fig. 5 when the LC-

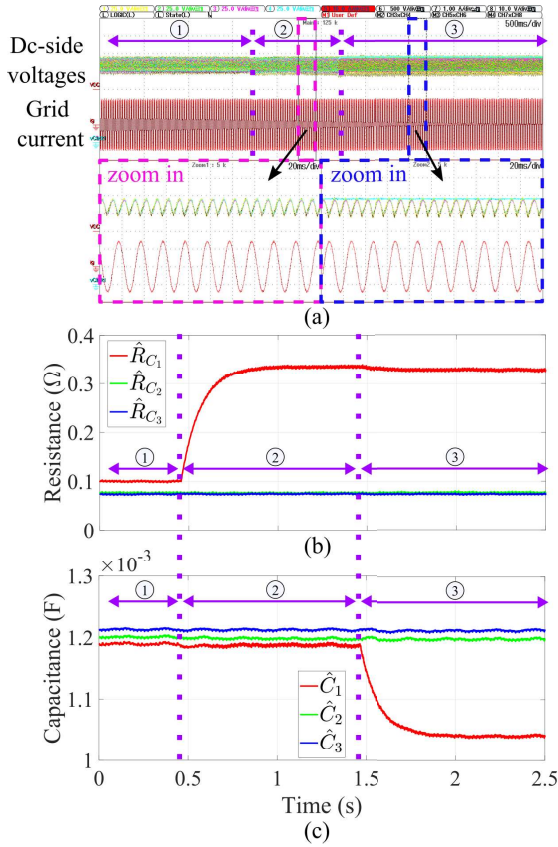


Fig. 5. Experimental waveforms for different operating conditions corresponding to ①, ②, ③ when the LC-StatCom is operating at 100%–rated capacitive power. (a) Oscilloscope waveforms where Channels CH1, 2, and 3 show the dc-side voltages (v_{dc_k}) in SM1-SM3, Channel CH4 shows the voltage across the capacitor that is disconnected in SM1, and Channel CH5 shows the grid current (i_L); (b) ESR value estimations; and (c) capacitance value estimations.

StatCom is processing 2kVA. The first operating condition, indicated as ①, corresponds to the case where healthy capacitors are emulated, i.e., the 0.25-Ω resistor in SM1 is bypassed (switches Q_1 and Q_2 are on). Next operating condition, indicated in Fig. 5 with ②, corresponds to the case wherein switch Q_1 is off, i.e., the 0.25-Ω resistor is added in series. The final operating condition, indicated in Fig. 5 with ③, corresponds to the case where a 150-μF capacitor is disconnected from SM1, i.e., switches Q_1 and Q_2 are off. As can be observed, the ESR values are accurately estimated and \hat{R}_{C_1} value sees 0.25Ω difference going from ① to ② as expected. The C values are accurately estimated as well and the \hat{C}_1 value drops by 150 μF when ③ starts. The proposed CCM method detects the capacitor parameters ESR and C in approximately 0.32 s. In addition, note that an expanded picture of the steady-state at operating points ② and ③ is provided, where the corresponding waveforms of grid current and dc-side voltages can be seen. In the expanded figures, the expected grid current waveform can be observed, i.e., a sinusoidal form. Besides, the dc-side voltages also behave as expected, namely, increasing the magnitude of the twice-fundamental-frequency oscillation in SM1 in ③ when the capacitance C_1 decreases by 150 μF.

In all the cases, the average dc-side voltages are balanced to the reference value of $\langle v_{dc_k}^* \rangle$. This shows that the control block is working correctly, and consequently, the switching signals S_k that are required to obtain the dc-side currents i_{dc_k} behave as expected.

IV. CONCLUSION

This letter has analysed an online approach for capacitor condition monitoring that takes into account the inherent twice-fundamental-frequency capacitor voltage and current oscillations in LC-StatComs, thus avoiding drawbacks of high-frequency methods. The approach does not use any additional hardware for sensing the capacitor current. Instead, it uses available steady-state quantities from standard control stages. This involves accounting for the antialiasing filter and ADC delays, which are in the capacitor impedance frequency range for a healthy capacitor. The approach effectively allows the capacitor monitoring in LC-StatComs since the experimental results show an almost noiseless capacitance and ESR value estimation signals.

REFERENCES

- [1] G. Farivar, B. Hredzak, and V. G. Agelidis, “Reduced-capacitance thin-film H-bridge multilevel STATCOM control utilizing an analytic filtering scheme,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6457–6468, Oct. 2015.
- [2] H. Soliman, H. Wang, and F. Blaabjerg, “A review of the condition monitoring of capacitors in power electronic converters,” *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4976–4989, Nov. 2016.
- [3] O. Abushafa, S. Gadoue, M. Dahidah, and D. Atkinson, “A new scheme for monitoring submodule capacitance in modular multilevel converter,” in *Proc. 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, pp. 1–6, Apr. 2016.
- [4] D. Xiang, Y. Zheng, H. Li, Y. Gu, N. Zhao, and J. Zheng, “Online ESR monitoring of dc-link capacitor in voltage-source-converter using damping characteristic of switching ripples,” *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7429–7441, Jul. 2021.
- [5] E. Rodriguez Ramos, R. Leyva, G. G. Farivar, C. D. Townsend, and J. Pou, “Capacitor condition monitoring for the low-capacitance StatCom: An online approach,” *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3697–3701, Apr. 2022.
- [6] K. Yao, W. Tang, X. Bi, and J. Lyu, “An online monitoring scheme of dc-link capacitor’s ESR and C for a boost PFC converter,” *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5944–5951, Aug. 2016.
- [7] I. Polanco and D. Dujic, “Condition health monitoring of modular multilevel converter submodule capacitors,” *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3544–3554, Mar. 2022.
- [8] A. M. R. Amaral and A. J. M. Cardoso, “A simple offline technique for evaluating the condition of aluminum-electrolytic-capacitors,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3230–3237, Aug. 2009.
- [9] B. Wang, J. Meng, and P. Zhao, “Aging condition monitoring for aluminum electrolytic capacitor in variable speed drives,” *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4564–4574, Apr. 2022.
- [10] T. Isobe, L. Zhang, H. Tadano, J. A. Suul, and M. Molinas, “Control of dc-capacitor peak voltage in reduced capacitance single-phase STATCOM,” in *Proc. IEEE 17th Workshop on Control and Modeling for Power Electron. (COMPEL)*, pp. 1–8, Jun. 2016.
- [11] G. Farivar, C. D. Townsend, B. Hredzak, J. Pou, and V. G. Agelidis, “Low-Capacitance cascaded H-bridge multilevel StatCom,” *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1744–1754, Mar. 2017.
- [12] G. Farivar, “Low-Capacitance cascaded H-bridge multilevel StatCom.” <https://scileap.org/library/publication/101c5ec2-e31e-4405-bced-18ea2a0fbf56>, Aug. 2021. [Online; accessed 23-March-2023].