Design of Loss-Free Resistors Terminated at a Generic Nonlinear Static Load

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***Abstract*— Modern DC-DC power conversion represents an important challenge because connected loads are not purely resistive as it has been conventionally considered. Furthermore, the corresponding power converters perform functions which are not limited to regulate either a specific output voltage or output current. One of these new functions is the transfer of a regulated power to different types of loads, which emerge in the context of microgrids and electric vehicles, in which the sliding-mode control (SMC) is an important actor because of its versality, robustness and systematic design. This paper presents SMC of a boost converter operating as a loss-free resistor (LFR), which supplies a constant power to the parallel connection of three canonical elements, namely, a constant power load (CPL), a constant current load (CCL) and a dc voltage source with internal resistance. The studied load is defined as a generic nonlinear static load (GNSL). The subsequent analysis of the connection of the controlled power converter and the GNSL reveals the existence of a single equilibrium point, which is unconditionally stable. This feature is preserved when the GNSL is particularized in the single load cases of battery, current source or resistor, and in all cases of two-element and three-element load combinations. The exception is the supply of a single CPL, which results in an infinite number of equilibrium points with marginally stable behavior. Simulation and measurements in a 1 kW prototype are in perfect agreement with the theoretical predictions.**

***Index Terms*— Sliding-mode control, loss-free resistor, generic nonlinear static load.**

I. Introduction

CANONICAL elements for power processing are the dc transformer, the power gyrator, and the loss-free resistor (LFR). They are two-port circuits that ideally model the steady-state behavior of dc-dc switching converters, and can be categorized as Power Output- Power Input (POPI) networks since the dc input power of the converter is equal to its dc output power in steady state [1]. This modeling is not only a formal aspect but it is rather an insightful tool in many practical cases. Namely, the design of a regulated output voltage in a switching converter [2] or the implementation of energy distribution in either power supplies [3] or dc microgrids [4]. Also, the LFR model facilitates the circuit design for compensating losses to improve the efficiency [5]-[6], eliminating undesired oscillations [7], correcting the power factor of a power device supplied by the ac grid [8] or matching a photovoltaic source in a power conversion chain [9].

LFRs present a virtual resistor in the input port and a power source supplying the load in the output port. Regarding their implementation, the traditional approach lies in the buck-boost operation in discontinuous conduction mode (DCM) [10]-[11], this being the case of references [5]-[9]. Another successful implementation is the result of the interconnection of several flyback converters in both DCM and interleaved operation [12]. On the other hand, LFR behavior results from the use of sliding-mode control (SMC) [13], which imposes proportionality between input voltage and current in steady-state and continuous conduction mode (CCM) in switching power converters with a series inductor in the input port and a resistor loading the output port. The same SMC-based principle allows to synthetize a CPL device in the input terminal of the same converters as reported in [14]. Besides, the extension to a three-phase rectifier of the LFR synthesis based on SMC has led to the notion of tetra-port LFR, i.e. a four-port device presenting a virtual resistor in each of the three input ports and a power source in the remaining output port [15].

Power factor correction (PFC) and impedance matching in photovoltaic (PV) systems are currently the main applications of the LFRs synthetized by an appropriate control. In the first case, PFC is the result of SMC either in a semi-bridgeless rectifier [16] or in a boost converter [17], while it stems from a current control with adaptive features in reference [18]. LFR behavior in a power converter for impedance matching is the result of the inner loop control in a two-loop strategy for maximum power point tracking in a PV system as described in [19]. In addition, SMC-based LFRs have been used to implement the first stage of versatile ballast for discharge lamps [20] and to adapt a sea wave energy harvesting transducer to a battery supplying a standalone payload [21].

SMC is well established in the control of modern power electronics equipment, which is based on the concept of multi-converter systems rather than on the classical notion of single converter. A recent example of this is the special issue devoted to SMC of power converters in renewable energy systems [22] compiling up to sixteen works, in which examples of both first and second order SMC are described in applications ranging from tracking a time varying reference in a three-phase PWM AC/DC voltage source converter to the control of a multiphase buck converter for battery emulation.

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The performance of first and second order sliding-mode controllers has been compared in a dual active bridge showing excellent regulation and robust characteristics in both cases but more sensitivity in the second order approach [23]. Second order SMC based on a cascade scheme of a super twisting algorithm has been implemented to regulate a buck converter and compared with other SMC algorithms showing the fastest response, smallest settling time and significant chattering reduction [24]. An SMC is used in [25] to track successfully a time-varying reference signal for a RF envelope in a buck converter operating in CCM using a first order approach with a sliding surface made up of a linear combination of the error plus the derivative and integral of the error, i.e. a sort of PID surface.

High-order converters such as the super-buck converter and the quadratic buck converter have also been the subject of recent SMC implementation in [26] and [27] respectively. In the first case, a sliding surface based on a linear combination of output voltage error and output current error allows a good output regulation with a relatively small deviation of the switching frequency for small changes of the nominal resistance. In the second case, a cascade control whose inner loop uses a SMC of the input inductor current and the outer loop regulates the output voltage and establishes the reference to the inner loop allows the output voltage regulation of the quadratic buck converter interfacing a 380 V dc domestic bus and a 48 V dc battery.

Output voltage regulation with suppression of time-varying disturbances and significant reduction of chattering is reported in [28], where a boost converter is controlled by a terminal SMC strategy, which uses a finite time disturbance observer.

Moreover, both the traditional approach and the use of an appropriate control result in an LFR whose input port is connected in parallel with the input power supply. Recently, the concept of series loss-free resistor (SLFR) has been disclosed in [29]. It consists in an LFR whose virtual resistance is connected in series between the input and output ports of a power stage while its power source is connected in parallel with the external energy source. Examples in that work illustrate a realization of the LFR based on a power converter operating in DCM. In [30], the SLFR concept is extended by differentiating load-side and source-side realizations depending on the power source connection. In the latter reference, a current controller in a converter operating in CCM imposes the LFR behavior in contrast with the work reported in [29].

It has to be pointed out that all implemented LFRs reported in the literature terminate at a resistor, and it has not be proved that they can exhibit the same performance if the resistor is substituted by other types of loads. Resistive load has been the classical approach to model the one-port device supplied by a centralized converter in telecom or computer equipment but the increased use of multi-converter systems in electric vehicles and microgrids has introduced the notion of constant power load (CPL) and constant current load (CCL). Besides, the existing interest for fast charging of electric vehicles [31] has brought up lithium-ion batteries as candidates for new type of load in converter systems [32].

Charging techniques consist in a first phase of either constant current (CC), constant power (CP) or other profiles, followed by a phase of constant voltage (CV) [33]. Hence, the first phase of the battery charging system can be modelled in some cases by a constant current source or by a constant power source in others. In both situations, the active source feeds a battery that can be effectively modelled as a voltage source in series with a resistor.

Note that an LFR-based converter transferring power to any type of load would regulate the power indirectly in a relatively simple way by means of the emulated resistor at the input port. In a clear-cut contrast, a direct regulation in any converter would require processing the product of current and voltage of the output port and result in a more complex system for both analysis and implementation.

Power regulation can be used not only in the implementation of the first phase of a CP-CV protocol for battery charging but also in the voltage regulation of power converters as an alternative to the current-mode approach. The latter is a two-loop control scheme in which the inner loop processes the inductor current to establish the transition from on to off and vice-versa while the outer loop regulates the output voltage and provides the appropriate reference to the inner loop [10]. The inner loop usually processes a function of the inductor current, which is associated to the dynamic behavior of its average, peak or valley values and can be equally implemented in pulse-width modulated or in hysteresis-modulated systems under the optics of SMC. In all cases, the function of the inductor current is independent of the input voltage. In the work here analyzed, the function of the inductor current is a linear combination of that current and the input voltage, which yields to a proportional relation between both signals and to regulate the input power through the proportionality coefficient (LFR resistance). In this sense, the LFR approach proposed here can open the way to power-mode control of dc-dc switching converters with any type of load if a subsequent systematic analysis to design the outer loop for voltage regulation is developed in future studies.

Therefore, it makes sense to explore the SMC-based LFR design in an appropriate converter loaded by the parallel connection of a CPL, a CCL and a battery with internal resistance. The resulting combination presents a current versus voltage nonlinear static characteristic, i.e. it constitutes a generic nonlinear static load (GNSL). It can be expected that particularization of GNSL in the case of CPL, CCL, a single resistor or a battery as well as in the combination of pairs of loads or groups of three loads can give sufficient insight for the design of power systems feeding loads from a constant power source.

More specifically, the main contributions of this paper are enumerated as follows:

• Definition of General Nonlinear Static Load (GNSL). From the observation of the type of load used in a classical power electronics equipment (resistor) and in new applications like electric vehicles and microgrids (CPL, CCL and battery), we propose a parallel combination of three of them to introduce the notion of GNSL. A realistic scenario in modern power distribution systems is a DC bus supplying a combination of the mentioned loads characterized by GNSL.

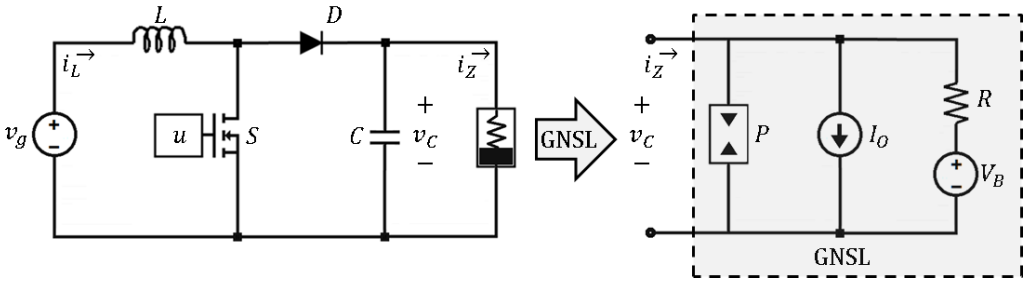


Fig. 1. Boost converter loaded with a GNSL.

• Power transference regulation. The design of a boost converter with LFR characteristics in the role of a DC bus allows the transference of regulated power to the GNSL. The SMC approach demonstrates that there is a single equilibrium point, which is unconditionally stable. The particularization of the GNSL in three cases of single load, six cases of couple of loads and four cases of three-load combination also results in a stable equilibrium point in each case. The stability is guaranteed by the active damping introduced by the virtual resistance of the LFR.

• Unfeasible supply of a CPL. If the LFR supplies only a CPL, the power of the source and the power of the sink must be equal to keep the POPI nature of the converter, which yields an infinite number of equilibrium points with marginally stable behavior.

The rest of the paper is organized as follows. Section II shows the existence of sliding motions in a boost converter loaded with a GNSL for a given switching surface and an appropriate switching law. The analysis of the equilibrium point is carried out in Section III, and the local stability is covered in Section IV. Simulation and experimental results are presented in Section V. The influence of the parasitic resistances is analyzed in Section VI. Finally, conclusions are summarized in Section VII.

II. SMC-Based LFR in a Boost Converter with GNSL

Fig. 1 shows a boost converter loaded by a GNSL, which is the parallel connection of a CPL, a CCL and a battery with internal resistance. The small letters in the figure represent instantaneous values of the converter variables. The objective of SMC is obtaining a two-port circuit whose steady-state equations are the following:

$$V_1 = rI_1 \quad (1)$$
$$V_1 I_1 = V_2 I_2 \quad (2)$$

Equations (1) and (2) characterize an LFR, so, in steady-state, Fig. 1 can be described as illustrated in Fig. 2 (Input port: $V_1 = V_g$ and $I_1 = I_L$, output port: $V_2 = V_C$ and $I_2 = I_Z$). Letter r represents the virtual resistance of the LFR ideally transferring the 100% of the absorbed power P from the input port to the output port. Capital letters stand for steady-state values of the converter variables.

In CCM, the converter in Fig. 1 can be described as follows

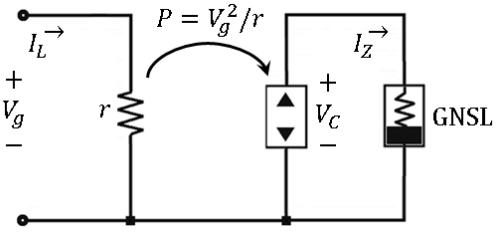


Fig. 2. Equivalent circuit of an LFR loaded with a GNSL.

$$L\frac{di_L}{dt} = V_g - v_C(1-u) \quad (3)$$
$$C\frac{dv_C}{dt} = i_L(1-u) - i_z \quad (4)$$

where $u = 1$ during ON state of the controlled switch and $u = 0$ during its OFF state, and current i_z is given by

$$i_z = \frac{P}{v_C} + I_o + \frac{v_C}{R} - \frac{V_B}{R} \quad (5)$$

To fulfil (1), $S(x)$ is selected as follows

$$S(x) = ri_L - V_g \quad (6)$$

which implies

$$S(x)\frac{dS(x)}{dt} = r\left(ri_L - V_g\right)\frac{V_g - v_C(1-u)}{L} \quad (7)$$

Given that $V_g - v_C < 0$, it can be deduced that $S(x) > 0$ and $u = 0$ will result in $S(x)\frac{dS(x)}{dt} < 0$. Similar result is obtained for $S(x) < 0$ and $u = 1$. Therefore, sliding motions will exist in the boost converter of Fig. 1 with the selected sliding surface and the associated switching law described above [13].

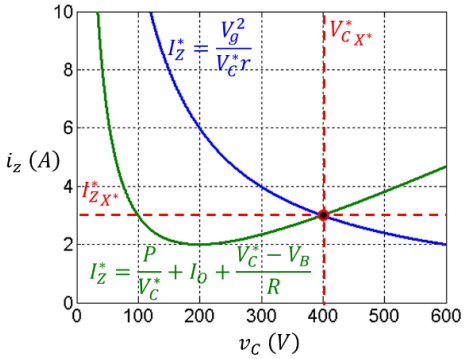
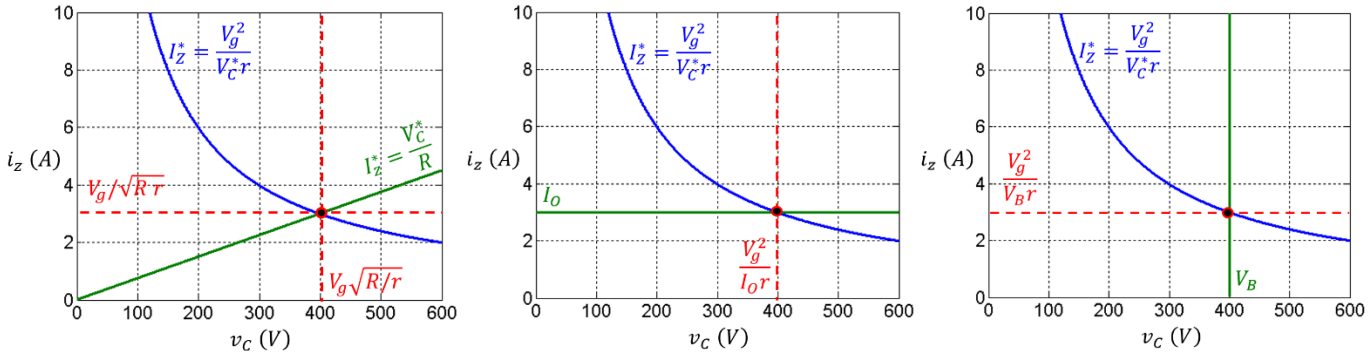


Fig. 3. Equilibrium point of the output port of the LFR loaded with a GNSL.



a) b) c)

Fig. 4. Equilibrium point for: a) resistive load; b) CCL; and c) voltage source load.

III. Equilibrium Point Analysis

The invariance condition $\frac{dS(x)}{dt} = 0$ results in the equivalent control [34] $u_{eq} = 1 - \frac{V_g}{v_C}$. Introducing the constraint $S(x) = 0$ in (3)-(4), and substituting u by u_{eq} in the same equations lead to the following ideal sliding dynamics

$$\frac{dv_C}{dt} = \frac{V_g^2}{Crv_C} - \frac{i_Z}{C}, \qquad i_L = \frac{V_g}{r} \tag{8}$$

In equilibrium, $v_C = V_C^*$, $i_Z = I_Z^*$, and $\frac{dv_C}{dt} = 0$, which implies $\frac{V_g^2}{r} = V_C^* I_Z^*$, or equivalently dc input power equal to dc output power in steady-state. However, I_Z^* is a nonlinear function of V_C^*, and therefore the equation describing the possible values of V_C^* is given by

$$\frac{V_g^2}{r} = P + V_C^* I_o + \frac{V_C^{*2}}{R} - \frac{V_C^* V_B}{R} \tag{9}$$

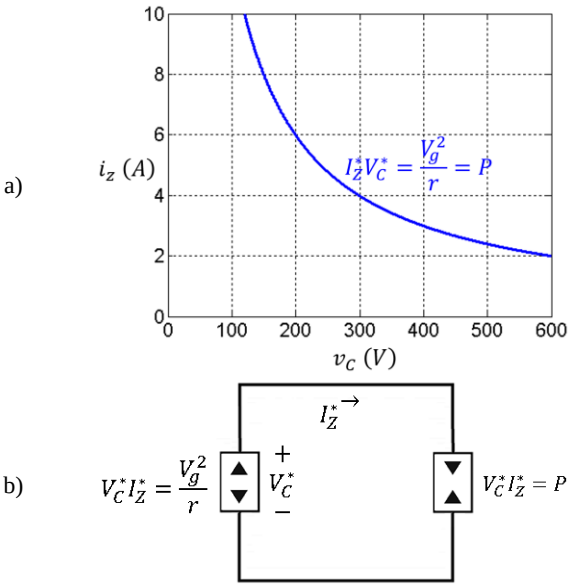
Assuming $\frac{V_g^2}{r} > P$, only one equilibrium point X^* will exist and the value of V_C^* will be given by

$$V_{C\,X^*}^* = \frac{V_B - I_0 R + \sqrt{(I_0 R - V_B)^2 + 4R\left(\frac{V_g^2}{r} - P\right)}}{2} \tag{10}$$

which corresponds to the horizontal coordinate of the intersection point of the i-v curve of the power source in Fig. 3 given by $I_Z^* = \frac{V_g^2}{V_C^* r}$ and the curve $I_Z^* = \frac{P}{V_C^*} + I_o + \frac{V_C^*}{R} - \frac{V_B}{R}$ corresponding to the GNSL in a MATLAB simulation for the set of parameter values $V_g = 240$ V, $r = 48\ \Omega$, $P = 400$ W, $I_o = 1$ A, $R = 100\ \Omega$ and $V_B = 300$ V.

Figs. 4a-4c show respectively the values of the equilibrium point when the GNSL becomes a resistive load ($P = 0$, $I_o = 0$ and $V_B = 0$), a CCL ($P = 0$ and $R = \infty$) or a voltage source ($P = 0$, $R = 0$ and $I_o = 0$). The CPL case, i.e. $R = \infty$ and $I_o = 0$ results in an infinite number of equilibrium points because the load and the power source are characterized by the same curve as illustrated in Fig. 5a. This case corresponds to the connection of a power source in parallel with a power sink (CPL), which is only consistent when both devices handle the same amount of power P (Fig.5b).

All the six possible combinations of pairs of canonical loads yield attainable equilibrium points as listed in Table I, where the value of V_C^* in the equilibrium point is given in each case. Similarly, the four possible combinations of three loads lead to a single equilibrium point as illustrated in Table II. Recall that expressions in Table I and Table II are obtained by particularizing expression (10) for each type of load combinations.



a)

b)

Fig. 5. Infinite number of equilibrium points for: a) CPL; and b) circuit interpretation.

IV. Stability of the Equilibrium Point

The ideal sliding dynamic behavior is described by the nonlinear differential equation (8), which can be rewritten as follows

$$C\frac{dv_C}{dt} = \frac{V_g^2}{rv_C} - i_Z := g(x) \tag{11}$$

The linearized system around the equilibrium point X^* will be given by

$$C\frac{d\widehat{v_C}}{dt} = \alpha\widehat{v_C} \tag{12}$$

TABLE I
OUTPUT VOLTAGE AT EQUILIBRIUM POINT FOR PAIRS OF LOADS

GNSL	V_C^*
CPL-R ($I_O = 0, V_B = 0$)	$\sqrt{R\left(\frac{V_g^2}{r} - P\right)}$
CPL-CCL ($R \to \infty$)	$\frac{1}{I_O}\left(\frac{V_g^2}{r} - P\right)$
CPL-Voltage source ($I_O = 0, R = 0$)	V_B
CCL-R ($P = 0, V_B = 0$)	$\frac{1}{2}\left(-I_O R + \sqrt{I_O^2 R^2 + 4R\frac{V_g}{r}}\right)$
Voltage source with R ($I_O = 0, P = 0$)	$\frac{1}{2}\left(V_B + \sqrt{V_B^2 + 4R\frac{V_g^2}{r}}\right)$
CCL-Voltage source ($P = 0, R = 0$)	V_B

TABLE II
OUTPUT VOLTAGE AT EQUILIBRIUM POINT FOR COMBINATIONS OF THREE LOADS

GNSL	V_C^*
CPL-Voltage source with R ($I_O = 0$)	$\frac{1}{2}\left(V_B + \sqrt{V_g^2 + 4R\left(\frac{V_g^2}{r} - P\right)}\right)$
CPL-R-CCL ($V_B = 0$)	$\frac{1}{2}\left(-I_O R + \sqrt{I_O^2 R^2 + 4R\left(\frac{V_g^2}{r} - P\right)}\right)$
CPL-CCL-Voltage source ($R = 0$)	V_B
CCL-Voltage source with R ($P = 0$)	$\frac{1}{2}\left(V_B - I_O R + \sqrt{(I_O R - V_B)^2 + 4R\frac{V_g^2}{r}}\right)$

where

$$\alpha = \frac{\partial g(x)}{\partial v_C}\bigg|_{v_C = V_C^*} = -\frac{V_g^2}{r V_C^{*2}} - \frac{\partial i_Z}{\partial v_C}\bigg|_{v_C = V_C^*} \tag{13}$$

On the other hand,

$$i_Z = \frac{P}{v_C} + I_o + \frac{v_C}{R} - \frac{V_B}{R} \tag{14}$$

Hence,

$$\alpha = -\frac{V_g^2}{r V_C^{*2}} + \frac{P}{V_C^{*2}} - \frac{1}{R} \tag{15}$$

Note that the system terminated with a GNSL will be always stable because the input power is always larger than the power absorbed by the CPL, namely,

$$\frac{V_g^2}{r V_C^{*2}} > \frac{P}{V_C^{*2}} \qquad \text{which implies } \alpha < 0 \tag{16}$$

It immediately follows from (15) and (16) that all the particular cases of GNSL considered in the previous section will be stable with the exception of the single CPL case. In this case, the system is marginally stable because α in (15) is zero since the left term of (16) equals the right term in equilibrium. This result coincides with the theoretical prediction given in [35] when a general polynomial sliding surface of first degree takes the particular expression given by (6).

Note that the active damping introduced by the virtual resistance r of the LFR ensures the stability. This fact is particularly remarkable in the case of a single CCL of current I_0, in which a classical approach based on the converter dynamic model predicts the presence of imaginary poles in the control to output transfer function $G_C(s)$ due to the absence of resistive elements in the power stage. In that case $G_C(s)$ will be given by

$$G_c(s) = \frac{V_g}{(1-D)^2}\left(1 - \frac{sLI_0}{V_g(1-D)}\right)\frac{1}{1 + \frac{s^2 LC}{(1-D)^2}} \tag{17}$$

where D is the steady-state duty cycle, and the necessary damping should be introduced by appropriate current feedback [36].

V. SIMULATION AND EXPERIMENTAL RESULTS

To validate the proposed study, several simulations have been carried out in PSIM software and a prototype of the boost converter has been built in our laboratory. The prototype utilizes $C = 20$ µF (MKP1848SE62050JP4C), $L = 550$ µH, one power MOSFET (STW25NM60ND) and one dual fast-recovery diode (STPSC20H12CWL). One leg is the diode of the converter, and the other one is used to give initial voltage $v_C(0) = V_g$ to guarantee the existence of sliding mode conditions at the start-up and therefore mitigate the inrush current [37]. The control circuit makes use of Hall-effect sensors measuring input voltage (LEM – LV25P) and inductor current (LEM – LA25NP) and analogue electronics for mathematical operations (AD633, LM324). Gate signal is applied using an opto-isolated driver (TLP350H) fed by a dedicated isolated source (TRACO TEN 3-2415N). Switching at a finite frequency in the system is induced by means of a hysteresis comparator implemented with analogue electronics (LM319, CD4027). The schematic diagram of the power stage of the converter prototype is illustrated in Fig. 6 while the controller circuitry is depicted in Fig. 7. From left to right, it is possible to observe the conditioning circuits for voltage and current measurements, mathematical operations to define the sliding surface, the circuit creating the limits of the hysteresis band and the hysteresis comparator based on the SR flip-flop.

The experimental set-up consists of an oscilloscope (Tektronix MDO3024) with one isolated current probe (U3401A) and two differential voltage probes (Yokogawa 700924), one power source feeding the power converter (ELEKTRO-AUTOMATIK EA PSI-9750-40), two power sources feeding the control circuits (TERMA 72-10505) and three programmable electronic loads (EA ELR-9750-44, EA EL-3400-25 and EA EL9750-75 HP). Fig. 8 is a picture of the experimental setup where the converter prototype, GNSL, oscilloscope, input voltage source and control supply can be identified.

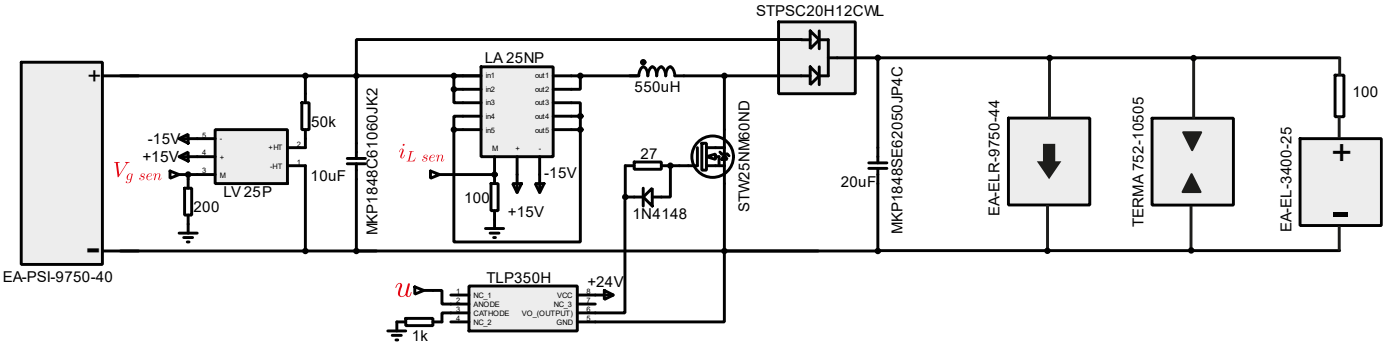


Fig. 6. Schematic diagram of the implemented boost converter circuit.

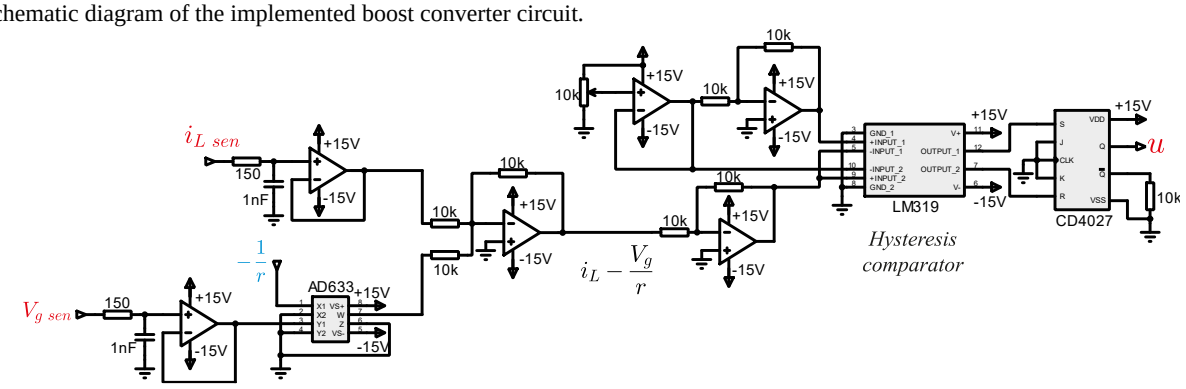


Fig. 7. Schematic diagram of the implemented controller circuit.

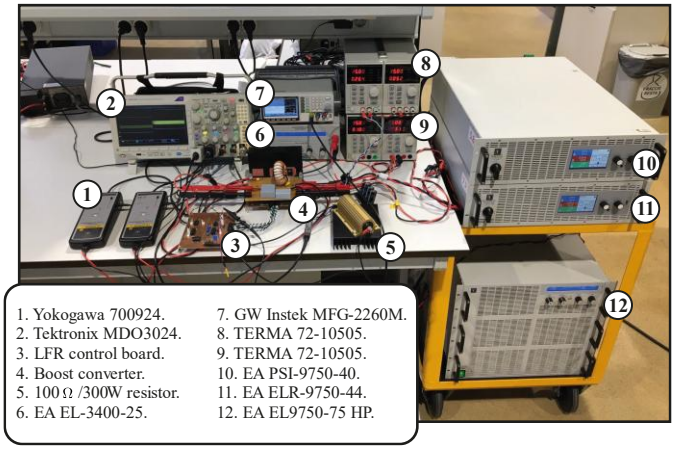


Fig. 8. Photography of the experimental setup and converter prototype.

Fig. 9 shows the simulated waveforms and the corresponding experimental results for the set of parameter values $V_g = 240$ V, $r = 52\ \Omega, P = 350$ W, $I_o = 0.92$ A, $R = 100\ \Omega, V_B = 287$ V. Figs. 9a and 9b depict the simulation and the measured results respectively of the inductor current and capacitor voltage waveforms in steady-state when the GNSL is composed of all studied elements. It can be observed that the average value of the simulated output voltage is the predicted value in expression (10).

Fig. 10 illustrates the simulation results for the stable transition from a first equilibrium point to a new one corresponding to a change in the virtual resistance of the LFR for different combination of loads in the GNSL (CCL, battery type, battery type and CPL, CCL and CPL, battery type and CCL, and battery type and CCL and CPL). As it can be observed, all the steady-states evaluated are stable and the transitions show the expected first-order dynamic behavior with a settling time given by $-4/\alpha$ as theoretically predicted by equation (12).

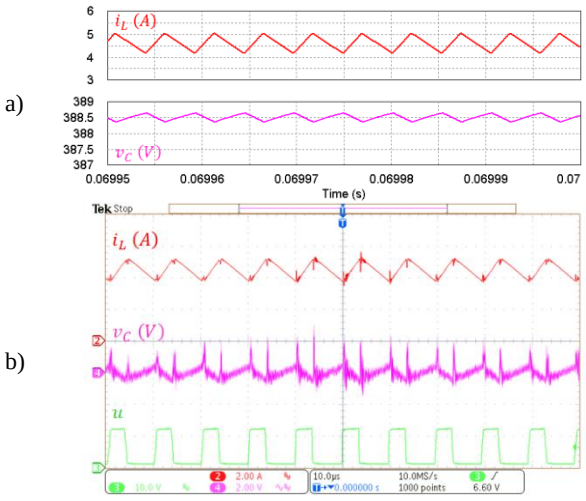


Fig. 9. Waveforms for GNSL with all the elements: a) PSIM simulation; and b) measured inductor current (DC+AC) and measured voltage (AC).

Fig 11 shows the experimental results for the same combination of loads in the GNSL used for simulations. A good agreement is observed between the steady-state values in simulations and measured waveforms. The time constant of the transitions is higher in experiments because the input capacitances of the electronic loads emulating the GNSL

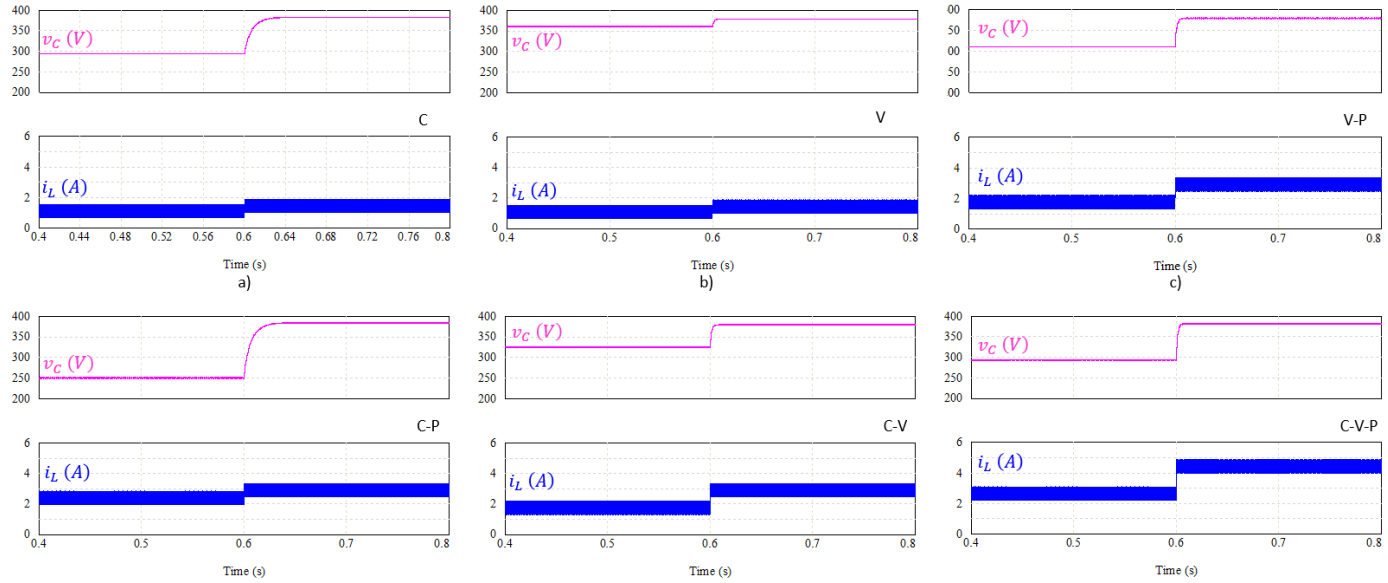


Fig. 10. Simulation results showing the system behavior when a step-type change is applied to the virtual resistance r and different combinations of elements in the GNSL are considered: a) CCL (r from 215 Ω to 164 Ω), b) Battery type load (r from 215 Ω to 164 Ω), c) Combination of a CPL with a battery type load (r from 136 Ω to 82 Ω), d) Combination of a CPL with a CCL (r from 100 Ω to 82 Ω), e) Combination of a CCL with a battery type load (r from 136 Ω to 82 Ω), and f) Combination of the three types of loads (r from 90 Ω to 54 Ω).

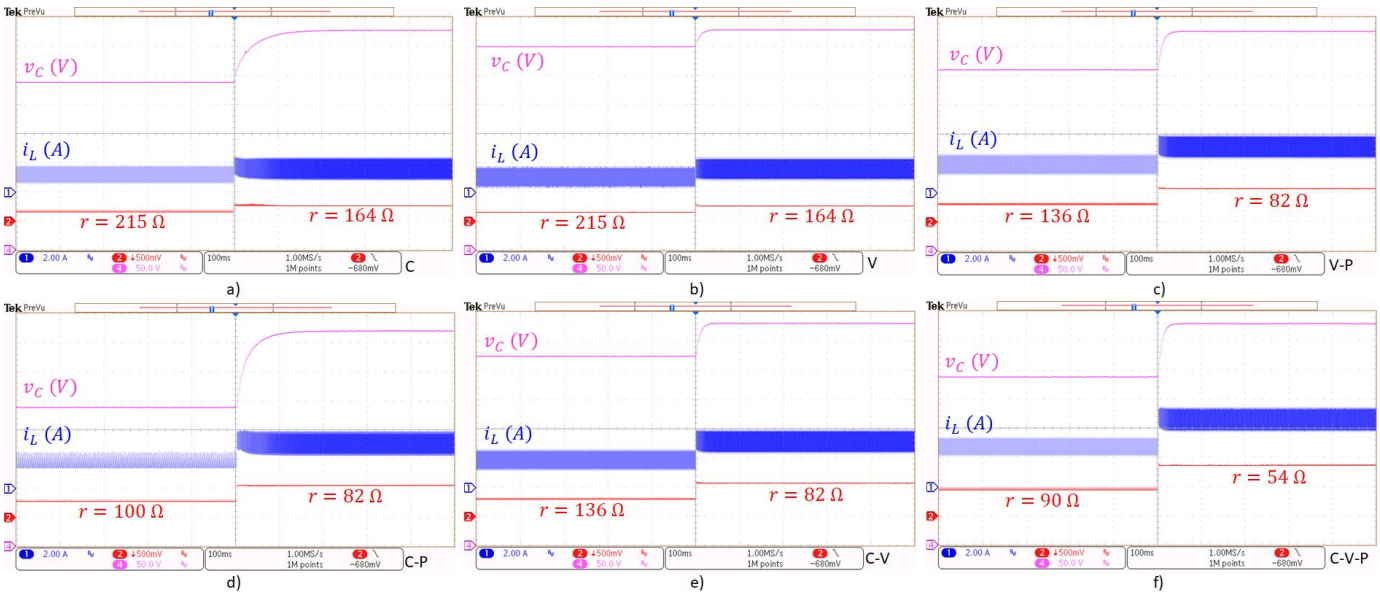


Fig. 11. Experimental results showing the system behavior when a step-type change is applied to the virtual resistance r and different combinations of elements in the GNSL are considered: a) CCL (r from 215 Ω to 164 Ω), b) Battery type load (r from 215 Ω to 164 Ω), c) Combination of a CPL with a battery type load (r from 136 Ω to 82 Ω), d) Combination of a CPL with a CCL (r from 100 Ω to 82 Ω), e) Combination of a CCL with a battery type load (r from 136 Ω to 82 Ω), and f) Combination of the three types of loads (r from 90 Ω to 54 Ω). Scales: Time – 100 ms/div, Ch. 1 (i_L) – 2 A/div, Ch. 2 (r) – 500 mV/div and Ch. 4 (v_C) – 50 V/div.

behavior are connected in parallel with the output capacitance of the boost converter but they have not been considered in the simulations.

Finally, we have simulated the case in which the converter controlled as an LFR feeds a pure CCL, and compared its behavior with the one in open loop feeding the same type of load. Two equilibrium points have been selected corresponding to output power values of 350 and 500 W respectively. Considering an input voltage $V_g = 240$ V, these points correspond to virtual resistances of $r = 164\ \Omega$ and $r = 115\ \Omega$ in the case of the LFR and duty cycles of $D = 0.37$ and $D = 0.56$ in the case of the converter operating in open loop. As it can be observed in Fig. 12a, the system operating as an LFR feeding the CCL shows a stable behavior in the corresponding equilibrium points and in the transition between them. Unlike the LFR case, the steady-state for converter operating in open loop is characterized by a sustained oscillation around the equilibrium average value whose frequency is derived from expression (17) and given by

$$f_0 = \frac{1-D}{2\pi\sqrt{LC}} \tag{18}$$

It can be observed in (18) that the oscillation frequency depends on the duty cycle and hence on the equilibrium point as illustrated in Fig 12.b. A higher value of the duty cycle results in a smaller value of the oscillation frequency.

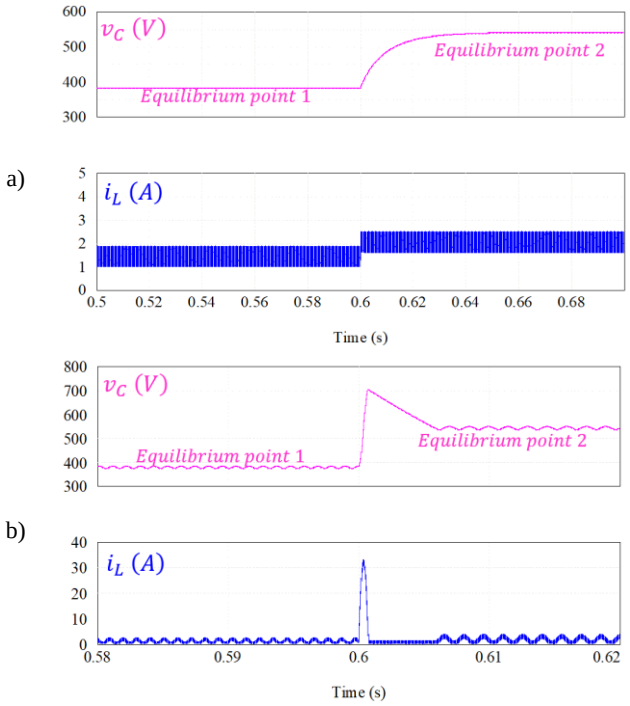


Fig. 12. Simulation results for a transition between two equilibrium points when the load is a CCL: a) change of the virtual resistance of the LFR from 64 to 115 Ω, and b) change of the duty cycle in open loop from 0.5 to 0.6.

VI. Influence of Parasitic Resistances

Parasitic resistances are present in the final implementation of any power converter and they mainly affect the resulting efficiency [38] but can also slightly change the expected value of the equilibrium output voltage in certain cases [35] or introduce a steady-state error in the estimated value of a load parameter [39]. In all cases, they model the conduction loss and are usually represented by a single resistor R_l in series with the inductor to represent equally the loss effect in the inductor and transistor during on state or in the inductor and diode during off state.

Assuming a resistor R_l in series with the inductor in Fig. 1 results in the following expression of the equivalent control

$$u_{eq}(x) = 1 - \frac{V_g - R_l i_L}{V_g} \tag{19}$$

Hence, the ideal sliding dynamics can be expressed as

$$\frac{dv_C}{dt} = \frac{V_g^2\left(1-\frac{R_l}{r}\right)}{Crv_C} - \frac{i_Z}{C}, \quad i_L = \frac{V_g}{r} \tag{20}$$

By comparing (8) and (20) it can be observed that the term V_g^2 in (8) is modified by the factor $\left(1-\frac{R_l}{r}\right)$ in (20), which represents the effect of the conduction loss.

Therefore, the steady-state power balance given by (9) will be expressed now as

$$\frac{V_g^2\left(1-\frac{R_l}{r}\right)}{r} = P + V_C^* I_0 + \frac{V_C^{*2}}{R} - \frac{V_C^* V_B}{R} \tag{21}$$

It can be observed that the left term of (21) is the difference between the dc input power and conduction loss in steady-state.

Hence, the horizontal coordinate $V_{C\,X^*}^*$ of the equilibrium point will be given by

$$V_{C\,X^*}^* = \frac{V_B - I_0 R + \sqrt{(I_0 R - V_B)^2 + 4R\left[\frac{V_g^2\left(1-\frac{R_l}{r}\right)}{r} - P\right]}}{2} \tag{22}$$

In the design here reported the emulated resistance r ranges from 54 Ω to 215 Ω and a realistic assumption for R_l is 1 Ω, which implies that in all the examples considered above the following approximation applies

$$V_g^2\left(1-\frac{R_l}{r}\right) \approx V_g^2 \tag{23}$$

Hence, expression (22) becomes expression (10) and therefore it can be concluded that the parasitic resistance R_l has a negligible effect in the coordinates of the equilibrium point provided that its value is considerably smaller than the virtual resistance r.

Similarly, the stability condition (16) becomes

$$\frac{V_g^2\left(1-\frac{R_l}{r}\right)}{rV_C^{*2}} > \frac{P}{V_C^{*2}} \tag{24}$$

Condition (24) is always fulfilled because the input power is higher than the sum of the power absorbed by the CPL and the conduction loss.

Nonetheless, the effect of the parasitic resistance R_l on the equilibrium point coordinates can be significant for small values of the emulated resistance r.

Fig. 13 shows simulated results regarding the steady-state and transient behavior of a nonideal boost converter operating as LFR and feeding a GNSL composed by the three studied elements ($V_g = 240$ V, $P = 350$ W, $I_o = 0.92$ A, $R = 100$ Ω and $V_B = 287$ V). The test consists in comparing the steady-state values and the transient response of the system for three different values of the parasitic resistance R_l (0 Ω, 1 Ω and 27 Ω) when a sudden change is applied in the reference of the input virtual resistor value r (from 90 Ω to 54 Ω). As it can be observed, the difference between the cases of 0 Ω and 1 Ω is imperceptible. Also, as predicted, for very large values of R_l the equilibrium point suffers a deviation caused by the loss of efficiency in the system. Complementarily, it is possible to observe that the transient response does not suffer a considerable deviation with the increment of the parasitic resistance. These results allow to confirm the validity of the theoretical study based on the ideal converter.

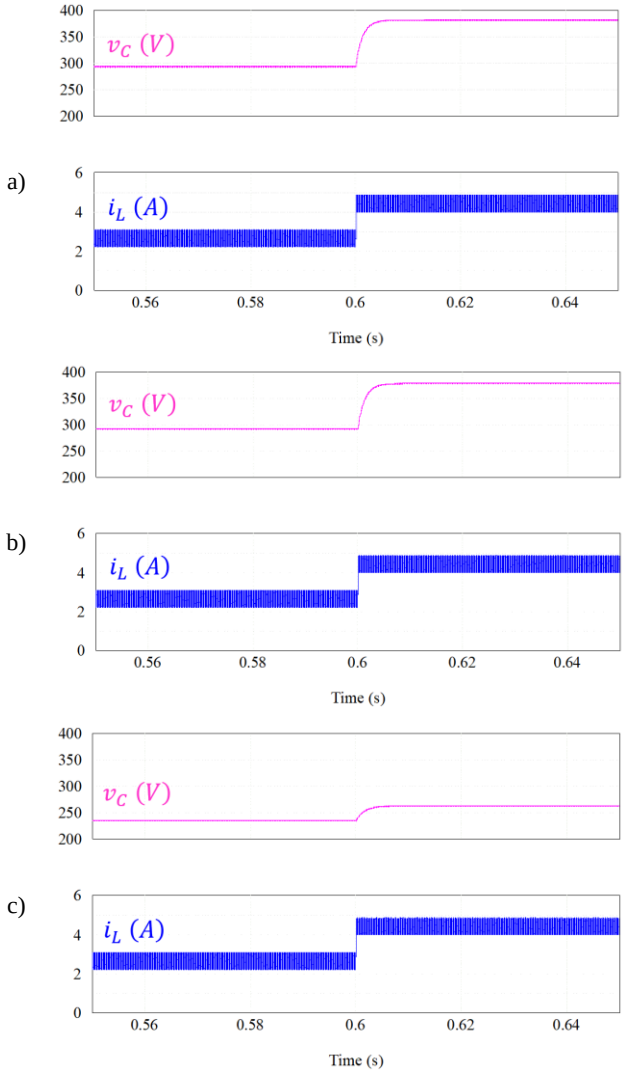


Fig. 13. Simulation results for a transition between two equilibrium points regarding the effect of the parasitic resistance R_l: a) 0 Ω, b) 1 Ω and c) 27 Ω.

VII. Conclusions

A boost converter terminated at a GNSL can exhibit LFR characteristics by imposing a sliding-mode behavior using the switching surface $S(x) = ri_L - V_g$, and the switching policy described in this article. The GNSL is a parallel connection of a CPL, a CCL, and a voltage source with internal resistance. The particularization of the GNSL in cases of single load, couple of loads, and three- load combination has led to one stable equilibrium point in each of them. The stability is guaranteed by the active damping introduced by the virtual resistance r. However, if the LFR supplies a CPL, there are infinite equilibrium points with marginally stable behavior.

The work reported here is a first step in the design of power-mode control of dc-dc switching converters. The insertion of an outer loop for voltage regulation to design a CP-CV protocol for battery charging is in progress. The need of robustness of the CV phase would require an ad-hoc SMC analysis either for an appropriate PI design [40] or for the inclusion of uncertainties in the theoretical approach [41].

Further research contemplates the extension of the analysis to the SEPIC and Ćuk converter for cases of voltage step-down applications.

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