Comparison of Three-Clamping-Level and Two-Clamping-Level Discontinuous Modulations in Cascaded H-Bridge Static Compensators

***Abstract*—This paper formulates a three-clamping-level discontinuous pulse-width modulation (DPWM) for three-phase cascaded H-bridge static compensators with star configuration. Analytical expressions of capacitor voltage and zero-sequence voltage under the three-clamping-level DPWM are provided considering the inherent capacitor voltage oscillations. Based on the derived expressions, the paper analyses: (i) the inductive operation limits, and (ii) the total harmonic distortion (THD) and weighted THD of the output voltages. The results are compared with the continuous modulation and the conventional two-clamping-level DPWM, showing their different performances.**

I. Introduction

Discontinuous pulse width modulation (DPWM) is a widely used methodology to reduce switching losses. In the three-phase system, zero-sequence voltage (ZSV) offers the degree of freedom to clamp the converter voltages. Specifically, DPWM can be achieved by clamping the ac-side converter voltage to its corresponding dc-link voltage with a proper ZSV.

The implementation of DPWM is straightforward in the three-phase two-level voltage source converters since the needed ZSV for DPWM is merely the difference between the ac-side voltage and the dc-rail. However, in the low capacitance StatComs (LC-StatCom), because of its nonnegligible dc-link voltage dynamics, the implementation of DPWM should be treated with caution [1]. LC-StatCom operates with reduced dc-link capacitance, thus its dc-link voltages are subjected to large double-grid frequency voltage ripple [2]. In the LC-StatCom, the coupling between dc-link capacitor voltages and the injected ZSV cannot be neglected.

A DPWM strategy which takes into account such coupling relationship is proposed in [1]. Under the DPWM, the phase-arm with the largest absolute value of ac-side converter voltage references is clamped to either its positive or its negative dc-link voltage depending of the sign of the clamped converter voltage. Considering the coupling between the dc-link capacitor voltages and ZSVs, their analytical expressions under the DPWM are derived in [1] for control purposes. The DPWM in [1], referred as the 2DPWM, henceforth, only considers two clamping levels, i.e., positive or negative dc-link voltage. In 2DPWM frame, the injected ZSV for DPWM changes instantly between positive values and negative values, which involves large magnitude when modulation index is low. Such ZSV can significantly impacts the dynamic of the capacitor voltages, especially under unbalanced grid voltage conditions [3].

A three-clamping-level DPWM, allows a zero-voltage clamping level, thus providing an additional degree of freedom to improve the efficiency or other StatCom performances. Specifically, the analysis of dynamic performances and efficiency for a three-clamping-level DPWM can be found in [3], where it is compared with the 2DPWM. However, the studies in [3] focus on the control level, and the expression of the dc-link capacitor voltage and the ZSV under the DPWM are not given, which limits the analytical study and exploration of the approach in other important aspect, such as total harmonic distortion (THD) and weighted THD (WTHD) studies, and operational limits.

In this paper, analytical dc-link capacitor voltage and ZSV expressions under the three-level DPWM, referred as the 3DPWM, henceforth, are derived considering the inherent capacitor voltage oscillations. Based on the derived expressions, the paper studies the inductive operation limits, as well as THD and WTHD of the output voltages. The results are compared with the continuous modulation (CM) and the 2DPWM. The comparisons based on the derived analytical expressions complete the previous work in [3].

The rest of the paper is organized as follows. The mathematical model of the CHB StatCom is revisited in Section II. The ZSV injection principles of the 2DPWM and the 3DPWM are presented in Section III. Section IV derives the analytical expressions of the capacitor voltage and the ZSV under the 3DPWM. Section V analyses both inductive operation range and THD and WTHD of the output voltages. Experimental results are provided in Section VI to validate the studies. Finally, Section VII concludes the paper.

II. Mathematical Model of CHB StatComs

The circuit diagram of a CHB StatCom with star configuration is shown in Fig. 1. Each phase-arm of the converter consists of n H-bridge SMs. The ac-side positive terminals of the converter arms, (a), (b) and (c), are connected to the point of common coupling (PCC) grid voltages $v_{g,a}$, $v_{g,b}$ and $v_{g,c}$ through filter impedance (L_g, R_g), while the negative

terminals are connected together forming the neutral point of the converter. The dc-side of each SM consists of a capacitor with capacitance C.

When applying DPWM, the converter ac-side arm voltage, v_x, with $x \in \{a,\ b,\ c\}$, is the sum of a fundamental-frequency voltage v'_x and a ZSV for DPWM v_{Zd}, i.e.,

$$v_x = v'_x + v_{Zd}, \tag{1}$$

$$v'_x = L_g \frac{di_{g,x}}{dt} + R_g i_{g,x} + v_{g,x} + v_{Zb}. \tag{2}$$

Note that $i_{g,x}$ represents the StatCom current and v_{Zb} denotes the fundamental frequency ZSV for inter-phase balancing [4].

The power relationship between converter dc- and ac-side can be expressed as follows:

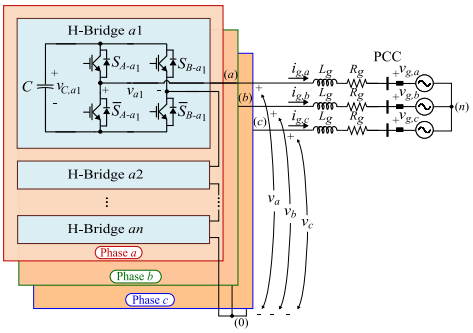

Fig. 1. Circuit diagram of a three-phase CHB StatCom with star configuration.

$$\frac{1}{2}\frac{C}{n}\frac{dv^2_{dc,x}}{dt} = -v_x i_{g,x},. \tag{3}$$

with $v_{dc,x} = \sum_{j=1}^{j=n} v_{C,xj}$, where $v_{C,xj}$ represents the capacitor voltage of the j^{th} H-bridge on phase x.

The modulating signal of the converter is defined as $\delta_x = v_x / v_{dc,x}$.

Considering sinusoidal grid voltage, v_g, and grid current, i_g, the fundamental-frequency voltage v'_x has also a sinusoidal form, according to (2),

$$v'_x = V' \cos(\theta_x), \tag{4}$$

$$i_{g,x} \ = I_g \sin(\theta_x), \tag{5}$$

where $\theta_x = \omega t + \phi_x$ is the phase angle, with ω as the angular frequency of the PCC grid voltages and $\phi_x \in \{0,\ -2\pi/3,\ 2\pi/3\}$ rad as the phase-shift among the phases. V' and I_g are the amplitude of v'_x and $i_{g,x}$, respectively. It is important to point out I_g and V' have the same sign in capacitive mode ($i_{g,x}$ lagging $\pi/2$ rad v'_x), and opposite sign in inductive mode ($i_{g,x}$ leading $\pi/2$ rad v'_x).

III. Zero-Sequence Voltage Injection Strategy

Under DPWM, at any time instant, a converter arm voltage v_x can be clamped to its corresponding dc-link voltage with positive polarity, $v_{dc,x}$, with negative polarity, $-v_{dc,x}$, or to zero, i.e., the corresponding ZSVs are named $v_{Zd,px}$, $v_{Zd,nx}$ or $v_{Zd,x0}$, respectively. Therefore, clamping can be achieved with three ZSV candidates in each arm. Specifically, the positive ZSV $v_{Zd,px}$ is the difference between the dc-link voltage and the corresponding fundamental-frequency arm voltage, i.e., $v_{Zd,xp} = v_{dc,x} - v'_x$. The negative ZSV $v_{Zd,px}$ is the difference between the negative dc-link voltage and the corresponding fundamental-frequency arm voltage, i.e., $v_{Zd,xn} = -v_{dc,x} - v'_x$. The value and sign of $v_{Zd,x0}$ depend on the corresponding fundamental-frequency arm voltage, i.e., $v_{Zd,x0} = -v'_x$.

To facilitating the grouping of positive and negative ZSV candidates, two virtual states of $v_{Zd,x0}$ are introduced, namely, a positive virtual state $v_{Zd,x0p}$ and a negative virtual state $v_{Zd,x0n}$, where

$$\begin{cases} v_{Zd,x0p} = \infty, \quad v_{Zd,x0n} = -v_x & \text{if } v'_x \geq 0, \\ v_{Zd,x0p} = -v_x, v_{Zd,x0n} = -\infty & \text{otherwise.} \end{cases} \tag{6}$$

The 3DPWM chooses the ZSV as the candidate with the minimum magnitude value, i.e.,

$$v_{Zd} = \begin{cases} v_{Zd,p} & \text{if } |v_{Zd,p}| < |v_{Zd,n}|, \\ v_{Zd,n} & \text{otherwise,} \end{cases} \tag{7}$$

where $v_{Zd,p}$ and $v_{Zd,n}$ represent the minimum value of all the positive ZSV candidates and the maximum value of all the positive ZSV candidates, respectively, i.e.,

$$\begin{cases} v_{Zd,p} & = \min\{v_{Zd,ap}, v_{Zd,bp}, v_{Zd,cp}, v_{Zd,a0p}, v_{Zd,b0p}, v_{Zd,c0p}\}, \\ v_{Zd,n} & = \max\{v_{Zd,an}, v_{Zd,bn}, v_{Zd,cn}, v_{Zd,a0n}, v_{Zd,b0n}, v_{Zd,c0n}\}. \end{cases} \tag{8}$$

The 2DPWM in [1], has the same ZSV selection criterion. However, it clamps a converter voltage only to its positive or negative dc-link,

$$\begin{cases} v_{Zd,p} & = \min\left\{v_{Zd,ap}, v_{Zd,bp}, v_{Zd,cp}\right\}, \\ v_{Zd,n} & = \max\left\{v_{Zd,an}, v_{Zd,bn}, v_{Zd,cn}\right\}. \end{cases} \tag{9}$$

Given the proposed ZSV candidates and the selection criterion in (7), the study can be carried out observing the StatCom voltage and current waveforms. Fig. 2 shows the waveforms of the CHB StatCom when the 3DPWM is applied. Note that the voltages in Fig. 2 are normalized with the maximum capacitor voltage $V_{dc,max}$ as the base value.

At rated capacitive current and nominal grid voltages, the capacitor voltage ripple under CM, denoted as r_n, and the modulation index, denoted as m_a, are defined as [2],

$$r_n = 1 - \frac{V_{dc,min}}{V_{dc,max}}, \; m_a = \frac{V'}{V_{dc,max}}, \tag{10}$$

where $V_{dc,min}$ is the minimum capacitor voltage.

In Fig. 2, it can be observed the symmetry among phase arms, and the differentiated behavior when the StatCom operates in capacitive or inductive mode. In addition, the discontinuous behavior is observed as well, with the zero-voltage level considered.

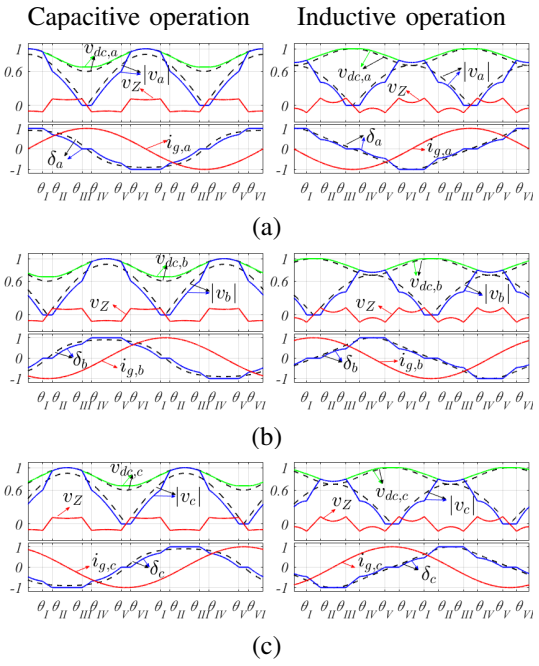

Fig. 2. Typical waveforms under the 3DPWM at $r_n = 0.4$ and $m_a = 0.9$. (a) Phase arm a, (b) Phase arm b, and (c) Phase arm c. Dashed lines are for CM and solid lines are for DPWM.

IV. Expressions of DC-link Capacitor Voltage and Zero-Sequence Voltage Under the 3DPWM

When a converter voltage v_x is clamped to its corresponding dc-link voltage $v_{dc,x}$, i.e.,

$$v_x = \text{sign}\left(v'_x\right) v_{dc,x}. \tag{11}$$

the following relationship between the converter dc- and ac-side currents applies, according to (3),

$$\frac{C}{n}\frac{dv_{dc,x}}{dt} = -\text{sign}\left(v'_x\right) i_{g,x}. \tag{12}$$

Substituting $i_{g,x}$ from (4) into (12), and integrating both sides of (12), the expression of $v_{dc,x}$ under dc-link voltage clamping can be analytically derived as,

$$v_{dc,x} = V_{cons} + V_\gamma \left|\cos\left(\theta_x\right)\right|, \tag{13}$$

where $V_\gamma = nI_g/\omega/C$, and V_{cons} is a degree of freedom to adjust the peak or the average value of dc-link voltages, and which can be considered constant due to the presence of capacitor voltage balance control loop.

Correspondingly, considering (1) and (11), and using the expression of $v_{dc,x}$ in (13), as well as the expression of v'_x in (4), the expression of v_{Zd} can be derived as,

$$v_{Zd} \;\; = \;\; V_Z \cos\left(\theta_x\right) + \text{sign}\left(v'_x\right) V_{cons}, \tag{14}$$

where $V_Z = V_\gamma - V'$.

As it can be observed from Fig. 2, the capacitor voltages are piecewise continuous, and which can be divided into six sectors in half-grid period. Due to the symmetry among phase arms under balanced grid conditions, in the following, only phase arm a is studied. Give the quarter-grid period symmetry of the capacitor voltage waveforms, the capacitor voltage and the ZSV expressions in the first four sectors are next derived considering a balanced grid condition, where the ZSV v_{Zb} for inter-phase balancing is zero [4].

Sector I: Phase arm a voltage is clamped to its positive dc-link voltage from period instant $-\theta_I$ to period instant θ_I. Note that $\theta_I \in [0, \pi/6]$. Therefore, according to (13) and (14), the ZSV, v_{Zd-I}, and the dc-link voltage in phase arm a, $v_{dc,a-I}$, during Sector I, correspond to,

$$v_{Zd-I} \;\; = \;\; V_Z \cos\left(\theta_a\right) + \text{sign}\left(v'_a\right) V_{cons}, \;\; v_{dc,a-I} = V_{cons} + V_\gamma \left|\cos\left(\theta_a\right)\right|, \tag{15}$$

Sector II: Phase arm b voltage is clamped to zero from period instant θ_I to period instant θ_{II}. Therefore, according to (3) and (4), the ZSV, v_{Zd-II}, and the square dc-link voltage in phase arm a, $v^2_{dc,a-II}$, during Sector II, correspond to,

$$v_{Zd-II} = -V' \cos(\theta_b), \tag{16}$$

$$v^2_{dc,a-II} = V^2_{dc,I} + \frac{\sqrt{3}}{2} V_\gamma V' (\theta_a - \theta_I) + \frac{\sqrt{3}}{2} V_\gamma V' \left[\cos\left(2\theta_a + \frac{\pi}{6}\right) - \cos\left(2\theta_I + \frac{\pi}{6}\right)\right], \tag{17}$$

where constant $V_{dc,I}$ is the value of $v_{dc,a}$ at the end of Sector I, i.e., $V_{dc,I} = v_{dc,a-I}|_{\omega t=\theta_I}$.

Sector III: Phase arm c voltage is clamped to its negative dc-link voltage from period instant θ_{II} to period instant θ_{III}. Similarly

$$v_{Zd-III} = V_Z \cos(\theta_c) + \text{sign}(v'_c) V_{cons}, \tag{18}$$

$$\begin{aligned} v^2_{dc,a-III} = {} & V^2_{dc,II} + \frac{\sqrt{3}}{2} V_\gamma V_Z (\theta_a - \theta_{II}) + \frac{1}{2} V_\gamma V' [\cos(2\theta_a) - \cos(2\theta_{II})] \\ & - \frac{1}{2} V_\gamma V_Z \left[\cos\left(2\theta_a - \frac{\pi}{3}\right) - \cos\left(2\theta_{II} - \frac{\pi}{3}\right)\right] + \text{sign}(v'_c)\, 2V_\gamma V_{cons} [\cos(\theta_a) - \cos(\theta_{II})], \end{aligned} \tag{19}$$

where constant $V_{dc,II}$ is the value of $v_{dc,a}$ at the end of Sector II, i.e., $V_{dc,II} = v_{dc,a-II}|_{\omega t=\theta_{II}}$.

Sector IV: Phase arm a voltage is clamped to zero from period instant θ_{III} to period instant θ_{IV}. Similarly

$$v_{Zd-IV} = -V' \cos(\theta_a), \; v^2_{dc,a-IV} = V^2_{dc,III}, \tag{20}$$

where constant $V_{dc,III}$ is the value of $v_{dc,a}$ at the end of Sector III, i.e., $V_{dc,III} = v_{dc,a-III}|_{\omega t=\theta_{III}}$.

As it can be observed from Fig. 2, θ_I is chosen such that $v_{Zd,I}|_{\omega t=\theta_I} = v_{Zd,II}|_{\omega t=\theta_I}$, which implies that

$$\theta_I = \phi - \arcsin\left(\frac{V_{cons}}{\sqrt{V'^2 + V_Z^2 + V'V_Z}}\right) \tag{21}$$

where $\phi = \arctan\left((V' + 2V_Z) / \left(\sqrt{3}V'\right)\right)$.

Note that given the symmetry of the three-phase system under balanced grid conditions, the sum of the lengths of two adjacent sectors, i.e., one zero-voltage clamping sector and one dc-link voltage clamping sector, is $\pi/3$ rad. Consequently, the lengths of zero-voltage clamping sector and dc-link voltage clamping sector are $2\theta_I$ and $\pi/3 - 2\theta_I$, respectively. Accordingly, the values of θ_{II} to θ_{VI} can be calculated based on the value of θ_I in (21) and the length of each sector.

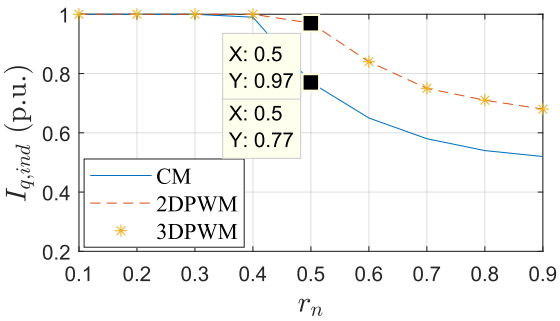

Fig. 3. Inductive operation range comparison under different r_n when $m_a = 0.9$.

As it can be observed from Fig. 2, in capacitive operation, $v_{dc,x}$ reaches to its maximum value when $\theta_x = 0 \pm k\pi$, and reaches to its minimum value when $\theta_x = \theta_{III}$, i.e., $V_{dc,min} = V_{dc,III}$. In contrast, in inductive operation, $v_{dc,x}$ reaches to its minimum value when $\theta_x = 0 \pm k\pi$, and reaches to its maximum value when $\theta_x = \theta_{III}$, i.e., $V_{dc,max} = V_{dc,III}$.

Another important remark that can be observed from Fig. 2 is that the capacitor voltages exhibit less double-grid frequency ripple under the 3DPWM than under the CM. Such feature can be used to enhance the inductive operation range of an LC-StatCom, which can be an important drawback for LC-StatComs. In next section, the inductive operation ranges of the CM, the 2DPWM, and the 3DPWM, are discussed for different nominal voltage ripple values.

V. Inductive Operation Range and Converter Voltage Quality Comparison

A. Inductive Operation Range Comparison

As it can be observed from Fig. 2, there is a $\pi/2$ rad phase-displacement between the double-grid frequency ripple of the capacitor voltage and the absolute value of the converter voltage, which limits the inductive operation range of CHB StatComs when r_n is large, namely, LC-StatComs. To study the inductive operation range under different modulations, the following inequation, which ensures the converter under modulation, is applied

$$|v_x| \leq v_{dc,x}. \tag{22}$$

With the knowledge of the capacitor voltage and ZSV expression in (15) to (21), the inductive operation range under different r_n can be accessed. Fig. 3 presents the inductive operation range of the CHB StatCom under the CM, the 2DPWM and the 3DPWM. As it can be observed, all the three modulations allow full inductive operation range when $r_n \leq 0.4$,

except that the CM provides maximum 0.99 p.u. inductive current at $r_n = 0.4$. When $r_n \geq 0.5$, the inductive operation range of the three modulations are limited. However, it should be highlighted that the 2DPWM and the 3DPWM have the same inductive operation limit, which is approximately 30% higher than the limit under the CM.

B. Converter Voltage Quality Comparison

It is noted that the difference in using ZSV among the modulations results in different modulating signals and capacitor voltages. Consequently, the pulse-width modulation (PWM) voltage waveforms under the studied modulations are different from each other. This section studies the THD and WTHD of the converter line-to-line PWM voltage under the CM, the 2DPWM and the 3DPWM. The definitions of THD and WTHD correspond to

$$THD_v = \sqrt{\frac{\sum_{h=1}^{\infty} V_{PWM(h)}^2}{V_{PWM(1)}^2} - 1}, \; WTHD_v = \sqrt{\frac{\sum_{h=1}^{\infty} \left(V_{PWM(h)}/h\right)^2}{V_{PWM(1)}^2} - 1}, \tag{23}$$

where $V_{PWM}(h)$ denotes the amplitude of the h_{th} harmonic in the converter PWM voltage.

Fig. 4(a) and (b) show the normalized line-to-neutral and line-to-line PWM voltage waveforms of a three-level CHB StatCom at $r_n = 0.4$, respectively. The clamping behaviors of the 2DPWM and the 3DPWM are evident in Fig. 4(a). Fig. 4(c) and (d) presents the THD and WTHD of the line-to-line PWM voltage in Fig. 4(b), respectively. Note that the phase-shifted PWM (PS-PWM) scheme with 2 kHz carriers is considered in this study.

As it can be observed from Fig. 4(c) and (d), both the 2DPWM and the 3DPWM have lower THD and WTHD than the CM. The 3DPWM presents similar THD and lower WTHD compared to the 2DPWM. Particularly, at $r_n = 0.4$, the 3DPWM presents 23% and 17% WTHD reduction than the CM and the 2DPWM, respectively.

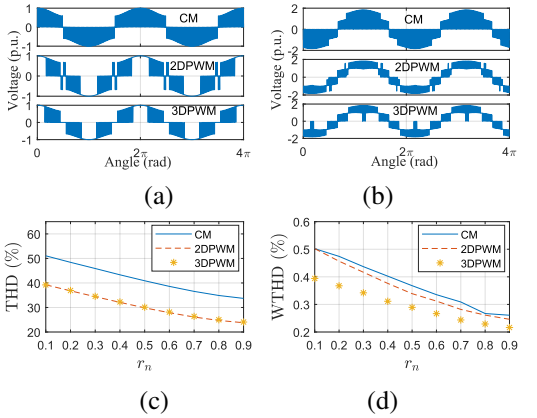

Fig. 4. THD and WTHD comparison at nominal capacitive operation. (a) Line-to-neutral PWM voltage, (b) line-to-line PWM voltage, (c) THD of line-to-line PWM voltage, and (d) WTHD of line-to-line PWM voltage.

VI. Experimental Results

Fig. 5 shows converter arm voltage experimental waveforms obtained using a 2.5 kVAr, five-level LC-StatCom prototype. The result clearly show the different clamping behaviors of the studied modulations. Due to the 5 pages limit, a complete experimental section (more results and more analysis) will be provided in the final paper.

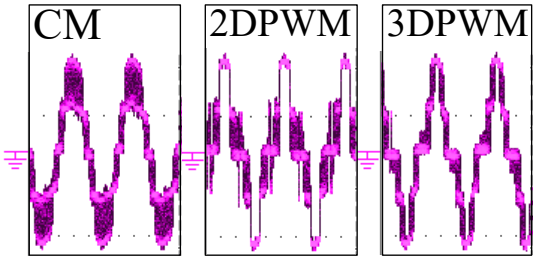

Fig. 5. Converter line-to-neutral PWM voltage under different modulations

VII. Conclusion

In this paper, a DPWM strategy, which considers zero-voltage level as the third clamping level, is presented. The analytical capacitor voltage and ZSV expressions under the proposed three-clamping-level DPWM are given. Based on the derived expressions, the inductive operation range, THD and WTHD of the output voltage, at different rated capacitor voltage ripples, are studied. Compared to the CM, the proposed three-clamping-level DPWM presents approximately 30% inductive operation range enlargement and more than 20% reduction in both PWM voltage THD and WTHD. When compared to a two-clamping-level DPWM, using zero-voltage level clamping improves neither the inductive operational range nor the voltage THD, but it improves the voltage WTHD by 15%. Both the proposed three-clamping-level DPWM and the conventional two-clamping-level DPWM outperform the CM.

Due to the 5 pages limit, only key references are included. The complete reference list will be provided in the final paper.

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