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Simulating Organic Thin Film Transistors Using Multilayer Perceptron Regression Models to Enable Circuit Design

Laurie E. Calvet, Sami El-Nakouzi, Zonglong Li, Yerin Kim, Amer Zaibi, Patryk Golec, Ie Mei Bhattacharyya, Yvan Bonnassieux, Lina Kadura, and Benjamin Iñiguez*

There is increasing interest in using specialized circuits based on emerging technologies to develop a new generation of smart devices. The process and device variability exhibited by such materials, however, can present substantial challenges for designing circuits. Three models are considered here: a physical compact model, an empirical look-up table, and an empirical surrogate model based on a multilayer perceptron (MLP) regression. Each one is fit to measurements of discrete organic thin film transistors in the low voltage regime. It is shown that the models provide consistent results when designing artificial neuron circuits, but that the MLP regression provides the highest accuracy and is much simpler to fit compared to the compact model. The targeted technology exhibits non-ideal behavior such as variable threshold voltage and hysteresis. Using the MLP regression model, the effect of such variability on the performance of an artificial neuron circuit is compared. It is found that these effects alter the neuron firing rate and change the time spent in the on/off states but do not change the basic operation.

1. Introduction

Recent research on emerging flexible electronics has shown that robust transistors and digital circuits can be realized with a low-cost and a greener manufacturing profile, but at the expense of device performance.[1,2] For many applications, such as continuous health monitoring devices[3] or environmental sensors, the end products target wide and relatively short-term use. The question of sustainability and cost can therefore be more important than state-of-the art performance. In this paper, we focus on low-power organic devices, which are most promising for wearable devices that integrate with the human body.

In conventional silicon research and development, mature physical compact models are able to capture the device behavior essential for designing circuits.[4] While there is a large literature on modeling Organic Thin Film Transistors (OTFTs),[5] it is a challenge is to develop a single model that can capture the wide variety of physical effects possible in the different technologies used for device fabrication. Most notably, the interfaces resulting from different techniques cause trap states, which can vary widely in their characteristics. In addition, modeling is complicated by changes due to light, moisture, and history that strongly influence OTFT behavior. These difficulties are especially important for circuit design at lower operating voltages (≤5 V) and typically models and circuits focus on higher voltage regimes.

Fitting devices to a physical compact model for a given technology has been widely investigated, but the process of determining the fitting parameters is often time-consuming. In this paper, we first compare three different OTFT modeling techniques: a physical compact model, an empirical Look Up Table (LUT), and an empirical model based on the Artificial Intelligence (AI) algorithm known as a multi-layer perceptron (MLP). The compact model is based on a quasi-static charge model,[6] which solves Poisson's equation self-consistently using an appropriate density of states and an electron/hole transport model based on variable range hopping. The fitting procedure takes into account both transfer (drain current, I_d, versus gate-source voltage, V_{gs}) and

L. E. Calvet, S. El-Nakouzi, Z. Li, Y. Kim, I. M. Bhattacharyya, Y. Bonnassieux
LPICM
CNRS, Ecole Polytechnique, Institute Polytechnique de Paris
Palaiseau 91128, France
E-mail: laurie.calvet@cnrs.fr

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Z. Li
Université Paris-Saclay
Gif-sur-Yvette 91190, France

A. Zaibi, B. Iñiguez
DEERA
University Rovira i Virgili
Tarragona 43007, Spain

P. Golec
Advanced Technology Institute
School of Computer Science and Electronic Engineering
University of Surrey
Guildford GU2 7XH, UK

L. Kadura
CEA-LITEN
Université Grenoble-Alpes
Grenoble 38000, France

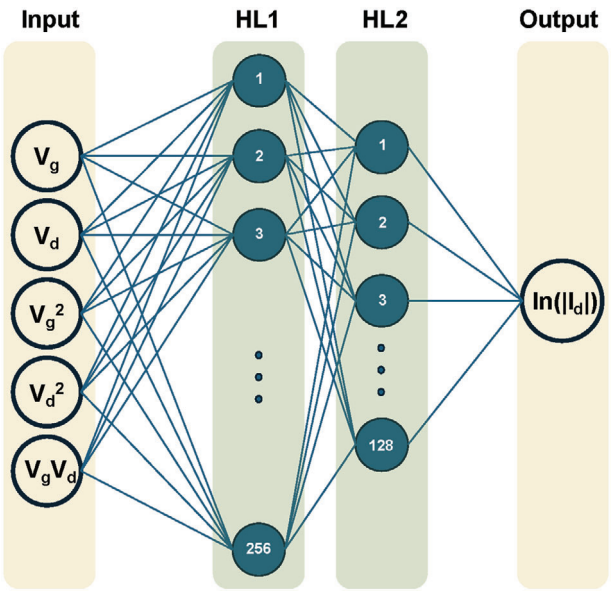

Figure 1. The MLP regression architecture. The input layer consists of a vector derived from polynomial terms of V_{gs}, V_{ds}. The first hidden layer (HL1) is connected to the input by a matrix that fully connects the 5 weights with each 256 elements. The second hidden layer (HL2) consists of 128 elements and is also fully connected to HL1. Finally, the output is a single value fully connected to HL2.

output (I_d versus drain-source voltage, V_{ds}) curves. It involves ≈20 fitting parameters. Nevertheless, the fitting procedure can be long, making it very difficult to explore how changes in transistor variability within a technology can impact circuits.

One possibility to overcome this difficulty is the use of empirical compact models. In this case, a large data set of OTFT transfer and output curves that includes the range of the targeted circuit operation is obtained. The simplest empirical model is to use a LUT, where empirical data is placed in a table and a linear interpolation between the data points enables a model of its behavior for circuit design. LUTs are easily implemented in standard design tools such as Cadence Spectre. Nevertheless, this simplistic model is not accurate in the presence of hysteretic effects, where the *Id* at fixed *Vds* and fixed *Vgs* can be different depending on the history of the device. To overcome the difficulties related to the hysteresis observed in this dataset, the LUT used here is based on the transfer (*Id* versus *Vgs*) curves.

Here we propose a model based on a well-known AI algorithm, the MLP regression, illustrated in **Figure 1**. In this method, the input consists of the particular function of V_{ds} and V_{gs} and the output is ln (I_d). To develop the parameters for the input vector, we first considered a linear regression to a typical diffusion transport in the sub-threshold regime.[5] It is given by:

$$I_{sub} = -I_0 \exp\left(\frac{Ln\,(10)}{S}\,(V_{GS} - V_0)\right)\left[1 - exp\left(\frac{qV_{DS}}{k_B T}\right)\right] \quad (1)$$

where I_0 is the prefactor normally dependent on the width, length, and mobility of the transistor, S is the subthreshold factor, V_{th} is the threshold voltage, k_B is Boltzmann's constant and T is temperature. Noting that the logarithm of this curve is linear, we first considered a linear regression of I_d versus ln(V_{gs}) characteristics. The data, as shown in **Figure 2**, is clearly non-linear. We therefore extended the linear fit to a polynomial of V_{ds} and V_{gs}. The results improved, but to obtain an even better result an MLP regression was used. Based on this initial analysis, we tested an input vector for the best accuracy using a polynomial of variables V_{ds} and V_{gs}. The best results were found for V_g, V_g^2, V_d, V_d^2, and V_gV_d, as depicted in Figure 1. The input layer is connected to two hidden layers, also each in the form of a vector, and finally a single output ln (I_d). Connections between the layers are matrices, whose values, known as weights, are optimized during the training process. During training, input values corresponding to known current output for all of the empirical data are used. The values include the ≈14000 current points from both transfer and output characteristics. A stochastic gradient descent method optimizes the weights. The final architecture with the trained values is encoded into VerilogA format that can then be read by a circuit simulator such as Cadence Spectre. Further details are provided in the Experimental section.

Our simulations focus on the low voltage regime of device operation because our goal is to simulate spiking neuron circuits. Such low-power circuits take advantage of the exponential dependence of the sub-threshold region.[7,8] A strong impetus for developing neuromorphic hardware in flexible materials lies in the observation that biological brains perform very well at very low speeds, low energies and with hardware prone to variability as in these technologies. While the first realization of neuromorphic hardware in organic technologies was considered more than a decade ago,[9,10] this field has recently blossomed following several very important breakthroughs.[11] The majority of recent demonstrations[12–15] have used organic electrochemical transistors (OECTs).[16] The gate action of these devices is driven by ionic doping/dedoping of the semiconductor, which has a direct analogy with the coupled ion/electron transport in biological neurons. OECTs offer facile integration with biological systems and provide an unparalleled opportunity in health sensors.[13,15,17,18] While circuits have been realized in OECTs,[19,20] the main drawback is the slow speed of the devices, at best 10–100s of milliseconds, typically due to the thickness of the electrolyte gate.

Although OTFT technologies are comparatively well-established compared to OECTs, neuromorphic functionalities lag in comparison.[21–25] Previous demonstrations have shown spiking organic neurons in the μWs and in the ≈Hz range. OTFTs, however, can operate up to MHz frequencies.[26] One target of these studies was the Axon-Hillock (AH) circuit, first proposed by Mead in 1989.[7] Biologically the AH neuron is where the membrane potentials from the synaptic inputs are summed before being transmitted to the axon. In circuit form, it is relatively simple to realize and therefore amenable to OTFT implementations. It is a self-resetting circuit where spikes are generated above a threshold that is dependent on the geometry of the transistors and their properties. Two demonstrations of organic neuron circuits have been reported.[25,27] In one case a complementary OTFT technology used relatively low cost (vacuum evaporation) and simple processing, however very large differences in the n- and p- transistor characteristics limited its performance.[27] In the second case, pOTFTs were fabricated using solution processing, and discrete resistors and capacitors

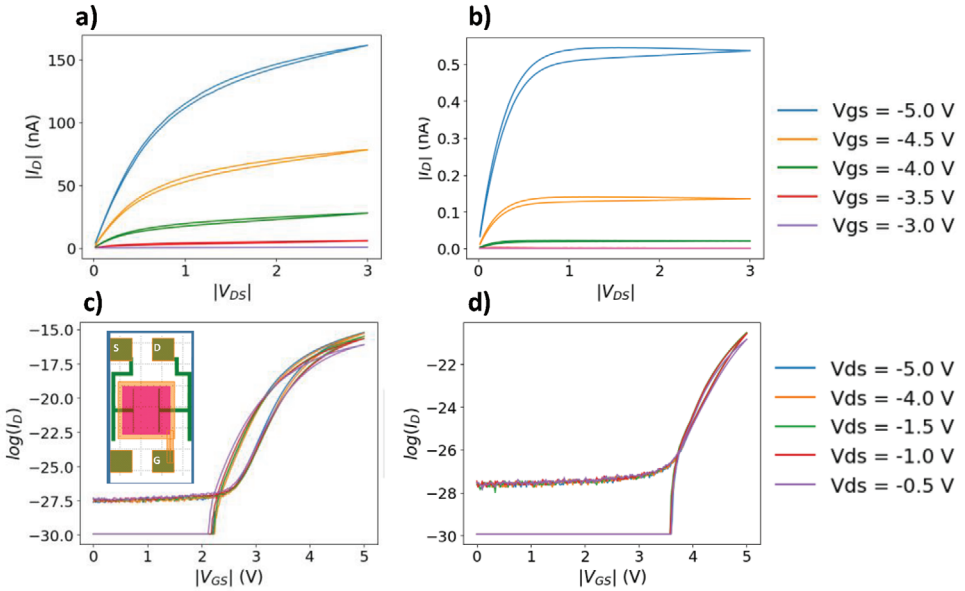

Figure 2. I_d versus V_{ds} for the a) 10 µm channel length, and b) 400 µm channel length transistors from die 1. All transistors have a 1 mm width. I_d versus V_g characteristics for the c) 10 µm channel length and d) 400 µm channel length transistors. The inset depicts a device schematic. The fabrication methods of these devices are discussed in the Experimental section. Data for all 10 die for these two devices are provided in Figures S1–S4 (Supporting Information).

were used. Spiking was observed when voltage spikes were applied to the input. Improving performance by modeling is one potential way to advance this line of research. While the first paper developed a novel modeling methodology, parameter extraction was shown to be quite time-consuming. The second paper used a simple MOSFET model with parameters corresponding to the organic devices. Little discussion was provided as to the reproducibility of these circuits.

To surmount these difficulties, we explore empirical modeling of OTFTs for circuit design. We focus on devices fabricated in a well-developed organic technology using flexible Thin Organic large-area electronics (TOLAE) processes. Current research has already demonstrated many capabilities of such technologies including analog front-end[28] multiplexing circuits,[29] and Serial-Parallel conversion.[30] To date, the majority of applications in organic hardware have focused on using conventional digital approaches, but there are much fewer explorations of analog and low-power operation.

2. Results

2.1. Characterization and Modeling of the OTFTs

We performed a detailed characterization at low voltages of a large set of p-type OTFTs consisting of 10 different size transistors repeated on 10 different die. Figure 2 shows a sample of the characteristics of two devices with 10 and 400 µm channel lengths with 1 mm widths. We observe an important hysteresis that complicates the modeling effort, where the voltage from zero toward greater negative voltages (forward sweep) has a lower absolute value of current compared to the sweep toward zero (reverse sweep). For the smaller length transistors, the hysteresis is larger but recovers more quickly as can be seen when comparing the hysteresis response of the I_d versus V_{ds} and I_d versus V_{gs} in the two transistor sizes. Hysteresis is likely due to charge trapping. Holes are trapped at defects in the forward sweep and then remain trapped causing a shift in the threshold voltage in the return sweep. The dependence of the hysteresis and the recovery time on the channel length suggests that the traps are dependent on the field due to the V_{ds}, possibly due to traps at the source/drain to channel interface. A complete understanding would require detailed measurements of the time dependence, which is outside the scope of this paper.

We next consider the variability in the technology. Figures S1–S4 (Supporting Information) show the large variability for the two different device sizes for 10 transistors that are nominally the same size but are located on different die. Note that the size of the hysteresis varies from device to device. **Figure 3** compares the transfer and output characteristics for ten 10 µm channel length devices on different dies for a fixed bias. We observe important changes in the threshold voltage and turn-on V_{on}, defined as the value of V_g at which the transistor current exceeds the background (in this case, when $|I_d| > 1 \times 10^{-13}$ A).

This large variability is an important concern when designing circuits. First, it prevents the use of a simple scaling rule to describe the technology, which is typically used in physical compact models. Instead, a model is needed for every device size and in fact for every device. A second concern is the impact of the large variation in V_{on} on the circuits.

The dataset describing the devices is done using DC measurements and the lack of time-dependent measurements precludes the realization of an AC model. This situation is not unique. It may be encountered when trying to use data provided by a foundry to develop a model for a device that is operating in a transport regime that is not mainstream, for instance at low voltage values. In this case, time-dependent measurements may not

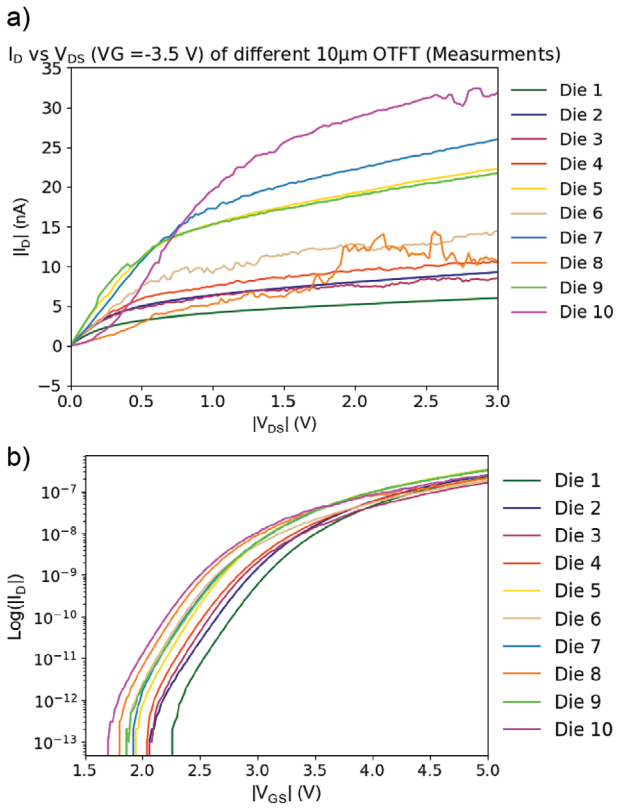

Figure 3. a) I_d versus V_{ds} at $V_g = -3.5$ V and b) I_d versus V_g at $V_{ds} = -3.5$ V measurements for all die for the 10 µm channel length devices.

be possible to obtain and yet circuit designs need to be realized based on the DC transistor measurements. For this reason, we develop a methodology that can be used to understand the impact of the observed hysteresis during circuit design based on the partial information provided by a forward and reverse sweep.

Our modeling analysis begins with **Figure 4**, which compares the fitting of the three models using the data from the forward sweep (from 0 toward negative bias). There is significantly more data for the transfer characteristics and as a result, the MLP regression and LUT (based only on the I_d–V_{gs} curves) fit better than the compact model. However, for the I_d–V_{ds}, where less data is available, the compact model is able to better capture the transport because it is based on physical reasoning. The time to simulate the transistor characteristics in cadence is ≈0.5 s and does not substantially differ from the three models, indicating that it is negligible compared to starting the Cadence software.

Table 1 compares the root mean square error (RMSE) (definition given in the Experimental section) for the three different models. The LUT model has zero RMSE for the transfer characteristics because the values of the transfer curves were used in the look-up table. The MLP has a significantly smaller RMSE compared to the compact model for the transfer curves. For the output characteristics, we see that the compact model always performs better. This is because there were much fewer points for the output characteristics and the compact model is able to work with fewer points in general. The MLP is able to capture the output characteristics better than the LUT for a large portion of the range. In Table S1 (Supporting Information) we report other error measures such as the relative root mean square error and the relative mean square error, which are necessary to compare the technique with other methods. We find that the compact model performs as well as previously reported compact models.[24] The MLP regression performs much better than the compact model for the transfer curves and very similarly to the output curves.

The fitting score (R^2, explained in the Experimental section) for all the MLP regressions (10 die each with 10 different device sizes) are reported in Figure S5 (Supporting Information). The model for Die 1, 10 µm channel length has an excellent accuracy >0.999, which can be seen as a typical value. The worst model has an overall accuracy of 0.98. We have chosen to use a fixed architecture for the MLP regression for the devices, as depicted in Figure 1. In future work, accuracies could be improved by optimizing the architecture for each individual device.

2.2. Inverter Circuit

Figure 5 shows simulations for an inverter consisting of a single transistor and a single resistor, which are important elements in the neuron circuit. A resistor-loaded inverter has several disadvantages compared to a CMOS inverter, mainly continuous power dissipation and a slower switching speed. However, here it allows us to reduce the variability of the circuit design by only using a single active transistor. An improved design could have a two-resistor, one-transistor design where one resistor serves as the pull-up load and the other is used in series with the transistor to limit the power consumption. Figure 5b compares the simulation results for the three models. Despite the differences in fitting from the previous section and also the different origins of the models, they result in very similar characteristics. Because the inverter only uses a single transistor, the simulation times for this circuit were also ≈0.5 s and it was hard to detect timing differences in the three models.

Next, we consider the role of the hysteresis and variability using the MLP regression model. **Figure 6** plots the variation of the inverter using the forward and reverse fits for all die from Figure 3. The inverter transition in the forward direction varies over 0.6 V and in the reverse direction by over 0.9 V. Note that there is a definite trend for V_{on} to shift to lower values as the die number increases. The hysteresis, shown in Figure 6d is relatively uniform ≈0 .5 V. These changes may be due to changes in the homogeneity of the materials. Variations may also be due to small misalignments that are propagated in the sheet. Given these large variations, it is not clear how the AH circuit will function in the presence of such effects.

2.3. Simulations of Spiking Neuron Circuits

We consider a pOTFT implementation of the AH circuit based on the work of Danneville et al,[31] depicted in **Figure 7a**. The implementation is very appealing for organic electronics because all transistors are the same dimensions allowing us to avoid the shift to higher $|V_g|$ that is experienced by V_{on} in larger channel-length devices. When no excitatory current is applied ($I_{exc} = 0$ A),

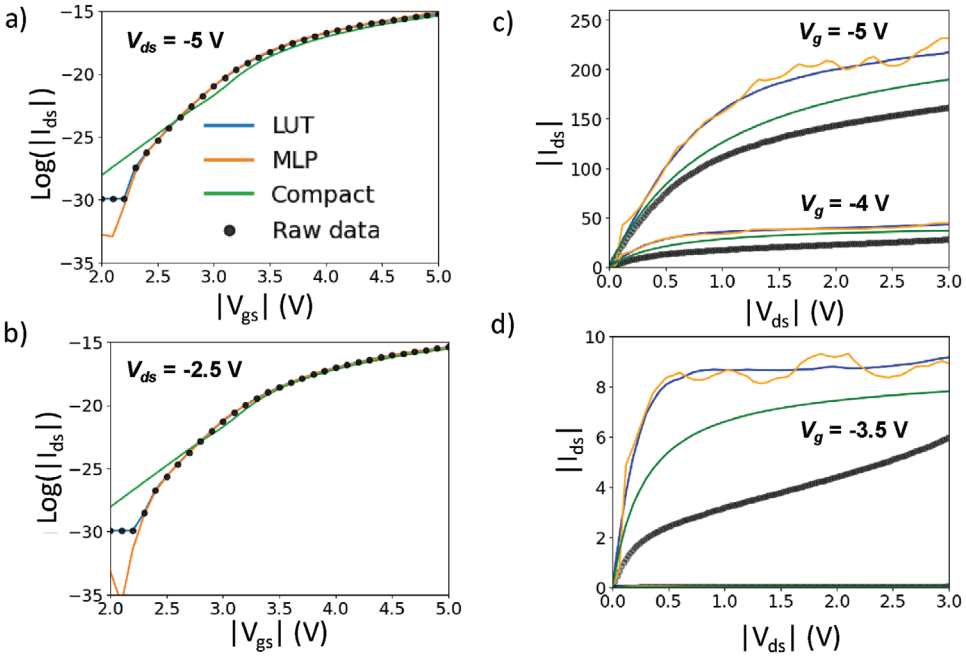

Figure 4. Transfer a), b) and output c), d) characteristics and fits for each of the three models for 10 and 400 µm channel lengths respectively. The fits used the forward sweep. Die 1 was used for both device sizes.

both the output voltage V_{out} and the membrane voltage V_{mem} are 0 V. The capacitor C_f is not charged and the output of the first inverter is high. As I_{exc} is increased, C_f begins to charge, causing V_{mem} to increase. When V_{mem} reaches the threshold voltage to switch the inverters, both inverters change state and V_{out} rises toward the supply voltage VDD. A positive feedback loop is then established through C_f, which raises V_{mem} to a value higher than V_{out}. When the reset current I_r through the transistor TR_r significantly exceeds I_{exc}, V_{mem} starts to decrease until it reaches the switching voltage of the first inverter. Consequently, the inverters switch again, bringing V_{out} back to 0 V, and the cycle repeats.

This circuit is different from the conventional AH circuit[7] which includes a capacitor C_{mem} connected from V_{mem} to ground. Here it is replaced by the parasitic input capacitance, which in this case corresponds to the capacitance of TR1, estimated to be ≈0.4 pF. This value is included by setting the parasitic capacitance in the simulation parameters.

We first consider the ideal case where all the transistors use the same forward sweep model. The goal is to benchmark the MLP regression against the compact model and then it will be used more broadly to understand the expected circuit behavior. Figure 7b,c show a comparison of the AH circuits realized using the three models. As with the inverter, we find that the AH simulations do not exhibit significant variations for the different models. We do observe a slightly smaller firing rate for the compact model, which is due to smaller resistances at larger voltages

Table 1. Root mean square error of the 3 different models for a sampling of transfer and output curves for the 10 µm channel length device from die 1.

	$I_d V_{gs}$				$I_d V_{ds}$		
	Compact	MLP Regression	LUT		Compact	MLP Regression	LUT
|V_{ds}| [V]	Root mean square error [nA]	Root mean square error [nA]	Root mean square error [nA]	|Vg_s|	Root mean square error [nA]	Root mean square error [nA]	Root mean square error [nA]
5	11.40	7.03	0	5	135	162	160
4.5	9.91	2.78	0	4.5	71.5	84.6	85.8
4	8.73	1.67	0	4	28.7	32.9	34.3
3.5	7.68	2.3	0	3.5	6.76	7.75	8.52
3	7.40	1.88	0	3	0.654	0.727	1
2.5	7.50	1.34	0	2.5	0.0858	0.0859	0.0859
2	7.96	9.67	0	2	0.0987	0.0972	0.105
2.5	8.72	1.22	0	2.5	0.108	0.108	0.108
1	9.04	1.72	0	1	0.132	0.132	0.132

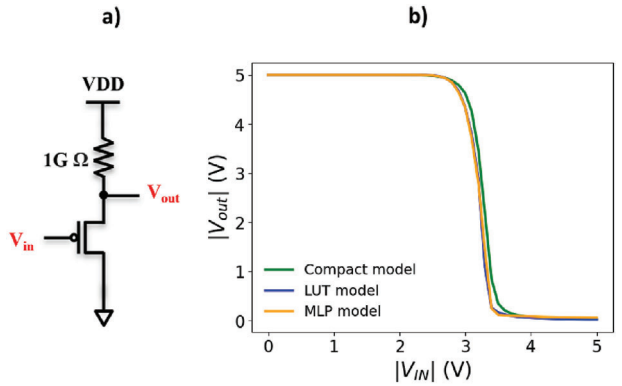

Figure 5. a) The inverter circuit used in the simulations. VDD is set to −5 V. b) Simulations comparing the results of the 3 models using Cadence Spectre based on the transistor from die 1 with the 10 µm channel length device and using the fit to the forward sweep.

(see Figure 4). Unlike the inverter and the transistor characteristics, we find an important difference in the simulation time of the three models, reported in **Table 2**, with the MLP model taking ≈2 order magnitudes longer. For small circuits like the AH circuit, the time is still not a barrier. The power consumption in the simulated circuits is found to be < 5 nW and the firing rate is ≈100 Hz. Having established that the MLP is representative of the transistors and provides similar results to the established compact models, we now consider simulations that explore the impact of the hysteresis and variability on the AH circuit.

We used the MLP model to fit other transistor sizes to test whether the model functions for other sizes and to test how the firing rate varies. **Table 3** reports results on the firing rate for different size devices. Increasing transistor sizes while keeping the resistors the same alters the switching voltage of the inverters and also changes the charging time. Due to larger resistance with device length, the firing rate decreases.

Figure 8 considers how the variation of V_{on} impacts the firing rate by comparing the AH circuits using different 10 µm transistors and the forward sweep MLP model. Note that the transistors in the circuit (TR_1, TR_2, TR_f) use the same model. The firing rate varies from 80 Hz in Die 1 to 100 Hz in Die 10. This shift corresponds to the shift in the transition in the inverter and also the shift of V_{on} of the discrete transistors. A second observation is that the faster spiking neurons have a smaller voltage difference between the ON/OFF states. The main impact of an increase in $|V_{on}|$ is to decrease the firing rate. Note that this effect is similar to what was observed with increasing channel length where devices also exhibit an increase in $|V_{on}|$ and slower firing rates.

We next consider how the variability of the transistors (TR_1, TR_2, TR_f) in the AH circuit impacts its output. **Table 4** lists the dies and the distance between the $|V_{on}|$ of the different transistors. **Figure 9** shows the resulting voltages of the circuits. We find that when TR_1 uses the model for Die 1, which has the largest $|V_{on}|$, the firing rate is reduced (curve 1 and curve 2 compared to curve 3). However, the firing rate is increased by a smaller $|V_{on}|$

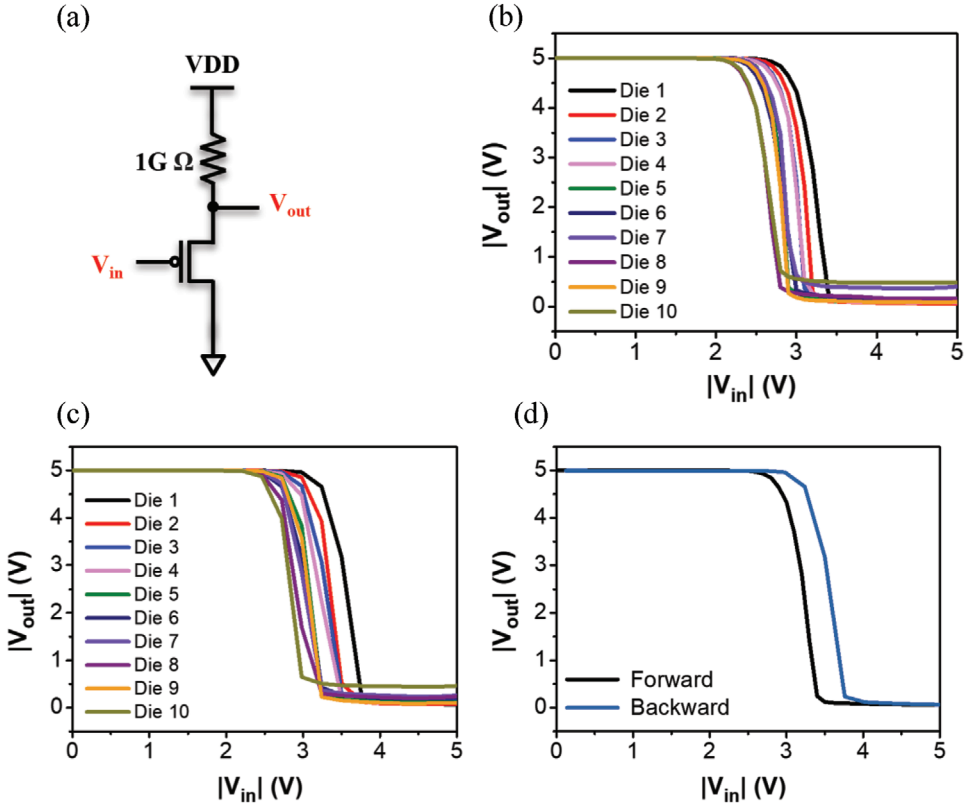

Figure 6. Variability and hysteresis of the inverter circuit a). The forward sweep b) and reverse sweep c) are shown for all ten 10 µm transistors. d) The impact of the hysteresis on inverter characteristics is plotted for die 1. V_{DD} was set at −5 V.

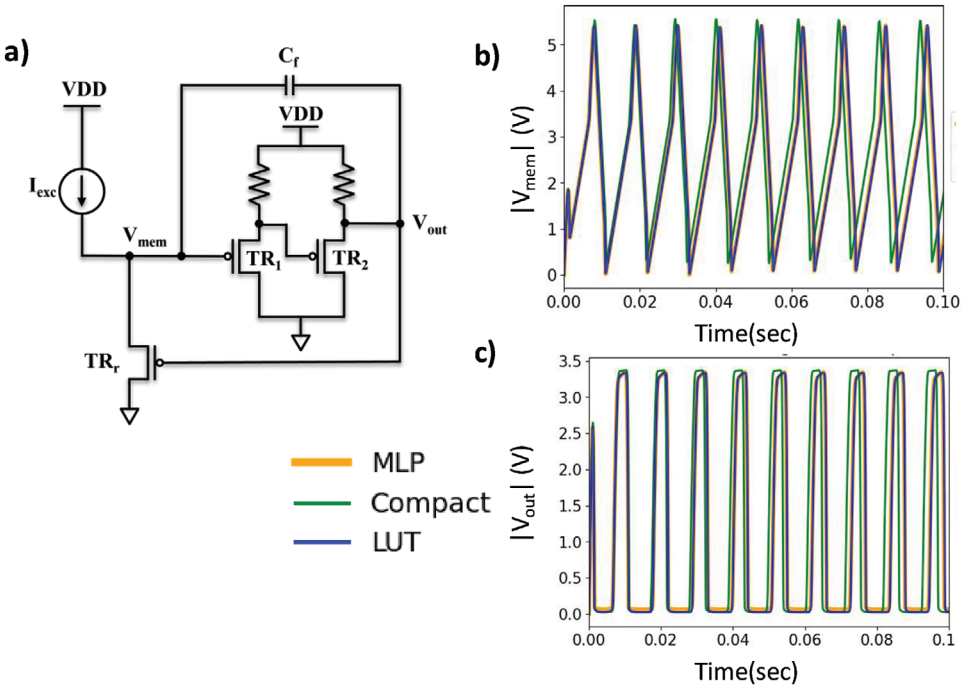

Figure 7. a) The OTFT AH circuit. VDD is set to −5 V, the resistances are 1 GΩ, C_f = 1 pF, I_{exc} is −1 nA. The V_{mem} b) and V_{out} c) from simulations using the three models for the 10 µm transistor from die 1. All transistors use the same model based on forward sweep.

in TR_2. This is true for not only the firing rate in curves 1 and 2 in Figure 9, but also for curves 1 and 2 compared to the firing rates in Figure 8. We also observe that the faster firing rate in curve No. 3 (red) has a higher low state, as for the faster firing rates in Figure 8. Overall the impact of the variability in TR_1, TR_2, TR_r is very similar to the variability when the same model is used for all three transistors: it causes a change in the spike rate and can impact the difference between high and low spikes but the circuit is still seen to be functional.

Finally, we use the forward and reverse models to consider the impact of the hysteresis on the AH circuit. To do this we introduce two circuit models in **Table 5** that account for the sweep states during circuit operation. The sweep states of the three transistors within the circuit differ depending on whether $|V_{out}|$ is high or low. When $|V_{out}|$ is low, $|V_{mem}|$ increases linearly until it reaches the switching threshold of TR_1. At this point, TR_1 switches from low to high and TR_2 switches from high to low. This causes $|V_{out}|$ to reach VDD and switch TR_r from low to high. Therefore, in the spike-up state TR_1 and TR_r undergo a forward sweep (circuit model 1), while TR_2 undergoes a reverse sweep. Conversely, during the spike-down state, TR_1 and TR_r follow a reverse sweep, while TR_2 undergoes a forward sweep (circuit model 2).

Figure 10 shows the simulations for the two models. In a circuit with hysteresis, we expect the $|V_{out}|$ and $|V_{mem}|$ to follow the red lines during the spike up state, and the green line in the spike down state. As a result, although there is a difference in the firing dynamics between the circuit models 1 and 2, the overall shape of the $|V_{out}|$ spiking remains unchanged. This suggests that while hysteresis of OTFTs can introduce variability in the firing dynamics, it does not significantly alter the fundamental waveform characteristics of the output voltage. The resulting firing rate will remain unchanged but the relative time spent in high and low states will be different. We also see that if the hysteresis increases with sweep time, which is typically the case, the time spent in the high/low spike states will also change. Such behavior has important implications for the reliability of signal

Table 2. Simulation times in Cadence Spectre for the AH circuit simulated for 100 ms for the three models. The simulation time for the inverter and the transistor characteristics was 0.5 s for all models.

	Compact	LUT	MLP
Simulation time (s) (1 I_d–V_{gs})	0.5	2	30

Table 3. Approximate firing rate when the AH circuit in Figure 7a is used for other transistor sizes. These simulations were done using die 1 for each size, the same transistor model in the forward sweep for TR_1, TR_2, and TRF, and a single transistor size. I_{exc} = −1 nA, the resistors were 1 GΩ, and C_f = 1 pF.

L	Spikes/sec
5 µm	128
10 µm	87
20 µm	91
100 µm	11
200 µm	9

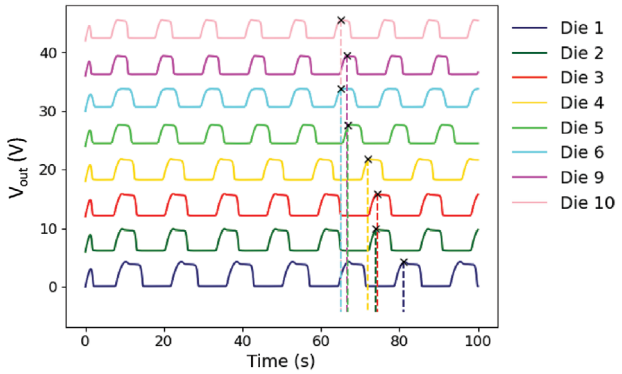

Figure 8. a) Comparison of V_{out} of the AH circuit using the MLP regression empirical model for transistors on different die that are 10 µm length. Each curve is offset by 5 V for clarity. The lines depict the change in the placement of the 7th or 8th spike in order to depict the variability due to changes in transistor characteristics.

transmission, as it suggests that the AH circuit can maintain consistent spiking patterns despite some hysteresis.

3. Discussion

3.1. Comparison of Modeling

The three models considered here have advantages in different instances. The compact model, which is based on physics, allows us to understand the mechanisms at work in the devices. It has much fewer parameters (~20) compared to the LUT (~12000 parameters) and the MLP (34176). The parameters of the compact model are physically relevant, such as the series resistance and the disorder parameter, which is used to model the variable range hopping in the semiconductor channel. The parameters can therefore be used to compare different technologies, and different batches of devices in order to optimize the fabrication process. For a more mature technology the compact models can provide scalability and fitting the model to each size is not necessary.

The LUT should in theory be the most realistic model given sufficient data. However, because of the discrepancy between the I_d versus V_{gs} and the I_d versus V_{ds} characteristics; only the I_d versus V_{gs} curves are used. At low values of V_{gs} and V_{ds}, we expect the LUT to become the least accurate. It is important to note that the LUT is dependent on the linear interpolation between successive points. This requires a very fine grid of points in the more complex regions. The MLP, however, is able to account for nonlinearities between data points and is therefore more capable of advanced interpolations.

Table 4. Transistors and their ΔV_{on} (distance between the V_{on} of the two transistors indicated) are used in Figure 9.

Curve no.	Transistor die TR_1, TR_2, TR_r	ΔV_{ON} TR_1, TR_2	ΔV_{ON} TR_1, TR_r	ΔV_{ON} TR_2, TR_r
1	1, 2, 5	< 0.10 V	0.50 V	0.40 V
2	1, 10, 5	0.75 V	0.50 V	0.25 V
3	4, 6, 5	0.20 V	0.10 V	< 0.10 V

The main disadvantage of the MLP is that it is essentially a black box regression and the large number of parameters do not have a physical meaning. Nevertheless, it is very easy to employ using standard Python coding. For designing small circuits and trying to quickly understand how variability will impact circuits, it is a very time-efficient method, especially if an individual model is needed for each device. It is able to capture some of the discrepancies due to the hysteresis and in some cases the fitting of the compact model may not be sufficient to obtain a working model.

We next consider the various metrics of the error. In Table 1 we considered the root mean square error (RMSE) to compare the three models. The unit of this error is the same as the data, making comparisons between it and the data very intuitive. The RMSE of the LUT in the transfer regime is of course zero. In the output characteristics, the LUT has a higher error in a large part of the regime compared to the other two models, indicating it is important to include the output characteristics in the modeling.

We compared our relative MSE with the only known accuracy for modeling that we were able to find in published data,[24] which refers to a single transfer curve. The errors in the transfer curves for the compact model were the same (≈0.02) as this previous work, but the MSE for all the data of the MLP is much lower (0.001). We believe that the more appropriate measure of comparison is the relative root mean square error (RRMSE) metric because, in the presence of larger errors, the real MSE can be very large. Here we find that the RRMSE is ≈0.1 in the output characteristics, which means that they can reproduce the data within 10%, which is a very good model considering the changes in the transport. For this reason, we believe that the MLP is an excellent model that can be used to explore the variability of devices when needed.

3.2. Generalization of the MLP Regression Technique

We have explored how an MLP regression can be used to model pOTFT transistors in the low-voltage regime. A natural question is whether this can be generalized to the entire regime. Similar research has explored the use of an MLP regression in a silicon nanowire reconfigurable (r)FET.[32] They showed that it was convenient to use two MLPs, one for the sub-threshold and another for the saturation regime, and to stitch the two together using a mathematical function. This type of generalization could be an interesting solution for modeling complementary OTFT circuits where the n-type devices may be in the on state and the p-type devices in the sub-threshold. In this case, the model sizes should be chosen very carefully to ensure that simulation times are not excessive. From our simulations, however, we do not expect that simulation times will be problematic because they are still quite small.

4. Conclusion

This paper considered modeling OTFTs in the low voltage regime using a physical compact model, a LUT, and an empirical model based on a MLP regression. The three models can be employed together to provide more insights into the device's physics or independently to facilitate the modeling of a technology when all

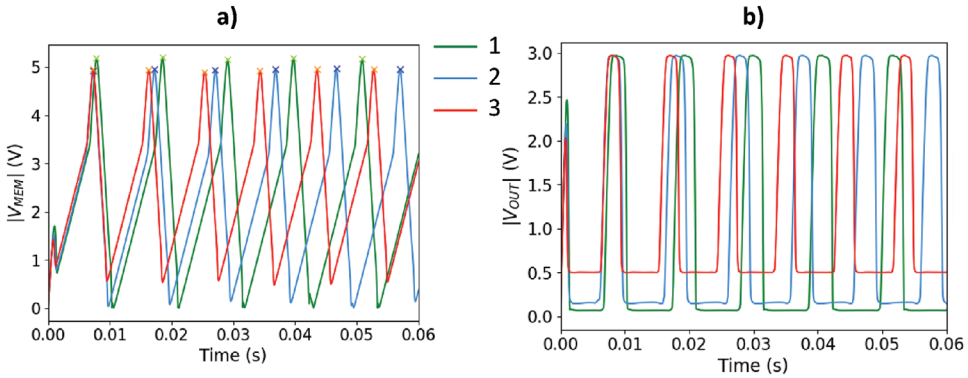

Figure 9. V_{mem} and V_{out} characteristics of the AH circuit when using different transistor models for TR_1, TR_2, and TR_r. in the circuit.

Table 5. Two circuit models are used to understand how the hysteresis might impact the AH circuit.

TR	Circuit Model 1	Circuit Model 2
TR_1	Forward model	Backward model
TR_2	Backward model	Forward model
TR_r	Forward model	Backward model

the effects cannot be described using the physical model. Our simulations indicate that organic biomimetic neurons using p-type OTFT technology are possible with firing rates >100 Hz and power consumption <5 nW for 10-micron channel-length devices. We found that the main impact of variability in $|V_{on}|$ results in variations in the firing rate. Hysteresis was found to change the relative time that V_{out} spends in the high and low states. The AH neuron circuit is found to be very compatible with OTFT technologies but care should be taken to choose neuromorphic applications that are robust against the variability of firing rates and its profile of high and low states. With improved design and a minimization of the parasitic capacitances, firing rates at least an order of magnitude larger should be possible than those previously reported. Finally, we believe that the variability in the device characteristics can be used advantageously to realize neuromorphic devices because, in such systems, stochasticity is often a source of improvement via effects such as stochastic resonance.

5. Experimental Section

The p-type OTFT transistors were realized using gravure printing on the Pilot Line at CEA-LITEN.[33] The source/drain contacts are 30 nm Au and are patterned by photolithography. It is subsequently coated with a self-assembled monolayer to improve the adhesion with the organic semiconductor. A 50 nm organic semiconductor (SP500 Lisicon polymer from Merck) with a mobility of 2 cm^2 Vs^{-1} is gravure printed. A 946 nm gate dielectric (Merck D320) of 2.2 is gravure printed. Interconnections between the source/drain and gate are achieved using vias. Finally, a conductive ink of PEDOT:PSS is screen-printed on top of the stack to establish the gate electrode. Initial layouts of the AH circuit are 4 mm × 4 mm in size and include two discrete 1GΩ resistors and 1 discrete pF capacitor.

Measurements were done at ambient conditions in the dark. The semi-automatic prober is connected to a semiconductor parameter analyzer (HP B1500A) with triaxial cables. I_d–V_{ds} characteristics were measured in steps of −20 mV, sweeping both up to negative V_{ds} and back for V_{gs} with a uniform step size between 0 to −5 V of −0.5 V every 1s. Forward and reverse I_d–V_{gs} characteristics were measured in steps of −20 mV with a V_{ds} step size

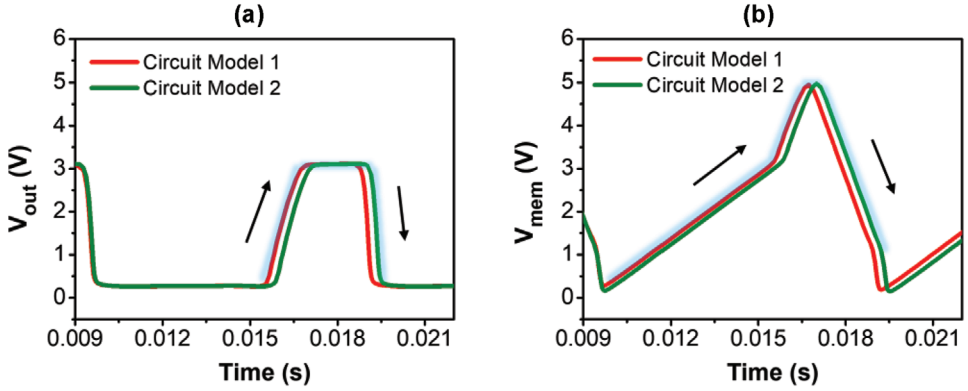

Figure 10. Simulation of the V_{out} a) and V_{mem} b) for the AH circuit using the two circuit models in Table 2. Simulations were done using Die 7 of the 10 µm channel length devices. V_{DD} was −5 V, I_{exc} was −1 nA and C_f was 1 pF.

of −0.1 V. This resulted in ≈14 000 data points that enabled us to use an MLP model.

Ten devices for transistors lengths of 5, 10, 20, 40, 60, 80,100, 200, 400, and 600 µm with 1000 µm width were measured in the sub-threshold region (V_{gs}, V_{ds} > −5 V). Typical mobilities were 1.8–2.0 $cm^2\ V^{-1}\ sec^{-1}$ with $V_t = -5V$.

The compact model is based on a DC and quasi-static charge model,[6] which solves Poisson's equation self-consistently using an appropriate density of states and an electron/hole transport model based on variable range hopping. Parameters for the model are fit to the measured devices for each size and each die. The model cannot take into account directly the hysteresis. For this reason, the fits were done either using the sweep toward more negative voltages or its return. The hysteresis impeded us from using the physical compact model for larger device sizes because the currents in the $I_d - V_{ds}$ characteristics were often not consistent with the currents in the $I_d - V_g$ characteristics at the same biasing conditions. The devices reported in the figures are those where the model fits well. The total number of parameters used in the compact model is ≈20. The parameter extraction and fitting were done in Matlab and the extracted parameters and final model were put into a VerilogA code for simulations in Cadence Spectre.

In order to surmount the difficulties of the compact model, a MLP regression was developed to fit the data for each device. Simulations were performed using cadence and the machine learning library Sklearn.[34] Simulations were done using a single CPU of Intel XEON microprocessor @ 3.2 GHz running on a Dell PowerEdge server. The training of an individual model requires ≈2 min. A ReLu activation function and standard Adam were used for an optimized gradient descent.[35] All 56 $I_d - V_g$ and all $I_d - V_{ds}$ curves were included in the fit, resulting in a fit with ≈14 000 experimental data points. It was assumed that the device characteristics could be described in terms of polynomials of V_{gs}, V_{ds}. To determine the best network architecture, a systematic exploration of the polynomial inputs (up to 4th order) was done, a number of hidden layers (up to 4), and several neurons (up to 1056). The optimal network, with a typical accuracy score of 0.9996, was found using five parameters: V_g, V_g^2, V_d, V_d^2, and $V_g V_d$, two hidden layers (256 for the first and 128 for the second). To benchmark the regression, the score was used to determine the R^2 (Figure S5, Supporting Information). It is defined as:

$$R^2 = 1 - \frac{\sum_i^N \left(x_i - p_i\right)^2}{\sum_i^N \left(\overline{x_i - \overline{x_i}}\right)^2} \tag{2}$$

After training in Python, the model was made compatible with VerilogA, where matrix multiplications are not available. In Cadence, $C_{min} = 1 \times 10^{-13}$ F was set to account for the parasitic capacitance.

To benchmark the different models, two measures were used: the root mean square error and 1- relative mean square error. These are defined as:

$$root\ mean\ square\ error = RMSE = \sqrt{\frac{1}{N}\sum_i^N \left(x_i - p_i\right)^2} \tag{3}$$

$$relative\ mean\ square\ error = Rel\ MSE = \sum_i^N \frac{\left(x_i - p_i\right)^2}{\sum_i^N x_i^2} \tag{4}$$

$$relative\ root\ mean\ square\ error = RRMSE = \sqrt{\frac{\frac{1}{N}\sum_i^N \left(x_i - p_i\right)^2}{\sum_i^N x_i^2}} \tag{5}$$

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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artificial neuron circuits, circuit simulations, device modelling, organic electronics

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