FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 37, Nº 4, December 2024, pp. 609 – 617
https://doi.org/10.2298/FUEE2404609B

Original scientific paper

DETERMING THE CHARACTERISTICS OF THE LOCALIZED DENSITY OF STATES DISTRIBUTION PRESENT IN MOS2 2D FETS*

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Abstract. *The behaviour of MoS_2 FETs, with channel lengths greater than the mean free path of carriers was analysed. Electrical behaviour of experimental devices with channel lengths of 5 μm and 0.1 μm was studied, modelled and simulated, concluding that the predominant transport mechanism observed was hopping. The presence of a localized density of states (DOS) distribution in the semiconductor layer, causing the behaviour observed in these devices, was studied and determined by both modelling and simulation.*

Key words: *DOS in MoS_2 2D FET, mobility of MoS_2 2D FETs, MoS_2 2D FET modelling and simulation*

1. INTRODUCTION

In the last years, the possibility of using 2D semiconductors to continue further scaling of metal-oxide-semiconductor field effect transistors has attracted much attention. The use of silicon multi-gate devices seems to be reaching their limit, reason why other approaches are being analysed [1].

To overcome the limitations in further scaling of 3D semiconductor devices, related to the so-called short channel effects, the use of two-dimensional (2D) semiconductor materials seems an interesting approach [2,3].

Received September 20, 2024; revised October 22, 2024 and October 27, 2024; accepted October 29, 2024
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The electrostatic characteristics of FET devices described by Poisson equation can be analysed using a parameter called characteristic channel length defined as [4]:

$$\lambda = \sqrt{(x_s x_i)\frac{k_s}{k_i}} \tag{1}$$

where k_s and k_i, the relative dielectric constants and x_s and x_i the thickness of the semiconductor layer and insulator, respectively.

From the above equation, the characteristic channel length can be reduced by reducing the thickness of the semiconductor or of the insulator layer, or by increasing the relative dielectric constant of the insulator layer.

However, with the reduction of the bulk semiconductor layer x_s, the electrostatic control of carriers in the channel is reduced, since for example, surface dispersion increases, affecting mobility.

In two-dimensional (2D) semiconductor materials, however, it is possible to confine electrons within a very thin channel formed by one or few monoatomic layers. It has been reported that carriers can be uniformly controlled by the gate voltage [2,3]. In principle, if the channel length of the transistor is less than the mean free path of carriers, in the order of or less than 20 nm, ballistic transport mechanism can be observed [5].

Several 2D semiconductor materials are being studied, among which dichalkogenide transition metals (TMDs) with a bandgap above 1 eV, as MoS_2, are among the most studied 2D materials for FET devices [3].

At present, 2D FETs with quite good characteristics, for channel lengths greater than the mean free path of carrier, have been already reported, [6-9]. At the same time, several compact models have also been developed for or applied to them [10-14]. It is interesting to notice that several of these models have satisfactorily considered a potential dependence of mobility with gate voltage, which is usually related to the presence of variable range hopping (VRH) as the main transport mechanism, even though the 2D semiconductor layer used, is expected to be crystalline.

The hopping mechanism of charge transport describes the movement of charge in the material by hopping between localized states present in the material. This transport mechanism is typical of disordered materials, as polycrystalline or amorphous. However, it can also be observed in crystalline materials, when a sufficiently high density of defects is present.

A detailed analysis of the characteristics of mono and several layers films, deposited using different deposition methods, have revealed the presence of defects, that can explain the presence of the hopping mechanism observed.

For example, Ghatak et al., studied the low-temperature electrical transport in monolayer, bilayer, and tri-layer MoS_2 transistors exfoliated onto Si/SiO_2 substrates, determining that, at room temperature, electrons are localized in the ultrathin MoS_2 layer and display VRH. They relate this behaviour to charges trapped at the MoS_2_SiO_2 interface, producing random potential fluctuations [15].

In [16], authors observed grains and grain boundaries in what they called highly crystalline monolayer molybdenum disulfide, arriving to the conclusion, that they were the reason of localized DOS, present in the layers deposited by CVD.

In [17-20], authors studied the presence of different defects, in TMD deposited layers, and their effects on the electrical properties of the devices, some of which can be represented as localized states within the bandgap.

In this work, we analyse the electrical behaviour of MoS_2 monolayer FETs, using simulation and modelling techniques. After reproducing their electrical characteristics, we determined and discussed the presence of a density of state (DOS) distribution in the gap of the semiconductor layer that can explain the observed behaviour. The characteristics of the localized DOS are reported.

2. MOS2 2D FETS: STRUCTURE AND MODELLING

For the analysis we used two bottom gate 2D FETs, T1 with a channel length of 5 µm and T2 with 100 nm. The fabrication process started with a highly dopped P-type silicon wafer used as the substrate, on top of which an Al_2O_3 layer with 22 nm equivalent oxide thickness (EOT) was deposited. A MoS_2 monolayer, of around 1 nm thick, previously deposited by Metal Organic Epitaxial Chemical Vapor Deposition, (MOCVD) on top of a sapphire substrate, was exfoliated and deposited on top of the Al_2O_3 layer. Lithography was used to define the area of the semiconductor layer. Afterwards Mo was deposited for the drain and source contacts, followed by another lithographic process to define the channel length and drain and source regions [6]. The structure cross section is shown in Fig. 1. Main structure parameters are shown in Table 1.

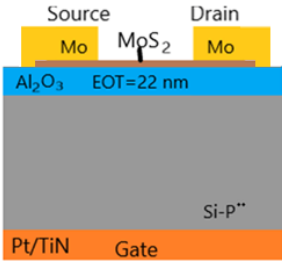


Fig. 1 Cross section of the device

Table 1 Structure parameters

Structure parameters		T1	T2
2D material		MoS_2	MoS_2
Deposition method		MOCVD	MOCVD
Exfoliation		Yes	Yes
Channel width [µm]	W	5	5
Channel length [µm]	L	5	0.1
2D layer thickness [nm]	ts	0.9	0.9
EOT [nm]		22	22
Structure		Bottom gate	Bottom gate

For analysing the transport mechanism observed in the 2D transistors, we modelled their electrical characteristics using the following expressions in Unified Model and Extraction Method (UMEM) developed for Thin Film Transistors (TFTs) [21]. The field effect mobility μ_{FE} is calculated as:

$$\mu_{FE} = \mu_0 \frac{n_{free}}{n_{localized}} \sim (V_G - V_T)^{\gamma_a} = \mu_0 \left(\frac{V_G - V_T}{V_{aa}}\right)^{\gamma_a} = \mu_1 (V_G - V_T)^{\gamma_a} \quad (2)$$

where μ_0 is an adjustment parameter; n_{free} is the free charge concentration; $n_{localized}$ is the localized charge concentration, and $n_{free} < n_{localized}$. After mathematical arrangements, mobility can be expressed as a power-law function, where V_T is the threshold voltage and γ_a is the field effect mobility parameter. Both are extracted as indicated in [21]. μ_1 is the field-effect mobility when V_G-V_T= *1,* expressed as*:*

$$\mu_1 = \left(\frac{\mu_0}{V_{aa}{}^{\gamma a}}\right) \tag{3}$$

where μ_o=1 cm^2/Vs and V_{aa} is a model parameter to be extracted calculating from the experimental data $I_{DS}^{\left(\frac{1}{1+\gamma a}\right)}$ vs.$(V_{GS} - V_T)$, its slope *Sl* and *K=(W*C$_i$)/L*:

$$V_{aa} = \frac{K V_{DS}}{Sl^{1+\gamma a}}^{1/\gamma a} \tag{4}$$

The final current model for above threshold, in linear and saturation regions of operation, for above-mentioned TFT transistors is similar as for MOSFETs [21]:

$$I_D = \frac{W}{L} C_i \mu_{FE} \frac{(V_G - V_T)}{1 + R\frac{W}{L} C_i \mu_{FE}(V_G - V_T)} \frac{V_D(1+\lambda V_D)}{\left[1+\left(\frac{V_D}{\alpha_S (V_G - V_T)}\right)^m\right]^{\frac{1}{m}}} \tag{5}$$

This mobility model is related to the carrier conduction mechanism of the above mentioned TFTs, where γ_a has been related to specific characteristics of the semiconductor material and has been satisfactorily used for different kinds of TFTs [21-24].

In the above threshold regime, the model parameters are: μ_0 or μ_1, V_T, γ_a, V_{aa}, R, α_S, m and λ. R is the total series resistance, α_S is the saturation parameter, while m and λ are the knee of the output characteristic and the channel length modulation parameter, respectively. They are extracted as indicated in [21].

In the subthreshold region near V_T, the current is described by an empirical expression neglecting R, where $V_T \rightarrow V_{FB}$; $\gamma_a \rightarrow \gamma_b$ and $V_{aa} \rightarrow V_{bb}$.

$$I_{Dsub} = \frac{W}{L} C_i \mu_0 \left(\frac{V_G - V_{FB}}{V_{bb}}\right)^{\gamma b} (V_G - V_{FB}) V_D \tag{6}$$

In the deep subthreshold regime, when the current transport mechanism is diffusion and the current has an exponential dependence, the following equation is used:

$$I_{Ddeepsub} = I_{Dsub}(V_G = V_{1A}) exp\left[\frac{2.3}{S}(V_G - V_{1A})\right] \tag{7}$$

The model parameters in the sub-threshold regime are *S, V_{FB}, V_{bb}, γ_b.* Current continuity between deep sub-threshold and sub-threshold is obtained by using the *tanh* function and parameters V_{1A}, V_1, Q_1 and between subthreshold and above threshold using parameters V_2 and Q_2, considering (5), (6) and (7).

The total subthreshold current is equal to:

$$I_{Dsubtotal} = \left|I_{Ddeepsub}\right|\left[1 - tanh[(V_{FB} + V_1)Q_1]\right] + \left|I_{Ddeep}\right|\left[1 - tanh[(V_{FB} + V_1)Q_1]\right] \tag{8}$$

The total current expression is:

$$I_{DS} = \left[(Io + I_{Dsubtotal}) \frac{\left[1 - tanh[(V_{GS} - (V_T + V_2))Q_2]\right]}{2} + |I_D| \frac{\left[1 + tanh[(V_{GS} - (V_T + V_2))Q_2]\right]}{2}\right] \tag{9}$$

where V_{1A}, V_1, Q_1, V_2 *and* Q_2 are adjusting parameters.

The obtained values for these adjusting parameters for T1 are: V_{1A}=-0.14 V; V_1=-0.14 V; $Q1$=20; V_2=1.13 V and $Q2$=3.76. For T2, V_{1A}=-0.13 V; V_1=-0.17 V; $Q1$=14.5; V_2=1.13 V and $Q2$=27.

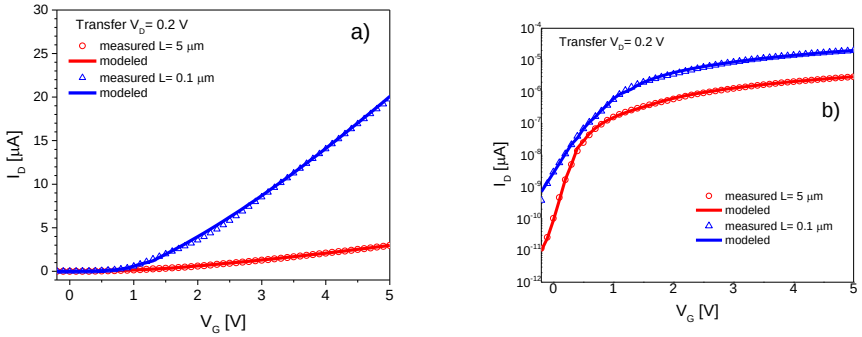


Fig. 2 Modelled and measured linear transfer characteristic for T1 and T2 in: a) linear scale and b) semilog scale

Fig. 2 and Fig. 3 show the measured and modelled linear transfer and output characteristics for devices T1 and T2, where an excellent agreement is observed. For device T1, the value of the field effect mobility at 5 V was μ_{FE}= 21.1 cm^2/Vs and for T2 μ_{FE}= 3 cm^2/Vs.

From the modelled transfer characteristics, using the procedure in [24], a characteristic energy for the localized DOS distribution in the semiconductor layer of 0.0036 eV was obtained for T1 and 0.034 eV for T2, corresponding to a characteristic energy E_{tA} of 0.034 eV. The values of field effect mobility, total resistance and DOS characteristic energy obtained from modelling, will be further used in simulations as initial values.

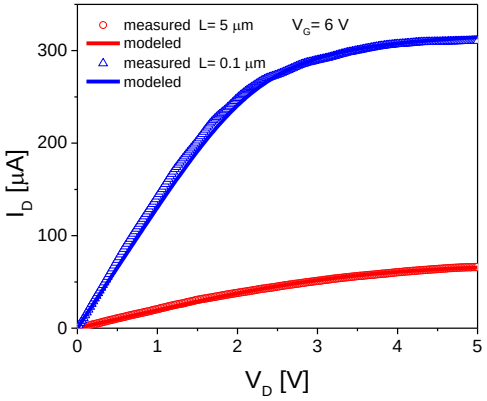


Fig. 3 Measured and modelled output characteristic for devices T1 and T2, at VG= 6 V

3. Simulation of 2D Transistors

To further analyse the presence and characteristics of a localized DOS, in the bandgap of the MoS_2 layer, we used simulation tools, in this case simulator Atlas from Silvaco [25]. The cross section of the simulated devices is shown in Fig. 4a. The thickness of the semiconductor layer was 0.9 nm. Fig. 4b shows a zoom of the semiconductor layer in Fig. 3a, where the channel length L of device T1 was 5 μm and of T2 was 100 nm. Other structure device parameters are shown in Table 1.

The semiconductor band gap, E_G, for the MoS_2 monolayer was 1.86 eV, which is a typical value for the direct bandgap present in monolayers, [26]. The charge concentration considered was $1.5x10^{18}$ cm^{-3} [27], N_C and N_V are the density of states at the bottom of the conduction band and top of the valence band, respectively and Q_f is the interface charge density, see Table 2.

Table 2 Material parameters used in simulations

E_G [eV] [26]	N_B [cm^3] [27]	Affinity [eV] [30]	k_s [28]	Metal WF [eV]	N_c [cm^{-3}]	N_v [cm^{-3}]	Q_f [cm^{-2}]	Si P^{++} N_B [cm^{-3}]
1.84	$1.5x10^{18}$	4.2	2.8	4.3	$5x10^{18}$	$5x10^{18}$	$3x10^{11}$	$1x10^{18}$

Table 3 Values of the FET devices obtained from simulations: mobility μ_{FE}, series resistance R, density of acceptor tail states N_{tA} and characteristic energy of acceptor tail states, E_{tA}.

	μ_{FE} [cm^2/Vs]	R [Ω]	N_{tA} [cm^{-3}]	E_{tA} [eV]
Device T1	23	250	$4.5x10^{20}$	0.034
Device T2	5.5	250	$4.5x10^{20}$	0.034

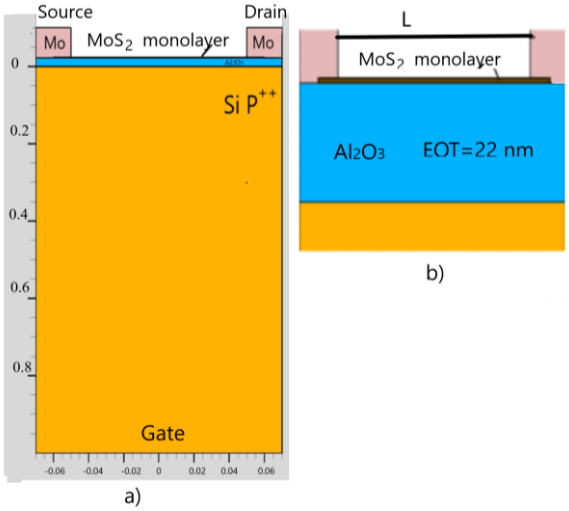
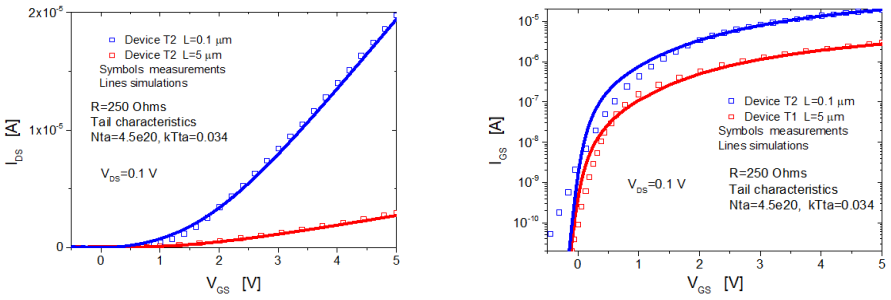


Fig. 4 a) Cross section of the T2 simulated structure, with scales in μm; b) Zoom of the semiconductor layer, where L is the channel length of each of the analysed devices

Table 3 shows the values of the field effect mobility μ_{FE}, interface fixed charge, total resistance, density of tail acceptors in the bandgap DOS distribution and its characteristic energy with which good adjustment between simulated and measured I-V curves in the above threshold region is obtained, see Fig. 5a and b. In the subthreshold region, especially in deep subthreshold, the adjustment was not as good, which can be due to external effects that become more important as the channel length is reduced and were not considered in the simulations. The value for the density of tail acceptors in the bandgap DOS obtained is equal to N_{tA}=4.5x10^{20} cm^{-3}.



a) b)

Fig. 5 Measured and simulated linear transfer curves for devices T1 and T2: a) in linear scale and b) in semilog scale

4. Analysis of Results

Using modelling and simulation, it was confirmed the presence of a localized tail distribution of states (DOS) in the semiconductor gap, which can be associated with defects present in the MoS_2 monolayer. The presence of defects in these monolayers or several layer films, has been observed previously by physical characterization of the layers and has been associated to the presence of grains, grain boundaries, and several types of defects, even though the deposition method should provide high quality crystalline layers [15-20].

It was also possible to determine the characteristic temperature and density of the tail acceptor states present in these devices, which has not been reported before. For the devices with different channel lengths, the simulations were done, using the same material parameters shown in Table 2. As can be seen from Table 3, the characteristics of the tail DOS for devices T1 and T2 are the same, as was to be expected since both types of devices were fabricated at the same time, varying only the channel length in the layout.

It is important to remark that in the analysed devices, the main transport mechanism observed is VRH hopping, in which we agree with previous reports.

5. Conclusions

The agreement between measured and simulated transfer characteristics in the analysed devices can be obtained, only if the simulation is done including the presence of a localized DOS distribution in the semiconductor MoS_2 layer. This result indicates that the deposited MoS_2 monolayers in these FETs present defects giving rise to a predominant hopping transport mechanism. Previously, transfer and output characteristics for both devices, T1

and T2, were modelled with good agreement between modelled and experimental curves, using an expression for mobility that depends as a potential law with the gate voltage. This dependence is normally observed in amorphous or polycrystalline devices, where the hopping transport mechanism is predominant. From the modelled curves, the characteristic energy of the DOS was determined. The two methods confirmed that a localized DOS distribution in the gap of the semiconductor layer is present, which gives rise to a hopping transport mechanism. These traps can be due to defects that have been preciously observed by other authors, in the semiconductor layer, despite the deposition method used.

Acknowledgement: *This work was funded by the European Union under contract 101099555 (BAYFLEX) and the Ministry of Science of Spain under contracts TED2021-130307B-I00 and PRX21/00726.*

REFERENCES

[1] C. Claeys, E. Simoen, "Challenges for Advanced End of the Roadmap, Beyond Si and Beyond CMOS Technologies", In Proceedings of the 32nd Symposium on Microelectronics Technology and Devices (SBMicro), 28 August 2017 - 01 September 2017, Fortaleza, Brazil.

[2] M. Chhowalla, D. Jena and H. Zhang, "Two-dimensional semiconductors for transistors", *Nature Reviews Materials,* vol. 16052, 2016.

[3] T. Wei, Z. Han, X. Zhong, Q. Xiao, T. Liu, D. Xiang, "Two dimensional semiconducting, materials for ultimately scaled transistors", *Science,* vol. 25, no. 105160, Oct. 21, 2022.

[4] J.P. Collinge, "Multiple-gae SOI MOSFETs," *Solid-State Electron.* vol. 48, pp. 897–905, 2004.

[5] G. Iannaccone, F. Bonaccorso, L. Colombo and G. Fiori, "Quantum engineering of transistors based on 2D materials heterostructures", *Nature Nanotechnology*, vol. 13, pp. 183–191, 2018.

[6] A. Sebastian, R. Pendurthi, T.H. Choudhury, J.M. Redwing and S. Das, "Benchmarking monolayer MoS2 and WS2 field-effect transistors", *Nature Communications,* vol. 12, no. 693, pp. 1–12, 2021.

[7] A.J. Yang, K. Huang, C. Ye, W. Wen, R. Zhu, R. Zhu, J. Xu, T. Yu, P. Gao, Q. Xiong and X. R. Wang, "Van der Waals integration of high-κ perovskite oxides and two-dimensional semiconductors", *Nature Electronics,* vol. 5, pp. 233–240, April 2022.

[8] X. Jing, Y. Illarionov, E. Yalon, P. Zhou, T. Grasser, Y. Shi and M. Lanza, "Engineering Field Effect Transistors with 2D semiconductor Channels: status and Prospects", *Adv. Funct. Mater.,* vol. 1901971, 2019.

[9] Y.Y. Illarionov, K.K.H. Smithe, M. Waltl, T. Knobloch, E. Pop and T. Grasser, "Improved Hysteresis and Reliability of MoS2 Transistors with High-Quality CVD Growth and Al_2O_3 Encapsulation", *IEEE Electron Device Letters*, vol. 38, no. 12, 2017.

[10] W. Cao, J. Kang, W. Liu and K. Banerjee, "A Compact Current–Voltage Model for 2D Semiconductor Based Field-Effect Transistors Considering Interface Traps, Mobility Degradation, and Inefficient Doping Effect", *IEEE Trans. Electron Devices,* vol. ED-61, no. 12, Dec. 2014.

[11] S.V. Suryavanshi and E. Pop, "S2DS: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities", *J. Appl. Phys.,* vol. 120, no. 224503, 2016.

[12] Y. Taur, J. Wu and J. Min, "A Short-Channel I–V Model for 2-D MOSFETs", *IEEE Trans. Electron Devices*, vol 63, no. 6, June 2016.

[13] C. Yadav, P. Rastogi, T. Zimmer and Y.S. Chauhan, "Charge-Based Modelling of Transition Metal Dichalcogenide Transistors Including Ambipolar, Trapping, and Negative Capacitance Effect", *IEEE Trans Electron Devices,* vol. ED-65, no. 10, Oct 2018.

[14] A. Mounir, B. Iñiguez, F. Lime, A. Kloes, T. Knobloch, and T. Grasser, "Unified Charge Control Model for Back-Gated 2D Field Effect Transistors", *IEEE Trans Electron Devices,* vol. ED-71 no. 1, pp. 884–889, 2024.

[15] S. Ghatak, A. Nath Pal, A. Ghosh, "The Nature of Electronic States in Atomically Thin MoS2 Field-Effect Transistors", 2011, *ACS Nano 2011*, vol. 5, pp. 2075–2081.

[16] A.M. van der Zande, P.Y. Huang, D.A. Chenet, T.C. Berkelbach, Y. You, G-H Lee, T.F. Heinz, D.R. Reichman, D.A. Muller, J.C. Hone, "Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide", *Nature Materials J*., vol. 12, 2013.

[17] K. Ko, M. Jang, J. Kwon, "Native point defects in 2D transition metal dichalcogenides: A perspective bridging intrinsic physical properties and device applications", *J. Appl. Phys.*, vol. 135, p. 100901, 2024.

[18] J.Y. Kim, Ł. Gelczuk, M.P. Polak, *et al.* "Experimental and theoretical studies of native deep-level defects in transition metal dichalcogenides", *npj 2D Mater Appl*, vol. 6, no. 1, p. 75, 2022.
[19] N. Fang, S. Toyoda, T. Taniguchi, K. Watanabe, K. Nagashio, "Full Energy Spectra of Interface State Densities for n- and p-type MoS_2 Field-Effect Transistors", *Adv. Funct. Mater*., p. 1904465, pp. 1–9, 2019.
[20] K. Kunstmann, T.B. Wendumu, G. Seifert, "Localized defect states in MoS_2 monolayers: Electronic and optical properties", *Phys. Status Solidi B*, pp. 1–8, 2016.
[21] A. Cerdeira, M. Estrada, R. García, A. Ortiz-Conde and F.J. García Sánchez, "New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions", *Solid-State Electronics*, vol. 45, no. 7, pp. 1077–1080, 2001.
[22] M. Estrada, A. Cerdeira, J. Puigdollers, L. Reséndiz, J. Pallares, L.F. Marsal, C. Voz and B. Iñiguez, "Accurate modelling and parameter extraction method for organic TFTs", *Solid-State Electronics,* vol. 49, pp. 1009–1016, 2005.
[23] M. Estrada, I. Mejía, A. Cerdeira, J. Pallares, L.F. Marsal and B. Iñiguez, "Mobility model for compact device modelling of OTFTs made with different materials", *Solid-State Electronics*, vol. 52, p. 787, 2008.
[24] Y. Hernandez-Barrios, A. Cerdeira, M. Estrada and B. Iñiguez, "An insight to mobility parameters for AOSTFTs, when the effect of both, localized and free carriers, must be considered to describe the device behaviour", *Solid-State Electronics,* vol. 149, pp. 33–37, 2018.
[25] Silvaco Inc.
[26] C-P. Lu, G. Li, J. Mao, L-M. Wang, E.Y. Andrei, Bandgap, "Mid-Gap States, and Gating Effects in MoS2", *Nano Lett*., vol. 14, pp. 4628−4633, 2014.
[27] K-C. Wang, T.K. Stanev, D. Valencia, J. Charles, A. Henning, V.K. Sangwan, A. Lahiri, D. Mejia, P. Sarangapani, M. Povolotskyi, A. Afzalian, J. Maasse G. Klimeck, M.C. Hersam, L.J. Lauhon, N.P. Stern, and T. Kubis, "Control of interlayer physics in 2H transition metal dichalcogenides", *Journal of Applied Physics*, vol. 122, 2017.
[28] M. Belete, S. Kataria, U. Koch, M. Kruth, C. Engelhard, J. Mayer, O. Engistro, M.C. Lemme, "Dielectric Properties and Ion Transport in Layered MoS2 Grown by Vapor-Phase Sulfurization for Potential Applications in Nanoelectronics", *ACS Appl. Nano Mater*. 2018, no. 1, pp. 6197−6204.
[29] M.D. Siao, W.C. Shen2, R.S. Chen, Z.W. Chang, M.C. Shih, Y.P. Chiu, C.-M. Cheng, "Two-dimensional electronic transport and surface electron accumulation in MoS2", *Nature Communications,* vol. 9, p. 1442, 2018.
[30] A. Nourbakhsh, A. Zubair, R.N. Sajjad, A. Tavakkoli K.G., W. Chen, S. Fang, X. Ling, J. Kong, M.S. Dresselhaus, E. Kaxiras, K.K. Berggren, D. Antoniadis and T. Palacios, "MoS2 Field-Effect Transistor with Sub-10 nm Channel Length", *Nano Lett.*, vol. 16, pp. 7798−7806, 2016.