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Discontinuous PWM Operation of a Single-Phase PV Generator with Low-Voltage Energy Storage

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***Abstract*—Using energy storage in grid-connected photovoltaic (PV) generators is an efficient solution to deliver regulated power to the grid despite fluctuations in solar irradiance. The paper analyses a single-phase grid-connected PV generators with energy storage, where the energy storage has a low voltage, namely without too many series-connected storing cells. The PV generator consists of three subsystems connected by a common dc-link capacitor: a PV unit, an energy storage unit, and an inverter. Furthermore, in the proposed solution, the inverter does not switch for a significant portion of the grid period, resulting in lower switching losses. The single-phase inverter discontinuous operation implies the need of an appropriate control strategy in the boost dc-dc converter of the energy storage unit. The proposed control employs an augmented state model that accounts for resonant variables. The proposed PV solution with low-voltage energy storage, including its control, is validated in a 350-VA experimental prototype to verify the novel approach.**

I. Introduction

Grid-connected photovoltaic (PV) generators can incorporate energy storage (ES) capability to address solar irradiance fluctuations and ensure grid code adherence [1]–[5]. A typical PV power plant with ES, as shown in Fig. 1, may consist of three subsystems connected by a common dc-link capacitor: (i) a PV unit that contains a solar array and a dc-dc converter acting as a maximum power point tracking (MPPT) regulator, (ii) an ES unit that contains a battery or a supercapacitor and a dc-dc converter working as an ES processor, and (iii) an inverter for grid power delivery. Optimizing the design of each of these subsystems and the overall system, specifically minimizing losses and cost, is of paramount importance for further expanding the deployment of PV generators. ES can be built with batteries, supercapacitors, or a combination of the two. Supercapacitors have advantages over batteries in PV applications because they have a higher power density and a lower equivalent series resistance. However, using a supercapacitor as an ES typically requires a low terminal voltage (less than 48 V). Even if an ES is built with batteries, due to charge equalization concerns, low-voltage battery design strategies could have advantatges in reliabiliy and safety terms [6], [7]. Low-voltage ES requires the ES processor to be a step-up topology.

In grid-connected PV applications without ES, the inverter's efficiency can be increased by using discontinuous modulation (DPWM) or unfolding strategies [8]–[14]. In both strategies, the inverter stops switching for a significant fraction of the grid period. In the context of DPWM, the inverter switches at a high frequency for a portion of the grid period, and the dc-link voltage is not intentionally shaped [10], [11], [13]. On the other hand, in the unfolding strategy, the inverter switches at the grid frequency, and the dc-link voltage is deliberately shaped to a rectified sinusoidal form. The shaping of the dc-link capacitor voltage is carried out by injecting a specific capacitor current with the purpose of synthesising a desired dc-link capacitor voltage waveform [8], [9], [12], [14]. DPWM is usually reported for three-phase inverters, as in [13], whereas it is in an incipient stage for single-phase multilevel inverters [10], [11]. Concerning unfolding strategy methods, [8], [9], [12] report buck-boost unfolding strategies for grid-connected single-phase PV inverters without ES, whereas [14] proposes an unfolding strategy for a three-phase motor drive application. Specifically, reference [8] uses an interleaved-boost stage cascaded with a buck stage to shape the dc-link capacitor voltage at the input of the H-bridge inverter, reference [9] uses a Cuk converter, and [12] uses a twisted buck-boost approach.

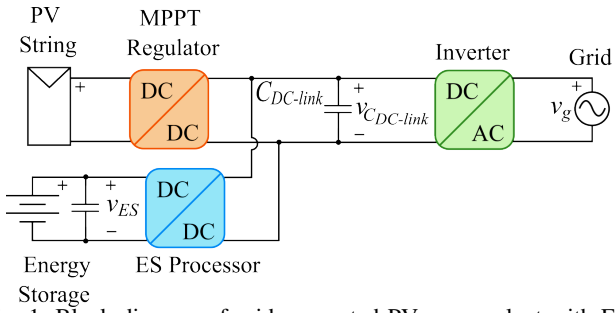

Fig. 1: Block diagram of grid-connected PV power plant with ES.

The approach proposed in this paper applies to single-phase PV generators with ES, combining the properties of DPWM and unfolding strategies. Specifically, it can be framed as DPWM, because the inverter does not switch for a significant portion of the grid period. Furthermore, it shares with unfolding strategies the feature that the dc-link capacitor voltage is shaped to a quasi-rectified sinusoidal shape. Fig. 2 depicts the voltage waveforms for the proposed voltage shaping approach and a conventional sinusoidal PWM (SPWM) in which the dc-link voltage is set to a constant value greater than the grid voltage peak. Note that the voltage variables in Fig. 2 are shown in Fig. 1, with the exception of v_{inv}, which is an

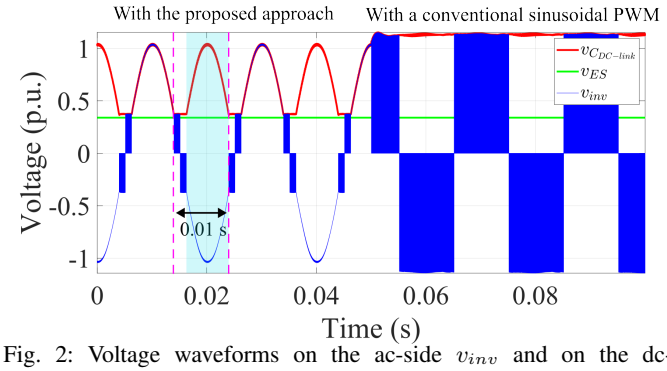

Fig. 2: Voltage waveforms on the ac-side v_{inv} and on the dc-side $v_{C_{DC-link}}$ of the H-bridge inverter, when operating the grid-connected PV generator with the proposed voltage shaping approach and with a conventional sinusoidal PWM approach.

internal voltage between the inverter H-bridge and the inverter filtering inductor. A cyan shaded area indicates the fraction of time within half a grid period in which the H-bridge inverter does not switch. The proposed strategy is inspired by [15]. Nevertheless, in [15], the ES processor is based on a buck converter, which is not suitable when the ES operates at low voltage.

The main contribution of the paper is the introduction of a novel approach for shaping the dc-link capacitor voltage as a quasi-rectified sinusoidal form for PV generators with low-voltage ES units, as well as the corresponding resonant-action-based control. In addition, the following can be considered secondary contributions:

- To enhance the tracking of the rapidly changing quasi-rectified sinusoidal voltage reference, the proposed PV generator with low-voltage ES uses a very small dc-link capacitor, which could result in a smaller inverter size.
- The proposed approach has been experimentally validated for a single H-bridge inverter, and it can be easily extended to a cascaded H-bridge topology.
- An analytical model of switching losses in the H-bridge inverter is developed and experimentally verified to assess the benefits of the proposed voltage shaping strategy.

The subsequent sections of the paper are organized as follows. In Section II, the system model of the grid-connected PV power plant with low-voltage ES in Fig. 1 is described, detailing each of the three subsystems. Section III presents the scaled-down experimental setup and some results. Finally, Section IV summarizes and concludes the paper's main ideas.

II. State-Space Model of the Grid-Connected PV Power Plant with Low-Voltage ES

Based on the system shown in Fig. 1, this section reviews the state-space model of each subsystem, i.e., the inverter, the PV unit, and the ES unit, in three subsections. Also, the proposed control laws are described.

A. Inverter Model

The inverter interfaces the dc-link capacitor voltage, $v_{C_{DC-link}}$, and the grid voltage, v_g, as shown in Fig. 3. The

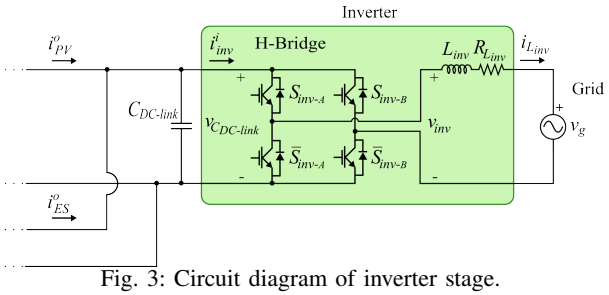

Fig. 3: Circuit diagram of inverter stage.

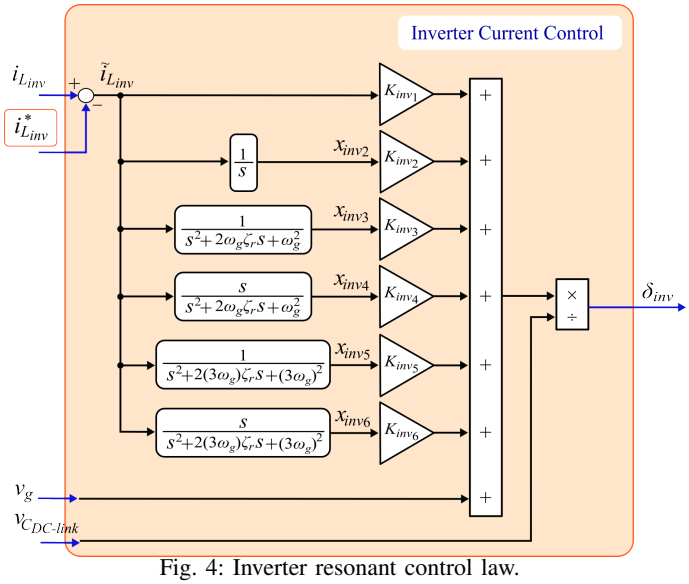

Fig. 4: Inverter resonant control law.

single-phase inverter consists of four power semiconductors, which form an H-bridge structure with three possible output voltage levels, and a filtering inductor, L_{inv}. The set of discontinuous switching positions $\{0, \ ,1\}$ of each top switch, S_{inv-A}, S_{inv-B}, are controlled by a fixed carrier frequency pulsewidth modulation (PWM) circuit, and complementarity between top and bottom switches is assumed. The locally-averaged dynamics of the inverter output current, $i_{L_{inv}}$, according to Fig. 3, is given by:

$$L_{inv}\dot{i}_{L_{inv}} = -R_{L_{inv}} i_{L_{inv}} + \delta_{inv} v_{C_{DC-link}} - v_g, \qquad (1)$$

where $C_{DC-link}$ is the dc-link capacitance and $R_{L_{inv}}$ models the series resistance of the filtering inductor, L_{inv}. Note that, as shown in Fig. 3, the locally-averaged H-bridge input current, i^i_{inv}, corresponds to $i^i_{inv} = \delta_{inv} i_{L_{inv}}$, where the modulation signal δ_{inv} represents the locally-averaged control input of the inverter over the PWM carrier period, T_c. Note that $\delta_{inv} \in [-1, \ 1]$.

The locally-averaged inverter output current, $i_{L_{inv}}$, has to track a sinusoidal reference, $i^*_{L_{inv}}$, to exchange a given active power, P^*_g, and reactive power, Q^*_g, with the grid,

$$i^*_{L_{inv}}(t) = \frac{\sqrt{2}P^*_g}{V_g}\cos(\omega_g t) + \frac{\sqrt{2}Q^*_g}{V_g}\sin(\omega_g t), \qquad (2)$$

where ω_g is the grid angular frequency, and V_g denotes the grid voltage rms value.

A control strategy has to be implemented to ensure that $i_{L_{inv}}$ tracks $i^*_{L_{inv}}$. A feedback control law that takes into account resonant variables is considered [16]. Other harmonic errors, such as the third harmonic $3\omega_g$, can be similarly considered. Also, the integral of the tracking error can be taken into account. Specifically, the applied resonant control strategy is shown in Fig. 4, where the control input δ_{inv} corresponds to,

$$\delta_{inv} = \frac{1}{v_{C_{DC-link}}} \left(v_g + \boldsymbol{K}_{inv} \boldsymbol{x}_{inv} \right), \tag{3}$$

with $\boldsymbol{K}_{inv} = \begin{bmatrix} K_{inv_1} & K_{inv_2} & \cdots & K_{inv_6} \end{bmatrix}$ and $\boldsymbol{x}_{inv} = \begin{bmatrix} \tilde{i}_{L_{inv}} & x_{inv_2} & \cdots & x_{inv_6} \end{bmatrix}^T$, and where $\tilde{i}_{L_{inv}} = i_{L_{inv}} - i^*_{L_{inv}}$ is the inverter output current tracking error, $x_{inv_2} = \int_0^t \tilde{i}_{L_{inv}}(\tau)\, d\tau$ is the integral of the tracking error, and x_{inv_3}, x_{inv_4}, x_{inv_5}, x_{inv_6} are resonant variables. Specifically,

$$\begin{bmatrix} \dot{x}_{inv_3} \\ \dot{x}_{inv_4} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\omega_g^2 & -2\zeta_r\omega_g \end{bmatrix} \begin{bmatrix} x_{inv_3} \\ x_{inv_4} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tilde{i}_{L_{inv}}, \tag{4}$$

where ω_g is the resonant frequency of system (4), and it coincides with the grid angular frequency, and ζ_r is a positive damping factor near to zero [16]. The actual control implementation includes additional resonant variables x_{inv_5}, x_{inv_6} to drive the steady-state error at three-times the angular grid frequency, i.e., $3\omega_g$, to zero. Namely,

$$\begin{bmatrix} \dot{x}_{inv_5} \\ \dot{x}_{inv_6} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -9\omega_g^2 & -6\zeta_r\omega_g \end{bmatrix} \begin{bmatrix} x_{inv_5} \\ x_{inv_6} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tilde{i}_{L_{inv}}. \tag{5}$$

Due to the desire to operate in discontinuous mode, the averaged control input δ_{inv} is saturated at 1 or -1. Forcing $|\delta_{inv}| = 1$ in (3), yields

$$1 = \frac{1}{v_{C_{DC-link}}} \left| v_g + \boldsymbol{K}_{inv} \boldsymbol{x}_{inv} \right|. \tag{6}$$

Consequently, $v_{C_{DC-link}}$ has to track the following reference,

$$v^*_{C_{DC-link}} = \left| v_g + \boldsymbol{K}_{inv} \boldsymbol{x}_{inv} \right|, \tag{7}$$

during the time that $v_{C_{DC-link}}$ is being shaped, i.e., during the time the inverter does not switch.

As will be explained below, the ES processor control is responsible to drive $v_{C_{DC-link}}$ to the reference $v^*_{C_{DC-link}}$. However, since the ES processor corresponds to a boost topology, the condition $|\delta_{inv}| = 1$ can only be satisfied when the ES voltage, v_{ES}, is below the dc-link voltage, $v_{C_{DC-link}}$, thus (7) must correspond to,

$$v^*_{C_{DC-link}} = \max\left\{ \left| v_g + \boldsymbol{K}_{inv} \boldsymbol{x}_{inv} \right|, v_{ES} \right\}, \tag{8}$$

over all the grid period.

Note that in (8), when the $\max\{\}$ function takes the first parameter, the inverter is not switching, as shown in Fig. 2; whereas when the $\max\{\}$ function takes the second parameter, the inverter switches with a constant carrier period T_c.

In summary, the inverter controller in Fig. 4 drives the grid current, $i_{L_{inv}}$, and also is in charge to indicate the reference signal $v^*_{C_{DC-link}}$ to the ES processor. In this solution, feedback gains K_{inv_1}, K_{inv_2}, ..., K_{inv_6} are chosen via pole-placement technique.

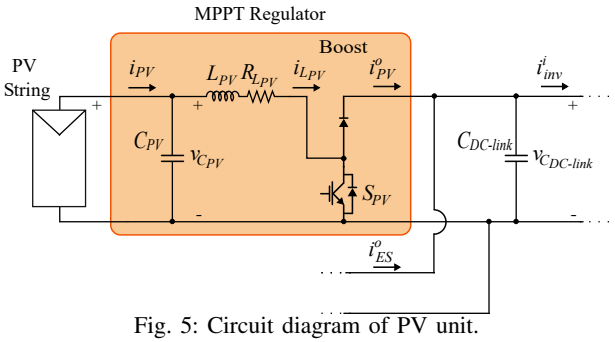

Fig. 5: Circuit diagram of PV unit.

B. PV Unit Model

A boost converter is used as the MPPT regulator, interfacing the PV array and the dc-link capacitor, as shown in Fig. 5. The boost converter consists of a capacitor C_{PV} at the PV array terminals with voltage $v_{C_{PV}}$, an inductor L_{PV} with current $i_{L_{PV}}$, and two power semiconductors. The bottom switch, $S_{PV} \in \{0,\ 1\}$, is controlled by a fixed carrier frequency PWM circuit. According to Fig. 5, the locally-averaged dynamics of the PV unit is given by:

$$L_{PV}\dot{i}_{L_{PV}} = v_{C_{PV}} - R_{L_{PV}} i_{L_{PV}} - d'_{PV} v_{C_{DC-link}}, \tag{9}$$

$$C_{PV}\dot{v}_{C_{PV}} = i_{PV} - i_{L_{PV}}, \tag{10}$$

where $R_{L_{PV}}$ models the parasitic resistance of the inductor L_{PV}, and $\{v_{C_{PV}}, i_{PV}\}$ are the locally-averaged PV array voltage and current, respectively, with $i_{PV} = f(v_{C_{PV}})$ a nonlinear mapping that models the PV array voltage-current relationship. Note that, as shown in Fig. 5, the locally-averaged PV unit output current, i^o_{PV}, corresponds to $i^o_{PV} = d'_{PV} i_{L_{PV}}$, where d'_{PV} stands for the complementary duty cycle of the switching signal S_{PV}.

The linearised model of the PV unit can be expressed as,

$$\begin{bmatrix} \dot{\tilde{i}}_{L_{PV}} \\ \dot{\tilde{v}}_{C_{PV}} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L_{PV}}}{L_{PV}} & \frac{1}{L_{PV}} \\ -\frac{1}{C_{PV}} & -\frac{m_{PV}}{C_{PV}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{L_{PV}} \\ \tilde{v}_{C_{PV}} \end{bmatrix} + \begin{bmatrix} \frac{v_{C_{DC-link}}}{L_{PV}} \\ 0 \end{bmatrix} \tilde{d}_{PV}, \tag{11}$$

where $\tilde{v}_{C_{PV}} = v_{C_{PV}} - V^*_{C_{PV}}$ is the PV capacitor voltage regulation error, with $V^*_{C_{PV}}$ as the PV capacitor voltage reference, $\tilde{i}_{L_{PV}} = i_{L_{PV}} - P^*_{PV}/V^*_{C_{PV}}$ is the inductor current regulation error, with P^*_{PV} as the PV power reference, $\tilde{d}_{PV}$ is the incremental duty cycle of the MPPT regulator, and m_{PV} is the slope of the PV nonlinear mapping at the operating point, and corresponds to $m_{PV} = -\,\partial f(v_{C_{PV}})/\partial v_{C_{PV}}|_{V^*_{C_{PV}}}$.

A control strategy has to be implemented to ensure that $v_{C_{PV}}$ tracks $V^*_{C_{PV}}$. The reference for the PV capacitor voltage $V^*_{C_{PV}}$ is provided by an MPPT [17], [18] (or flexible power point tracking [3], [19]) strategy. Namely, $\tilde{d}_{PV}$ in the proposed solution is chosen as,

$$\tilde{d}_{PV} = \frac{1}{v_{C_{DC-link}}} \begin{bmatrix} K_{PV_1} \\ K_{PV_2} \\ K_{PV_3} \end{bmatrix}^T \begin{bmatrix} \tilde{i}_{L_{PV}} \\ \tilde{v}_{C_{PV}} \\ x_{PV_3} \end{bmatrix}, \tag{12}$$

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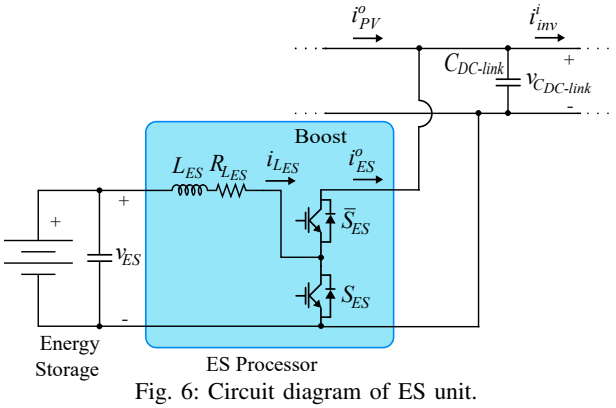

Fig. 6: Circuit diagram of ES unit.

where $x_{PV_3} = \int_0^t \tilde{v}_{C_{PV}}(\tau)\, d\tau$ is the integral of PV capacitor voltage regulation error. In this solution, feedback gains K_{PV_1}, K_{PV_2}, K_{PV_3} are chosen via pole-placement technique. Note that the MPPT regulator duty cycle expression corresponds to,

$$d_{PV} = \left(1 - \frac{V^*_{C_{PV}}}{v_{C_{DC-link}}}\right) + \tilde{d}_{PV}. \tag{13}$$

Since the MPPT regulator is based on a boost topology, the condition $V^*_{C_{PV}} \leq v_{C_{DC-link}}$ has to be fulfilled for correct PV unit behaviour. Note that a boost topology has been chosen for simplicity, but other topologies, such as buck-boost, could have been considered.

C. ES Unit Model

A bidirectional boost converter is used as ES processor, interfacing the low-voltage ES and the dc-link capacitor, as shown in Fig. 6. The boost converter consists of an inductor L_{ES} with current $i_{L_{ES}}$, and two power semiconductors. The bottom switch, $S_{ES} \in \{0,\ 1\}$, acts as the subsystem control variable. According to Fig. 6, the locally-averaged dynamics of the ES unit is given by:

$$L_{ES}\dot{i}_{L_{ES}} = v_{ES} - R_{L_{ES}} i_{L_{ES}} - d'_{ES} v_{C_{DC-link}}, \tag{14}$$

$$C_{DC-link}\dot{v}_{C_{DC-link}} = d'_{ES} i_{L_{ES}} + i^o_{PV} - i^i_{inv}, \tag{15}$$

where $R_{L_{ES}}$ models the parasitic resistance of the inductor L_{ES}, v_{ES} is the ES voltage, and d'_{ES} stands for the complementary duty cycle of the switching signal S_{ES}. Note that, as mentioned, locally-averaged current variables i^o_{PV} and i^i_{inv} in (15), correspond to $i^o_{PV} = d'_{PV} i_{L_{PV}}$ and $i^i_{inv} = \delta_{inv} i_{L_{inv}}$, respectively.

The nonlinear averaged dynamics of the ES unit subsystem are linearised around the reference trajectory $v^*_{C_{DC-link}}$, according to (8), with reference values $i^*_{L_{ES}}$ and d'^*_{ES} coherent with (14) and (15), resulting in,

$$\begin{bmatrix} \dot{\tilde{i}}_{L_{ES}} \\ \dot{\tilde{v}}_{C_{DC-link}} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L_{ES}}}{L_{ES}} & -\frac{d'^*_{ES}}{L_{ES}} \\ \frac{d'^*_{ES}}{C_{DC-link}} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_{L_{ES}} \\ \tilde{v}_{C_{DC-link}} \end{bmatrix} + \begin{bmatrix} \frac{v^*_{C_{DC-link}}}{L_{ES}} \\ -\frac{i^*_{L_{ES}}}{C_{DC-link}} \end{bmatrix} \tilde{d}_{ES}, \tag{16}$$

where $\tilde{i}_{L_{ES}} = i_{L_{ES}} - i^*_{L_{ES}}$ represents the inductor current error in the ES processor, $\tilde{v}_{C_{DC-link}} = v_{C_{DC-link}} - v^*_{C_{DC-link}}$ denotes the dc-link capacitor voltage tracking error, and $\tilde{d}_{ES}$ stands for the incremental duty cycle of the ES processor. Note that a coherent reference value for $i^*_{L_{ES}}$ corresponds to

$$i^*_{L_{ES}} = \frac{1}{d'^*_{ES}} \left(C_{DC-link}\dot{v}^*_{C_{DC-link}} - i^o_{PV} + i^i_{inv}\right), \tag{17}$$

where $d'^*_{ES} = v_{ES}/v^*_{C_{DC-link}}$. Note that including the terms i^o_{PV} and i^i_{inv} feedforwards changes in the PV current and the grid current, respectively. Besides, the derivative term $\dot{v}^*_{C_{DC-link}}$ is calculated by means of the quadrature component of $v^*_{C_{DC-link}}$ when the inverter is not switching, while it is zero when the inverter is switching. These feedforward terms improve the transient behaviour, and consequently, the error integral terms in the controller have smaller excursions. Next, control state variables, including error integral terms, are explained.

The reference $v^*_{C_{DC-link}}$, according to (8), has an important component at twice the fundamental frequency, thus the control should take into account resonant variables in a similar way as it is described in the inverter control. Specifically, a state-feedback controller that considers the resonant variables and has the form $\tilde{d}_{ES} = \boldsymbol{K}_{ES}\boldsymbol{x}_{ES}$, with $\boldsymbol{K}_{ES} \in \mathbb{R}^7$, is considered, being $\boldsymbol{x}_{ES}$,

$$\boldsymbol{x}_{ES} = \left[\tilde{i}_{L_{ES}},\, \tilde{v}_{C_{DC-link}},\, x_{ES_3},\, x_{ES_4},\, \cdots,\, x_{ES_7}\right]^T. \tag{18}$$

Fig. 7 shows the proposed state-feedback control law for the ES processor.

State variables $\{x_{ES_3},\, x_{ES_4},\, x_{ES_5}\}$, defined in (19) and (20), ensure zero steady-state error in the dc component of $\tilde{v}_{C_{DC-link}}$, and zero steady-state error in the twice-fundamental-frequency component of $\tilde{v}_{C_{DC-link}}$,

$$\dot{x}_{ES_3} = \tilde{v}_{C_{DC-link}}, \tag{19}$$

$$\begin{bmatrix} \dot{x}_{ES_4} \\ \dot{x}_{ES_5} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -4\omega_g^2 & -4\zeta_r\omega_g \end{bmatrix} \begin{bmatrix} x_{ES_4} \\ x_{ES_5} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tilde{v}_{C_{DC-link}}, \tag{20}$$

where $2\omega_g$ is the resonant frequency of system (20). Note that other additional resonant variables could be added to consider multiples of twice the angular grid frequency. In fact, in the experimental prototype, resonant variables to impose zero steady-state error in the four-times-fundamental-frequency component of $\tilde{v}_{C_{DC-link}}$, i.e., at $4\omega_g$, have been considered.

It is also important to note that the ES processor must follow a fast current reference $i^*_{L_{ES}}$, according to (17), which implies that the inductor L_{ES} must be small enough, and consequently the current ripple is nonnegligible. Furthermore, increasing the switching frequency may not always be technically appropriate. State variables $\{x_{ES_6},\, x_{ES_7}\}$, defined in (21), observe high-frequency components in $\tilde{d}_{ES}$ and can be

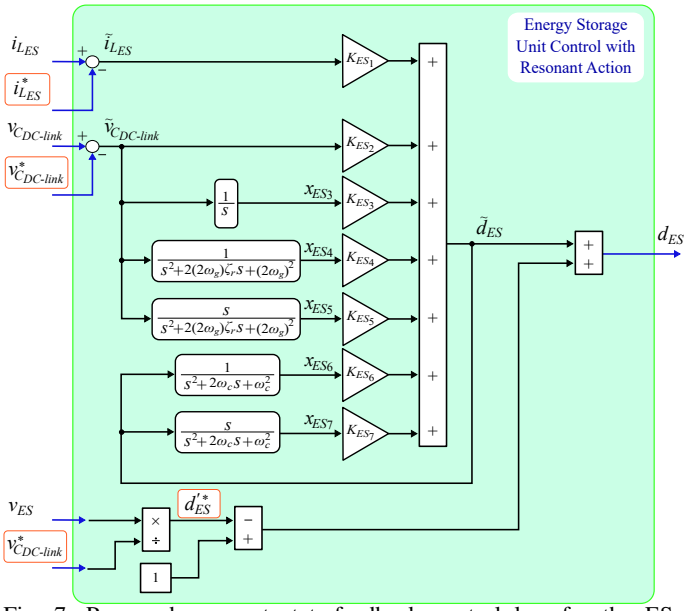

Fig. 7: Proposed resonant state-feedback control law for the ES processor.

added to the system model and fed back for limiting high-frequency components in the control signal $\tilde{d}_{ES}$,

$$\begin{bmatrix} \dot{x}_{ES_6} \\ \dot{x}_{ES_7} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\omega_c^2 & -2\omega_c \end{bmatrix} \begin{bmatrix} x_{ES_6} \\ x_{ES_7} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tilde{d}_{ES}, \tag{21}$$

where $\omega_c = 2\pi/T_c$ (T_c is the fixed PWM carrier period).

The control feedback gains $\boldsymbol{K}_{ES}$ can be determined using the pole-placement technique, similar to the inverter and PV unit. Nevertheless, given that in the ES processor dynamics (16), most of the coefficients can have a nonnegligible uncertainty, the determination of the control feedback gains has been carried out using a linear matrix inequalities (LMIs) strategy [20]–[22] that treats the uncertainty in a polytopic manner [23], [24]. Specifically, the uncertain parameters considered are $\left\{v^*_{C_{DC-link}},\, i^*_{L_{ES}},\, d'^*_{ES}\right\}$, i.e., $v^*_{C_{DC-link}} \in \left[v_{ES},\, \sqrt{2}V_g\right]$, $d'^*_{ES} \in \left[v_{ES}/\left(\sqrt{2}V_g\right),\, 1\right]$, and $i^*_{L_{ES}} \in \left[-I^{max}_{L_{ES}},\, I^{max}_{L_{ES}}\right]$, being $I^{max}_{L_{ES}}$ a prescribed maximum value for the energy-storage processor current. Thus, the uncertainty polytope has dimension three, viz., it is an hiperectangle with eight vertices. Also, the LMI strategy is able to incorporate constraints to limit the switching ripple propagation, as reported in [22]. Note that the choice of the desired location of the poles in the pole-placement technique can be made in an iterative manner. Also, the region where the poles are to be located in the LMI technique could require a few iterations.

III. Experimental Results

With the purpose of illustrating the performance of the proposed resonant-action control law for a discontinuously-operated grid-connected PV generator with low-voltage ES, experimental results are obtained on a scaled-down laboratory prototype that is shown in Fig. 8. In the prototype, the grid voltage is provided by an ITECH IT7900-series power supply,

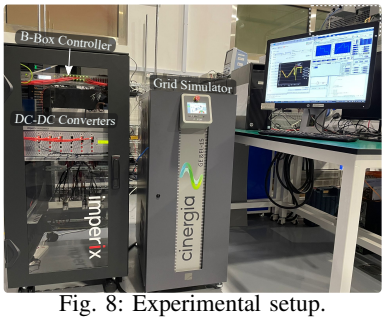

Fig. 8: Experimental setup.

TABLE I: Parameters of the Experimental Setup

Parameter	Value
Nominal grid voltage, V_g	80 V
Grid angular frequency, ω_g	100π rad/s
Inverter stage inductance, L_{inv}	5 mH
ES voltage, V_{ES}	48 V
DC-link capacitance, $C_{DC-link}$	60 μF
ES processor inductance, L_{ES}	333 μH
PV maximum power (standard test conditions)	344 W
PV maximum power point voltage (standard test conditions)	80 V
MPPT regulator inductance, L_{PV}	200 μH
PV-side capacitance, C_{PV}	200 μF
PWM carrier frequency, f_c	20 kHz

and the low-voltage ES is emulated by a GE&EL 15 kVA CINERGIA working as a bi-directional dc power supply. IMPERIX PEH2015 H-bridge modules are used to implement the three converters, i.e., the inverter, the MPPT regulator, and the ES processor. Parameters of the scaled-down prototype are shown in Table I. It can be appreciated that the size of the dc-link capacitor, $C_{DC-link}$, and the inductance of the ES processor, L_{ES}, are small, thus allowing a fast dynamic. The proposed control schemes depicted in Fig. 4 and Fig. 7 are implemented using a B-Box RCP board from IMPERIX. The B-Box RCP has a dual-core DSP (2x ARM Cortex A9 1GHz, 1GB DDR3), in which the proposed controller is implemented with 60 kHz sampling. Specifically, the duty cycles are generated at a sample rate of 60 kHz for the PV unit, the ES unit, and the inverter. The PWM is implemented in a Kintex-grade FPGA (Xilinx Kintex 7 125K) with a time resolution of 4 ns, using a 20-kHz 32-bit triangular carrier. Voltage and current magnitudes depicted in the following figures have been captured using a YOKOGAWA DLM4038 oscilloscope.

In the proposed control law for the inverter (3), depicted in Fig. 4, the feedback gains have been chosen such that the closed-loop transfer function has three pairs of two complex-conjugate poles at $-\zeta_i\omega_{n,i} \pm j\omega_{n,i}\sqrt{1-\zeta_i^2}$, with $\omega_{n,i} = 4/\left(\zeta_i T_{set,i}\right)$, where $T_{set,i}$ and ζ_i are the desired settling time and damping coefficient of the ith pair ($i \in \{1, 2, 3\}$), respectively. Specifically, $T_{set,1} = 7.5$ ms, $T_{set,2} = 10$ ms, $T_{set,3} = 12.5$ ms, and $\zeta_i = \sqrt{2}/2$, $\forall i$. Particularly, the inverter

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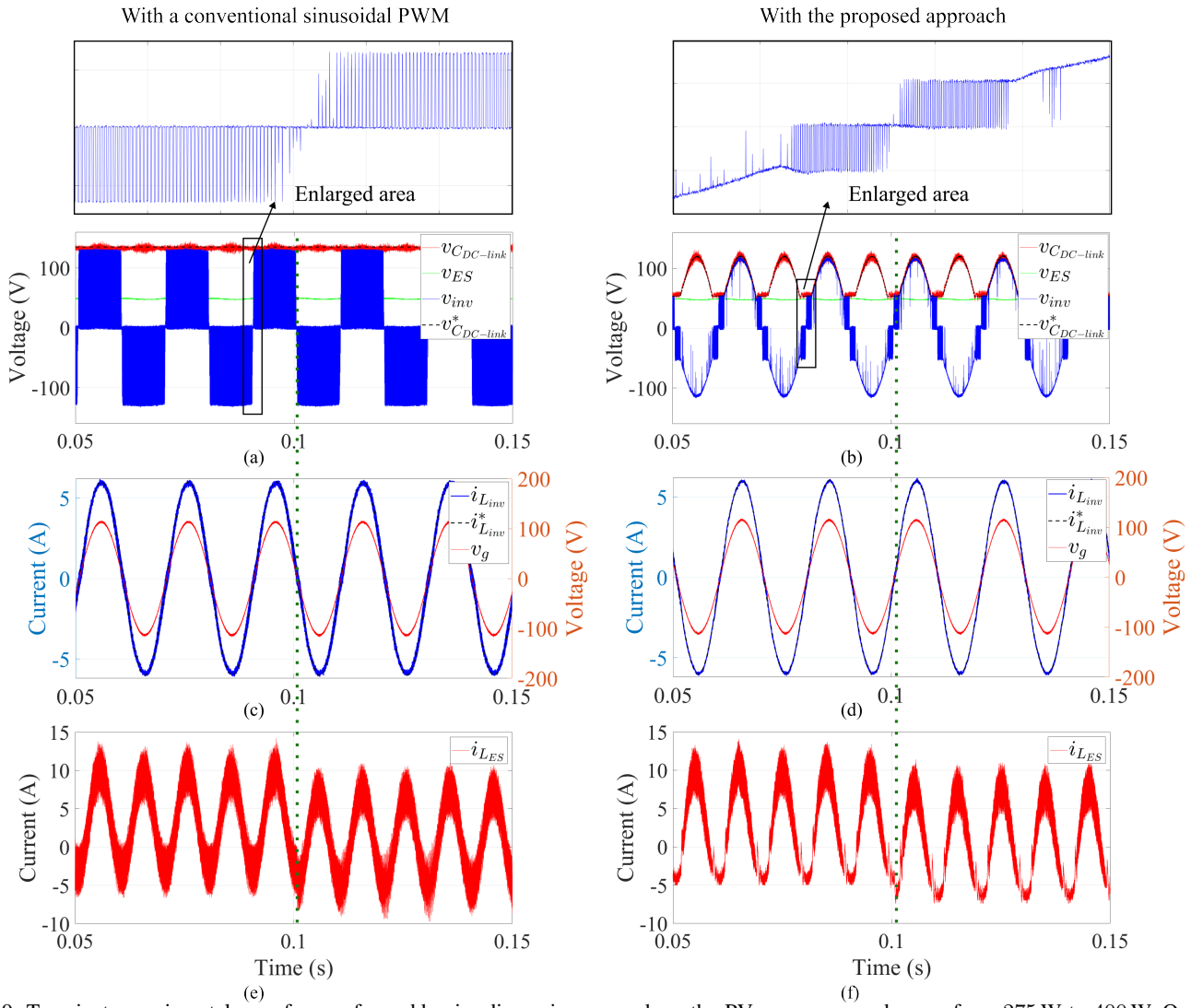

Fig. 9: Transient experimental waveforms of a sudden irradiance increase where the PV array power changes from 275 W to 400 W. On the left side, the conventional sinusoidal PWM with $v^*_{C_{DC-link}} = 135$ V. On the right side, the proposed voltage shaping approach. Both control strategies operating at $P^*_g = 480/\sqrt{2}$ W and $Q^*_g = 0$. Upper plots: PWM inverter voltage, v_{inv}, dc-link capacitor voltage, $v_{C_{DC-link}}$, and the 48-V ES voltage, v_{ES}; Middle plots: grid voltage, v_g, and grid current, $i_{L_{inv}}$; Bottom plots: ES current, $i_{L_{ES}}$.

feedback gains are,

$$\boldsymbol{K}_{inv} = \big[\ -12.3321,\quad -2259.2129,\quad -542454.2395,\quad -2365.4614,\quad 1265767.9895,\quad -6257.4191\ \big]. \tag{22}$$

Regarding the PV unit, the feedback gains of control law (12) have been chosen such that the closed-loop transfer function has a simple pole at $-4/T_{set}$, and a pair of two complex-conjugate poles at $-\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2}$, with $\omega_n = 4/(\zeta T_{set})$, $T_{set} = 0.8$ ms, and $\zeta = \sqrt{2}/2$. Particularly, the PV unit feedback gains are $K_{PV_1} = 2.9937$, $K_{PV_2} = -3.0220$, $K_{PV_3} = -10204.0816$.

The proposed control for the ES processor considers not only the resonant variables at twice the fundamental frequency ($2\omega_g$) in the capacitor voltage tracking error $\tilde{v}_{C_{DC-link}}$, as in (20), but also resonant variables at $4\omega_g$. Therefore, the state feedback gain $\boldsymbol{K}_{ES}$ is augmented with two additional gains. We refer to the augmented state feedback gain as $\boldsymbol{K}^a_{ES}$ in the experimental description. Using the parameters from Table I, setting the prescribed maximum value for the ES processor current as $I^{max}_{L_{ES}} = 8$ A, the following feedback gain $\boldsymbol{K}^a_{ES}$ is obtained using an LMI approach [24],

$$\boldsymbol{K}^a_{ES} = \big[\ -0.0150,\quad -0.0062,\quad -1.8672,\quad 74.9488,\quad -4.1879,\quad 13671111904.9396,\quad 173006.0733,\quad -3794.8340,\quad -6.4543\ \big]. \tag{23}$$

Next, the paper discusses the experimental results obtained when the PV array power is providing 275 W and the inverter is delivering an active power $P_g = 480/\sqrt{2}$ W, as well as the effects of a sudden change in the PV array power. The proposed approach also allows for the exchange of a specific amount of reactive power. The harmonic content of grid-side signals, and switching losses of the converters, are also discussed, for both the proposed voltage shaping strategy and a conventional SPWM strategy. In both strategy cases, the feedback control gains used, shown in (22) and (23), and the dc-link capacitance, $C_{DC-link} = 60\,\mu$F, are the same.

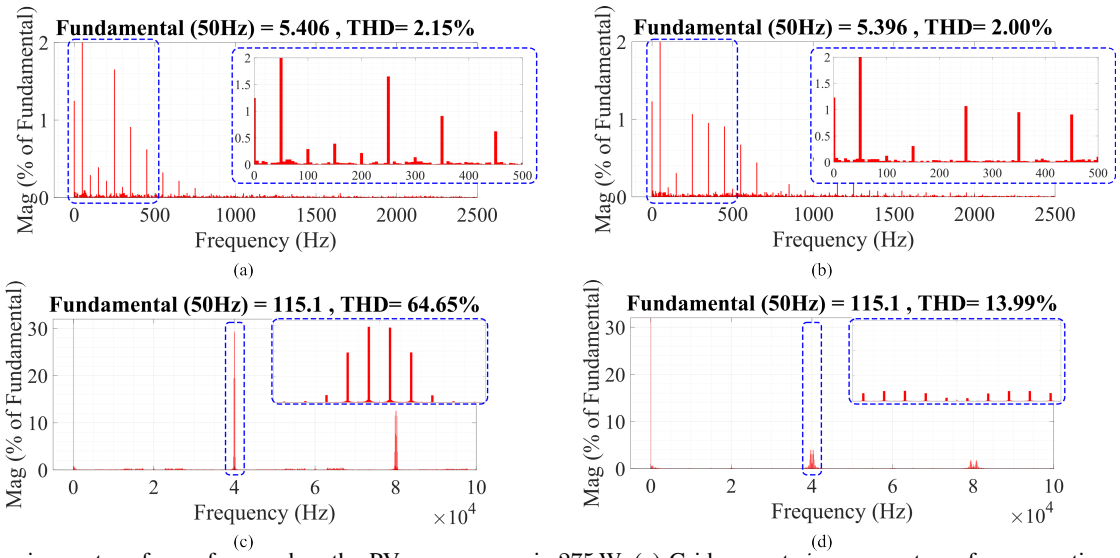

Fig. 10: Harmonic spectra of waveforms when the PV array power is 275 W. (a) Grid current, $i_{L_{inv}}$, spectrum for conventional PWM. (b) Grid current, $i_{L_{inv}}$, spectrum for the proposed voltage shaping approach. (c) PWM inverter voltage, v_{inv}, spectrum for conventional PWM. (d) PWM inverter voltage, v_{inv}, for the proposed voltage shaping approach.

Fig. 9 shows the experimental waveforms in the ES unit and the inverter when the PV array power is providing 275 W and suddenly changes to 400 W at $t = 0.1$ s. In this specific experiment, the inverter is providing a current $i_{L_{inv}}(t) = 6\cos(\omega t)$ to a grid voltage $v_g(t) = 80\sqrt{2}\cos(\omega t)$. The left-column plots of Fig. 9, i.e., Fig. 9(a), Fig. 9(c) and Fig. 9(e), show the behaviour when the dc-link capacitor voltage is controlled to $v^*_{C_{DC-link}} = 135$ V, whereas the right-column plots of Fig. 9, i.e., Fig. 9(b), Fig. 9(d) and Fig. 9(f), correspond to the case when the dc-link capacitor voltage is shaped according to (8), with $v_g(t) = 80\sqrt{2}\cos(\omega t)$ and $v_{ES} = 48$ V. It can be observed that, in both cases, the transient in ES unit and inverter waveforms is very fast, in terms of the grid period. It is worth noting that the dc-link voltage, $v_{C_{DC-link}}$, in Fig. 9(b), is accurately shaped to the desired quasi-rectified sinusoidal shape, $v^*_{C_{DC-link}}$, which corroborates that the proposed resonant structure works as expected. The shaped quality of $v_{C_{DC-link}}$ allows an almost perfect discontinuous operation in the inverter, which can be corroborated by the reduction of the number of switching events over a grid period in the PWM inverter voltage, v_{inv}, despite the fact that the inverter has its own controller. In Fig. 9(c) and Fig. 9(d), it can be observed that the grid current, $i_{L_{inv}}$, and grid voltage, v_g, exhibit an excellent sinusoidal shape and the transient is almost imperceptible. This means that the controller of the ES processor completely rejects disturbances coming from the PV unit, as well as allows the desired discontinuous operation. This rejection of disturbances is obtained thanks to the ES current reference used, i.e. $i^*_{L_{ES}}$ in (17), which includes feedforward terms. Also, it is worth noting that the ES current, $i_{L_{ES}}$, for both cases, shown in Fig. 9(e) and Fig. 9(f), present approximately the same peak-to-peak range, and the transient at $t = 0.1$ s is fast.

In Fig. 9(d), it can be observed that the grid current, $i_{L_{inv}}$, tracks accurately its sinusoidal reference despite the discontinuous operation. The harmonic spectra of the grid current, $i_{L_{inv}}$, is depicted in Fig. 10(a) and Fig. 10(b), for the conventional SPWM and the proposed voltage shaping strategy, respectively. The obtained total harmonic distortion (THD) (calculated considering up to 50th harmonic order, and the steady-state condition corresponding to the first half of Fig. 9) is reported in the corresponding figures. It can be observed that the proposed strategy reduces the even harmonics in the current compared to the conventional approach. Notably, the second harmonic is reduced from 0.3% in the conventional approach to 0.1% with the proposed approach. Moreover, the fourth harmonic experiences a notable reduction from 0.2% to nearly 0%, and the sixth harmonic similarly decreases from 0.1% to nearly 0% when employing the proposed voltage shaping strategy. The bottom plots of Fig. 10, i.e., Fig. 10(c) and Fig. 10(d), show the corresponding harmonic spectra of the PWM inverter voltage, v_{inv}, for the conventional SPWM and the proposed voltage shaping strategy, respectively. In this case, the THD has been calculated across the entire frequency range. As can be seen, the proposed strategy significantly reduces PWM inverter voltage THD from 64.65% to 13.99%, facilitating the filtering action or, equivalently, allowing the use of smaller filtering inductors.

It is important to note that with the proposed approach, the inverter only switches for about one-third of the fundamental period, for the experimental parameters given in Table I, as shown in Fig. 9(b), which stands in contrast with the conventional SPWM that switches over all the grid period, as shown in Fig. 9(a). Moreover, in the proposed approach, the inverter switches when the grid current is close to zero. This means that the inverter switching losses are significantly reduced (analysis is reported in the Appendix section). For the experimental parameters from Table I, and using (32), results in a 95% reduction in the inverter switching losses. With regard to the losses in the ES processor, it is worth

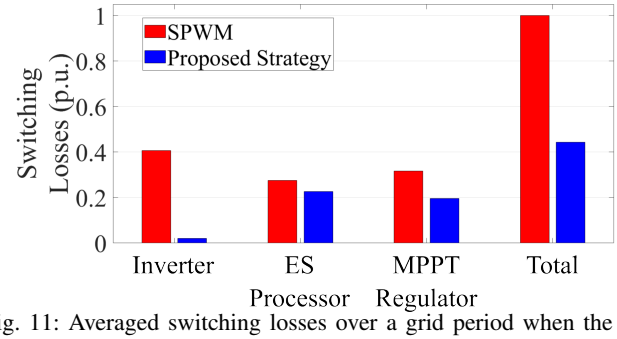

Fig. 11: Averaged switching losses over a grid period when the PV array power is 275 W. Red represents the conventional sinusoidal PWM strategy, while blue represents the proposed voltage shaping strategy.

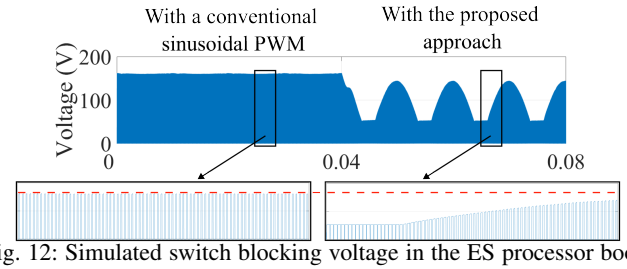

Fig. 12: Simulated switch blocking voltage in the ES processor boost converter (bottom switch) when operating the grid-connected PV generator with a conventional sinusoidal PWM approach and with the proposed voltage shaping approach.

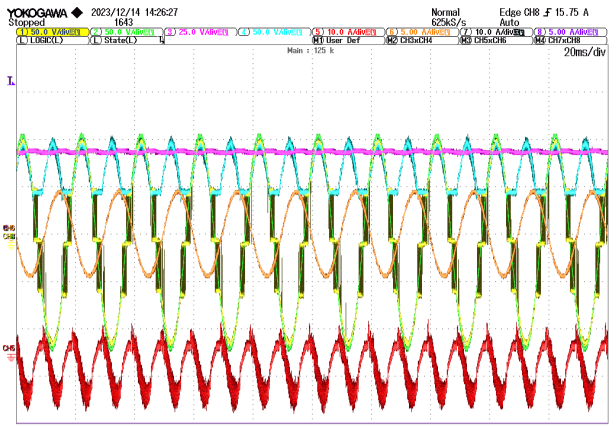

Fig. 13: Experimental waveforms when operating at $P_g^* = -320/\sqrt{2}$ W and $Q_g^* = -320/\sqrt{2}$ var. Channel CH1 (yellow) shows the PWM inverter voltage, v_{inv}, Channel CH2 (green) shows the grid voltage, v_g, Channel CH3 (magenta) shows the 48-V ES voltage, v_{ES}, Channel CH4 (cian) shows the dc-link capacitor voltage, $v_{C_{DC-link}}$, Channel CH5 (red) shows the ES current, $i_{L_{ES}}$, and Channel CH6 (orange) shows the grid current, $i_{L_{inv}}$.

mentioning that, as shown in Fig. 9(e) and Fig. 9(f), both strategies have similar shapes and RMS values of ES current, $i_{L_{ES}}$. Furthermore, the switch blocking voltage of the ES processor, i.e., $v_{C_{DC-link}}$, is reduced in the proposed strategy. This means that adopting the proposed strategy does not decrease the efficiency of the ES processor, but it increases it. For the same reason, the efficiency of the MPPT regulator does not change significantly. Specifically, for the prototype shown in Fig. 8 and parameters from Table I, the loss reduction has been corroborated using the recorded experimental data corresponding to the steady-state condition of the first half of Fig. 9, i.e., when the PV array power is 275 W. Fig. 11 depicts the obtained switching losses values normalised with respect to the total switching losses in the conventional SPWM strategy. The reduction in switching losses in the inverter is 95%, which is consistent with the expected value according to the Appendix analysis. Additionally, the switching losses in the ES processor and MPPT regulator have been reduced by 18% and 38%, respectively. This reduction is due to the fact that the blocking voltage of the dc-dc converter switches corresponds to the quasi-sinusoidally rectified dc-link capacitor voltage in (8) when adopting the proposed strategy. The instantaneous switching losses, which are proportional to the blocking voltage at the switching instant [25], are lower with the proposed approach compared to using a fixed voltage with a conventional strategy, as shown in Fig. 12. Furthermore, from measurements of the battery voltage and current, PV array voltage and current, and grid voltage and current, it can be stated that the proposed voltage shaping strategy reduces the overall losses, which includes conduction losses, by 45%. This reduction in overall losses, as well as the THD results, justify the proposed resonant control technique used in the ES processor, which allows for voltage shaping of the dc-link capacitor.

As a final feature of the proposed approach, it is worth mentioning that the proposed PV generator can manage the exchange of reactive power with the grid, according to (2). Fig. 13 shows the waveforms of the PV generator when it is exchanging $P_g^* = -320/\sqrt{2}$ W and $Q_g^* = -320/\sqrt{2}$ var with the grid. It can be observed that the proposed strategy is able to shape the dc-link capacitor voltage as desired such that the inverter does not switch for a significant portion of the grid period.

IV. Conclusion

The paper has proposed a novel control of a grid-connected PV generator with low-voltage ES that reduces the switching losses. The PV generator consists of three subsystems connected by a common dc-link capacitor: a PV unit, an ES unit, and an inverter. The inverter is operated in discontinuous mode, which implies that the common dc-link capacitor voltage is shaped to a quasi-rectified sinusoidal shape. The controller for the ES unit that shapes the dc-link capacitor voltage uses integral and resonant variables. It ensures zero steady-state error at dc and at twice and four times the grid frequency. Experimental results corroborate an excellent behaviour of the overall system design, which yields a 95% saving in averaged switching losses in the inverter while reducing PWM inverter voltage THD from 64.65% to 13.99%, facilitating the filtering action. The proposed PV generator can exchange both active and reactive power with the grid. Experimental results show fast transitions for changing irradiance conditions.

APPENDIX
ASSESSMENT OF SWITCHING LOSSES

The switching losses in the H-bridge inverter are assumed to be proportional to the product between the switch blocking voltage $v_{C_{DC-link}}$ and the current $i_{L_{inv}}$ through the switch device at the switching instant, i.e.,

$$p_{sw} = \alpha\, v_{C_{DC-link}}\, |i_{L_{inv}}|\,, \tag{24}$$

where constant α represents the switching losses at $v_{C_{DC-link}} = 1\,\text{p.u.}$ and $i_{L_{inv}} = 1\,\text{p.u.}$

The averaged switching losses over a grid period $T_g = 2\pi/\omega_g$ is, in turn, proportional to p_{sw}, and can be modeled as,

$$\langle p_{sw}\rangle_{T_g} = \frac{1}{T_g}\int_{-T_g/2}^{T_g/2} p_{sw}\,(\tau)\; d\tau. \tag{25}$$

Assuming steady-state operation and unity-power factor, i.e., $Q_g^* = 0$ in (2), the averaged switching losses over a grid period correspond to,

$$\langle p_{sw}\rangle_{T_g} = 2\frac{\alpha'}{T_g}\int_{0}^{T_g/2} v_{C_{DC-link}}\,(\tau)\, i_{L_{inv}}\,(\tau)\; d\tau. \tag{26}$$

where the odd symmetry of the integrand, i.e., $v_{C_{DC-link}} i_{L_{inv}}$, over $[-T_g/2,\, T_g/2]$, has been considered, and where α' depends on α and also on the number of switching events per grid period. Note that there is a shift in the time variable, i.e., $t = \tau - T_g/4$, such that $\cos(\omega_g t)$ term in (2) becomes $\sin(\omega_g \tau)$.

For a conventional SPWM strategy, where the dc-link voltage is controlled to a constant value V_{dc}^*, the averaged switching losses over a grid period in (26) becomes

$$\langle p_{sw}\rangle_{T_g}^{\text{SPWM}} = \frac{\alpha'}{\pi} V_{dc}^* \frac{\sqrt{2}P_g^*}{V_g}\int_{0}^{\pi} \sin(\theta)\; d\theta, \tag{27}$$

where $d\theta = \omega_g\, d\tau$, which can be solved as,

$$\langle p_{sw}\rangle_{T_g}^{\text{SPWM}} = 2\frac{\alpha'}{\pi} V_{dc}^* \frac{\sqrt{2}P_g^*}{V_g}. \tag{28}$$

On the other side, for the proposed voltage shaping strategy, where the dc-link voltage is controlled according to (8), the averaged switching losses over a grid period in (26) becomes

$$\langle p_{sw}\rangle_{T_g}^{\text{shaping}} = 2\frac{\alpha'}{\pi} v_{ES} \frac{\sqrt{2}P_g^*}{V_g}\int_{0}^{\theta_c} \sin(\theta)\; d\theta, \tag{29}$$

where $[\theta_c,\, \pi - \theta_c]$ corresponds to the time period in which the inverter does not switch, i.e., $\delta_{inv} = 1$. Note that the threshold between the switching and nonswitching region, θ_c, satisfies the following equality,

$$\sqrt{2}V_g \sin(\theta_c) = v_{ES}, \tag{30}$$

which assumes negligible voltage drop in the filtering inductor; and after operating,

$$\langle p_{sw}\rangle_{T_g}^{\text{shaping}} = 2\frac{\alpha'}{\pi} v_{ES} \frac{\sqrt{2}P_g^*}{V_g}\left(1 - \cos(\theta_c)\right). \tag{31}$$

Therefore, the per-unit reduction in the inverter switching losses can be calculated as,

$$1 - \frac{\langle p_{sw}\rangle_{T_g}^{\text{shaping}}}{\langle p_{sw}\rangle_{T_g}^{\text{SPWM}}} = 1 - \frac{v_{ES}}{V_{dc}^*}\left(1 - \sqrt{1 - \left(\frac{v_{ES}}{\sqrt{2}V_g}\right)^2}\right). \tag{32}$$

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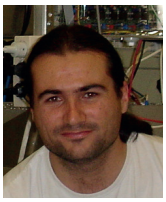

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