Model Predictive Control for Inter-Submodule State-of-Charge Balancing in Cascaded H-Bridge Converter-Based Battery Energy Storage Systems

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***Abstract*—In the operation of battery energy storage systems based on the cascaded H-bridge converter, it is beneficial to balance the state of charge of batteries in different submodules within the converter phase-arm. This is achieved by distributing the active power among the submodules. Although multiple methods have been proposed for this purpose, they face the challenge of rendering optimal active power distributions that maximize balancing speed while meeting power constraints in the battery energy storage system. To overcome this challenge, a model predictive control scheme is developed in this paper. The proposed method is remarkably robust against parametric uncertainties (battery voltage, capacity, etc.), as evidenced by its ability to tolerate a substantial 50% uncertainty in the parameters, resulting in a mere 0.05% steady-state error. Furthermore, because the predictive control can be executed at a low frequency, the computational burden is comparable to other existing methods.**

I. Introduction

The global installed capacity of grid-scale battery energy storage systems (BESSs) was around 16 GW at the end of 2021 and is expected to reach 680 GW in 2030 according to the Net Zero Emission Scenario [1]. In a BESS, power electronic converters are used as the interface between the batteries and the power system. Among the potential candidates, the cascaded H-bridge (CHB) converter is a suitable one for medium-/high-voltage applications [2]. Its advantages include modularity, high power conversion efficiency, ability to accommodate heterogeneous energy storage technologies, etc.

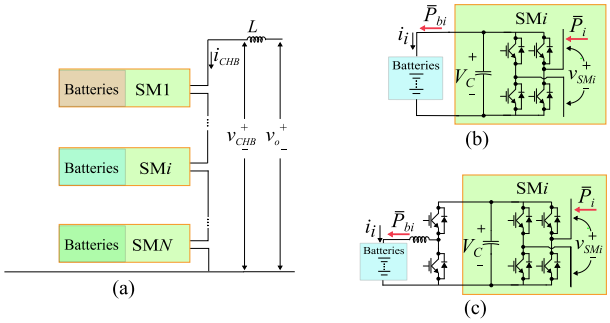

Fig. 1. Circuit diagram of (a) CHB converter-based BESS, (b) battery modules directly connected to the SM, and (c) battery modules connected to the SM via a boost converter.

Fig. 1(a) depicts the circuit diagram of a single-phase CHB-based BESS (CBESS), which consists of multiple submodules (SMs). Batteries can be integrated into the SMs directly or via a dc-dc converter, as depicted in Figs. 1(b) and (c) [3], respectively. The direct integration is simpler and more efficient, while using a dc-dc converter allows the control of battery currents and capacitor voltages. The CBESS can accommodate either homogeneous or heterogeneous batteries (in terms of technology, chemistry, capacity, power rating, etc.). The use of homogeneous batteries simplifies the design and control of the CBESS, while the use of heterogeneous batteries can reduce the volume and capital cost of the CBESS [4], [5].

In the operation of CBESSs, it is desired that batteries in different SMs within each phase have the same state of charge (SoC), referred to as inter-SM SoC balance henceforth. Without inter-SM SoC balance, batteries in some SMs can become fully charged/discharged earlier than others, which will reduce the power capacity of the system. To achieve the inter-SM SoC balance, the active power of the CBESS needs to be distributed among the SMs in an appropriate fashion. In order to fully utilize battery capacities, a fast state of charge (SoC) balancing speed is generally preferred [6], which necessitates a highly unbalanced distribution of active power among the SMs. However, the inter-SM active power distribution needs to satisfy certain constraints [7]. The constraints include the hardware limits that relate to the

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power rating of the SMs and batteries, and the control limits that relate to the disparity among the SM active powers [8]. Multiple methods have been proposed for the inter-SM SoC balance [9], which can be broadly classified into direct and indirect methods as below.

Indirect methods modify the SM output voltage references according to the SoC imbalance, thus indirectly affecting the active power distribution among the SMs. For instance, the method in [10] adds a fundamental-frequency voltage component to the SM output voltage reference. The magnitude of the added component is calculated with a proportional-integral (PI) controller according to the SoC imbalance and its phase is synchronized with the arm current. Then, the switching signals of the SMs are obtained using the phase-shift pulse-width modulation (PWM) technique. The methods in [11]–[13] follow the same principle as [10] except that the component added to the SM output voltage reference is synchronized with the arm voltage. An artificial neural network can be included in PI-based SoC balancing methods to improve the accurace of the SoC imbalance estimation [14]. In [6], an adaptive method is proposed to decide the control gain of the proportional controller for rapid SoC balancing.

Different from the PI-based methods [15], the indirect methods in [16]–[18] first calculate the number of SMs to insert at each sampling instant using techniques like the level-shifted PWM [19]. Thereafter, the SMs are sorted according to their SoC values and inserted in a way that discharges SMs with higher SoCs and charges SMs with lower SoCs. While the previously mentioned indirect methods can balance the battery SoC, they cannot guarantee adherence to active power constraints [7]. This limitation is a result of the indirect manipulation of active power. Certain SMs may be charged/discharged with excessive power, posing a potential safety risk to the CBESS.

A rule-based method (RBM) that directly distributes active power among the SMs is proposed in [7]. This method first analytically calculates the SM active power references that can balance the SoC values and assesses whether the calculated power references satisfy the operating constraints. If these constraints are not satisfied, the active power references are modified to become feasible. Eventually, a controller is used to regulate the SM active powers to their corresponding references. However, this method may result in a conservative inter-SM active power distribution, thus yielding a suboptimal SoC balancing speed. Additionally, the RBM performance is dependent on the accurate knowledge of CBESS parameters, particularly the battery capacitiy, battery voltage, and power conversion efficiency per SM.

From the above discussion, none of the existing methods can optimize the inter-SM active power distribution for the SoC balancing. The generated active power distribution can violate the constraints and/or suffer from a suboptimal SoC balancing speed. To overcome these drawbacks, this paper proposes a direct SoC balancing method via a constrained predictive approach. The contributions of this paper include:
(i) Developing a model predictive control (MPC) scheme to optimize the active power distribution for rapid SoC balancing without violating active power constraints.
(ii) Analyzing the sensitivity of the proposed MPC scheme to parametric uncertainties.
(iii) Pointing out and verifying that, due to the slow dynamics of the variables (i.e., SoC), the MPC scheme can update the SM active power references at a frequency even lower than the fundamental grid frequency to reduce the associated computational burden.

The rest of the paper is organized as follows. Section II explains the background of SoC balancing and reviews the RBM used as a benchmark in this paper. Section III develops the MPC scheme and Section IV investigates its robustness against parametric uncertainties. Experimental results are provided in Section V. Finally, Section VI concludes this paper.

II. Inter-SM SoC Balancing

This section first introduces the principle of inter-SM SoC balancing and the SM active power constraints. Then, the RBM [7], which is the state-of-the-art method in the literature that ensures the satisfaction of power constraints, is reviewed.

A. Background

In a CBESS with N SMs per phase, as depicted in Fig. 1(a), the instantaneous SoC of the battery module in the ith ($i \in \{1, 2 \cdots N\}$) SM can be calculated as [20]:

$$SoC_i(t) = SoC_i(0) + \frac{\int_0^t i_i dt}{Q_i}, \tag{1}$$

where $SoC_i(t)$ and $SoC_i(0)$ correspond to the instantaneous SoC and the initial SoC, respectively, i_i refers to the battery current, and Q_i denotes the capacity of the battery module.

Although i_i may contain considerable ripple [3], SoC_i is almost ripple free as Q_i is normally large for batteries. Hence, SoC_i can be calculated as [7]

$$SoC_i(t) = SoC_i(0) + \frac{\int_0^t \bar{i}_i dt}{Q_i}, \tag{2}$$

where $\bar{i}_i$ refer to the averaged value i_i in one fundamental grid period (T_g). Note that $\bar{i}_i$ corresponds to:

$$\bar{i}_i = \frac{\bar{P}_{bi}}{V_{bi}}, \tag{3}$$

where $\bar{P}_{bi}$ refers to the average active power of the battery module, as shown in Fig. 1, and V_{bi} is the battery voltage. The value of $\bar{P}_{bi}$ depends on the average active power of the corresponding SM, i.e. [7]

$$\bar{P}_{bi} = \eta_i \bar{P}_i, \tag{4}$$

where $\bar{P}_i$ refers to the average active power of the SM from its ac side, as shown in Fig. 1, and η_i accounts for the converter losses. Due to the power losses, $\eta_i \leq 1$ when the battery is charging ($\bar{P}_{bi} \geq 0$), and $\eta_i > 1$ when the battery is discharging ($\bar{P}_{bi} < 0$). Combining (2)-(4) yields [7]

$$\dot{SoC}_i(t) = \frac{\bar{P}_i}{\alpha_i}, \tag{5}$$

with

$$\alpha_i = \frac{Q_i V_{bi}}{\eta_i}. \tag{6}$$

Note that the values of $\bar{P}_i$ can differ among the SMs [8], which provides a degree of freedom to balance the SoC values. Nevertheless, there are constraints on $\bar{P}_i$, as explained in the next subsection.

B. SM Active Power Constraints

In the operation of the CBESS, the constraints on the distribution of SMs active power ($\bar{P}_i$) are classified into summation constraints, hardware constraints, and disparity constraints [7]. The reference values of $\bar{P}_i$, denoted as $\bar{P}_i^*$, should therefore satisfy these constraints, as explained below.

1) Summation Constraint: The sum of the SMs active power within a phase arm should be equal to the phase-arm active power reference (denoted as $\bar{P}^*_{CBESS}$). Thus, $\bar{P}_i^*$ must adhere to [7]

$$\sum_{i=1}^{N} \bar{P}_i^* = \bar{P}^*_{CBESS}. \tag{7}$$

2) Hardware Constraints: Due to component ratings, there are upper and lower active power limits for each of the N SMs, denoted as $\bar{P}_{ui}$ and $\bar{P}_{li}$ for the ith SM, respectively. Hence, $\bar{P}_i^*$ should satisfy [7]

$$\bar{P}_{li} \le \bar{P}_i^* \le \bar{P}_{ui}, \forall i \in \{1, 2 \cdots N\}. \tag{8}$$

3) Disparity Constraints: According to the study in [21], [22], there is a limit for the active power disparity among the SMs. This disparity limit can be formulated as [21]

$$\begin{gathered}
\bar{P}_i^* \le \bar{P}^{\{i\}}_{max-1}, \forall i \in \{1, 2 \cdots N\}; \\
\bar{P}^*_{i_1} + \bar{P}^*_{i_2} \le \bar{P}^{\{i_1, i_2\}}_{max-2}, \forall i_1 \ne i_2; \\
\cdots\cdots \\
\bar{P}^*_{i_1} + \bar{P}^*_{i_2} \cdots + \bar{P}^*_{i_{(N-1)}} \le \bar{P}^{\{i_1, i_2 \cdots i_{(N-1)}\}}_{max-(N-1)},
\end{gathered} \tag{9}$$

which means that the sum of $\bar{P}_i^*$ of any n SMs ($n \in \{1, 2 \cdots N-1\}$) is upper bounded by the corresponding $\bar{P}^{\{i_1, i_2 \cdots i_n\}}_{max-n}$. The derivation of $\bar{P}^{\{i_1, i_2 \cdots i_n\}}_{max-n}$ is explained in [21], [22], and hence is not repeated in this paper for the sake of brevity. If the SM power references violate the disparity constraints, the SMs will fail to track their corresponding references, which can cause detrimental consequences, such as overcharging batteries in some SMs.

C. Constrained Rule-Based Method

Among the reported SoC balancing methods, the RBM in [7] is the only one that considers all the aforementioned constraints (7)-(9), hence it is considered as the benchmark in this paper.

The operating principle of the RBM is illustrated in Fig. 2. Firstly, the SM active power references ($\bar{P}_i^*$) are calculated as [7]

$$\bar{P}_i^* = \frac{\alpha_i (SoC^* - SoC_i)}{\sum_{i=1}^{N} \alpha_i (SoC^* - SoC_i)} \bar{P}^*_{CBESS}, \tag{10}$$

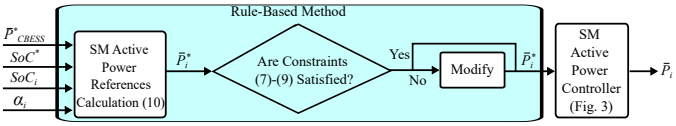

Fig. 2. Constrained RBM.

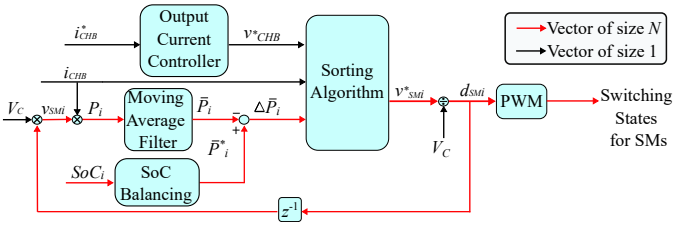

Fig. 3. SM active power controller [21].

where SoC^* is a prescribed reference value. If the SM active powers ($\bar{P}_i$) are regulated to the $\bar{P}_i^*$ values defined in (10), the SoC_i of all the SMs will reach SoC^* after

$$T_{bal} = \frac{\sum_{i=1}^{N} \alpha_i (SoC^* - SoC_i)}{\bar{P}^*_{CBESS}}, \tag{11}$$

where T_{bal} refers to the time required to balance the SoCs. Note that if an improper SoC^* causes $T_{bal} < 0$, the RBM will fail to balance the SoCs. Hence, one suggested practice in [7] is to set SoC^* as the allowed upper bound for SoC_i (for instance, 0.8 in [7]) when $\bar{P}^*_{CBESS} > 0$, and as the lower bound (for instance, 0.2 in [7]) when $\bar{P}^*_{CBESS} < 0$, which secures $T_{bal} > 0$ but can render a slow SoC balancing speed.

Note that $\bar{P}_i^*$ defined in (10) satisfies the summation constraint (7), i.e., $\sum_{i=1}^{N} \bar{P}_i^* = \bar{P}^*_{CBESS}$. Nevertheless, $\bar{P}_i^*$ may violate constraints (8) and (9), and in that case, $\bar{P}_i^*$ needs to be modified. For instance, if the jth SM active power reference ($\bar{P}_j^*$) is higher than its upper bound ($\bar{P}_{uj}$), which violates the constraint (8), $\bar{P}_j^*$ will be saturated at $\bar{P}_{uj}$ by subtracting $\Delta\bar{P}_j^* = \bar{P}_j^* - \bar{P}_{uj}$. Then, to have $\sum_{i=1}^{N} \bar{P}_i^* = \bar{P}^*_{CBESS}$, $\Delta\bar{P}_j^*$ will be distributed among the remaining $\bar{P}_i^*$ ($j \ne i$). Specifically, a larger ratio of $\Delta\bar{P}_j^*$ will be added to those $\bar{P}_i^*$ that are further away from their upper bound ($\bar{P}_{ui}$), while a smaller ratio will be added to those $\bar{P}_i^*$ that are closer to their upper bound, thus ensuring that the constraints are satisfied after the modification.

After deciding $\bar{P}_i^*$, a controller is implemented to regulate $\bar{P}_i$ to their corresponding references [21], which is depicted in Fig. 3. Firstly, a moving average filter (MAF) is used to calculate $\bar{P}_i$. According to the difference between $\bar{P}_i^*$ and $\bar{P}_i$, a sorting algorithm is used to decide the output voltage reference (v^*_{SMi}) for each SM. Then, the switching of the SMs is decided using the phase-shift PWM technique.

According to the above discussion, the RBM satisfies active power constraints but can suffer from a slow SoC balancing speed.

III. Proposed Model Predictive Control

This section proposes an MPC scheme to optimize the SoC balancing performance. Afterwards, simulation results are

obtained to verify the performance of the developed MPC scheme.

A. Proposed Optimization Problem

From (5), a SoC prediction model can be derived as

$$SoC_i(k+1) = SoC_i(k) + \frac{\bar{P}_i(k)}{\alpha_i} T_d, \tag{12}$$

where T_d refers to the sampling period, $SoC_i(k)$ refers to the SoC_i at the time instant kT_d (k is the sampling index), $\bar{P}_i(k)$ stands for the active power between kT_d and $(k+1)T_d$.

To calculate the optimal distribution of SM active power references $\bar{P}_i^*(k)$ that satisfy the constraints (7)-(9) and eliminate the SoC imbalance quickly, the following optimization problem is defined:

$$\begin{aligned} u^{opt}(k) = \quad & \underset{u(k)}{\arg\,\text{minimize}}\, J(u(k)), \\ & \text{subject to}\, g(u(k)), \end{aligned} \tag{13}$$

where $u(k)$ refers to the optimization variables, $g(u(k))$ refers to the constraints, $J(u(k))$ refers to the cost function, and $u^{opt}(k)$ refers to the optimal $u(k)$ that minimizes the value of $J(u(k))$.

Optimization variables $u(k)$ correspond to the SM power references, i.e.,

$$u(k) = [\bar{P}_1^*(k),\, \bar{P}_2^*(k) \cdots \bar{P}_N^*(k)]^T. \tag{14}$$

Constraints $g(u(k))$ correspond to (7)-(9). The cost function $J(u(k))$ is defined as

$$J(u(k)) = \sum_{i=1}^{N} [SoC_{bal}(k+1) - SoC_i(k+1)]^2, \tag{15}$$

where $SoC_i(k+1)$ is given in (12) while $SoC_{bal}(k+1)$ refers to the reference SoC value for all the SMs at $k+1$. At any time instant k, $J(u(k))$ reaches its minimum if and only if SoC_i becomes balanced at $k+1$, i.e.,

$$SoC_i(k+1) = SoC_{bal}(k+1),\, \forall i \in \{1, 2 \cdots N\}, \tag{16}$$

which ensures a fast SoC balancing speed. The derivation of $SoC_{bal}(k+1)$ is given below.

Multiplying both sides of (12) by α_i and adding $SoC_i(k+1)$ yields

$$\sum_{i=1}^{N} \alpha_i SoC_i(k+1) = \sum_{i=1}^{N} \alpha_i [SoC_i(k) + \frac{\bar{P}_i^*}{\alpha_i} T_d]. \tag{17}$$

According to (7), (17) can be rewritten as

$$\sum_{i=1}^{N} \alpha_i SoC_i(k+1) = \sum_{i=1}^{N} \alpha_i SoC_i(k) + \bar{P}_{CBESS}^* T_d. \tag{18}$$

Assuming the SoC balance condition where $SoC_i(k+1) = SoC_{bal}(k+1)$ for any i, then $SoC_{bal}(k+1)$ is derived as

$$SoC_{bal}(k+1) = \frac{\sum_{i=1}^{N} \alpha_i SoC_i(k)}{\sum_{i=1}^{N} \alpha_i} + \frac{\bar{P}_{CBESS}^* T_d}{\sum_{i=1}^{N} \alpha_i}. \tag{19}$$

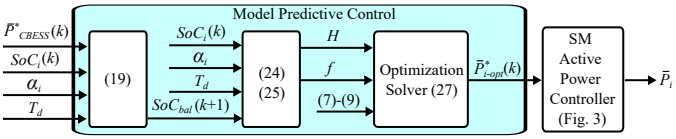

Fig. 4. Developed MPC.

Note that $SoC_i(k+1) = SoC_{bal}(k+1)$ may not be achievable in practice due to the system constraints in (7)-(9). Nevertheless, the reference $SoC_{bal}(k+1)$ is still calculated as in (19), and the MPC will provide the solution that minimizes $J(u(k))$, i.e., minimizes the SoC imbalance at $k+1$. Note that the present SoC reference at k corresponds to

$$SoC_{bal}(k) = \frac{\sum_{i=1}^{N} \alpha_i SoC_i(k)}{\sum_{i=1}^{N} \alpha_i}, \tag{20}$$

which is the present SoC mean value if α_i is similar for all the SMs. Accordingly, (19) can be rewritten as

$$SoC_{bal}(k+1) = SoC_{bal}(k) + \frac{\bar{P}_{CBESS}^* T_d}{\sum_{i=1}^{N} \alpha_i}. \tag{21}$$

Since the optimization variables are the SM active power references $\bar{P}_i^*(k)$, $J(u(k))$ should be rewritten as a function of $\bar{P}_i^*(k)$. Substituting (12) into (15), $J(u(k))$ becomes

$$J(u(k)) = \sum_{i=1}^{N} [SoC_{bal}(k+1) - SoC_i(k) - \frac{T_d}{\alpha_i} \bar{P}_i^*(k)]^2. \tag{22}$$

Alternatively, $J(u(k))$ can be rewritten in the standard quadratic programming (QP) formulation [23]:

$$J(u(k)) = \frac{1}{2} u(k)^T H u(k) + f^T u(k) + ct, \tag{23}$$

where

$$H = 2T_d^2 \begin{bmatrix} \frac{1}{\alpha_1^2} & 0 & \cdots & 0 \\ 0 & \frac{1}{\alpha_2^2} & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & \frac{1}{\alpha_N^2} \end{bmatrix}, \tag{24}$$

$$f = 2T_d \begin{bmatrix} \frac{1}{\alpha_1} SoC_1(k) - \frac{1}{\alpha_1} SoC_{bal}(k+1) \\ \frac{1}{\alpha_2} SoC_2(k) - \frac{1}{\alpha_2} SoC_{bal}(k+1) \\ \vdots \\ \frac{1}{\alpha_N} SoC_N(k) - \frac{1}{\alpha_N} SoC_{bal}(k+1) \end{bmatrix}, \tag{25}$$

$$ct = \sum_{i=1}^{N} [SoC_{bal}(k+1) - SoC_i(k)]^2. \tag{26}$$

Note that ct is independent from $u(k)$ and hence it can be omitted in the optimization problem.

Eventually, the developed MPC scheme corresponds to

$$\begin{aligned} u^{opt}(k) = \quad & \underset{u(k)}{\arg\,\text{minimize}}\, \tfrac{u(k)^T H u(k)}{2} + f^T u(k), \\ & \text{subject to}\, (7)-(9), \end{aligned} \tag{27}$$

which can be solved using a standard QP solver [23], [24]. A flowchart of the MPC is depicted in Fig. 4. Since the control

variables (SoC_i) change slowly, a low execution rate can be chosen to reduce the computational burden associated to the QP solver.

B. Unconstrained Solution of the MPC

To provide further insight into the proposed MPC scheme, this subsection derives and discusses its unconstrained solution.

From (27), the unconstrained solution corresponds to

$$u_{unc}(k) = -H^{-1} f, \tag{28}$$

where H^{-1} always exists as H is positive definite. According to (24) and (25), $u_{unc}(k)$ corresponds to

$$u_{unc}(k) = [\bar{P}^*_{1\text{-unc}}(k),\ \bar{P}^*_{2\text{-unc}}(k) \cdots \bar{P}^*_{N\text{-unc}}(k)]^T, \tag{29}$$

with

$$\bar{P}^*_{i\text{-unc}}(k) \quad = \quad \frac{\alpha_i}{T_d}[SoC_{bal}(k\ +\ 1)\ -\ SoC_i(k)]. \tag{30}$$

Substituting (30) into (12) yields $SoC_i(k+1) = SoC_{bal}(k+1)$, which implies that the developed MPC tends to balance the SoC values within T_d, as a dead-beat control. Note that this solution is for an ideal case where the converter has unlimited capacity (no restriction on power distribution). In practice, if $u_{unc}(k)$ violates the constraints (7)-(9), the power distribution is unattainable and SoC balance cannot be achieved in one step.

Moreover, substituting (21) into (30) yields

$$\bar{P}^*_{i\text{-unc}}(k) = \frac{\alpha_i}{T_d}\Delta SoC_i(k) + \frac{\alpha_i}{\sum_{i=1}^{N}\alpha_i}\bar{P}^*_{CBESS}, \tag{31}$$

with

$$\Delta SoC_i(k) = SoC_{bal}(k) - SoC_i(k). \tag{32}$$

Note that $\Delta SoC_i(k)$ refers to the present SoC imbalance. From (31), $\bar{P}^*_{i\text{-unc}}(k)$ consists of two parts. The first part, ${}^{\alpha_i \Delta SoC_i(k)}/_{T_d}$, eliminates the present SoC imbalance ($\Delta SoC_i(k)$). The second part, ${}^{\alpha_i \bar{P}^*_{CBESS}}/_{\sum_{i=1}^{N}\alpha_i}$, maintains the SoC balance.

C. Simulation Verification

To verify the performance of the developed MPC and compare its performance with the existing methods, simulation results are obtained from a CBESS, where the batteries are directly connected to the SMs, as in Fig. 1(b). Parameters of the CBESS are provided in Table I. Simulation results with the CBESS charging with 110 kW are provided in Fig. 5, where the left column depicts the SoC of the SMs while the right column shows the SM powers.

Fig. 5(a) shows the performance of the proposed MPC. As observed, the SoCs become balanced within 4 s and the SM powers are constrained within the safe range (below 33 kW). Specifically, before the SoC balance, the power of SM1 is saturated to the upper bound ($\bar{P}_1 = 33$ kW) as it has the lowest SoC.

Fig. 5(b) shows the performance of the RBM. The SM powers are also constrained within the safe range but the SoC balancing speed is slower (around 60% slower than the proposed MPC in this case study). Figs. 5(c) and (d) show the performance of the PI- and rule-based methods, which fail to constrain the SM powers within the safe range, as highlighted with red shade. In conclusion, the proposed MPC outperforms the rest of the methods, yielding the fastest SoC balance with consideration of the BESS's safety.

TABLE I
PARAMETERS OF THE SIMULATED AND EXPERIMENTAL CBESS

Parameter	Simulation	Experiment
Number of SMs per arm, N	4	4
SM capacitor voltage, V_C	500 V	100 V
Battery nominal voltage, V_b	500 V	48 V
Battery nominal capacity, Q_{nom}	0.7 Ah	18 Ah
Safe range for SM power, $[\bar{P}_{li}, \bar{P}_{ui}]$	$[-33, 33]$ kW	$[-470, 470]$W
Filter inductance, L	5 mH	7.6 mH
Boost converter inductance, L_b	NA	0.95 mH
Nominal output voltage (rms), V_o	1.1 kV	220 V
Nominal output current (rms), I_{CHB}	100 A	7 A
Nominal output power, S_{nom}	110 kVA	1.54 kVA
Fundamental frequency, f	50 Hz	50 Hz
Carrier frequency, f_C	10 kHz	20 kHz
Sampling rate of the controller, f_{sc}	10 kHz	20 kHz
Execution rate of the MPC, f_{MPC}	20 Hz	20 Hz

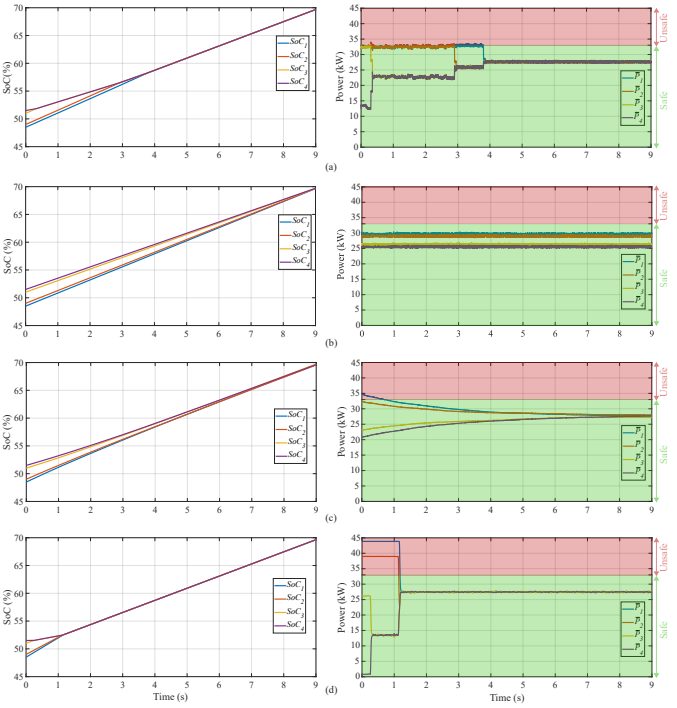

Fig. 5. Simulation results with different SoC balancing methods: (a) Proposed MPC, (b) RBM [7], (c) PI-based method [10], and (d) sorting-based method [18].

IV. Robustness Analysis

According to (19) and (23)-(25), the proposed MPC scheme requires the knowledge of parameter α_i, which is determined according to (6) by the battery capacity (Q_i), battery voltage (V_{bi}), and power conversion efficiency (η_i). In the operation of the CBESS, these parameters can change depending on the operating conditions. The battery capacity slowly declines due to battery degradation [20], the battery voltage changes with the SoC and current [25], and the efficiency varies with the processing power [26]. Although these parameters can be measured/estimated online, estimation errors in the values of α_i, referred to as parametric uncertainties in this paper, are inevitable. This section analyses the steady-state performance of the MPC scheme with parametric uncertainties, and then it corroborates the analytical predictions via simulations.

A. Analytical Steady-State Error

As revealed in Section III, in the steady-state, the SM active power references correspond to the unconstrained solution $\bar{P}^*_{i\text{-unc}}(k)$ in (31) to maintain the SoC balance. If there are estimation errors in the parameters $\{Q_i,\ V_{bi},\ \eta_i\}$, $\bar{P}^*_{i\text{-unc}}(k)$ will be affected according to the propagation error through the control block diagram in Fig. 4, which may undermine the SoC balancing performance.

Let us assume that α_j of the jth SM ($j \in \{1, 2 \cdots N\}$) is estimated as

$$\alpha_j^{'} = \alpha_j + \Delta\alpha_j, \tag{33}$$

where α_j refers to the actual value and $\Delta\alpha_j$ refers to the parametric uncertainty.

Substituting α_j for $\alpha_j^{'}$ in (20), the calculated $SoC_{bal}(k)$ corresponds to

$$SoC_{bal}^{'}(k) = \frac{\sum_{i=1}^{N} \alpha_i SoC_i(k) + \Delta\alpha_j SoC_j(k)}{\sum_{i=1}^{N} \alpha_i + \Delta\alpha_j}. \tag{34}$$

Alternatively, (34) can be rewritten as

$$SoC_{bal}^{'}(k) = SoC_{bal}(k) + \Delta SoC_{bal}(k), \tag{35}$$

where the error due to parametric uncertainty is given by

$$\Delta SoC_{bal}(k) = \frac{-\Delta\alpha_j}{\sum_{i=1}^{N} \alpha_i + \Delta\alpha_j}[\frac{\sum_{i=1}^{N} \alpha_i SoC_i(k)}{\sum_{i=1}^{N} \alpha_i} - SoC_j(k)]. \tag{36}$$

Using (20) and (32), the expression of $\Delta SoC_{bal}(k)$ in (36) can be simplified as

$$\Delta SoC_{bal}(k) = \frac{-\Delta\alpha_j}{\sum_{i=1}^{N} \alpha_i + \Delta\alpha_j} \Delta SoC_j(k). \tag{37}$$

If $\Delta SoC_{bal}(k)$ has some error, the calculated SoC imbalance, $\Delta SoC_j^{'}(k)$, will also be affected. Specifically, substituting $SoC_{bal}(k)$ for $SoC_{bal}^{'}(k)$ in (32), $\Delta SoC_j^{'}(k)$ corresponds to

$$\Delta SoC_j^{'}(k) = \Delta SoC_j(k) + \Delta SoC_{bal}(k). \tag{38}$$

Note that the imbalance error occurs in all the SMs and not only in the jth SM with parametric uncertainty.

With the errors in $SoC_{bal}^{'}(k)$ and $\Delta SoC_j^{'}(k)$, the calculated SM active power references, $\bar{P}_j^{'}(k)$, are accordingly affected. Particularly, substituting α_i for $\alpha_j^{'}$ in (31) and substituting $\Delta SoC_i(k)$ for $\Delta SoC_j^{'}(k)$ in (31), the calculated $\bar{P}_j^{'}(k)$ corresponds to

$$\bar{P}_j^{'}(k) = \bar{P}^*_{j\text{-unc}}(k) + \Delta\bar{P}^*_j(k), \tag{39}$$

where the error due to parametric uncertainty is given by

$$\Delta\bar{P}^*_j(k) = \Delta\alpha_j \frac{\sum_{i=1}^{N} \alpha_i - \alpha_j}{\sum_{i=1}^{N} \alpha_i + \Delta\alpha_j}[\frac{\Delta SoC_j(k)}{T_d} + \frac{\bar{P}^*_{CBESS}}{\sum_{i=1}^{N} \alpha_i}]. \tag{40}$$

If $\Delta\alpha_j = 0$, $\Delta\bar{P}^*_j(k)$ is also equal to zero, and the SoC balance will be achieved with deadbeat response as discussed in Section III. However, if $\Delta\bar{P}^*_j(k) \neq 0$, according to (12) and (32), the SoC values will exhibit some steady-state error. Particularly, substituting (40) into (12), the SoC imbalance of the jth SM corresponds to

$$\Delta SoC_j(k+1) = -\frac{T_d}{\alpha_j} \Delta\bar{P}^*_j(k). \tag{41}$$

Substituting (40) into (41) yields the following recursive sequence

$$\Delta SoC_j(k+1) = \lambda_j \Delta SoC_j(k) - \beta_j, \tag{42}$$

where

$$\lambda_j = -\frac{\Delta\alpha_j}{\alpha_j} \frac{\sum_{i=1}^{N} \alpha_i - \alpha_j}{\sum_{i=1}^{N} \alpha_i + \Delta\alpha_j},$$
$$\beta_j = \frac{\Delta\alpha_j (\sum_{i=1}^{N} \alpha_i - \alpha_j)}{(\sum_{i=1}^{N} \alpha_i + \Delta\alpha_j)(\sum_{i=1}^{N} \alpha_i)\alpha_j} \bar{P}^*_{CBESS} T_d. \tag{43}$$

If $|\lambda_j| < 1$, $\Delta SoC_j(k)$ will converge to ${}^{\beta_j}/_{(\lambda_j - 1)}$ [27], i.e.,

$$\Delta SoC_j \to \frac{\beta_j}{\lambda_j - 1} = -\frac{\sum_{i=1}^{N} \alpha_i - \alpha_j}{(\sum_{i=1}^{N} \alpha_i)^2} \frac{\Delta\alpha_j}{\alpha_j + \Delta\alpha_j} \bar{P}^*_{CBESS} T_d. \tag{44}$$

Equation (44) reveals the steady-state imbalance of the jth SM (ΔSoC_j) due to $\Delta\alpha_j$. However, $\Delta\alpha_j$ also affects ΔSoC_i ($i \neq j$) of the other SMs and hence their calculated active power reference $\bar{P}_i^{'}(k)$. With a similar analysis, when $|\lambda_j| < 1$, ΔSoC_i will converge to

$$\Delta SoC_i \to \frac{\alpha_j}{(\sum_{i=1}^{N} \alpha_i)^2} \frac{\Delta\alpha_j}{\alpha_j + \Delta\alpha_j} \bar{P}^*_{CBESS} T_d, \forall i \neq j. \tag{45}$$

According to (44) and (45), if $|\lambda_j| < 1$, the SoC imbalance among the SMs (ΔSoC_j and ΔSoC_i) will converge to certain values that are proportional to the parametric uncertainties ($\Delta\alpha_j$). Since $\Delta\alpha_j$ is typically small compared to α_j, $|\lambda_j| < 1$ in the normal condition, and the converged values of ΔSoC_j and ΔSoC_i are relatively small, as demonstrated in Subsections IV-B and V-A.

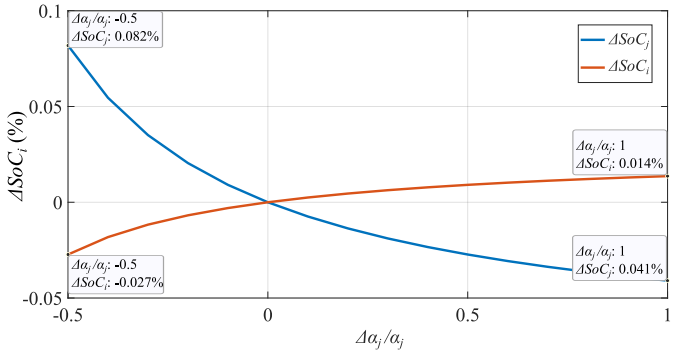

Fig. 6. $\Delta SoC_j(k)$ and $\Delta SoC_i(k)$ $(i \neq j)$ due to various $\Delta\alpha_j$.

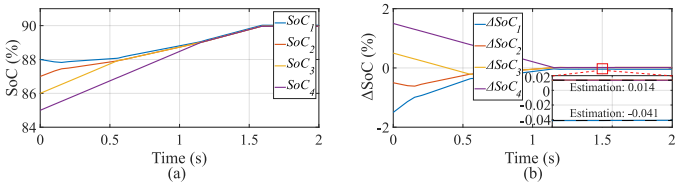

Fig. 7. Simulation results with the proposed MPC ($\Delta\alpha_1 = \alpha_1$): (a) SoC_i, and (b) ΔSoC_i.

B. Simulation Verification

Considering the CBESS with the parameters provided in Table I, the steady-state values of $\Delta SoC_j(k)$ and $\Delta SoC_i(k)$ $(i \neq j)$ due to $\Delta\alpha_j$ are displayed in Fig. 6. As observed, when $\Delta\alpha_j$ is between $[-0.5\alpha_j, \alpha_j]$, which is a relatively wide range, the steady-state values of $\Delta SoC_j(k)$ and $\Delta SoC_i(k)$ are within [-0.04%,0.08%]. Hence, the proposed MPC scheme has good robustness against parametric uncertainties.

As an example, simulation results are obtained assuming the estimated Q_1 is twice its actual value ($\Delta\alpha_1 = \alpha_1$), and the results are provided in Fig. 7. In the simulation, the CBESS is first charging with the nominal power and the charging ceases if the SoC of any SM reaches 90% for battery protection. According to Fig. 7(a), despite the large error in Q_1, the SoC values are closely balanced at around $t = 1.2$ s. According to Fig. 7(b), the steady-state SoC imbalance is negligible and match with the estimated values in Fig. 6. The results verify the accuracy of the analysis in this section.

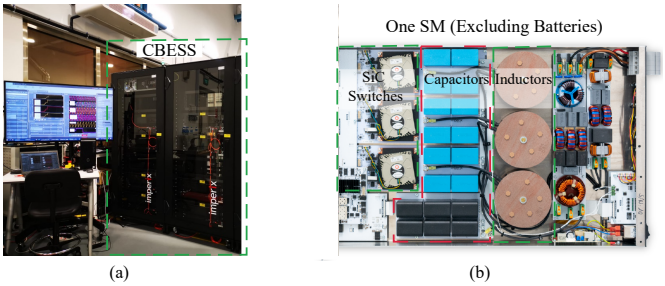

Fig. 8. Pictures of the experimental setup: (a) CBESS and (b) SM (excluding batteries).

TABLE II
BATTERY CAPACITIES IN THE EXPERIMENTS

	SM1	SM2	SM3	SM4
Capacity	$1.04Q_{nom}$	$1.01Q_{nom}$	$0.97Q_{nom}$	$0.94Q_{nom}$

V. EXPERIMENTAL VERIFICATION

To verify the effectiveness of the proposed MPC, experiments are conducted on a CBESS as shown in Fig. 8. Each SM is integrated with an Eaton 9SX extended lead-acid battery module via a boost converter (Fig. 1(c)). Each battery module consists of eight lead-acid cells, whose nominal voltage is 12 V and whose nominal capacity is 9 Ah. Inside the module, four cells are connected in series as a string and two strings are connected in parallel. The control of the boost converter is similar to that in [22], and a proportional resonant controller is used to regulate the output current of the CHB converter [28]. Parameters of the CBESS are provided in Table I. The batteries in different SMs present slightly different capacity values, as provided in Table II.

Experiments are conducted with both the developed MPC and the RBM [7]. Particularly, the execution rate of the MPC (f_{MPC}) is chosen as 20 Hz, while the reference SoC^* of the RBM is chosen as 30% when $\bar{P}_{CBESS} > 0$ and 20% when $\bar{P}_{CBESS} < 0$. The experiments are conducted in two different scenarios, viz., with and without parametric uncertainties.

A. Experiment I: With Parametric Uncertainties

In this experiment, the CBESS is charging with 1.54 kW under unity power factor. Nominal system parameters are considered within the control, specifically, $Q_i = 18$ Ah, $V_{bi} = 48$ V, and $\eta_i = 0.95$ for all the SMs. In practice, these parameters can change according to the operating conditions, hence this experiment is subjected to a certain degree of parametric uncertainty, namely, $\Delta\alpha_i \in [-0.15\alpha_i, 0.15\alpha_i]$.

In Fig. 9, the left and right columns depict the experimental results with the MPC and the RBM, respectively. Fig. 9(a) provides the SM active powers, which are constrained within the safe range $[-470, 470]$ W. The battery currents of the SMs are depicted in Fig. 9(b). Figs. 9(c) and (d) provide the measured battery voltages and estimated efficiencies (η_i), which are assumed as 48 V and 0.95 within the control for the calculation of SM active power references. Figs. 9(e) and (f) depict the SoC values and imbalance (ΔSoC_i) of the SMs, respectively. Although the initial SoC values are unbalanced, the proposed MPC balance the SoC values within 120 s despite the parametric uncertainties. However, with the RBM, the SoC imbalance becomes even larger after 150 s. The experimental results verify that the proposed MPC has higher robustness than the RBM.

Fig. 10 compares the computational complexity of the RBM (Fig. 2) and the proposed MPC (Fig. 4). The horizontal axis indicates the execution frequency of the RBM/MPC, while the vertical axis refers to the percentage of processors (two ARM Cortex A9@1GHz) used by the control platform as the complexity indicator. As observed, the proposed MPC

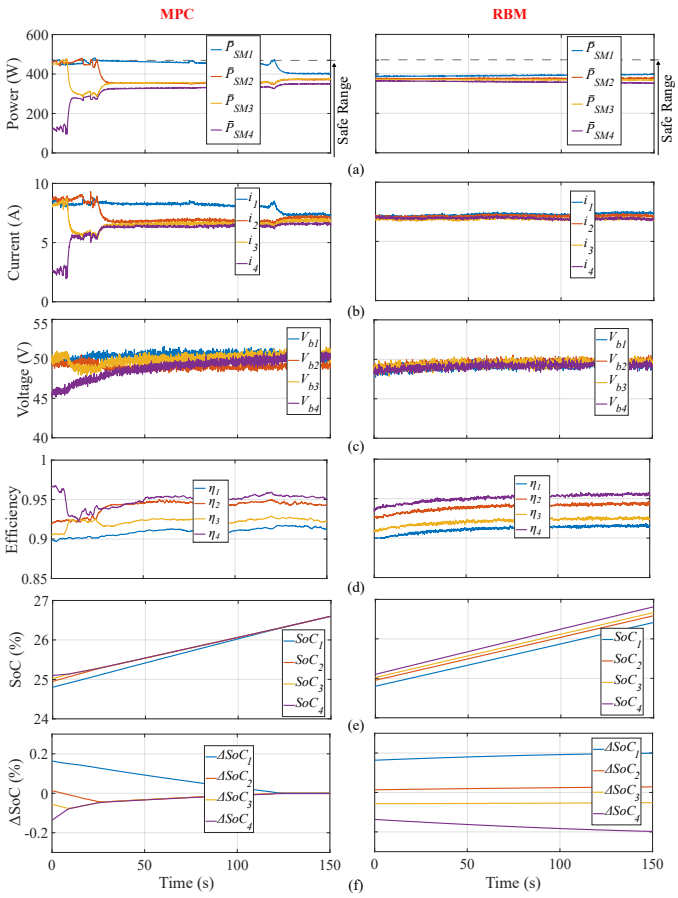

Fig. 9. *Experiment I* (left column: MPC, right column: RBM): (a) SM active power, (b) battery current, (c) battery voltage, (d) efficiency (η_i), (e) SoC values, and (f) SoC imbalance (ΔSoC_i).

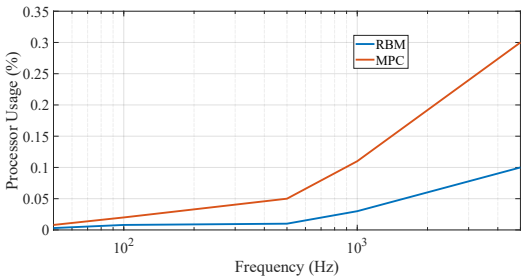

Fig. 10. Computational complexity of the MPC and RBM.

requires a higher usage of the processor than the RBM. Nonetheless, the difference reduces significantly with a lower execution frequency and this difference is within 0.01% when the frequency is below 100Hz. As mentioned before, the MPC/RBM can perform well at a low frequency, for instance, 20 Hz in this experiment. Moreover, in this experiment, the processor usage of the overall control scheme (phase-locked loop, current control, moving average filters, etc. [22]) at 20 kHz is around 32%. Hence, the proposed MPC does not impose a significant burden on the processor, especially when it is executed at a low frequency.

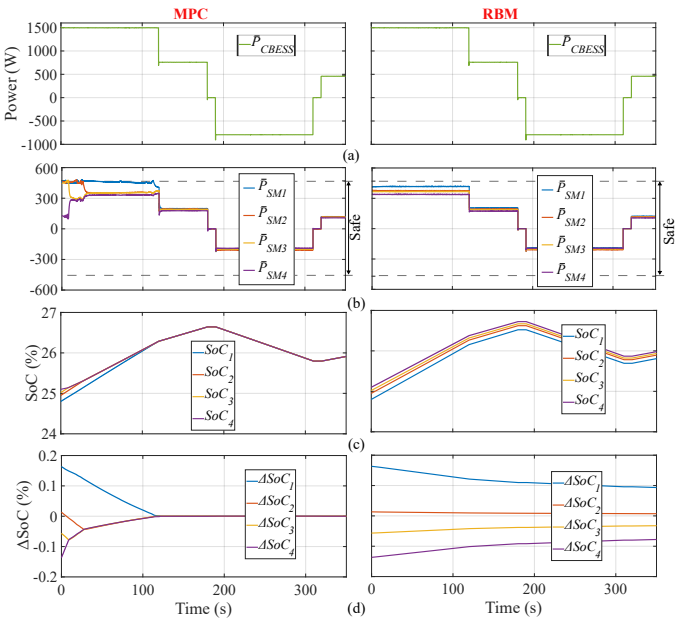

Fig. 11. *Experiment II* (left column: MPC, right column: RBM): (a) Phase arm power, (b) SM active power, (c) SoC values, and (d) SoC imbalance (ΔSoC_i).

B. Experiment II: Without Parametric Uncertainties

In this experiment, the CBESS is charging and discharging with different power values under unity power factor. Moreover, unlike in *Experiment I*, the actual values of Q_i (as in Table II) are used in the control, and the values of V_{bi} and η_i are measured and updated online, to minimize parametric uncertainty.

In Fig. 11, the left and right columns depict the experimental results with the MPC and the RBM, respectively. Figs. 11(a) and (b) provide the active power of the phase arm and of the individual SMs, respectively. Figs. 11(c) and (d) depict the SoC values and the SoC imbalance (ΔSoC_i) of the SMs, respectively. As seen in the left column, SM1 has the lowest SoC value initially and thus its power is saturated to the maximum value (470W) from t =0 s to t =120 s, indicating that the MPC can optimize the SM active powers and balance the SoC values at the fastest speed. Consequently, the SoC values become and remain balanced after t =120 s. However, with the RBM, the active power of SM1 is not saturated to the maximum value, yielding a slower SoC balancing speed. As observed, the SoCs are not fully balanced after 350 s. This slow SoC balancing speed is because the RBM tends to balance the SoCs when they all reach the reference value, namely 30% when $\bar{P}_{CBESS} > 0$ and 20% when $\bar{P}_{CBESS} < 0$. If a better (or worse) reference is given, the SoC balancing speed will be faster (or slower). Theoretically speaking, with an optimal reference, the RBM can achieve a rapid SoC balancing speed similar to the proposed MPC. However, it remains an open question to choose the optimal reference, which depends on the initial SoC imbalance, the active power of the phase arm, battery capacities, etc. This can be a future direction to improve the RBM.

VI. Conclusion

A model predictive control scheme has been developed for the inter-submodule state of charge balancing in battery energy storage systems based on the cascased H-bridge converter. Compared to the existing methods, the proposed control scheme optimizes the active power distribution among the submodules, hence it balances the state of charge quickly and constrains the submodule active powers within a prescribed safe range. Moreover, the proposed control scheme has good robustness against parametric uncertainties. Simulation and experimental results demonstrated the good performance of the proposed scheme.

References

[1] IEA, "Grid-scale storage (tracking report)," Sept. 2022. [Online].Available:https://www.iea.org/reports/grid-scale-storage.

[2] G. G. Farivar, W. Manalastas, H. D. Tafti, S. Ceballos, A. Sanchez-Ruiz, E. C. Lovell, G. Konstantinou, C. D. Townsend, M. Srinivasan, and J. Pou, "Grid-connected energy storage systems: State-of-the-art and emerging technologies," *Proc. of the IEEE*, pp. 1–24, Jun. 2022. Early access, doi:10.1109/JPROC.2022.3183289.

[3] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, Jan. 2015.

[4] T. Noh, J. Ahn, H. M. Ahn, and B. K. Lee, "Optimal design of hybrid battery energy storage system for minimizing the number of batteries with high efficiency control algorithm based on fuzzy logic," in *Proc. IEEE Appli. Power Electron. Conf. and Expo.*, pp. 1630–1634, Mar. 2018.

[5] I. Mathews, B. Xu, W. He, V. Barreto, T. Buonassisi, and I. M. Peters, "Technoeconomic model of second-life batteries for utility-scale solar considering calendar and cycle aging," *Appli. Energy*, vol. 269, pp. 115–127, Jul. 2020.

[6] F. Eroglu, M. Kurtoglu, A. Eren, and A. M. Vural, "A novel adaptive state-of-charge balancing control scheme for cascaded H-bridge multilevel converter based battery storage systems," *ISA Trans.*, Oct. 2022.

[7] G. Liang, E. R. Rodriguez, G. G. Farivar, S. Ceballos, C. D. Townsend, N. B. Y. Gorla, and J. Pou, "A constrained inter-submodule state-of-charge balancing method for battery energy storage systems based on the cascaded H-bridge converter," *IEEE Trans. Power Electron.*, Apr., 2022. Early Access.

[8] G. Liang, G. G. Farivar, S. Ceballos, H. Dehghani Tafti, J. Pou, C. Townsend, and G. Konstantinou, "Unbalanced active power distribution of cascaded multilevel converter-based battery energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 13022 – 13032, Dec. 2021.

[9] F. Eroglu and A. M. Vural, "A critical review on state-of-charge balancing methods in multilevel converter based battery storage systems," in *Proc. 4th Global Power, Energy, Communi. Conf.*, pp. 14–19, IEEE, Jun. 2022.

[10] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (SoC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[11] M. Vasiladiotis and A. Rufer, "Balancing control actions for cascaded H-bridge converters with integrated battery energy storage," in *Proc. of Euro. Conf. Power Electron.Appli.*, pp. 1–10, IEEE, Oct. 2013.

[12] K. Kandasamy, M. Vilathgamuwa, and K. J. Tseng, "Inter-module state-of-charge balancing and fault-tolerant operation of cascaded H-bridge converter using multi-dimensional modulation for electric vehicle application," *IET Power Electron.*, vol. 8, no. 10, pp. 1912–1919, Oct. 2015.

[13] H. Liu, Q. Xiao, H. Yu, S. Tian, W. Wang, C. Tian, Y. Mu, and H. Jia, "An improved multilayer state of charge balancing control strategy for the cascaded H-bridge-based battery energy storage system," in *Proc. IEEE 4th Int. Conf. Smart Power Inet. Energy Syst.*, pp. 1939–1944, Dec. 2022.

[14] Z. Xia and J. A. Abu Qahouq, "State-of-charge balancing of lithium-ion batteries with state-of-health awareness capability," *IEEE Trans. Ind. Appl.*, vol. 57, no. 1, pp. 673–684, Feb. 2021.

[15] G. Liang, E. Rodriguez, G. G. Farivar, G. N. B. Yadav, N. Beniwal, J. Pou, and G. Konstantinou, "A comparison of PI-based and sorting-based state of charge balancing methods in cascaded H-bridge converters," in *Proc. IEEE ECCE*, pp. 1–7, Nov. 2022.

[16] C. Young, N. Chu, L. Chen, Y. Hsiao, and C. Li, "A single-phase multilevel inverter with battery balancing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1972–1978, Jul. 2012.

[17] E. Chatzinikolaou and D. J. Rogers, "Cell SoC balancing using a cascaded full-bridge multilevel converter in battery energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5394–5402, May 2016.

[18] Q. Yuan, F. Yang, A. Li, and T. Ma, "A novel hybrid control strategy for the energy storage modular multilevel converters," *IEEE Access*, vol. 9, pp. 59466–59474, Apr. 2021.

[19] F. Eroglu, M. Kurtoglu, A. Eren, and A. M. Vural, "Level-shifted pulse width modulation based battery state-of-charge balancing method for single-phase cascaded H-bridge multilevel converters," in *Proc. Int. Conf. Electr. Electron. Eng.*, pp. 560–564, Nov. 2021.

[20] B. Jiang, H. Dai, X. Wei, and T. Xu, "Joint estimation of lithium-ion battery state of charge and capacity within an adaptive variable multi-timescale framework considering current measurement offset," *Applied Energy*, vol. 253, p. 113619, Nov. 2019.

[21] G. Liang, H. Dehghani Tafti, G. G. Farivar, J. Pou, C. D. Townsend, G. Konstantinou, and S. Ceballos, "Analytical derivation of inter-submodule active power disparity limits in modular multilevel converter-based battery energy storage systems," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2864–2874, Mar. 2020.

[22] G. Liang, H. Dehghani Tafti, G. G. Farivar, J. Pou, C. Townsend, G. Konstantinou, and S. Ceballos, "Effect of capacitor voltage ripples on submodule active power control limits of cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5952–5961, Jun. 2021.

[23] B. Stellato, G. Banjac, P. Goulart, A. Bemporad, and S. Boyd, "Osqp: An operator splitting solver for quadratic programs," *Math. Program. Comput.*, vol. 12, no. 4, pp. 637–672, Feb. 2020.

[24] E. R. Rodriguez, R. Leyva, C. D. Townsend, G. G. Farivar, H. D. Tafti, and J. Pou, "Constrained control of low-capacitance delta cascaded H-bridge statcoms: A model predictive control approach," *IEEE Trans. Power Electron.*, Jun. 2021.

[25] M. Coleman, C. K. Lee, C. Zhu, and W. G. Hurley, "State-of-charge determination from emf voltage estimation: Using impedance, terminal voltage, and current for lead-acid and lithium-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2550–2557, Aug. 2007.

[26] G. Wang, G. Konstantinou, C. D. Townsend, J. Pou, S. Vazquez, G. D. Demetriades, and V. G. Agelidis, "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 1778–1790, Jul. 2016.

[27] E. Gaughan, *Introduction to analysis*, vol. 1. American Mathematical Soc., Jan. 2010.

[28] A. Kuperman, "Proportional-resonant current controllers design based on desired transient performance," *IEEE Trans.Power Electroni.*, vol. 30, pp. 5341–5345, Oct. 2015.

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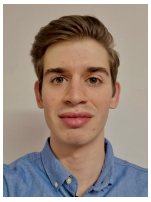

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