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RESEARCH ARTICLE

Modeling and Control of a Three-Phase Interleaved Buck Converter as a Battery Charger

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ABSTRACT In this paper, a control design methodology is proposed for the implementation of a three-phase interleaved buck converter as a battery charger. The control strategy consists of a multiple-loop controller in cascade configuration to implement the constant-current constant-voltage (CC-CV) protocol for the fast charging of an electric vehicle (EV) battery. To compensate for the inherent asymmetric distribution of the current between the phases, the first control loop (inner loop) is dedicated to implement the democratic current sharing technique, while the two outer loops constitute a seamless controller, which allows a soft transition from CC mode to CV mode when charging the battery. The controllers are designed using the root locus method and conventional rules for cascade controllers. The design methodology is validated and tested by numerical simulations of the switched model system implemented in PSIM© software. The obtained results put in evidence a robust performance in front of input voltage and load variations, failure conditions and other parametric uncertainties. A 1.5 kW experimental prototype is implemented to charge a battery of 48 V from a 100 V DC input voltage and to validate the theoretical predictions and the simulation results. The proposal opens the way for subsequent research in ultrafast charging of batteries.

INDEX TERMS Battery charger, interleaved buck converter, cascade control, fast charging.

NOMENCLATURE

PARAMETERS

C	Output capacitance.
C_{s1}, C_{s2}, C_{s3}	Parasitic capacitances.
d	Average duty cycle.
D_1, D_2, D_3	Diodes in each phase.
ΔI_L	Peak-to-peak inductor current ripple.
Δv_o	Peak-to-peak output voltage ripple.
ξ	Damping ratio.
f_s	Switching frequency.
K_p	Proportional gain.
K_{P3}	Proportional gain of inner loop PI .
L	Common inductance.
L_1, L_2, L_3	Phase inductances.
Mp	Specified percent overshoot.
Q	Battery capacitance.
R_b	Battery resistance.
R_{L1}, R_{L2}, R_{L3}	Parasitic resistances.
$S_1, S_2 S_3$	MOSFETs in each phase.
SoC	Battery instantaneous state of charge.
SoC_0	Battery initial state of charge.

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τ_i	Time constant.
τ_{i3}	Time constant of inner loop PI.
t_s	Specified settling time.
ω_n	Natural frequency.

VARIABLES

G_{cl-v}	Voltage closed loop transfer function.
G_{di}	Control to inductor current transfer function.
G_{dv}	Control to output voltage transfer function.
G_{PI_2}	Output voltage loop PI transfer function.
G_{PI_1}	Outer loop PI transfer function.
G_{PI_3}	Inner loop PI transfer function.
G_v	Plant transfer function for voltage loop.
I_{bat}	Battery current.
I_{CC}	Desired battery charging current.
i_{L_i}	Phase inductor current.
$\widetilde{I}_{ref}$	Current reference for inductor current loop.
$u_1,\ u_2, u_3$	Control signal of each MOSFET.
v_{bat}	Constant battery voltage.
$\widetilde{V}_{com}$	Saturated output of outer loop PI.
$\widetilde{V}_{CV}$	Desired output voltage.
V_{float}	Desired battery charging voltage.
v_o	Output voltage.
V_{oc}	Open-circuit voltage-controlled source.

ACRONYMS

AC	Alternating Current.
CAN	Controller Area Network.
CC	Constant Current.
CCM	Continuous Conduction Mode.
CP	Constant Power.
CV	Constant Voltage.
DC	Direct Current.
EV	Electric Vehicle.
IC	Integrated Circuit.
KCL	Kirchhoff Current Law.
KVL	Kirchhoff Voltage Law.
LTO	Lithium-Titanium-Oxide.
LUT	Look Up Table.
MSCC	Multi-step Constant Current.
MV	Medium Voltage.
PCB	Printed Circuit Board.
PI	Proportional Integral controller.
PNGV	New Generation of Vehicle.
PWM	Pulse Width Modulation.
SCADA	Supervisory Control and Data Acquisition.
SISO	Single Input Single Output.
SoC	State of Charge.
SRC	Sinusoidal Ripple Current.
SST	Solid State Transformer.

I. INTRODUCTION

Environmental awareness and concerns related to the increase in carbon emissions due to the use of conventional internal combustion engine vehicles have led to a high interest toward the adoption of Electric Vehicle (EV) use during recent years. As a result, the EVs sales is breaking records and as a consequence their charging infrastructures are increasingly expanding all over the world. Both industry and academia have been pushed therefore toward EV charging stations research and development. However, with the current technology, the charging process of EVs batteries takes several hours, and slow charging methods are not satisfying the entire needs of drivers, particularly as medium and long-distance trips are concerned. As a result, the need to reduce charging times has boosted the development of fast and ultra-fast charging technologies, aiming to decrease the charging time for more widespread EV adoption. The necessity of ultrafast charging infrastructures to reduce the charging time of EV batteries has introduced the trend of upscaling the nominal power of EV chargers. In this context, efficient DC-DC switching converters with high output power and wide output voltage range are required. A way to increase the output power is the parallel connection of DC-DC switching converters. When paralleling multiple DC-DC switching converters, the amount of power that could be handled is higher compared to a single DC-DC converter topology, which makes the modular structure more suitable for the ultrafast charging of EV batteries. Other advantages are higher power density, better thermal management and higher efficiency [1]. In addition, by adding an appropriate control strategy, that exhibits resilience to uncertainties prioritizing robustness and reliability, a wide range of output voltages will be achieved. These are key advantages for the future expansion of the ultrafast EV charging infrastructure around the world allowing EV users to contribute in the reduction of the carbon emissions. Moreover, in stations with a single charging point and galvanic isolation within the electrical architecture, a non-isolated converter can be used as the interface between the DC bus and the EV battery. This converter must be unidirectional as it is mainly devoted to the charging of EV batteries [2]. Interleaved operation in the output stage of an off-board EV battery charger has been the subject of several works. A recent paper [3] has studied the simulation of the interleaved operation of a 36-phase buck converter that handles a power of 350 kW for ultrafast EV battery charging. The objective was to charge an 800 V battery from a 1500 V DC bus in less than 10 min. It was shown that a high range of power, reduced ripple in both output current and output voltage, and better performance could be achieved in a real implementation. In the same context, the modeling and characterization of N-phase interleaved buck converter were addressed in [4], where a stability comparison between a single buck converter, two-phase and three-phase interleaved buck converters was carried out. A first conclusion in that paper was that the three-phase interleaved buck converter is more stable than a single-phase buck converter when parasitic elements are taken into account. Furthermore, the three-phase interleaved buck converter exhibits less conductive losses than a single buck converter. However, the analysis has considered a resistive load in the modeling process and

a rheostat in experiments but has not addressed the charge of an actual battery. In another work [5], the hardware implementation of a two-phase interleaved synchronous buck converter for Li-Ion battery charging has been discussed, including a closed-loop control algorithm implemented on a microcontroller. This work has come to the conclusion that the interleaved operation of the DC-DC converter provides smoother output voltage and improved charging efficiency. However, no information related to the distribution of the current when considering the interleaved operation has been provided. The efficiency of the energy transference of a similar structure has also been reported in [6], where the phases of a three-phase interleaved buck converter are activated according to the state of charge (SoC) of the battery, predicting by Matlab simulation a 98% efficiency in the fast-charging region. This procedure has been extended to a buck-boost converter that operates in buck and boost modes in the charging and discharging process of the battery respectively [7].

On the other hand, several strategies for the charging of batteries have been reported. The multi-step constant current (MSCC) charging method [8], pulse current [9], sinusoidal ripple current (SRC) [10] and the CC-CV charging protocol [11] have been analyzed to reduce the charging time, extend the life cycle of the battery and provide high-quality high-efficiency charging process. Moreover, the modeling of the battery is also important in the assessment of the performance of the battery charger during the charging process. Three common equivalent circuit models can be considered, i.e. the internal resistance model, the Thevenin model, and the Partnership for a New Generation of Vehicle (PNGV) model, which adds battery capacitance on the basis of the Thevenin model. The performance and applicability of these three models, under various working conditions of lithium-ion batteries are investigated in [12].

This paper focuses on the modular connection of DC-DC power units based on interleaved buck converters for the fast charging of EV batteries. The first objective is to obtain a simple model for the three-phase interleaved buck converter considering ideal conditions in order to systematically design the control for a battery charger based on this converter. A second objective is to design a controller that can regulate the inductor current of the three phases taking into account the effect of interleaving, and simultaneously perform the control for the charging of the battery following a specific protocol. The proposed control strategy uses pulse width modulation (PWM), and a three -loop cascade architecture. The first control loop (inner loop) regulates the inductor currents and implements the democratic current sharing technique in order to solve the problem of current unbalance between the different phases. This is achieved by means of a proportional-integral (PI) controller in each phase sharing the same reference that is provided by the voltage control loop. The two outer loops implement the CC-CV charging protocol, with an inner loop regulating the output voltage and an outer loop controlling the battery current with a saturation block that limits the contribution of the battery current controller. The transition from the CC phase to the CV phase is performed in a seamless way when the output voltage reaches the desired value. The parameters of the controller are designed using the root locus method taking into account conventional rules related to multiple-loop cascade schemes. The validation of the modeling and control of the three-phase interleaved buck converter-based battery charger is performed in simulation using PSIM© software and in laboratory experiments considering a reduced scale of power. Robustness against disturbances in the input voltage and the load, and parametric uncertainty is assessed in controlled conditions as well as a complete charging cycle with a real battery. Perfect agreement with the theoretical predictions has been obtained.

The main contributions of this paper are summarized below:

- A simplified continuous-time modeling for the interleaved operation of buck converters feeding a battery type load.
- A control strategy for democratic current sharing in the system.
- A multi-loop control approach to implement the CC-CV battery charging protocol with a seamless transition between CC and CV modes.

The rest of the paper is organized as follows. Section II is devoted to the description, modeling and design of a three-phase interleaved buck converter. The description of both battery models and CC-CV charging protocol is presented in the same section. The three-loop control strategy is addressed in Section III, where the design methodology is presented and the parameters of the three controllers are obtained. A first proof of concept in a 1.5 kW battery charger design is illustrated in Section IV by simulating the system switched model by means of PSIM© software. Both the steady-state and the transient responses of the system are described. In Section V, an experimental laboratory prototype is presented and the obtained experimental results are discussed validating the theoretical predictions and the numerical simulations. Finally, the conclusions of the work and future perspectives are given in Section VI.

II. DESCRIPTION, MODELING AND CONVERTER DESIGN

A. CIRCUIT DESCRIPTION

The proposed battery charger is based on non-isolated unidirectional DC-DC converters in parallel connection. It consists of three buck converters in interleaved operation, sharing the same DC input voltage v_{in} and the output load consisting of a battery. As depicted in Fig. 1, the circuit is composed of three controlled MOSFETs S_1, S_2 and S_3, three diodes D_1, D_2 and D_3, three inductors with inductances L_1, L_2 *and* L_3, and a common filter capacitor with capacitance C. The MOSFETs are controlled by three distinct control signals u_1, u_2 and u_3, with a 120° phase-shift between them to enforce symmetric interleaved operation.

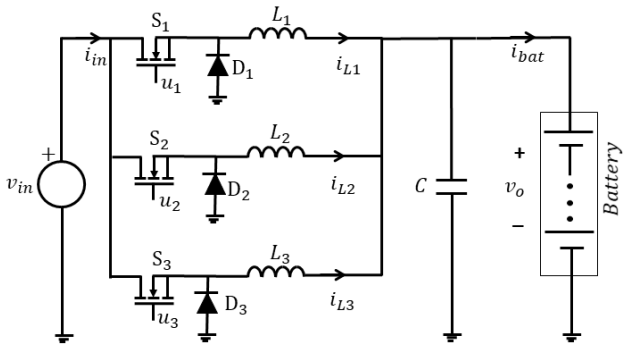

FIGURE 1. Parallel connection of three buck converters sharing the sameinput source and output load.

B. BATTERY MODELLING

Considering that the battery model describes the relationship between voltage, current, state of charge (SoC) and other factors that have effect in the device performance under normal operating conditions, it is important to well define the model. Thus, in a first approach, a basic battery model has been considered in order to facilitate the analytical study. The corresponding circuit diagram of this model is illustrated in Fig. 2-a, where the battery is represented by a voltage source v_{bat} connected in series with a resistance R_b. In order to assess the performance of the system following the charging protocol, the model uses an open-circuit voltage-controlled voltage source V_{oc} in series with the resistance R_b that represents the internal resistance of the battery as illustrated in Fig. 2-b.

The voltage V_{oc} is controlled by the SoC according to a look up table (LUT) defining the dependence of the open-circuit voltage V_{oc} in terms of the SoC. This dependence is illustrated in Fig. 2-c. The SoC of the battery has been obtained using the Coulomb counting method, also known as Ampere-Hour Integral method defined in equation (1) [13].

$$SoC = SoC_0 - \frac{1}{Q}\int I_{bat}\,dt \tag{1}$$

where SoC and SoC_0 represent the instantaneous SoC and the initial SoC of the battery respectively, Q indicates the rated battery capacity and I_{bat} represents the battery current.

C. MODELING OF THE POWER CONVERTER

The mathematical model of the three-phase interleaved buck converter is obtained by applying KVL and KCL to the circuit depicted in Fig. 1 where parameters and variables of the different phases are identified by the index $i = \{1, 2, 3\}$. During the ON state of each phase, the following current equation is obtained:

$$\frac{di_{L_i}}{dt} = \frac{v_{in}}{L_i} - \frac{v_o}{L_i} \tag{2}$$

During the OFF state of each phase, the current equation is as follows:

$$\frac{di_{L_i}}{dt} = -\frac{v_o}{L_i} \tag{3}$$

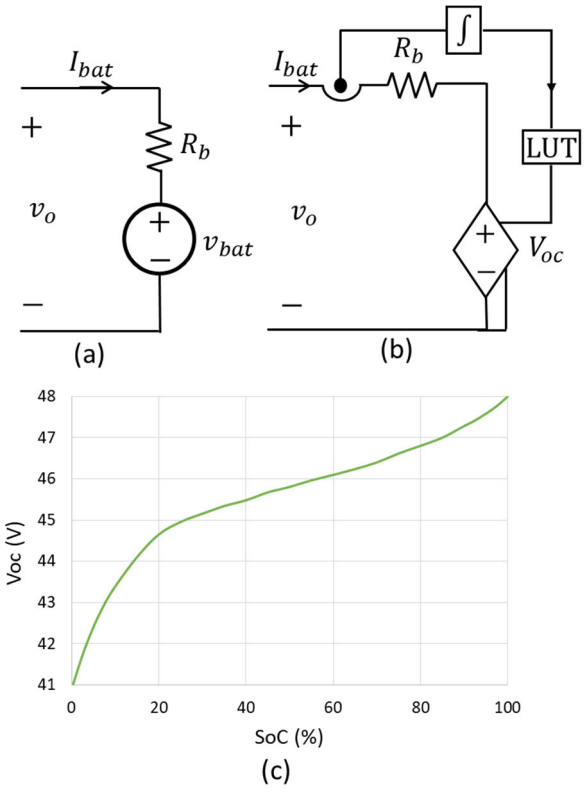

FIGURE 2. Battery model. a) simple battery model. b) equivalent circuitmodel. c) open-circuit voltage dependence on the battery SoC.

For both ON and OFF states, the voltage equation is as follows:

$$\frac{dv_o}{dt} = \frac{i_{L_1} + i_{L_2} + i_{L_3}}{C} - \frac{v_o}{R_b C} + \frac{v_{bat}}{R_b C} \tag{4}$$

By using the binary control signals u_1, u_2 and u_3, the ON-state and OFF-state equations can be compacted together hence obtaining the following switched model.

$$\begin{aligned}
\frac{di_{L_1}}{dt} &= \frac{v_{in}}{L_1}u_1 - \frac{v_o}{L_1} \\
\frac{di_{L_2}}{dt} &= \frac{v_{in}}{L_2}u_2 - \frac{v_o}{L_2} \\
\frac{di_{L_3}}{dt} &= \frac{v_{in}}{L_3}u_3 - \frac{v_o}{L_3} \\
\frac{dv_o}{dt} &= \frac{i_{L_1} + i_{L_2} + i_{L_3}}{C} - \frac{v_o}{R_b C} + \frac{v_{bat}}{R_b C}
\end{aligned} \tag{5}$$

$u_i = 1$ during ON state and $u_i = 0$ during OFF state.

D. AVERAGE AND SMALL SIGNAL MODELS

To design the controller, the first step is to obtain the average nonlinear small-signal models. In order to simplify the analytical development, three assumptions are considered. First, the passive components and semiconductors of the circuit are all considered ideal. The second assumption is related to the inductances of the circuit, where an identical value is assumed for the three phases ($L_1 = L_2 = L_3 = L$).

Finally, the voltage source v_{bat} of the battery model is considered constant for the controller design but varying according to the SoC for numerical simulations. The average model is derived by replacing the control variables u_1, u_2 and u_3 in (5) by their common duty cycle d hence obtaining the following equations:

$$\frac{di_L}{dt} = \frac{v_{in}}{L}d - \frac{v_o}{L} \tag{6}$$

$$\frac{dv_o}{dt} = \frac{3i_L}{C} - \frac{v_o}{R_bC} + \frac{v_{bat}}{R_bC} \tag{7}$$

By perturbing the state variables in (6) and (7), linearizing in the vicinity of the operating point and applying the Laplace transform, the following small signal model of the system is obtained:

$$\widetilde{V}_o(s) = G_{dv}(s)\widetilde{d}(s) + G_{iv}(s)\,\widetilde{V}_{in}(s) + G_{bv}(s)\widetilde{V}_{bat}(s) \tag{8}$$

$$\widetilde{I}_L(s) = G_{di}(s)\widetilde{d}(s) + G_{ii}(s)\,\widetilde{V}_{in}(s) + G_{bi}(s)\widetilde{V}_{bat}(s) \tag{9}$$

where $G_{dv}(s)$, $G_{iv}(s)$, $G_{bv}(s)$, $G_{di}(s)$, $G_{ii}(s)$, $G_{bi}(s)$ are the different transfers functions of the system. In particular, the transfer function from control to output voltage $G_{dv}(s) = \widetilde{V}_o(s)/\widetilde{d}(s)$ and the transfer function from control to inductor current $G_{di}(s) = \widetilde{I}_L(s)/\widetilde{d}(s)$ can be expressed as follows:

$$G_{dv}(s) = \frac{\widetilde{V}_o(s)}{\widetilde{d}(s)} = \frac{1}{LC}\frac{3V_{in}}{s^2 + \frac{1}{R_bC}s + \frac{3}{LC}} \tag{10}$$

$$G_{di}(s) = \frac{\widetilde{I}_L(s)}{\widetilde{d}(s)} = \frac{V_{in}}{L}\frac{\left(s + \frac{1}{R_bC}\right)}{s^2 + \frac{1}{R_bC}s + \frac{3}{LC}} \tag{11}$$

The other transfer functions are expressed below

$$G_{iv}(s) = \frac{1}{LC}\frac{3D}{s^2 + \frac{1}{R_bC}s + \frac{3}{LC}} \tag{12}$$

$$G_{bv}(s) = \frac{1}{LC}\frac{\frac{1}{R_bC}s}{s^2 + \frac{1}{R_bC}s + \frac{3}{LC}} \tag{13}$$

$$G_{ii}(s) = \frac{D}{LC}\frac{\left(s + \frac{1}{R_bC}\right)}{s^2 + \frac{1}{R_bC}s + \frac{3}{LC}} \tag{14}$$

$$G_{ib}(s) = -\frac{1}{LR_bC}\frac{1}{s^2 + \frac{1}{R_bC}s + \frac{3}{LC}} \tag{15}$$

The next step is to introduce an appropriate control in the interleaved converter that can impose constant current in the output port and subsequently constant voltage while ensuring a smooth transition from the first to the second mode, i.e., using the same control for both modes and not by switching from a specific control for CC to another one for CV. To synthesize the controller, the transfer functions associated to the three-phase interleaved buck converter must be obtained.

E. BATTERY CHARGING PROTOCOL

A battery charger requires the application of a control strategy to implement the charging protocol. In this work, we have selected the well-known CC-CV protocol, which is illustrated in Fig. 3. This method charges a battery initially with a CC phase, until the battery voltage reaches a desired voltage. After that, the CV phase begins during which the battery voltage is controlled to maintain the desired value while the charging current gradually decreases. The whole charging process is terminated when the current in the CV phase decreases to the cutoff current, which is usually 0.1 C or 0.05 C. Note that C stands for the C-rate, which is a current rate normalized to cell nominal capacity [11], [14], [15].

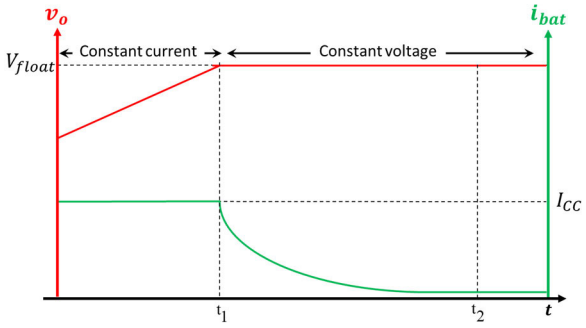

FIGURE 3. Characteristics of the classical CC-CV battery charging protocol.

F. CONVERTER DESIGN

When designing a converter, it is imperative to accurately define the operating constraints, which includes the input and output voltages, switching frequency, rated power, inductor current ripple and capacitor voltage ripple. This process should also take into consideration the accessibility of components in the market.

1) CONVENTIONAL BUCK CONVERTER DESIGN

Considering a conventional buck converter operating on continuous current mode (CCM), the inductance and output capacitor values can be calculated using equations (16) and (17) respectively [16].

$$L = \frac{v_o\,(v_{in} - v_o)}{\Delta I_L\, f_s\, v_{in}} \tag{16}$$

$$C = \frac{\Delta I_L}{8\Delta v_o f_s} \tag{17}$$

where f_s is the switching frequency, ΔI_L and ΔV_o are the desired ripple in inductor current and output capacitor voltage, respectively.

2) INTERLEAVED BUCK CONVERTER DESIGN

Since three interleaved buck converters are considered, a 120° phase-shift is introduced between the control signals u_1, u_2 and u_3, and as a consequence the switching ripple in the inductor current and capacitor voltages are reduced by a factor of 3 [17]. Hence, the inductance and output capacitance values of a three-phase interleaved buck converter are given

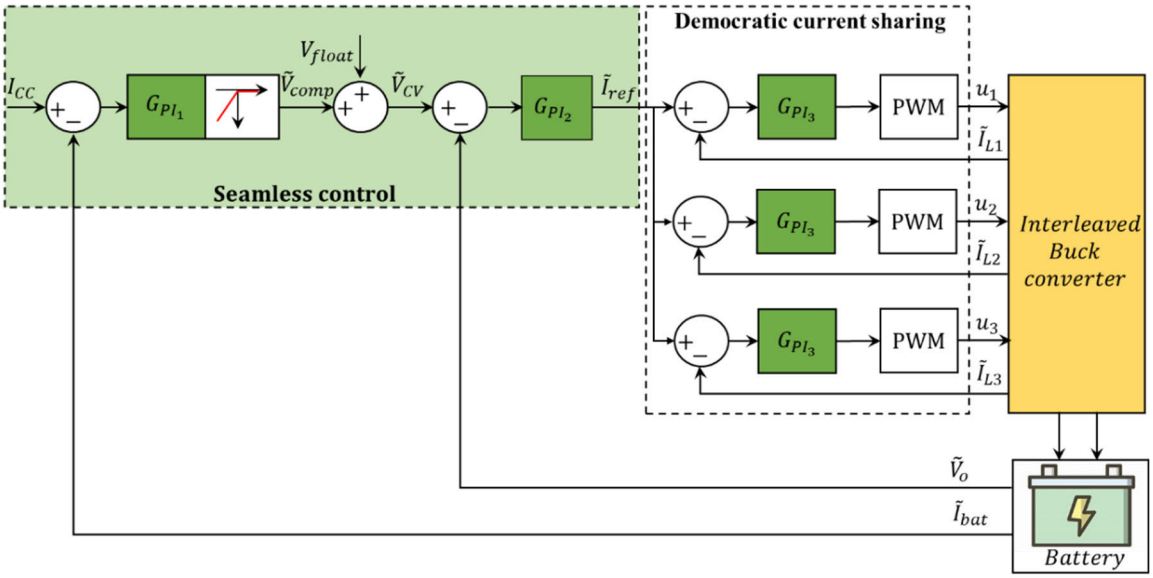

FIGURE 4. Complete scheme of the proposed three-loop cascade controller.

by equations (18) and (19) respectively.

$$L = \frac{v_o\,(v_{in} - v_o)}{3\Delta I_L\, f_s v_{in}} \tag{18}$$

$$C = \frac{\Delta I_L}{24\Delta v_o\, f_s} \tag{19}$$

In this paper, the inductance value is selected in such a way that the inductor peak-to-peak ripple ΔI_L is 20% of its DC steady-state value. In the same way, the output capacitance value is selected so that the capacitor voltage peak-to-peak ripple Δv_o is 1% of its DC steady-state value.

III. THREE-LOOP CASCADE CONTROLLER DESIGN

The complete control scheme of the proposed battery charger is presented in Fig. 4. We can clearly distinguish a multiple-loop controller, which consists of three loops in cascade configuration, where each loop has its dedicated proportional integral (PI) controller. As illustrated, the inner loop is devoted to the control of the inductor currents, while the two outer loops, namely output voltage and battery current loops, implement the protocol for battery charging. Considering a single-input single-output (SISO) model, the three PI controllers are here designed using the root locus method, both graphically and analytically, to determine the control parameters, i.e., the proportional controller gain K_p and the time constant τ_i of each loop (see Appendix for details).

A. CONTROLLER DESIGN FOR INDUCTOR CURRENT LOOP

As we are assuming equal inductances and no parasitic resistances, the three phases are identical. As a consequence, the inductor current of each phase is regulated by the same PI controller $G_{PI_3}(s)$ as illustrated in Fig. 4. The reference $\tilde{I}_{ref}(s)$ for each PI is given by the first outer loop (output voltage loop) and is the same for all the phases. The latter fact enforces democratic current sharing and ensures equal distribution of the current among the three phases. The block diagram of the system inner loop considering the dynamic current model described by equation (9) is depicted in Fig. 5. To design the control parameters K_{P3} and τ_{i3}, the specification of both maximum overshoot and settling time are considered. In order to obtain these parameters analytically, the first step of the design is to determine the natural frequency and damping coefficient that can ensure optimal system performance and reliability under expected operating conditions. These parameters are obtained using (20) and (21), considering maximum overshoot Mp and settling time t_s that allows a fast response without oscillations [18].

$$\xi = \frac{-\ln(Mp)}{\sqrt{\pi^2 + \ln(Mp)^2}} \quad 0 < M_p < 1 \tag{20}$$

$$\omega_n = \frac{4}{\xi t_s} \tag{21}$$

where ξ is the desired damping coefficient and ω_n is the natural angular frequency.

Now, we assume complex conjugate dominant poles given by:

$$s_1, s_1^* = -\omega_n\xi \pm \omega_n\sqrt{1-\xi^2}\,i \tag{22}$$

The position of the zero of the integral term of the controller z_{PI_3} is determined graphically by applying the angle criterion. The proportional term of the controller is obtained by applying the magnitude criterion, hence resulting in a PI controller with the following transfer function:

$$G_{PI_3}(s) = \frac{K_{P3}\,(1 + s\,\tau_{i3})}{s\tau_{i3}} \tag{23}$$

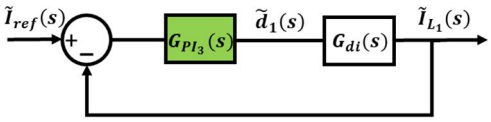

FIGURE 5. Block diagram of inductor current control loop.

where the time constant of the PI controller is related to its zero by:

$$\tau_{i3} = \frac{1}{z_{PI_3}}$$

B. CONTROLLER DESIGN FOR OUTPUT VOLTAGE LOOP

The first outer loop regulates the output voltage. Fig. 6 presents the block diagram of this loop and its relation with the inductor current control loop.

The reference voltage $\widetilde{V}_{CV}(s)$ during the CV mode is obtained as the sum of the contribution of the output $\widetilde{V}_{com}(s)$ of the most outer loop and the desired battery voltage V_{float} as illustrated in Fig. 4. To design the controller, the first step is to determine the transfer function $G_v(s)$ defined in Fig. 6. This can be expressed as follows:

$$G_v(s) = G_{dv}(s) \times \frac{G_{PI_3}(s)}{1 + G_{PI_3}(s) \times G_{di}(s)} \tag{24}$$

Now, the voltage controller is designed following the used method for the current loop, i.e., specifying both overshoot and settling time. As it is well known, in a cascade control strategy, the inner loop must be faster than the primary loop. A widely accepted rule is that the inner loop must be at least ten times faster than the outer loop. Accordingly, in order to design the output voltage controller $G_{PI_2}(s)$, we define an adequate settling time and a maximum overshoot.

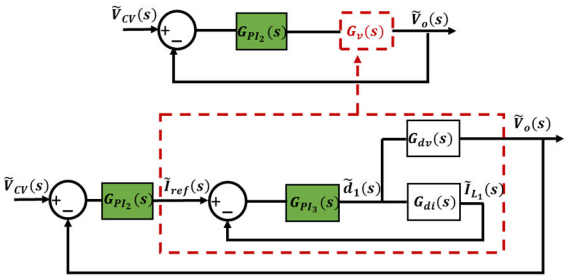

FIGURE 6. Block diagram of output voltage and inductor current cascade controller.

C. CONTROLLER DESIGN FOR BATTERY CURRENT LOOP

The most outer loop regulates the battery current at the desired reference I_{CC} during the CC phase by means of the PI controller $G_{PI_1}(s)$. A limiter is inserted in the loop to saturate the output of the controller for negative values. This loop imposes initially the CC mode and is deactivated when the output voltage reaches the desired voltage V_{float}. Fig. 7 presents the block diagram of the battery current control loop in cascade with the voltage control loop. First, it is necessary to determine the closed-loop voltage transfer function $G_{cl-v}(s) = \frac{\widetilde{V}_o(s)}{\widetilde{V}_{CV}(s)}$ in order to design the current controller $G_{PI_1}(s)$.

$$G_{cl-v}(s) = \frac{G_v(s) \times G_{PI_2}(s)}{1 + G_v(s) \times G_{PI_2}(s)} \tag{25}$$

Taking into account the battery model in Fig. 2-a, we define the relation between the output voltage and battery current as follows:

$$\widetilde{V}_o(s) = \widetilde{V}_{bat}(s) + R_b \times \widetilde{I}_{bat}(s) \approx R_b \times \widetilde{I}_{bat}(s) \tag{26}$$

Then, from (25) and (26), we obtain the required transfer function $G_i(s) = \frac{\widetilde{I}_{bat}(s)}{\widetilde{V}_{com}(s)}$ for the design of the controller, as illustrated in Fig. 7.

$$G_i(s) = \frac{G_{cl-v}(s)}{R_b} \tag{27}$$

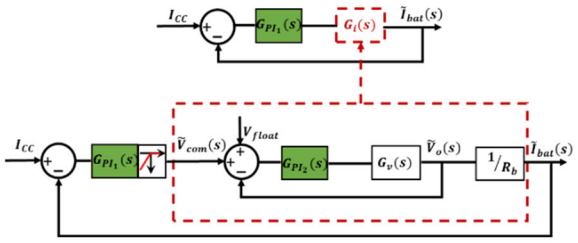

FIGURE 7. Block diagram of battery current and output voltage cascade controller.

Finally, using the root locus method, the current battery controller is designed according to the specifications of maximum overshoot and settling time, keeping in mind that the inner loop (voltage loop) must be at least ten times faster than the outer loop.

D. CONTROLLER RESULTS

In order to evaluate the operation of the three proposed controllers, the system parameters of Table 1 have been considered. Moreover, an overshoot of 10% ($M_p = 0.1$) has been specified for the design of the three PI controllers to ensure minimal deviations around the desired references. Another design criteria is the settling time of each control loop. To be conservative, a maximum settling time of 0.7 ms, which is twice the settling time of the open-inner loop system, has been defined for the inner loop controller PI_3. Furthermore, in accordance with the conventional criteria for cascade control systems, maximum values of 7 ms and 70 ms have been defined for the settling times of PI_2 and PI_1 controllers respectively.

The parameters of the obtained PI controllers are presented in Table 2.

Fig. 8 illustrates the pole-zero map of the inductor current closed loop, where the specified settling time and overshoot

TABLE 1. System parameter.

Symbol	Parameter	Value	Unity
V_{in}	Input Voltage	100	V
f_s	Switching Frequency	100	kHz
L	Inductance	124.8	µH
C	Output Capacitance	5.2	µF
V_{bat}	Battery Voltage	40-48	V
I_{bat}	Battery Current	30	A
R_b	Battery Resistance	50	mΩ
Q	Battery Capacity	30	Ah

TABLE 2. Controller parameters.

Controller	K_p	τ_i
PI_3	0.008	0.6839 ms
PI_2	5.486	0.6890 ms
PI_1	0.045	6.87 ms

have restricted the design in the white region. As it can be seen, the designed PI controller, namely $G_{PI_3}(s)$, meets the requirements considering only the closed loop pole in the white region because the closed loop pole in the shadowed area is canceled by the proximate closed loop zero.

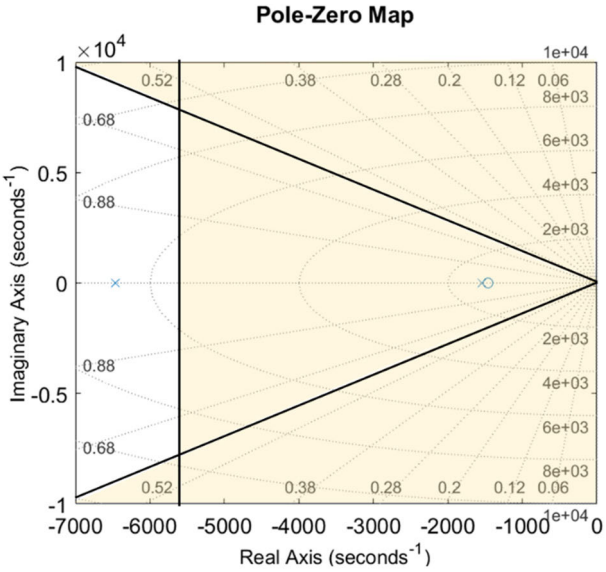

FIGURE 8. Pole-zero map of inductor current closed loop.

In the same way, Figs. 9 and 10 present the pole-zero maps of the output voltage closed loop and battery current closed loop respectively. It can be concluded that the designed controllers satisfy the specified requirements.

IV. SIMULATION RESULTS

A. STEADY-STATE RESPONSE

To validate the correct operation of the system, its switched model has been simulated by means of PSIM© software for

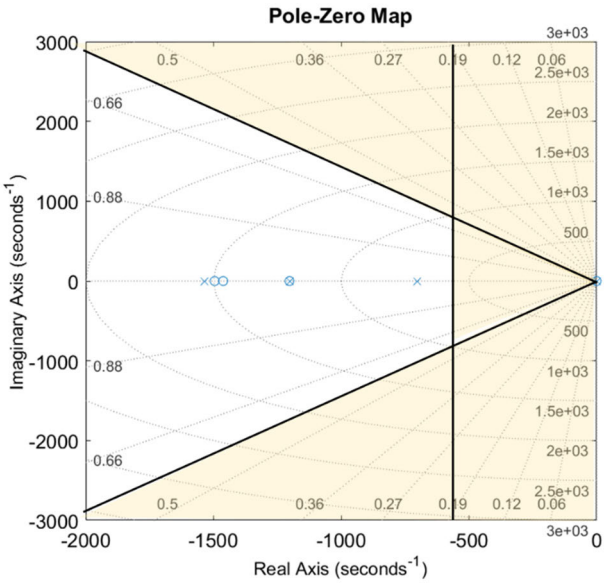

FIGURE 9. Pole-zero map of output voltage closed loop.

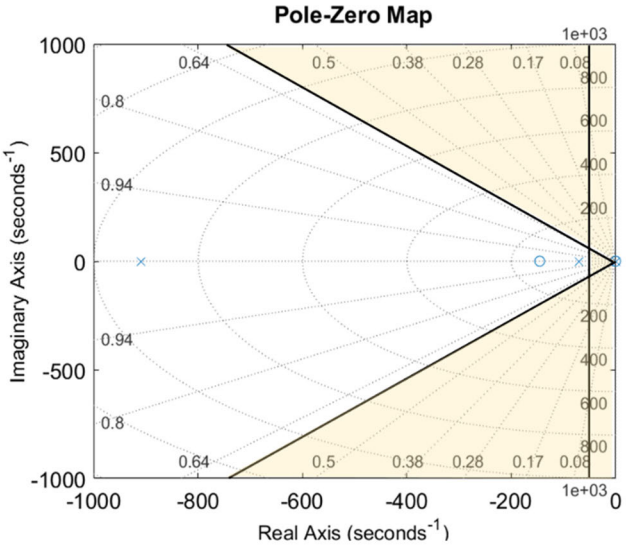

FIGURE 10. Pole-zero map of battery current closed loop.

the converter parameters and PI parameters listed in Table 1 and Table 2 respectively. Considering the simple battery model in Fig. 2-a, the steady-state waveforms of inductor current in each phase, the output voltage and the battery current are presented in Fig. 11.

Each inductor current has an average steady-state value of 10 A, imposed by the desired reference, with a peak-to-peak ripple of 2 A as theoretically designed, while the output voltage and battery current are 48 V and 30 A respectively. Moreover, as a consequence of the democratic current sharing technique, the current is equally distributed between the three phases and peak to peak ripples of 25 mV and 0.52 A are achieved in the output voltage and in the battery current respectively.

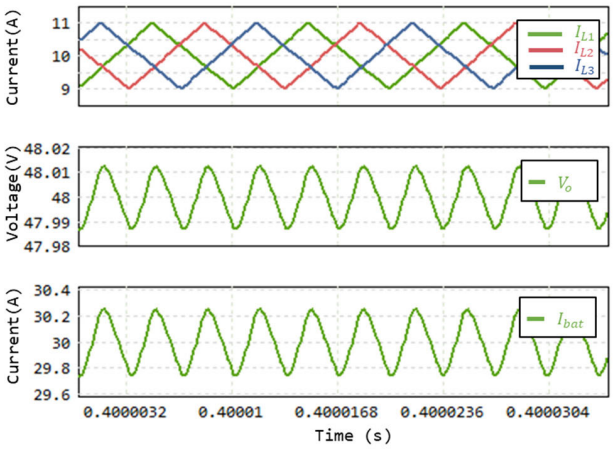

FIGURE 11. Steady-state waveforms of inductor current, output voltage and battery current.

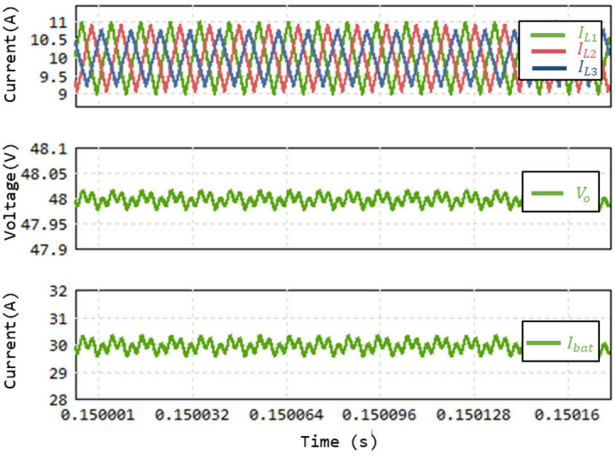

FIGURE 12. Steady-state behavior of the system considering tolerances ininductances and parasitics in inductors and MOSFETs.

The system has also been simulated considering tolerances in the parameters of the converter and parasitic components. Fig. 12 illustrates the simulation results of the state variables of the converter for the inductance values $L_1 = 124.8\ \mu$H, $L_2 = 1.1\ L_1$, $L_3 = 1.3\ L_1$, parasitic resistances $R_{L1} = 50\ \text{m}\Omega$, $R_{L2} = 1.25\ R_{L1}$, $R_{L3} = 1.15\ R_{L1}$, and parasitic capacitances in the switches $C_{s1} = 0.23$ nF, $C_{s2} = 1.1\ C_{s1}$, $C_{s3} = 1.2\ C_{s1}$.

It can be observed that the designed controller has low sensitivity to the tolerances in converter parameters, and to the presence of parasitic components in the circuit.

B. TRANSIENT RESPONSE

In order to test the response of the designed controller to different disturbances, input voltage and load variations are introduced first in the ideal converter. Then, simulation tests are performed taking into account tolerances in inductance values and parasitic resistances in the inductors and capacitances in the MOSFETs of the converter.

1) INPUT VOLTAGE VARIATION

Considering both the ideal converter and the converter with parameter uncertainties, step-type disturbances have been introduced in the input voltage. Initially, the system operates at 50% of the nominal input voltage. At instant $t = 40$ ms, a positive step change of 100% of the nominal value is applied, followed by a negative step change of 50% at $t = 100$ ms. Fig. 13 shows the response of the ideal converter, where deviations in both output voltage and battery current are rejected within a lapse of 9 ms for the first disturbance and 7 ms for the second one. Similarly, Fig. 14 illustrates the response of the converter to the same input voltage variations considering parameter uncertainties introduced by the parasitics. The deviations in this case are rejected in approximately 12 ms and 7 ms, respectively. Additionally, the responses of the ideal converter (Fig. 13) and the converter with parameter uncertainties (Fig. 14) are quite similar.

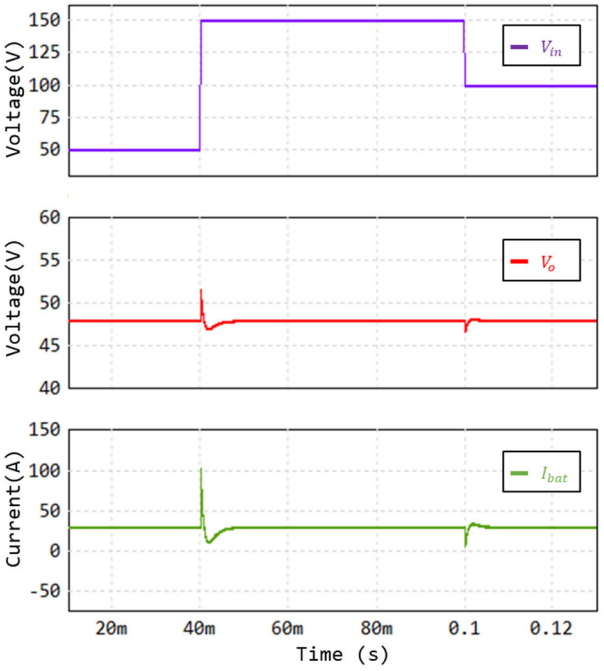

FIGURE 13. Input step voltage disturbance effect on output voltage and battery current considering an ideal converter.

Thus, we can conclude that the system has a good response to the disturbances in input voltage, regardless of the tolerances in converter parameters and parasitic parameters in its components.

2) LOAD VARIATION

The system has also been simulated to assess the behavior of the controller in regard to the variations in the load. It should be noted that these simulations have been performed assuming worst-case scenarios, involving sudden changes in both

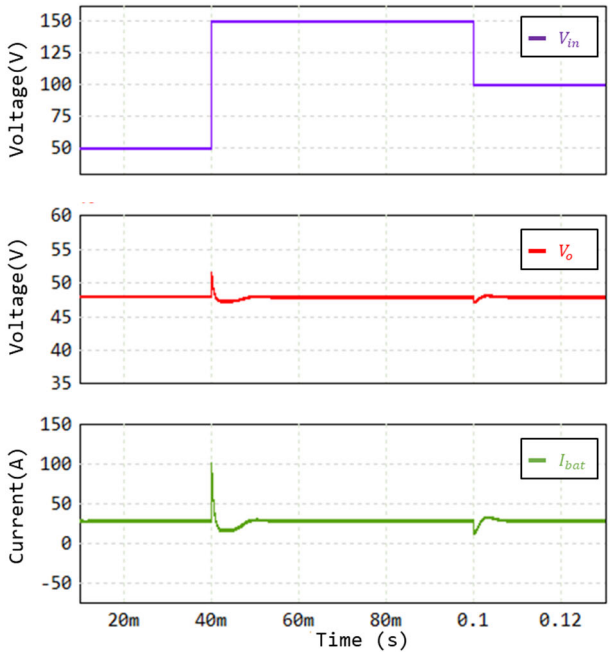

FIGURE 14. Input step voltage disturbance effect on output voltage and battery current considering parasitic components.

battery voltage and battery resistance. Despite these types of changes do not appear in the real operation of the battery charger, they are useful to demonstrate the robustness of the system.

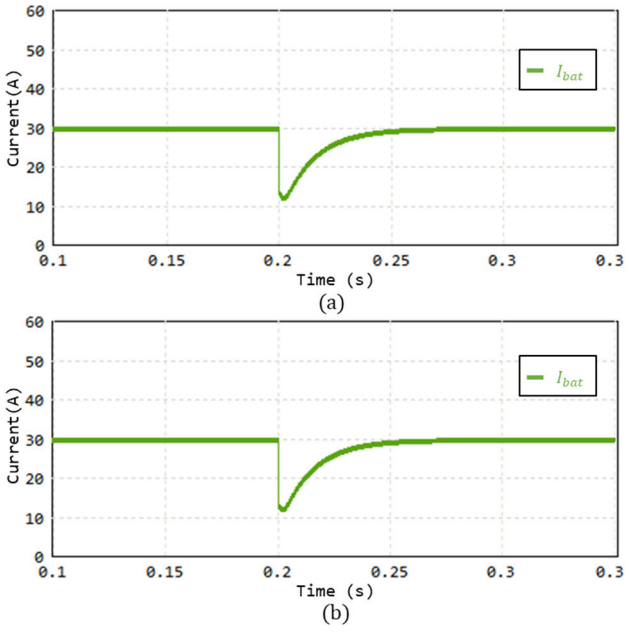

FIGURE 15. Response of the system to the disturbances in battery voltage. a) ideal converter, b) converter with parasitic components.

Fig. 15 illustrates the battery current response when a step change of 2 V is introduced in the battery voltage at $t = 0.2$ s considering the battery model in Fig. 2-a. It can be observed

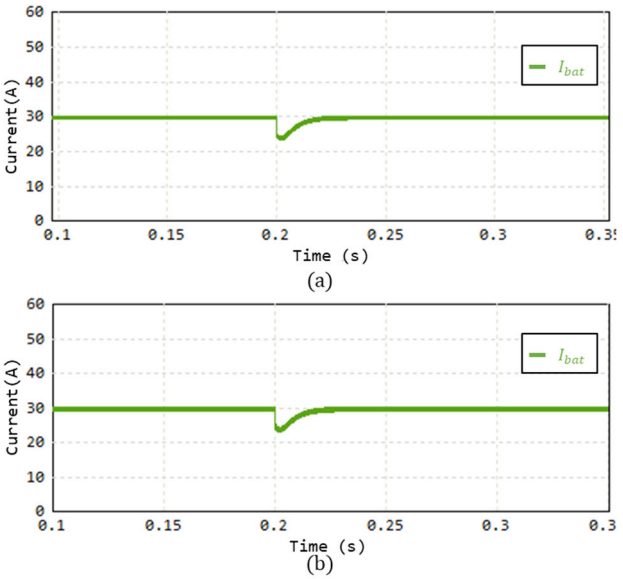

FIGURE 16. Response of the system to the disturbances in battery resistance. a) ideal converter, b) converter with parasitic components.

that the system is operating correctly in both cases, and the battery current returns to its initial value in around 60 ms.

3) SYSTEM'S BEHAVIOR UNDER STRESS CONDITIONS

To assess the system's behavior under stress conditions, an additional simulation has been performed, enforcing the system to operate under extreme output power fluctuations beyond typical operating conditions. Initially operating at 20% of its nominal power, a step type change is introduced in the battery voltage at instant $t = 40$ ms, the system transitioning from 20% to 100% of the nominal power. Subsequently, at instant $t = 100$ ms, a second step change is applied, adjusting the system's operation from 100% to 60% of nominal power. As depicted in Fig. 17, the different deviations in the output voltage are rejected in approximately 6 ms and the system is operating properly despite the abrupt extreme changes in the power.

4) SYSTEM RESPONSE TO A FAILURE EVENT

An additional PSIM© simulation is conducted to evaluate the converter's response to potential failures. Fig. 18 illustrates the system's behavior when one phase of the converter becomes inoperative. At instant $t = 40$ ms, the control system compensates for the phase failure by increasing the inductor current to 15 A in the remaining two phases, thereby maintaining the 30 A battery charging current. Hence the designed controller is operating correctly, rejecting the deviation in both the output voltage and battery current in approximately 6 ms.

C. CC-CV CHARGING PROTOCOL SIMULATION

A PSIM© simulation of the system considering the battery model of Fig. 2-b has been performed to evaluate the

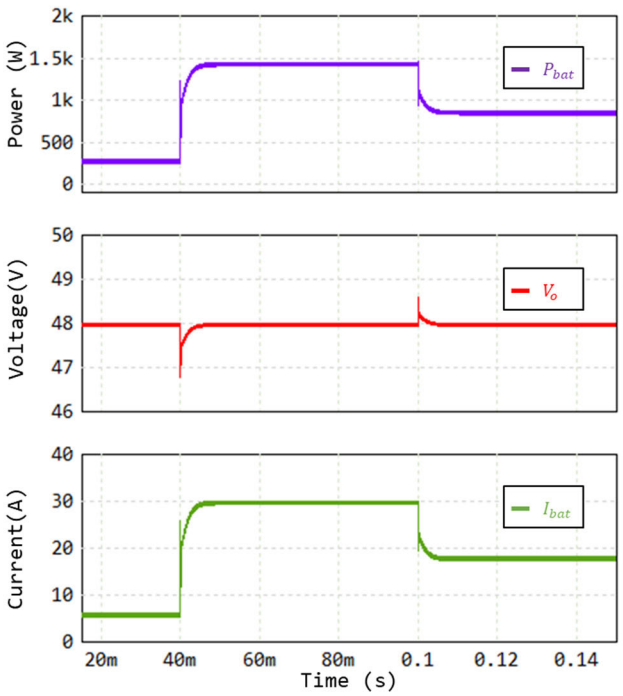

FIGURE 17. Response of the system to sudden changes in the demanded output power.

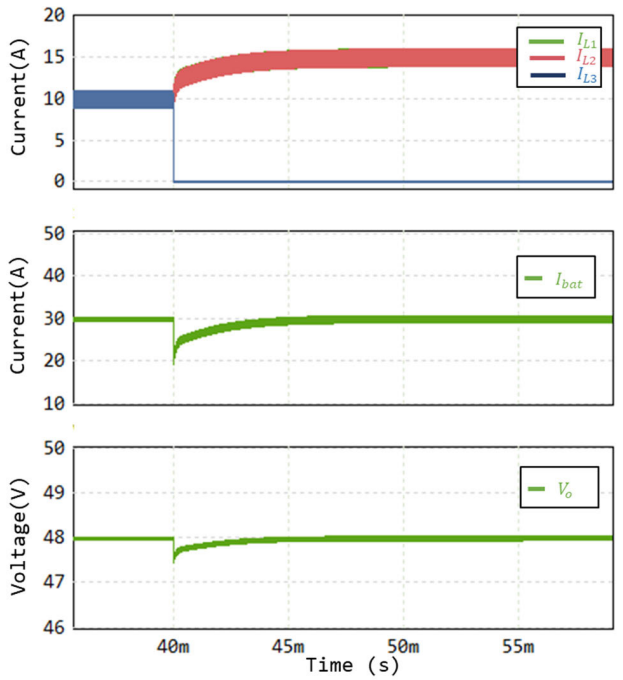

FIGURE 18. Response of system to one phase failure.

effectiveness of the designed controller with respect to the CC-CV charging protocol.

Fig. 19 shows the waveforms of battery current, battery voltage and output voltage during a complete CC-CV

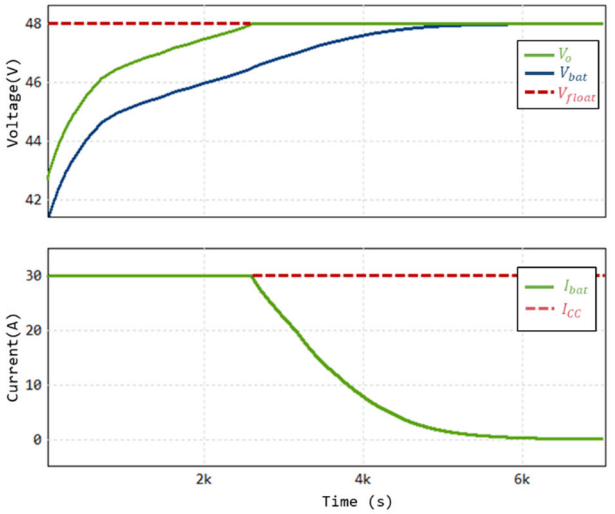

FIGURE 19. Battery current, battery voltage and output voltage during a complete CC-CV charging cycle.

charging cycle. During the CC phase, the battery is maintaining the desired constant current of $I_{CC} = 30$ A while the battery voltage and thus the output voltage are increasing. Once the output voltage reaches the desired reference $V_{float} = 48$V, the CV phase begins, where the battery charger maintains a constant voltage and the current starts decreasing. The battery charging continues until the battery current drops to zero.

V. EXPERIMENTAL VALIDATION

A. EXPERIMENTAL PROTOTYPE

In order to validate the theoretical work and to verify the correct operation of the battery charger discussed in the previous sections, an experimental prototype has been developed as illustrated in Fig. 20 together with the experimental setup. The implementation is divided into two main parts. The first one is the power stage of the three-phase interleaved buck converter and the second one is the analogue circuit required for the PWM and the controllers of Fig. 4. The nominal values of the parameters are the ones depicted in Table 3.

1) POWER STAGE IMPLEMENTATION

The laboratory prototype of the converter is designed to handle 1.5 kW for a regulated DC input voltage of 100 V and an output voltage ranging from 42 to 48 V. The first step has been to design the printed circuit board (PCB), which has been performed using Altium program. Two MOSFETs C3M0016120K have been used to implement the controlled switches in each phase instead of the combination of MOSFET and diode, in order to achieve synchronous rectification and, consequently, higher efficiency. The NCD57256DR2G isolated driver has been used to drive the gate signals of the MOSFETs configured with a dead time of 200 ns. The source for the high-side driver is implemented using the well-known technique of the bootstrap diode. The characteristics of the

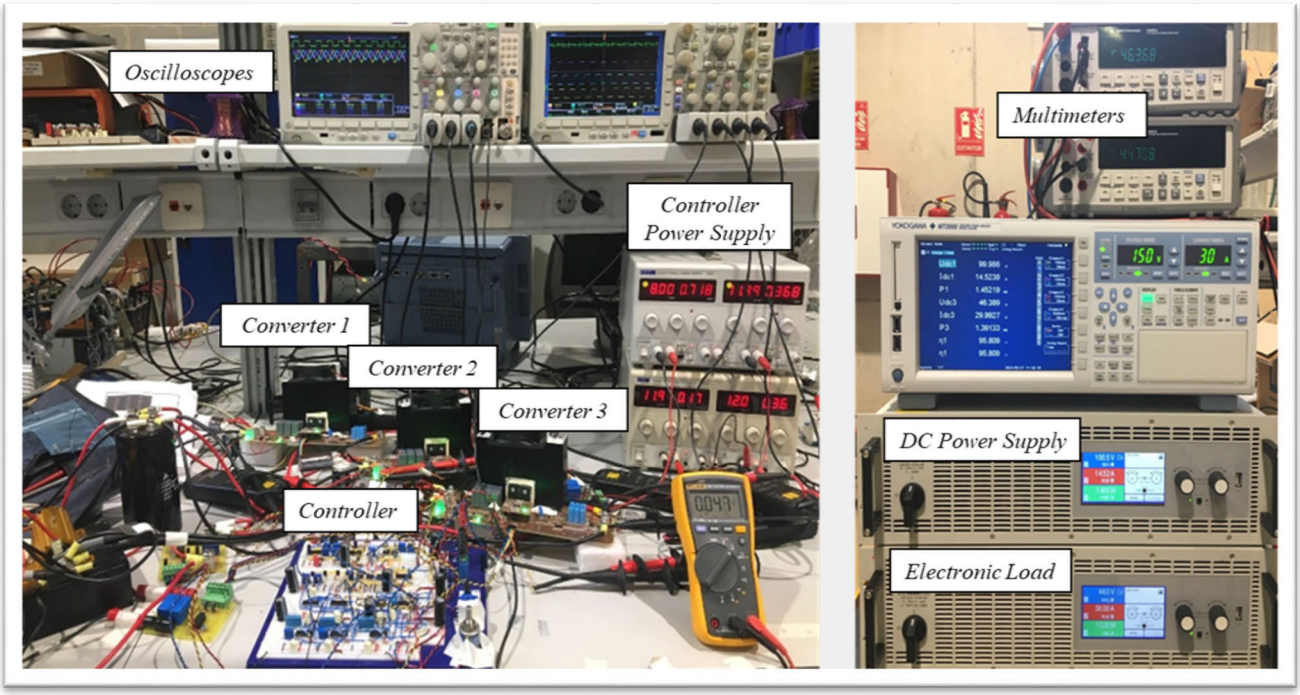

FIGURE 20. Picture of the experimental setup and battery charger prototype.

TABLE 3. Selected components.

Component	Characteristic	Reference
MOSFETS	Silicon Carbide Power MOSFET 1200 V, 115 A	C3M0016120K
Drivers	High current, 2.5 kV, 2 channel isolated gate driver	NCD57256DR2G
Input Capacitors	3 × 1 µF, 1000 V, Film 800 µF, Electrolytic type	R71QR41004010K
Output Capacitors	3 × 1 µF, 250 V, Film type	PHE426HD7100JR06L2

selected components for the building of the power stage are listed in Table 3. Subsequently, the inductors have been implemented in the laboratory with the following inductances $L_1 = 142\ \mu\text{H}, L_2 = 104\ \mu\text{H}, L_3 = 83\ \mu\text{H}$. The different inductance values have allowed us to test the behavior of the system with uncertainties in the converter parameters.

2) CONTROLLER IMPLEMENTATION

The following step has been to implement the multiple loop cascade controller for democratic current sharing and the CC-CV charging protocol. The three-loop control stage has been implemented analogically on a breadboard for more flexibility on the testing and verification of the controller. The PI controller of each loop has been implemented using the integrated circuit (IC) LF347N. The references for output voltage and battery current control loops are provided by simple voltage dividers implemented with 10-turn potentiometers. To measure the inductor current in each phase, three Hall effect sensors LA25-NP with a gain of 0.45 have been used. Similarly, the battery current and output voltage are measured by sensors CAS 25-NP and LV25-P respectively, with a gain of 0.125 for current sensor and 0.144 for voltage sensor. The three PWM signals have been obtained from the comparison of the outputs of the three inductor currents controllers and the modulation sawtooth carriers using the integrated circuit LM319. The carriers are generated from the signal generator XR2206 providing a 50 kHz sinewave, two 120° phase shifters and three precision rectifiers, which are all implemented using the IC LF347. The rectified signals are used to generate thin pulses for the zero-vicinity detection which are used to generate the sawtooth carriers using 2N2222 transistors. The square gate signals are refined using NAND gates from the CD4093. The circuit diagram of the resulting controller is shown in Fig. 21.

B. TESTING INSTRUMENTATION

The measurement setup that has been used for this experiment is presented in Fig. 20 and is composed of two oscilloscopes MSO3014, two multimeters U3401, three current probes

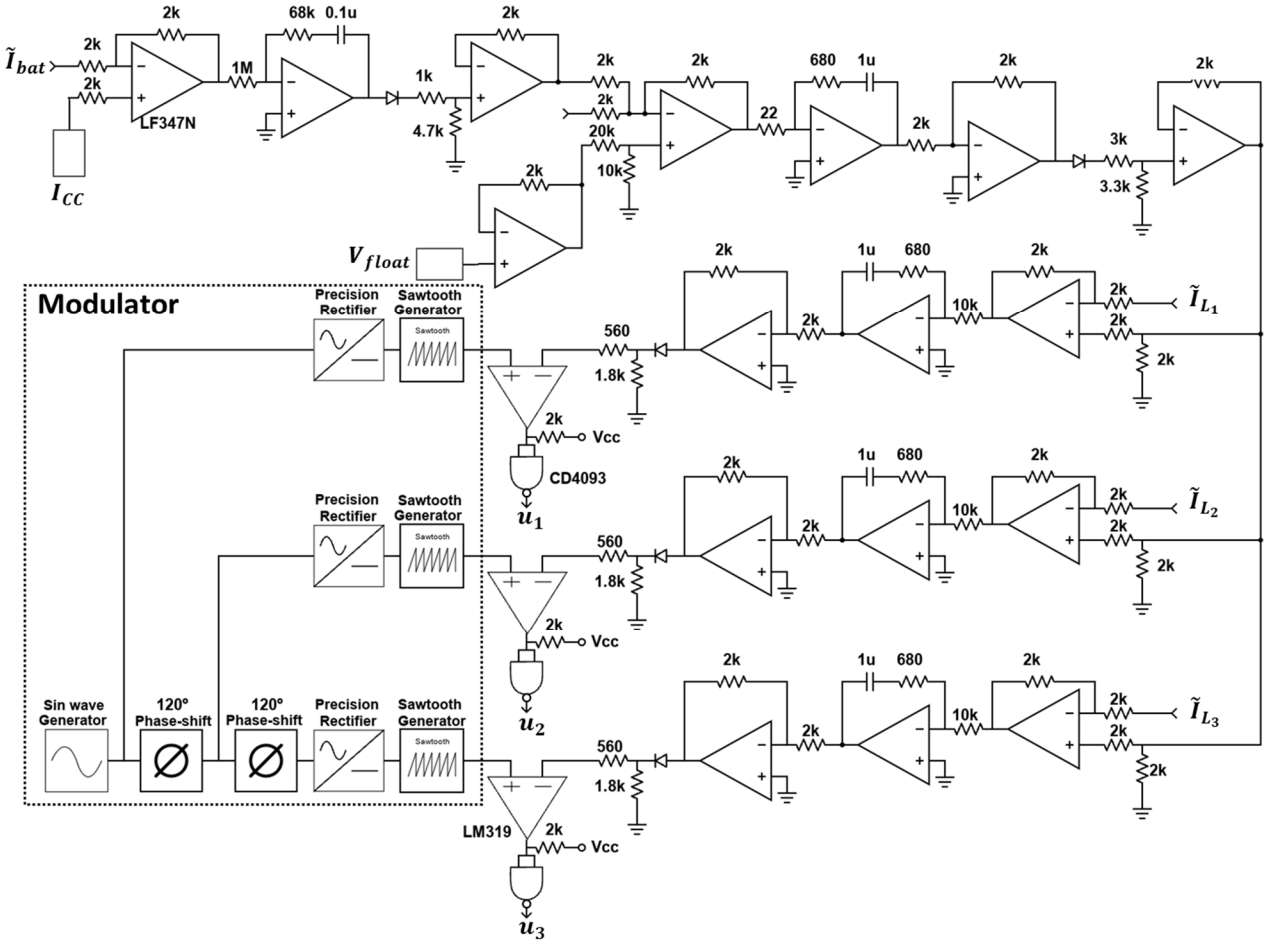

FIGURE 21. Schematic circuit diagram of the implemented controller.

TCP0020 and one differential probe THDP200. The power supply PSI 9750-40 has been used as input voltage source, the battery has been emulated by the electronic load ELR-9750-44 and two triple DC power supply EX354RT 300 W and EX354T 300 W has been used to supply the control stage.

C. RESULTS

1) STEADY-STATE MEASUREMENTS

The developed battery charger is first tested using an electronic load to emulate the behavior of the battery. In order to test the ability of the prototype in handling different levels of power, measurements have been carried out over an operating range from 400 W to 1600 W. A first test for an output voltage of 42 V and a current of 30 A has been performed. The waveforms of inductor currents of the three phases in steady state, are shown in Fig. 22-a, while the waveforms of the output voltage and the gate signals of the three transistors are illustrated in Fig. 22-b. It can be seen that the inductor current in each phase has an average value of 10 A (the depicted current is a quarter of the actual inductor current). Moreover, the current ripples in the three phases are different, which can be explained by the differences in the values of the inductances. Then, multiple measurements have been performed by testing the battery charger for different voltages (in a range of 42- 48 V), and for different references of the current. It can be concluded that the implemented charger achieves a correct operation within the desired range of 42 to 48 V and from 0 to 30 A. The experimental results of the three-phase interleaved battery charger in the CV phase for an electronic load with a voltage of 48 V at different operation points are illustrated in Fig. 23.

2) CHARGING PROTOCOL

The next step in our study has been to utilize the implemented prototype for the charging process of a real battery. In this context, a pack of twenty cells of 2.3 V, 30 Ah, Lithium-Titanium-Oxide (LTO) battery from ELERIX has been used. To supervise current, voltage and temperature of the battery cells during the validation test of the proposed charger, a Supervisory Control and Data Acquisition (SCADA) system has been employed.

The measurement of the variables is accomplished by means of sensors for individual cells included in the Battery Management System (Smart BMS by 123Electric).

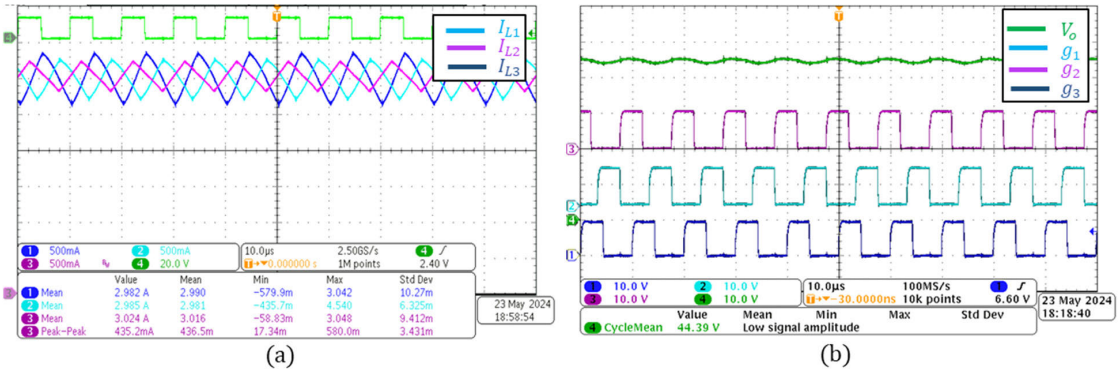

FIGURE 22. Experimental results at the start of the CC phase of the charging process (42 V, 30 A). a) waveforms of the inductor currents in steady state. b) output voltage and the gates signals of the three MOSFETs.

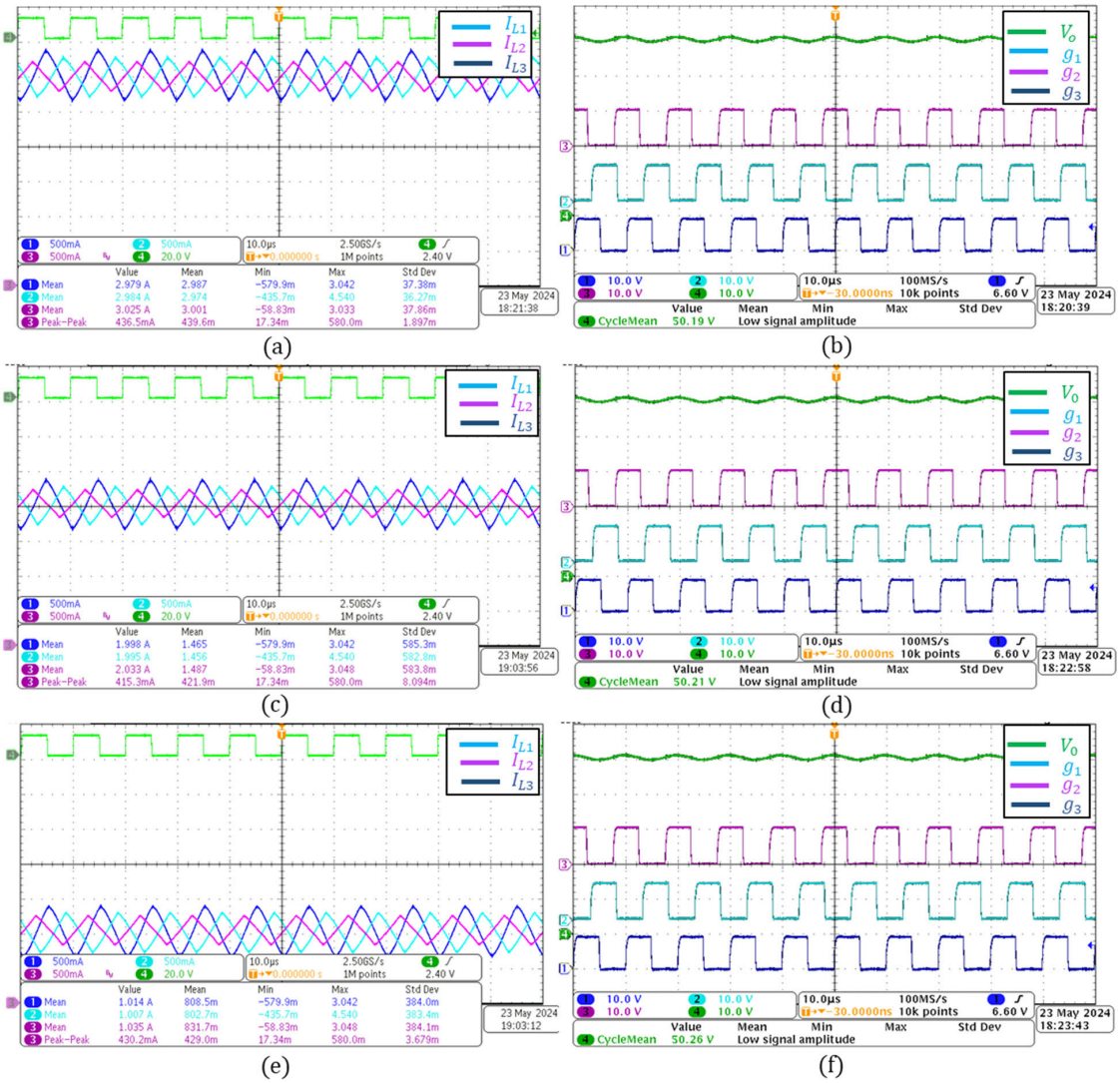

FIGURE 23. Experimental waveforms at the CV phase of the charging process for an output voltage of 48 V and battery current of: a) 30 A.c) 20 A. e) 10 A.

The BMS communicates with a LabVIEW software application through sbRIO-9627 card from National Instruments using the Controller Area Network (CAN) protocol and an in-house developed data packaging method. The data

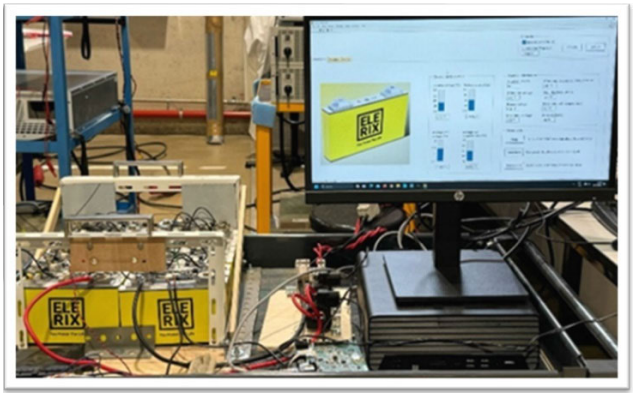

FIGURE 24. Battery pack and SCADA system.

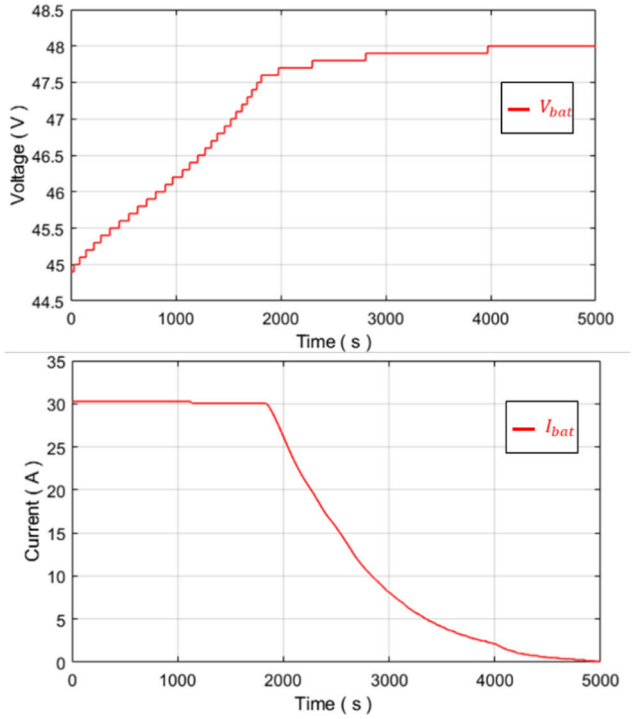

FIGURE 25. Battery current and battery voltage during a complete CC-CV charging cycle.

of voltage, current, temperature and SoC for the complete charging cycle are stored in an Excel file, accessed and plotted off-line using Matlab. The experimental setup including the battery pack and the SCADA system employed to acquire the data is shown in Fig. 24. The charging of the battery array is carried out using the standard CC-CV charging protocol with a charging rate of 1 C. As illustrated in Fig. 25, during the CC interval, the charging current remains constant at a value of 30 A, while the battery voltage continues to increase until it reaches 48 V. Once this threshold is attained, the charger shifts to a constant voltage CV phase, where it maintains the constant voltage while the charging current is gradually decreasing. Moreover, the maximum power of 1.44 kW is achieved during the transition from CC to CV mode.

3) EFFICIENCY MEASUREMENT

The efficiency of the system has been measured using the precision power analyzer YOKOGAWA WT3000 for a constant input voltage of 100 V and output power varying along the operation points of one cycle of the battery charging process. The results presented in Fig. 26 show that the efficiency is always above 95%, and a peak efficiency of 96.57% is obtained for an output power around 30% of the rated power.

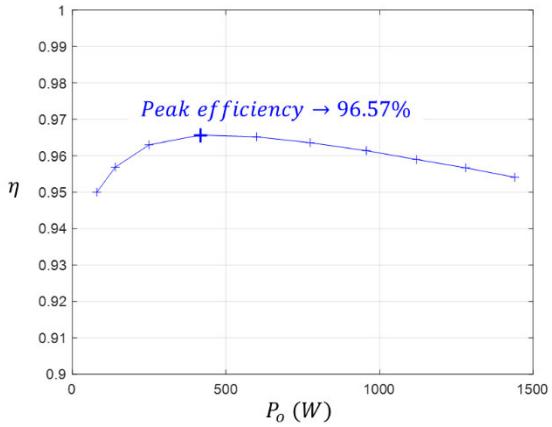

FIGURE 26. Experimental measurement of efficiency along one cycle of battery charging.

4) THERMAL BEHAVIOR MEASUREMENT

The thermal behavior of the system has been studied using a FLIR T420 thermographic camera. The test consists in providing 1.44 kW (100% of the rated power) to the system in steady-state operation during two hours and capturing thermographic images for inductances and active elements. As can be observed in Fig. 27, the surface temperature in the three heatsinks of the MOSFETs is around 31 °C while the temperature of the MOSFETs' case is around 57 °C degrees with a deviation between converter phases of around 5%. The external temperature of the inductances is balanced in the three converter phases around 25 °C.

VI. SCALED-UP BATTERY CHARGER FOR FAST EV CHARGING

A. 24-PHASE INTERLEAVED-BUCK-BASED BATTERY CHARGER

The battery charger proposed in this work could be used for an EV fast charging station if an appropriate scaling-up is performed. It is generally accepted that modularity is the key element for implementing higher power levels [19]. On the other hand, the state of the art of commercial buck converters carried out in [3] reveals that 10 kW single buck modules could be successfully used in a real scale implementation.

While keeping the same principle for the multiple-loop control described above, the extension to a high number of phases, i.e., 36 like in [3] to attain ultrafast charging, would require a digital implementation to warranty the accuracy of the phase shifting. This will imply design and analysis in

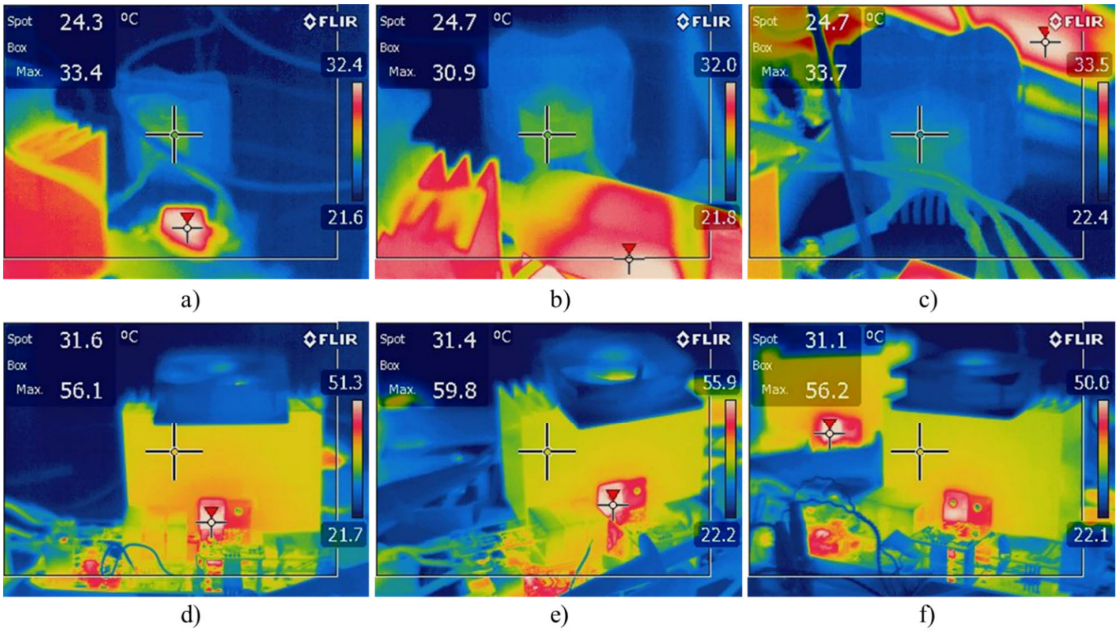

FIGURE 27. Thermal behavior of the system operating after two hours at100% output power: a) inductor of converter 1, b) inductor of converter 2, c) inductor of converter 3, d) power stage of converter 1, d) power stage of converter 2, and e) power stage of converter 3.

TABLE 4. Comparative analysis.

Ref	Input Voltage (V)	Converter Type	Load	f_s (kHz)	Switching device technology	Number of modules	Max Power (kW)	Charge rate	Type of control	η %	Validation
This work	100	Buck	Battery (48 V, 30 Ah)	100	Silicon Carbide power MOSFETs C3M0016120 K	3	1.44	1C	Analog	95.5	S & E
[3]	1500	Buck	Battery (800 V, 75 Ah)	20	--	36	350	6C	Analog	--	S
[4]	S: 200 E: 50	Buck	S: Battery (48-60 V) E: Rheostat	20	Silicon power MOSFETs IRFP260N	3	S: 0.6 E: 0.37	--	Microcontroller LAUNCHXL-F28379D	--	S & E
[5]	120	Buck	Battery (48 V, 30 Ah)	100	SiC MOSFET and GaN transistor	2	1.5	0.5 C	Microcontroller TMS320F28027	--	E
[6]	200	Buck	Battery (48V, 100 Ah)	200	SiC MOSFET	3	10	2C	Digital (Unreported)	90-98	S
[7]	S: 350 E: 159	Buck-Boost	S: Battery (96 V, 100 Ah) E: Rheostat	100	SiC MOSFET SCT3060ALG C11	3	S: 12 E: 0.25	--	Microcontroller TMS320F28335	--	S & E

Ref: Referenced work, S: Simulation, E: Experimental, f_s: Switching frequency, η: Efficiency.

discrete time and implementation of the proposed control in a digital device. For example, with the use of the real-time microcontroller TMS320F28379D, it is possible to handle until 24 modules covering a power range until 240 kW.

TABLE 5. Scaled-up system parameters.

Symbol	Parameter	Value	Unity
V_{in}	Input Voltage	1500	V
f_s	Switching Frequency	50	kHz
L	Inductance	531.55	µH
C	Output Capacitance	6.52	µF
V_{bat}	Battery Voltage	340-450	V
I_{bat}	Battery Current	500	A
R_b	Battery Resistance	100	mΩ
Q	Battery Capacity	250	Ah

TABLE 6. Controller parameters.

Controller	K_p	τ_i
PI_3	0.0012	0.0001 s
PI_2	0.4103	0.0012 s
PI_1	0.0891	0.0118 s

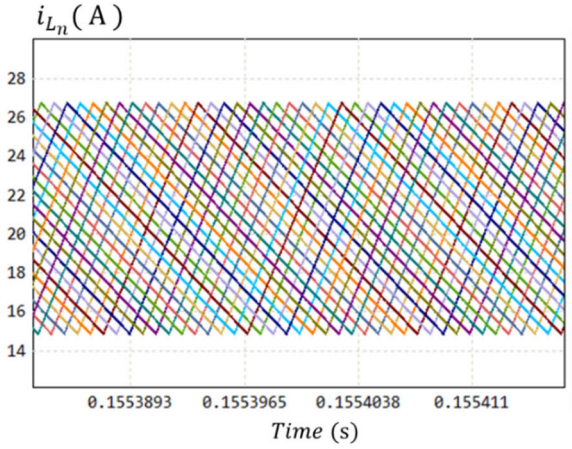

FIGURE 28. Steady state waveforms of the inductor current in the different phases identified by the index $n = \{1, 2, \ldots, 24\}$.

The corresponding phase shift will be of 15 degrees. Figs. 28-30 show the PSIM simulation results corresponding to the proposed battery charger, which has been scaled up to provide a power of 240 kW from a 1500 V DC bus to charge an EV battery of 400 V with a 100 kWh capacity. This would represent a real scale case of fast charging. The battery charger discussed in this section, is based on 24-phase interleaved buck converter and uses the same principle, small signal modelling and control design as for the three-phase converter, the number of phases having been appropriately adapted. The battery charger is simulated considering the converter parameters of Table 5 and controller parameters of Table 6.

Fig. 28 presents the steady-state waveforms of inductor current in each phase with an average value of 20.83 A, while the steady-state waveforms of output voltage and battery current are depicted in Fig. 29. The output voltage and

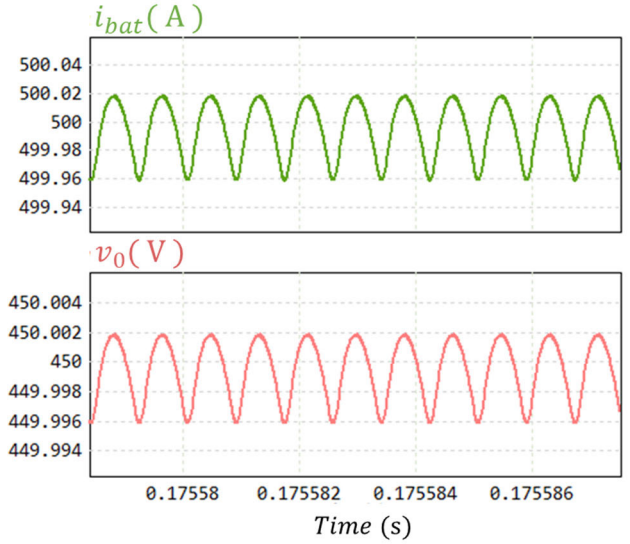

FIGURE 29. Steady state waveforms of output voltage and battery current.

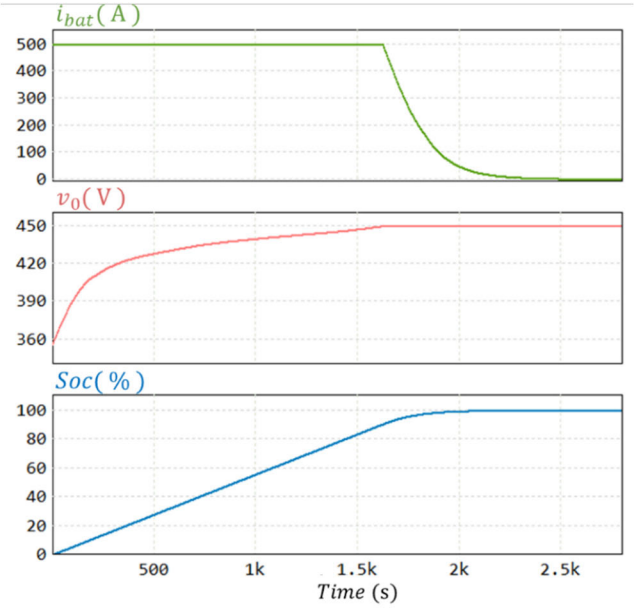

FIGURE 30. Battery current, output voltage and SoC of the battery during a complete CC-CV charging cycle.

battery current have an average value of 450 V and 500 A respectively.

Fig. 30 shows the waveforms of battery current, output voltage and SoC of the battery during a complete CC-CV charging cycle. The charging of the battery is performed at 2C rate considering a 250 Ah capacity, and a voltage v_{bat} in a range of 360-450 V. As depicted, during the CC phase the battery is maintaining the desired current of 500 A while the output voltage is increasing until it reaches the voltage reference of 450 V. Once the output voltage reaches the desired reference, the CV phase begins and lasts until the battery is fully charged while the current decreases

exponentially until zero. The SoC of the battery attains 80% in approximately 24 min.

VII. INTEGRATION TO GRID SYSTEM AND RENEWABLE ENERGIES

The proposed battery charger can be integrated to grid systems if galvanic isolation within the electrical architecture is provided by another stage [2]. The work in [20] proposes an electrical architecture for an ultrafast charging station, where the scaled-up version of the charger could be integrated. The charging station in [20] is based on a hybrid energy distribution system where the MV grid supplies the station through a solid-state transformer (SST) and the internal power distribution is carried out by means of an AC bus of 220 V and two DC buses of 600 V and 1500 V. The SST is used there to increase the efficiency, reduce the volume and weight of the electrical architecture, and allow the integration of renewable energies and energy storage systems [21], [22]. The transition between the different operating modes required to manage the charging station system is studied in [23]. The proposed battery charger could supply the EV from the 1500 V DC bus, while the 600 V DC bus would integrate a photovoltaic array and a wind turbine in the station.

VIII. CONCLUSION

The control of a battery charger based on a three-phase interleaved buck converter has been addressed in this paper. In the theoretical analysis, the modeling of the converter and the design of its parameters have been achieved. In addition, the transfer functions required to synthesize the controller have been obtained. Consequently, a three-loop cascade controller has been designed, where the most inner loop is dedicated to the democratic sharing of inductor current for equal distribution between the three phases of the converter. The two outer loops constitute a seamless controller in which a CC-CV charging protocol has been implemented with a soft transition from the CC phase to the CV phase. Moreover, the controller has been designed considering cascaded control system rules and root locus method to determine the parameters of each PI controllers.

The designed controller has been validated by PSIM© simulation. Different tests have been performed in order to assess the robustness of the controller. Simulation results have shown that the designed controllers can maintain a stable behavior, fast dynamic response and robustness independently of the disturbances and uncertainties in the converter parameters. In addition, a laboratory prototype has been implemented to validate the theoretical work. The first tests have been conducted using an electronic load to emulate the operation of a battery. Subsequently, a 30 Ah LTO battery pack has been charged at 1 C rate using the implemented battery charger, thus achieving the expected fast charging operation.

Further research contemplates the digital implementation of the proposed control. This will improve the flexibility and reprogramming of controller parameters, reduce considerably the required printed circuit board (PCB) area, add precision in the phase shifting, and allow to apply more sophisticated techniques of control. In addition, the digital implementation would facilitate wide operation conditions in output voltage and processed power. Also, gain scheduling, data-driven automatic tuning, fault-tolerance control, reconfiguration of connected phases could be easily addressed.

Another prospective work contemplates the extension of interleaved operation to the implementation of a constant power (CP)-constant voltage (CV) battery charging protocol [24].

APPENDIX

A. ROOT LOCUS OF INDUCTOR CURRENT LOOP WITH PI CONTROLLER

To design the controller of the inner loop using root locus method, equation (28) is derived following the block diagram in Fig. 5 (Section III-A).

$$T_i(s) = \frac{K_{P3} V_{in}}{LC} \frac{\left(s + z_{PI_3}\right)\left(s + \frac{1}{R_b C}\right)}{s\left(s^2 + \frac{1}{R_b C} s + \frac{3}{LC}\right)} \tag{28}$$

The root locus method involves plotting the poles and zeros of the open-loop transfer function and analyzing their movement as system parameters vary. Hence, the characteristic equation to obtain the poles is defined in (29) and the zero is obtained in (30).

$$s^2 + \frac{1}{R_b C} s + \frac{3}{LC} = 0 \tag{29}$$

$$z_1 = \frac{1}{R_b C} \tag{30}$$

Consequently, following converter parameters of Table 1 (Section III), the poles and the zero of the open inductor current loop are as follows:

$$p_{i1} = -1.202 \times 10^3 \text{rad/s}$$
$$p_{i2} = -3.845 \times 10^6 \text{rad/s}$$
$$z_{i1} = -3.846 \times 10^6 \text{rad/s}$$

The root locus of the inner loop is presented in Fig. 31.

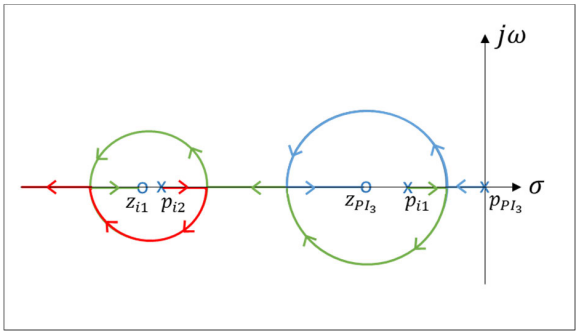

FIGURE 31. Root locus of inductor current loop.

B. ROOT LOCUS OF OURPUT VOLTAGE LOOP WITH PI CONTROLLER

In the same way, following the block diagram in Fig. 6 (Section III-B), the transfer function of the open output voltage loop is obtained as:

$$T_v(s) = K_{P3}K_{P2}\frac{3V_{in}}{LC}\frac{\left(s+z_{PI_3}\right)\left(s+z_{PI_2}\right)}{s\Delta_v(s)} \tag{31}$$

where $\Delta_v(s)$ and the coefficients α_0, α_1 and α_2 are defined as follows:

$$\begin{aligned}\Delta_v(s) &= \left(s^3+\alpha_2 s^2+\alpha_1 s+\alpha_0\right)\\ \alpha_0 &= \frac{K_{P3}V_{in}z_{PI_3}}{LR_bC}\\ \alpha_1 &= \frac{3}{LC}+\frac{K_{P3}V_{in}}{LR_bC}+\frac{K_{P3}V_{in}z_{PI_3}}{L}\\ \alpha_2 &= \frac{1}{R_bC}+\frac{K_{P3}V_{in}}{L}\end{aligned}$$

By factoring the characteristic polynomial $\Delta_v(s)$ as:

$$\Delta_v(s) = (s+p_{v1})(s+p_{v2})(s+p_{v3}) \tag{32}$$

The poles of the open output voltage loop are:

$$\begin{aligned}p_{v1} &= -1.5\times10^3 \text{rad/s}\\ p_{v2} &= -6.5\times10^3 \text{rad/s}\\ p_{v3} &= -3.845\times10^6 \text{rad/s}\end{aligned}$$

The root locus of the output voltage loop is presented in Fig. 32.

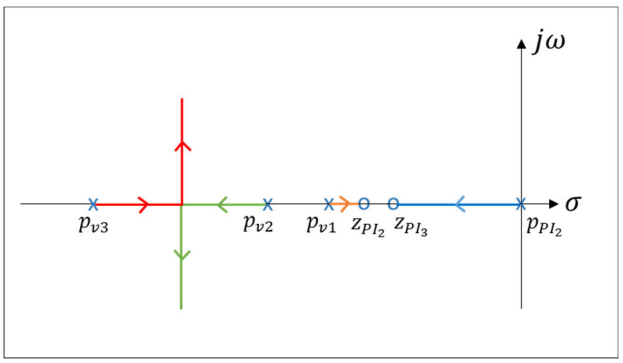

FIGURE 32. Root locus of output voltage loop.

C. ROOT LOCUS OF BATTERY CURRENT LOOP WITH PI CONTROLLER

Finally, to obtain the root locus of the battery current loop, the block diagram of Fig. 7 (Section III-C) is considered, and the open loop transfer function is obtained.

$$T_{i_{bat}}(s) = K\frac{\left(s+z_{PI_3}\right)\left(s+z_{PI_2}\right)\left(s+z_{PI_1}\right)}{s\Delta_i(s)} \tag{33}$$

where $\Delta_i(s)$, K and the coefficients β_0, β_1, β_2 and β_3 are defined as follows:

$$\begin{aligned}\Delta_i(s) &= s^4+\beta_3 s^3+\beta_2 s^2+\beta_1 s+\beta_0\\ K &= \frac{3V_{in}}{LCR_b}K_{P3}K_{P2}K_{P1}\\ \beta_0 &= \frac{3V_{in}}{LC}K_{P3}K_{P2}z_{PI_3}z_{PI_2}\\ \beta_1 &= \frac{V_{in}K_{P3}z_{PI_3}}{LR_bC}+(z_{PI_3}+z_{PI_2})\frac{3V_{in}K_{P3}K_{P2}}{LC}\\ \beta_2 &= \frac{3+3V_{in}K_{P3}K_{P2}}{LC}+\frac{V_{in}K_{P3}}{LR_bC}+\frac{V_{in}K_{P3}z_{PI_3}}{L}\\ \beta_3 &= \frac{V_{in}K_{P3}}{L}+\frac{1}{R_bC}\end{aligned}$$

By factoring the characteristic polynomial $\Delta_i(s)$, one gets:

$$\Delta_i(s) = \left(s+p_{i_{b1}}\right)\left(s+p_{i_{b2}}\right)\left(s+p_{i_{b3}}\right)\left(s+p_{i_{b4}}\right) \tag{34}$$

The poles of the system with closed output voltage loop and open battery current loop are:

$$\begin{aligned}p_{i_{b1}} &= -701.1 \text{ rad/s}\\ p_{i_{b2}} &= -1536 \text{ rad/s}\\ p_{i_{b3}} &= -1.137\times10^4 \text{ rad/s}\\ p_{i_{b4}} &= -3.8393\times10^4 \text{ rad/s}\end{aligned}$$

The root locus of the battery current loop is presented in Fig. 33.

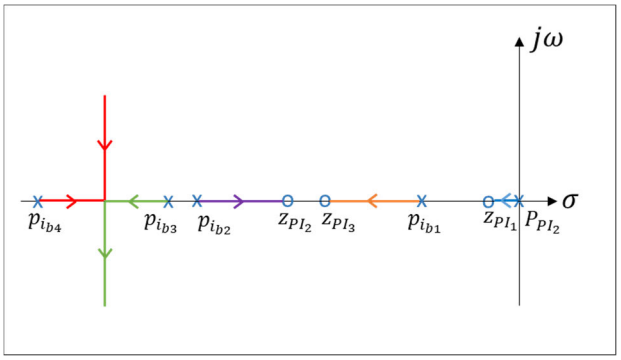

FIGURE 33. Root locus of battery current loop.

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