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Design of a Dual-Inverter Structure for a Point-to-Point Multifrequency Power Transfer

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ABSTRACT "This paper presents the design of a dual-inverter structure for multifrequency power transfer applications in microgrids. The proposed system significantly reduces filtering requirements throughout the microgrid by restricting the multifrequency operation to a specific section of the power distribution line. The dual-inverter device integrates two synchronized full-bridge inverters to enable independent control of voltage and current components at different frequencies. Expanding beyond a single device, a system configuration incorporating two sender/receiver dual-inverter devices enables multifrequency power exchange between nodes in a microgrid. The proposed system is validated through small-signal stability analysis, simulation results, and experimental testing of a demonstrator incorporating the enhancements developed in this work."

INDEX TERMS Inverter, multifrequency, third harmonic.

I. INTRODUCTION

The evolution of power distribution systems is addressing contemporary challenges affecting the grid's power quality, including issues such as the presence of harmonics, transients, and voltage fluctuations [1]. One primary factor contributing to these challenges is the increasing power demand [2], mainly driven by the growth in the adoption of DC systems, like in the integration of electric vehicle charging stations. Another critical aspect is the fragmentation of generating points due to the escalating use of Renewable Energy Sources (RES) [3], a consequence of the recognized environmental impact of the traditional energy sources. How to deal with RES irregular generation pattern is a central challenge in the current energy engineering era [4], emphasizing the critical role of efficient energy distribution and storage management in the integration of renewable energies.

In response to all these challenges, substantial progress has emerged from more adaptive and efficient distributions, mostly coming from microgrid type proposals [5]. In contrast to the traditional energy systems, where energy is often produced in large, centralized power plants located at far distances, microgrids offer a more decentralized approach with smaller energy-generating points closer to where it is consumed. This localized distribution reduces the power losses associated with long-distance electricity transportation and contributes to a more efficient utilization of the local resources of the microgrid, thereby facilitating the integration of RES.

Smart Grids (SG) serve as a clear example of decentralized energy management within a microgrid, as data is continuously exchanged between energy producers and consumers for better coordination and adaptability [6]. There are additional microgrid proposals specifically addressed to the integration of RES and the fulfillment of instantaneous power demand for DC consumers, such as Hybrid AC/DC microgrid distributions [7]. In this configuration, a DC power bus operates separately from the common AC Power Distribution Line (PDL) to supply exclusively the DC loads.

Exploring further into these combined systems (see Table 1), [8] investigates the benefits of unified AC/DC microgrids where a DC component (0 Hz) is superimposed onto the AC PDL (50 Hz). This configuration establishes an

TABLE 1. Combined Power Distribution Systems

Combined systems	Technology	Distribution	Power channels
Hybrid AC/DC [7]	SST or multi-stage	Separate Lines	AC, DC
MF AC+DC [8]	SST and AF	MF Line	AC, DC
MF AC1+AC2 [9]	SST	MF Line	AC, AC
MF AC1+AC2 [10]	Decentralized converters	MF Line	AC, AC

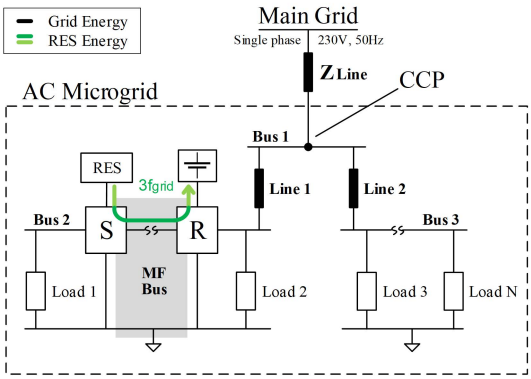

FIGURE 1. Example of a point-to-point power transfer by the decentralized AC1+AC2 type multifrequency system inside a Microgrid structure. At the multifrequency bus (MF Bus), S stands for Sender and R for Receiver.

AC+DC multifrequency (MF) system centrally controlled by a Solid-State Transformer (SST) responsible for the combined voltage regulation, located at its Common Connection Point (CCP) between the microgrid and the LV/MV grid. This approach simplifies the distribution infrastructure as it utilizes the existing AC distribution lines for both AC and DC power. However, additional power stages are required in the connection to the microgrid to perform an active filtering of the line signals, depending on whether the type of load requires AC or DC power, a drawback that increases with the microgrid size.

Other multifrequency systems achieve similar advantages for distribution simplification while reducing the filtering requirements. One case is the AC1+AC2 type multifrequency system from [9]. In this proposal, two synchronized converters are installed at the desired generating and consuming points as sender and receiver to perform a point-to-point power transfer through a secondary AC power channel (AC2). The central SST is the responsible for distorting the microgrid voltage with a new component at an additional frequency (150 Hz), different from the grid one (50 Hz), with an amplitude chosen by the allowable Total Harmonic Distortion (THD). The resulting low voltage component at 150 Hz makes the filtering action unnecessary in those specific cases where the presence of harmonics is not critical for the microgrid consumers. However, exchanging power through this AC2 channel requires of high currents that will face limitations in the PDL total current capacity. Additionally, this configuration brings inherent power losses, as all the microgrid loads withdraw current at 150 Hz.

In a previous work, [10] presents a decentralized approach for a point-to-point power transfer that is also based on an AC1+AC2 type multifrequency system. In this configuration, the sender and receiver converters limit the presence of AC2 distortion inside the defined section of the PDL where the selective power transfer is executed. Thus, the proposal allows the microgrid to forego the centralized management based on an SST, enabling it to operate in wider types of microgrid structures. To illustrate a possible scenario for this technology, Fig. 1 shows a microgrid structure where one RES is linked with one storage system by the proposed multifrequency system in a single-phase PDL. The green path represents the point-to-point power transfer through the secondary power channel AC2, with voltage and current components at 150 Hz. Since there is no distortion left outside the boundaries of the multifrequency section, no filtering action is required for those other PDL consumers.

Selecting a multifrequency approach enables the implementation of peak-shaping strategies [11] to control the peak voltage amplitude and the rms current values. The chosen frequencies (50 Hz + 150 Hz) result in the pseudo-squared voltage and current waveforms from (1). Assuming that $\sqrt{2}V_1$ remains within the cable's voltage range, selecting $V_3 = V_1/3$ and $\theta = 0$ ensures that the maximum value of $v(t)$ is approximately 94% of the peak amplitude of the grid harmonic component, $\sqrt{2}V_1$.

$$\begin{aligned} v_{bus}(t) &= \sqrt{2}\,V_1 \sin(\omega_0 t) + \sqrt{2}\,V_3 \sin(3\,\omega_0 t + \theta) \\ i_{bus}(t) &= \sqrt{2}\,I_1 \sin(\omega_0 t) + \sqrt{2}\,I_3 \sin(3\,\omega_0 t + \theta) \end{aligned} \quad (1)$$

Regarding the current rms values, assuming that I_M is the maximum rated rms current of the cable with a reasonable safety margin, restriction (2) must be fulfilled.

$$\sqrt{I_1^2 + I_3^2} \leq I_M \quad (2)$$

Since the loads at 50 Hz correspond to those of the preexisting single-frequency system ($I_3 = 0$ A), I_1 is treated as an independent variable having to comply with $I_1 \leq I_M$. Consequently, the current that could be injected by the 150 Hz power transfer utilizes the available cable "capacity" [12] not occupied by the 50 Hz transfer, leading to the restriction given in (3). It can be deduced that the $i(t)$ peak reduction will depend on the ratio between the two current components expressed in (4).

$$I_3 \leq \sqrt{I_M^2 - I_1^2} \quad (3)$$

$$r = I_3/I_1 \quad (4)$$

To clarify the system operation, Fig. 2(b) illustrates the internal structure of the conversion blocks used as sender and receiver. One single bidirectional structure has been designed to perform both roles, allowing the users to configure it at

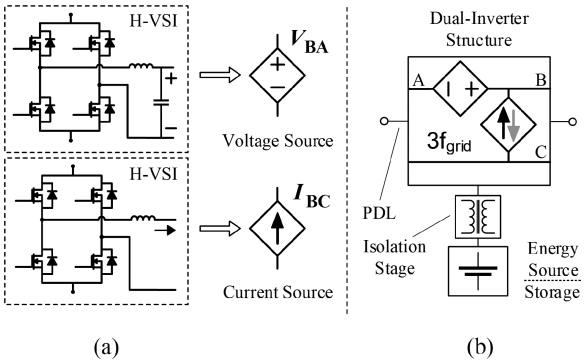

FIGURE 2. Diagram for the dual-Inverter structure. (a) Full-bridge voltage-source inverter used as one voltage and one current source. (b) Disposal of the different stages with the terminals A-B-C.

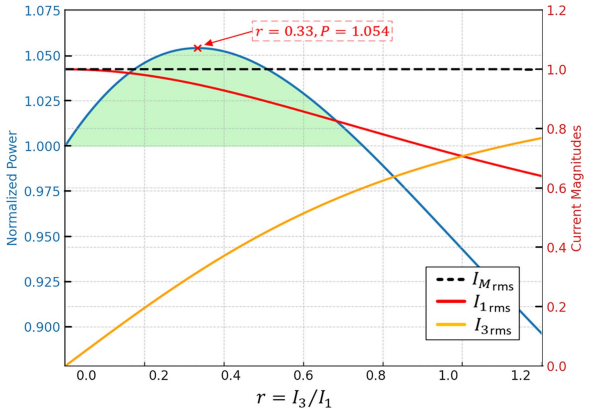

FIGURE 3. Multifrequency bus active power change by I_3/I_1 ratio.

the time of installation, depending on whether the conversion block is connected to an energy source or a storage system. The voltage source inserted in series to the PDL (*A* to *B* connection) is the responsible for regulating the additional voltage component V_{BA} at 150 Hz inside the multifrequency section, thus performing a voltage addition at the sender side and a synchronized subtraction at the receiver side. To accomplish the desired power transfer through the secondary power channel of AC2, the voltage component at 150 Hz requires an in-phase current component I_{BC} (see "the Principle of Orthogonal Power Flow" [13]). This current is provided by the current source connected in parallel to the PDL (*C* to *B* connection), allowing either to inject or extract current from the MF Bus. Additionally, Fig. 2(a) shows the implementation of each of these sources by one full-bridge voltage source inverter structure (H-VSI). To acquire their role as voltage or current source, each inverter requires a proper design of the AC output power filters and a suitable control strategy for direct regulation of the output voltage V_{BA} and current I_{BC}. Placing one isolation stage between the inverters and the energy source or storage system helps to decouple the performance of the converter from the irregular renewable generation or the State of Charge (SOC) of a possible battery.

The active power transmitted through the two-frequency bus can be obtained by averaging the instantaneous power through an integer number of periods of the two components (50 Hz and 150 Hz). Let's consider as the minimum averaging interval duration be the period of the 50 Hz signals, $T = \frac{1}{50\text{ Hz}} = 20$ ms.

$$P_{bus} = \overline{p_{bus}}(t) = \frac{1}{T}\int_{t_0}^{t_0+T} p_{bus}(\lambda)\,d\lambda = \frac{1}{T}\int_{t_0}^{t_0+T} V_{bus}(\lambda)\,I_{bus}(\lambda)\,d\lambda \tag{5}$$

According to the harmonics considered for the voltage and current in (1), the instantaneous power will have four components:

$$p_{bus}(t) = p_{11}(t) + p_{13}(t) + p_{31}(t) + p_{33}(t) \tag{6}$$

Where,

$$p_{11}(t) = 2V_1I_1\sin^2(\omega_0 t);$$
$$p_{13}(t) = 2V_1I_3\sin(\omega_0 t)\sin(3\omega_0 t + \theta);$$
$$p_{31}(t) = 2V_3I_1\sin(3\omega_0 t + \theta)\sin(\omega_0 t);$$
$$p_{33}(t) = 2V_3I_3\sin^2(3\omega_0 t + \theta);$$

By taking into consideration well known trigonometrical identities and the orthogonality principle, the active powers transmitted at 50 Hz and 150 Hz are,

$$P_{11} = \overline{p_{11}}(t) = V_1I_1;\ P_{33} = \overline{p_{33}}(t) = V_3I_3\cos\theta \tag{7}$$

while the mixed-frequency terms $p_{31}(t)$ and $p_{13}(t)$ have zero average and do not contribute to any active power transfer.

$$P_{31} = \overline{p_{31}}(t) = 0;\ P_{13} = \overline{p_{13}}(t) = 0 \tag{8}$$

From the expression of P_{33} it is clear that the active power at 150 Hz will be maximized for $\theta = 0$. The synchronization scheme between the 150 Hz and the 50 Hz signals is described in detail in Section III-A.

Finally, the active power of the multifrequency bus can be expressed as:

$$P_{bus} = V_1I_1 + V_3I_3 \tag{9}$$

Considering $V_3 = V_1/3$ and I_M restriction (2), the maximum power that the multifrequency system can transfer is given by:

$$P_{bus\_max} = V_1I_1 + \frac{V_1}{3}\sqrt{I_M^2 - I_1^2} \tag{10}$$

Then, introducing r into the equation,

$$P_{bus\_max} = \frac{V_1I_M}{\sqrt{1+r^2}}\left(1 + \frac{r}{3}\right) \tag{11}$$

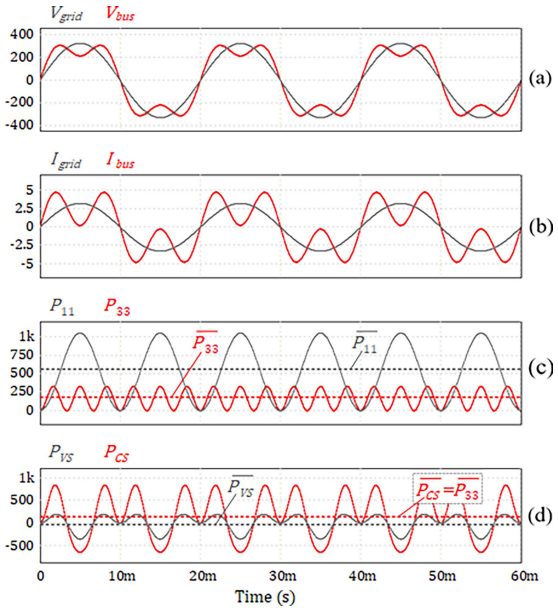

FIGURE 4. Dual-inverter signals. (a) Grid voltage V_{grid} and Bus voltage V_{bus}. (b) Grid current I_{grid} and Bus current I_{bus}. (c) Grid power P_{11} and AC2-channel power P_{33}. (d) Contribution to the power transfer of each source.

Fig. 3 illustrates the evolution of $P_{bus-max}$ as a function of the current ratio r (4), normalized to the power achieved by the conventional single-frequency power transfer under the same current limit I_M, where $P_{11} = V_1 I_M$. The figure demonstrates a power increase for $r \leq 0.75$, with a maximum power optimization of 5.4% at $r \approx 0.33$. For $r > 0.75$, line utilization becomes suboptimal, although multifrequency power transfer remains fully functional. However, this scenario is unlikely, as the dual inverter is primary designed to support secondary energy systems in the microgrid, where $I_1 \gg I_3$ is expected.

An example with $P_1 \approx 5$ kW and $P_3 \approx 1$ kW, with corresponding rms currents $I_1 \approx \frac{5\text{ kW}}{230} = 21.74$ A, and $I_3 \approx \frac{1\text{ kW}}{230/3} = 13.04$ A ($r \approx 0.33$), disregarding losses, is provided in Section V. See Figs. 29 and 30 and the associated text.

For better understanding, Fig. 4 illustrates the interactions between the dual-inverter structure and the microgrid signals, where: $V_1 = V_{grid}$; $V_3 = V_{BA}$; $I_1 = I_{grid}$; *and* $I_3 = I_{CB}$. Fig. 4(a) shows the grid voltage V_{grid} compared to the voltage signal V_{bus}, which results from the in-phase addition of V_{BA} inside the multifrequency section (sender behavior). Regarding the currents in Fig. 4(b), a similar waveform I_{bus} results from the in-phase addition of I_{BC}. Fig. 4(c) shows the different circulating effective powers in the system (7). Firstly, P_{11} is the power delivered to the grid loads connected at 50 Hz and it results from the single interaction of V_{grid} and I_{grid}. Secondly, P_{33} corresponds to the point-to-point transferred power between sender and receiver, with V_{BA} and I_{BC} components at 150 Hz. Lastly, Fig. 4(d) details the individual contribution to P_{33} of the independent sources that constitute the dual inverter. In the case of P_{VS}, corresponding to the voltage source, the resulting average power is close to zero and is a consequence of cyclical balancing with the receiver voltage source that is subtracting V_{BA} to limit the multifrequency section. The marginal value of P_{VS} corresponds simply to operating and conduction losses. On the other hand, the power P_{CS} resulting from the 150 Hz in-phase current injection performed at the current source corresponds to the totality of the transferred power P_{33}. Moreover, the action of the voltage source remains essential for the effectiveness of the power channel AC2.

This paper deepens into the hardware and control design of the dual-inverter structure, which is briefly described in [10]. It consequently provides a revised version of the circuit for the structure shown in Fig. 2(b). This document also compiles a comprehensive overview of the challenges encountered during the development of the converter, detected either through circuit analysis, simulation, or fieldwork experimental feedback. Finally, the corresponding adopted solutions for each challenge are presented.

The remainder of this paper is structured as follows: In Section II, improvements in the hardware design are discussed. Section III focuses on the control stage, addressing challenges arising from the digital implementation. Section IV includes circuit simulations to validate the adopted hardware and control solutions for the system stability and viability in the point-to-point power transfer. Section V presents the final prototype, supported by experimental results obtained in a validation setup. Finally, in Section VI, conclusions are drawn, and the advantages and limitations of the point-to-point power transfer multifrequency system are discussed.

II. DUAL-INVERTER STRUCTURE DESIGN

This section details the improvements made to the system's hardware. Each subsection discusses a relevant issue in the design process, delving into the available alternatives in the literature before concluding with a description of the adopted solution.

A. SHARED DC-SOURCE ISOLATION REQUIREMENTS

The isolation stage depicted in Fig. 2(b), positioned between the energy source and the two-inverter power stage, is highlighted in [10] as an unresolved issue regarding "a possibly required DC/DC module" between the inputs of each inverter. This stage is intended to provide galvanic isolation, as the system is designed to share a single DC energy source or sink (RES or storage system). Ignoring this point could lead to numerous system failures, as the main DC source can be short-circuited through the full-bridge structures. Fig. 5 illustrates two specific cases where a short circuit occurs through the common terminal (terminal B) due to random switching events arising from the independent control of the two inverters. Incorporating an isolation stage at the input of each inverter would prevent this issue by eliminating any electrical loop between the inverters. Furthermore, the decoupling introduced by the isolation stage would mitigate control-related challenges, such as preventing the distortion in the input DC voltage caused by the operation of one inverter from affecting the DC input of the other.

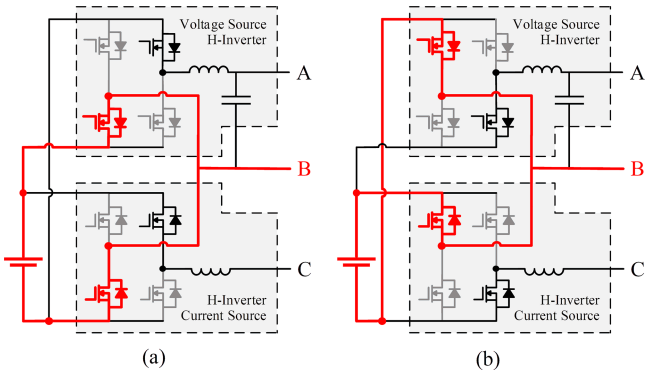

FIGURE 5. Particular scenarios where the DC Source is short-circuited through the common terminal B.

There exist consolidated solutions in the literature that meet the requirements for isolating various DC supplied converters. One common solution is the Dual-Active-Bridge (DAB) topology, primarily used to isolate storage systems due to its high efficiency [14]. With two full-bridge inverters connected around a high-frequency transformer, this isolated DC/DC converter transfers power by high-frequency switching of the DC source voltage across the primary side of the transformer, recovering it in DC mode through rectification on the secondary side. Applying a single-phase DAB stage to each DC input of the dual-inverter structure would provide the necessary isolation, while its bidirectional capability still allows to use a single design for both sender and receiver. Additionally, the presence of the transformer allows to configure a different ratio of turns from primary to secondary, lowering the voltage level requirements for the DC source or storage, thereby facilitating the integration of a greater variety of DC systems.

The possible resulting structure for the dual inverter applying two DAB stages is illustrated in Fig. 6(a). Now the system, including the two DAB, the VSI and CSI, has a total of six full-bridge active power structures that require at least four individual control loops.

In an effort to reduce the potential drawbacks in the control domain stemming from a substantial increase in active elements, alternative solutions in the literature have been examined. This is seen in [15], where a particular case of the Triple-Active-Bridge (TAB) topology with three ports connecting different energy sources and loads is presented. This DC/DC converter utilizes a single transformer with three windings, each one connected to one full-bridge structure that access one DC source or load. The resulting structure adopting one TAB stage for the dual inverter (Fig. 6(b)) reduces the number of active elements to five full-bridge structures and requires three control loops. However, sharing magnetics reintroduces cross-coupling issues, as power transients in one port can cause distortions in the others. The decoupling condition is recovered in [16] by using two individual transformers for the three ports of a TAB structure. Consequently, this structure brings complexity to the battery-side stage when collecting energy

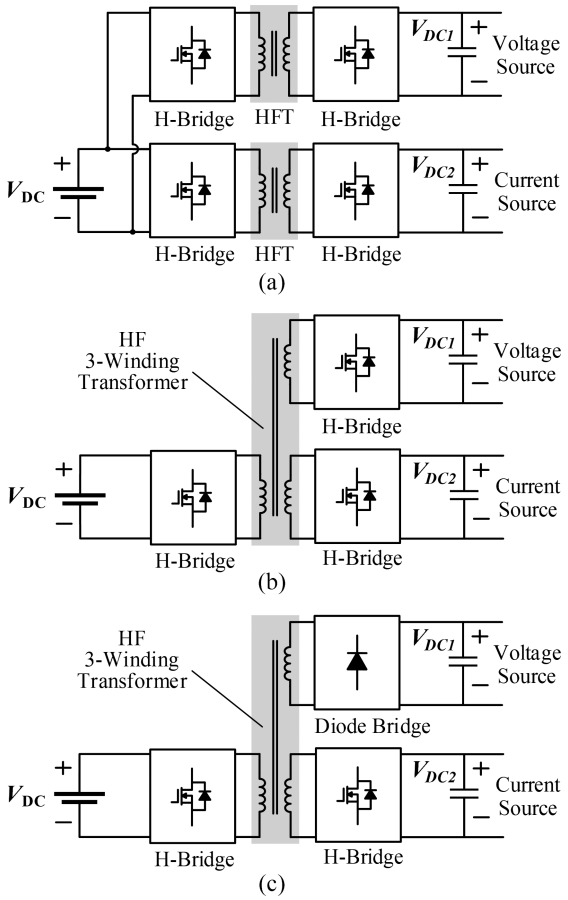

FIGURE 6. DC/DC isolating solutions for the dual inverter. (a) Two Dual-Active-Bridge (DAB) stages. (b) One Triple-Active-Bridge (TAB) stage. (c) A Three-port transformer with one DAB and one diode bridge (DB).

from two transformers with a single inverter, requiring additional active devices and making control more challenging.

Upon revisiting the analysis of circulating powers in the multifrequency bus during the point-to-point power transfer (see Fig. 4), the low consumption from the voltage source inverter has been considered as marginal compared to the current source. Given this, a less-efficient passive circuit supplying the voltage source would imply little impact on the total power loss while contributing to reduce the number of active power stages. Fig. 6(c) proposes an alternative for the three-port DC/DC stage combining active and passive ports. One active bridge links the energy source and the current source through two ports of the high-frequency transformer, similarly to the mentioned DAB structure [14]. On the third port of the transformer, one diode bridge supplies the voltage source, following the unidirectional concept of a high-frequency-link converter topology presented in [17] for grid integration of RES. Now, the voltage source's low consumption appears as a parasitic loss in the transformer for the DAB stage. This ensures the necessary galvanic isolation for the safe operation of the system and reduces the number of full-bridge active power stages down to four and three individual control

TABLE 2. Properties of DC-Isolating Stage Solutions

Properties	Solution (a)	Solution (b)	Solution (c)
Stages Combined	2x DAB	TAB	DAB + DB
HF Transformers	2 (Dual-Port)	1 (Three-Port)	1 (Three-Port)
Active Switches	16	12	8
Passive Switches	0	0	4
Control Complexity	Low	High	Low

loops. Additionally, for the voltage source's passive input, one switch controlling the activation of a resistor in parallel with the DC capacitor can help in the regulation of V_{DC1}. See a detailed comparison of each solution in Table 2.

B. INVERTERS OUTPUT FILTER SELECTION

Similarly to the majority of power electronic converters, Electromagnetic Compatibility (EMC) is a crucial aspect also for the dual-inverter structure, as its operation relies on the simultaneous functioning of both the voltage source and the current source. Electromagnetic Interferences (EMI) can occur in the form of conducted or radiated disturbances, and appear in switching converters from large voltage transients, high current switching, or parasitic elements within the circuit [18]. Failing to ensure EMC within a group of interconnected systems, such as a microgrid, can lead to the injection of undesired harmonics in the PDLs and the subsequent deterioration of the power quality. Additionally, a grid-tied converter that receives a high amount of Harmonic Distortion (HD) from either the line signals or a nearby system can experience malfunctions in certain control devices, putting in risk the correct operation of the converter. As pointed out in [19], properly filtering the output signals of the converter can significantly reduce the intensity of EMIs and improve the THD in the system.

To obtain low THD and enhance the system's compatibility, the inverter's output filters from [10] are redesigned with increased complexity to improve performance. To accommodate the additional resources required by the enhanced filter designs, an initial measure involved upgrading the Pulse-Width Modulation (PWM) technique from bipolar to a modified unipolar version, enabling the design of smaller filters for the given same output switching ripple specifications. It is important to note, as concluded in [20], that the THD improvement between bipolar and unipolar modulation techniques is negligible at high switching frequencies. However, the switching losses are halved.

Fig. 7 illustrates the key waveforms in the implementation of both techniques, bipolar and modified unipolar. The bipolar switching technique (Fig. 7(a)), results in only two possible output voltage levels for V_H modulated at the switching frequency: $-V_{DC}$ and $+V_{DC}$. As pointed in [21], the modified unipolar technique (Fig. 7(b)) obtains one additional level for the output voltage V_H: $-V_{DC}$, 0 V and $+V_{DC}$. With both inverters operating at 400 V (V_{DC1} and V_{DC2}) and 100 kHz

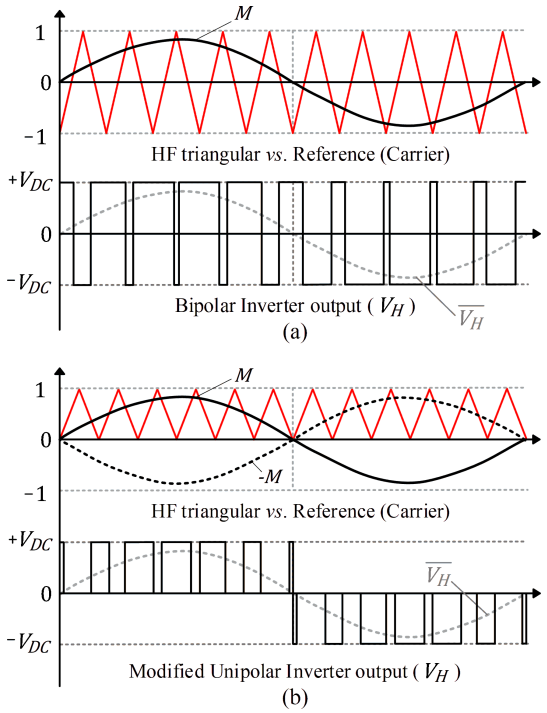

FIGURE 7. PWM-techniques implementation: (a) Bipolar and (b) Modified Unipolar.

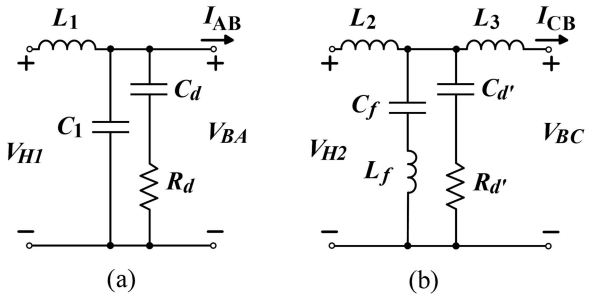

FIGURE 8. Proposed output filters for the dual inverter structure. (a) LC-RC filter for the voltage source. (b) LLCL-RC filter for the current source.

switching frequency (f_{sw}), the filters redesign results as follows.

At the AC side of the voltage source, the *LC-RC* filter illustrated in Fig. 8(a) is employed to reduce the high-frequency content from the full-bridge output signal V_{H1} and obtain the desired sinusoidal waveform of V_{BA} [22]. Firstly, the filter is formed by the main *LC* circuit (12), with values $L_1 = 640\ \mu$H and $C_1 = 1\ \mu$F resulting from the design procedure in [23]. Considering the inverter's switching frequency f_{sw} and the fundamental frequency of the output signal $f_0 = 150$ Hz, the filter's asymptotic corner frequency is intentionally set at $f_{res,\,LC} = 6.2$ kHz.The corresponding frequency response of the filter is depicted in blue on the Bode plot in Fig. 9. As expected, there is a resonance peak (13) at the corner frequency, a phenomenon inherent to all *LC* circuits that can introduce harmonic distortion and transients if it is not properly addressed [24]. To dampen the excitation of this

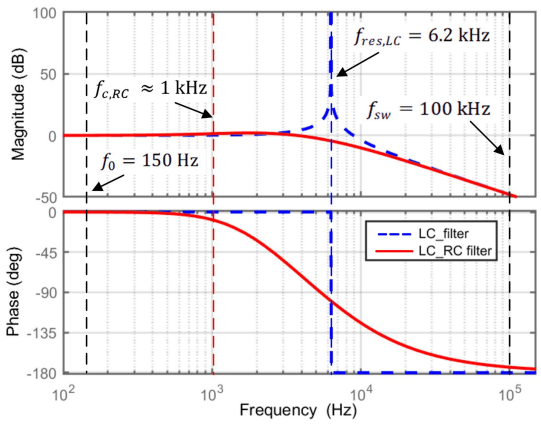

FIGURE 9. Bode diagram of the voltage source filter steps: LC filter (blue), Damped LC-RC filter (red).

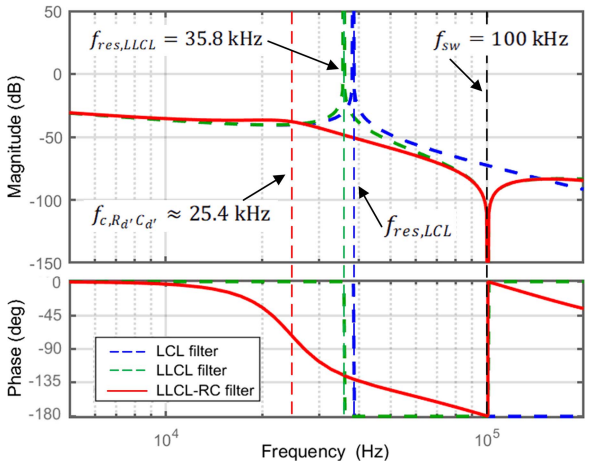

FIGURE 10. Bode diagram of the current source filter steps: LCL filter (blue), LLCL filter (green), Damped LLCL-RC filter (red).

resonance, the *LC-RC* filter incorporates a secondary branch consisting in a series *RC* circuit [25] in parallel to C_1. This new damping branch configures an earlier corner frequency (14) at $f_{c,\,RC} \approx 1$ kHz, with values $R_d = 15\ \Omega$ and $C_d = 10\ \mu$F.

$$H_{LC}(s) = \frac{V_{BA}}{V_{H1}}(s) = \frac{1}{1 + L_1 C_1 s^2} \tag{12}$$

$$f_{res,LC} = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{13}$$

$$f_{c,RC} = \frac{1}{2\pi\, R_d C_d} \tag{14}$$

Upon revisiting the Bode plot in Fig. 9, the *LC-RC* filter response in red depicts a significant attenuation of the *LC* filter resonance. The final transfer function $H_{LC-RC}(s)$ for the *LC-RC* filter implemented for the voltage source is presented in (15).

$$H_{LC-RC}(s) = \frac{V_{BA}}{V_{H1}}(s) = \\ = \frac{R_d C_d s + 1}{L_1 C_1 R_d C_d s^3 + (C_1 + C_d) L_1 s^2 + R_d C_d s + 1} \tag{15}$$

To obtain the sinusoidal current waveform of I_{CB} at the output of the full-bridge inverter implementing the current source, the *LLCL-RC* circuit shown in Fig. 8(b) is utilized. The depicted filter blocks the high-frequency harmonics present at V_{H2}, based on the working principle of the *LCL* filter. Opting for an *LCL*-type structure (16) allows significantly smaller inductors than in a conventional *L*-type filter, thanks to its greater damping effect [26]. However, increasing the order of the filter can make the inverter regulation more complex due to the increased phase lag and the inherent undamped resonance at $f_{res,\,LCL}$ (17), located relatively close to $f_{sw}/2$ (see Nyquist criteria [27]).

$$H_{LCL}(s) = \frac{I_{CB}}{V_{H2}}(s) = \frac{1}{L_2 L_3 C_f s^3 + (L_2 + L_3)\, s} \tag{16}$$

$$f_{res,\,LCL} = \frac{1}{2\pi}\sqrt{\frac{L_2 + L_3}{L_2 L_3 C_f}} \tag{17}$$

To improve the phase response of the filter, the *LLCL* (18) variation is proposed in [28], where an additional inductor L_f in series with C_f creates a frequency trap intentionally tuned at f_{sw}. This design achieves superior attenuation near the switching frequency compared to an *LCL* filter when identical values for L_2, L_3, and C_f are utilized. The values of each component are determined through the design methodology presented in [28] as: $L_2 = 1$ mH, $L_f = 20\ \mu$H, $C_f = 125$ nF, and $L_3 = 160\ \mu$H. The resulting filter's resonance (19) is now located at $f_{res,\,LLCL} = 35.8$ kHz.

To prevent this resonance to interact with other possible grid distortions at frequencies different from f_{sw}, [29] presents a precise passive *RC*-damping design to attenuate high-frequency harmonics in the *LLCL* filter. For this case, $R_{d'} = 25\ \Omega$ and $C_{d'} = 250$ nF set a corner frequency (19) of the *RC* damping branch at $f_{c,\,R_{d'}C_{d'}} \approx 25.4$ kHz.

$$H_{LLCL}(s) = \frac{I_{CB}}{V_{H2}}(s) = \\ = \frac{L_f C_f s^2 + 1}{\left(L_2 L_3 C_f + (L_2 + L_3) L_f C_f\right) s^3 + s\,(L_2 + L_3)} \tag{18}$$

$$f_{res,\,LLCL} = \frac{1}{2\pi}\frac{1}{\sqrt{\left(\frac{L_2 L_3}{L_2 + L_3} + L_f\right) C_f}} \tag{19}$$

The Bode plot in Fig. 10 illustrates the frequency responses of the different filters studied for the current source, comparing them with the adopted *LLCL-RC* circuit, drawn in red. The resulting transfer function $H_{LLCL-RC}(s)$ for the current source filter is presented in (20).

$$H_{LLCL-RC}(s) = \frac{I_{CB}}{V_{H2}}(s)$$

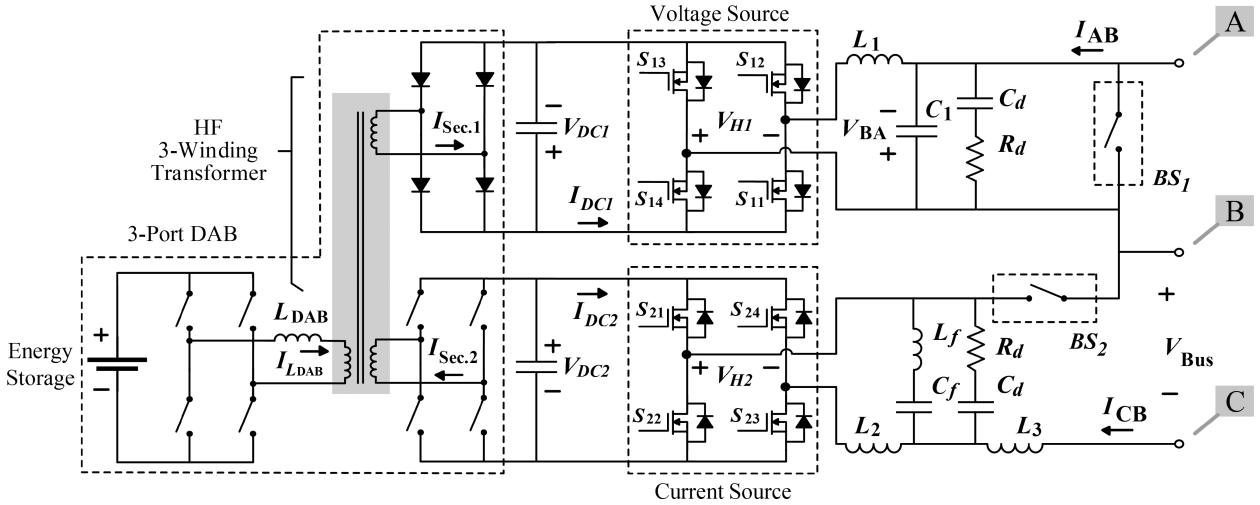

FIGURE 11. Proposed structure of the dual inverter power block with three connection points to the power distribution line (terminals A, B and C).

$$\frac{I_{CB}}{V_{H2}}(s) = \frac{L_f C_f R_{d'} C_{d'}\, s^3 + L_f C_f\, s^2 + R_{d'} C_{d'}\, s + 1}{a\, s^5 + b\, s^4 + c\, s^3 + d\, s^2 + e\, s} \tag{20}$$

Where,

$$a = L_2 L_3 L_f C_f C_{d'}$$
$$b = \left(L_2 L_3 + (L_2 + L_3)\, L_f\right) R_{d'} C_{d'} C_f$$
$$c = (L_2 L_3 \left(C_{d'} + C_f\right) + L_f C_f\, (L_2 + L_3)$$
$$d = R_{d'} C_{d'}\, (L_2 + L_3)$$
$$e = (L_2 + L_3)$$

C. CONVERSION BLOCK INTEGRATION.

Fig. 11 illustrates the complete structure for the dual inverter that integrates the technological solutions previously discussed for the DC/DC and AC/DC stages approached in Fig. 2(b). For the DC/DC stage, the three-port transformer from Section II-A supplies the current source with its active secondary port, while the voltage source is supplied by the passive third port. At the AC outputs of each inverter, the dual inverter uses the corresponding filters designed in Section II-B. Although no direct efficiency measurements were conducted on the proof-of-concept prototype, a preliminary estimation derived from the literature demonstrates the potential for achieving high efficiencies.

The TAB stage achieves 97% efficiency (η_{TAB}) for its active ports in [14], while the third port with a secondary diode bridge exhibits 90.6% efficiency (η_{DB}) in [17]. For the two full-bridge inverters forming the VSI and CSI, application notes [30] report an individual efficiency of 98.5% (η_{VSI} and η_{CSI}). Given the negligible power processed by the VSI relative to the CSI, as shown in Fig. 4, assuming $\overline{P_{CS}} \approx \overline{P_{33}}$, the overall efficiency is estimated as 95.5% as per equation (21).

$$\eta_{Total} \approx \eta_{TAB} \times \eta_{CSI} \tag{21}$$

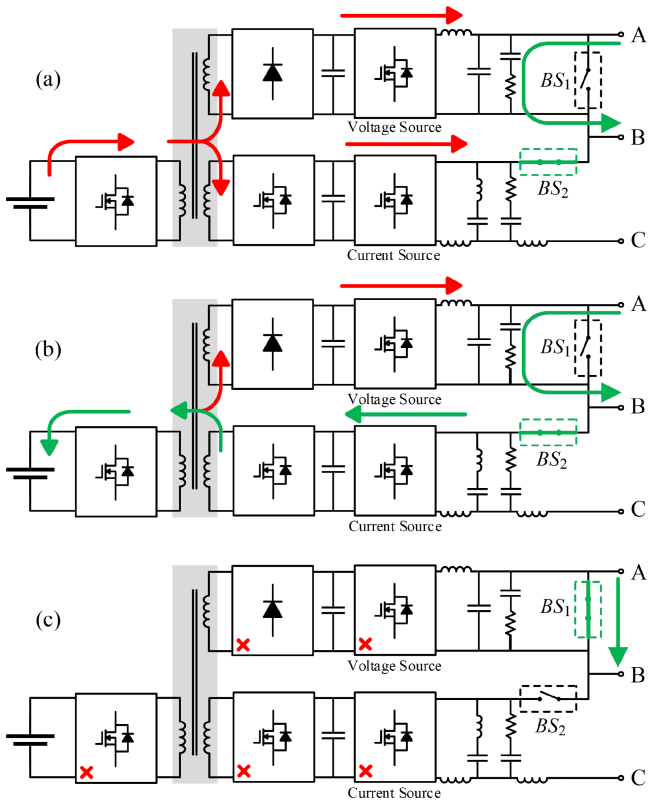

FIGURE 12. Dual inverter operating states: Active operation as (a) Sender and (b) Receiver. (c) Deactivated and bidirectional switches action.

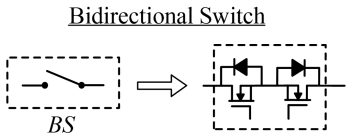

FIGURE 13. Equivalent circuit of the ideal bidirectional switch.

Fig. 12 details the operating protocols for the dual inverter, depicting three possible states: working as sender (Fig. 12(a)), operating as receiver (Fig. 12(b)), and deactivated (Fig. 12(c)). For the first two active states (Fig. 12(a) and (b)), the current source is the responsible for injecting or subtracting energy, depending on whether the system's role in the power transfer is either sender or receiver. During these two active states, the unidirectional voltage source regulates the third-harmonic voltage component synchronized with the grid.

To perform the Off-State where the dual inverter is deactivated (Fig. 12(c)), two bidirectional switches are included in the ABC-terminals connecting to the PDL. Even though the filters are designed to minimize the line power distortion, the presence of the damping branches can introduce additional power losses. Introducing bidirectional switches (Fig. 13) to neutralize the effect of the output filters contributes to reduce power losses while improving the system's robustness, acting as a protection in case of failures in any of the full-bridge structures. To deactivate the voltage source, the in-series connection with the PDL requires to close BS_1 to short-circuit A-B terminals and avoid the Line-current flow through $(C_1//R_dC_d)$. To deactivate the current source, the BS_2 opens the circuit and disconnects the C-B terminals from the MF bus.

III. CONTROL DESIGN

The active states of the converters, whether operating in sender or receiver mode, require the implementation of control loops to ensure proper regulation of voltage and current components. Additionally, for a successful 150 Hz power transfer, synchronization with the microgrid frequency, 50 Hz, is required for both the in-phase injection and extraction of the additional third harmonic components. Fig. 14 illustrates the control structure of the dual inverter, showing the block diagram for controlling the two inverters operating as output sources. Each inverter is individually controlled using the Unipolar-PWM technique at a 100 kHz switching frequency, with MOSFET safety ensured through appropriate dead-time selection.

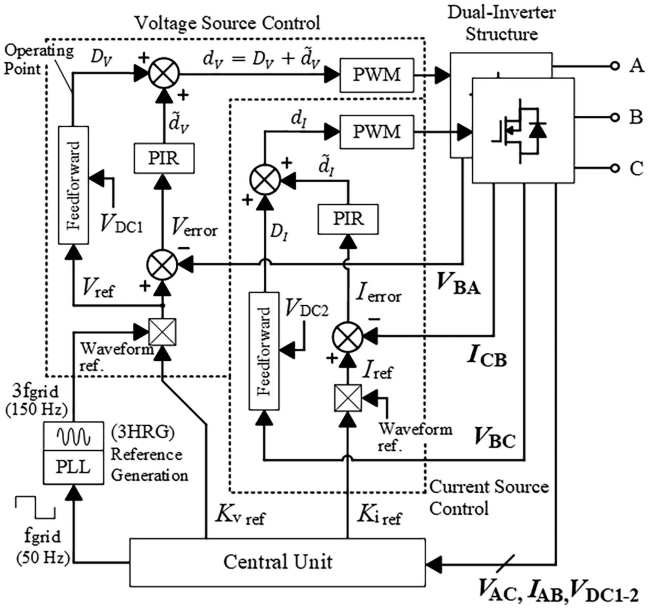

FIGURE 14. Dual inverter control stage diagram.

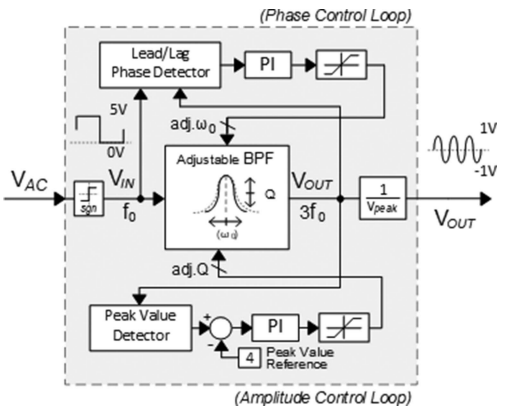

FIGURE 15. 3HRG BPF-based architecture.

A. THE THIRD HARMONIC REFERENCE GENERATOR

Possible fluctuations in the microgrid frequency can pose a challenge for converter synchronization if not properly accounted for. To address this, a Third Harmonic Reference Generator (3HRG), specifically designed for this work, provides a synchronized reference for the dual inverter. Its operation relies on a control approach inspired by a Phase-Locked Loop (PLL) [31], applied to an adjustable Band-Pass Filter (BPF).

The 3HRG system, illustrated in Fig. 15, captures the instantaneous grid frequency as a square wave signal and extracts a sinusoidal signal corresponding to the third harmonic through a filtering process. The 3HRG is designed to accommodate a ±1 Hz variation in the grid frequency, producing an output signal ranging from 147 Hz to 153 Hz ($\pm 3 \cdot 1$ Hz). This adaptive capability is achieved through the adjustable characteristic of the designed BPF, ensuring robust synchronization even under dynamic grid conditions.

The BPF serves as the central element, where two control loops are implemented to regulate key filter parameters. The first loop, a phase adjustment loop, ensures the central frequency (ω_0) is maintained around 150 Hz. The second loop regulates the quality factor (Q) by maintaining a constant output signal amplitude. The BPF general expression $H_{BPF}(s)$ is presented as follows:

$$H(s) = \frac{K \cdot \left(\frac{s}{\omega_0}\right)}{\left(\frac{s}{\omega_0}\right)^2 + 2\xi\left(\frac{s}{\omega_0}\right) + 1} \tag{22}$$

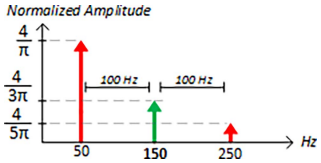

FIGURE 16. Main harmonics of a 50 Hz square wave signal.

Where,

$$\xi = \frac{1}{2Q};\ Q = \frac{\omega_0}{BW};\ \omega_0 = 2\pi f_0$$

Then, the gain of $H_{BPF}(s)$ at the central frequency ($s = j\omega_0$) is obtained, showing the well-known dependency on the filter's quality factor:

$$|H(j\omega_0)| = K \cdot Q \tag{23}$$

Fig. 16 illustrates the attenuation of harmonic components, following the Fourier series shown in (24) for the proposed square wave input signal at 50 Hz. The target frequency component to filter of 150 Hz has the adjacent harmonics positioned at a distance of 100 Hz.

$$x(t) = \frac{4}{\pi} \sum_{n=1,3,5,\cdots} \frac{1}{n} \sin(n\omega_0 t) \tag{24}$$

Notice in Fig. 16 that the first harmonic at 50 Hz exhibits a normalized amplitude three times greater than the third harmonic at 150 Hz. To minimize the impact of these adjacent harmonics on the BPF performance and obtain an undistorted 150 Hz output signal, a greater output amplitude is requested to the close-loop control, for this case 4 V_{peak}, thus configuring high Q factors. Consequently, a high Q results in a steep phase slope around the resonance frequency, leading to a narrowed bandwidth, a characteristic that makes the filter highly sensitive, where small variations in its configuration can lead to significant performance deviations. The active synchronization of the filter from Fig. 15, effectively mitigates these challenges by ensuring precise tuning of the filter. The experimental validation of the 3HRG is presented in Section VI.

B. VOLTAGE SOURCE CONTROL

In the Voltage Source Control (VSC), the control signal d_V consists of two components, derived from a combination of Positive Feedforward (PFF) and Negative Feedback (NFB) control strategies [32].

First, the PFF strategy generates a low-frequency control component, D_V, where a proportional controller takes the DC voltage V_{DC1} and sets the instantaneous operating point of the inverter based on the output voltage reference V_{ref} (25). The presence of the PFF helps to reduce the low-frequency AC requirement from the NFB control, leading to a reduction in the control effort. This allows more resources to be allocated

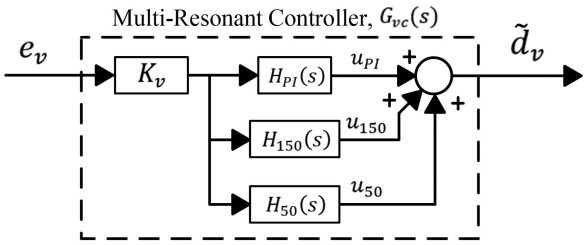

FIGURE 17. Structure of the Voltage Source Multi-Resonant controller $G_{vc}(s)$: Proportional-Integer-Resonant (PIR).

for the high-frequency tracking of the voltage reference.

$$D_V = \frac{V_{ref}}{V_{DC1}} \tag{25}$$

Second, to complement the control carrier D_V and maintain the desired voltage regulation, the NFB strategy feeds the remaining voltage error into a Multi-Resonant (MR) controller to generate the high-frequency control component $\tilde{d}_V$. This controller, characterized by Proportional and Resonant (PR) properties, provides the AC regulation requirement of the output with infinite gains at specific frequencies where the multiple resonances are set [33]. To avoid the stability problems derived from computing those resonant infinite gains, the PR controller is modified to a damped equivalent Quasi-Resonant (QR) controller. The finite gains at the resonance frequencies of the QR controller is a more suitable option for digital control, with proven superior performance and less computational costs [34]. An Integral characteristic (I) is added to prevent offset in the output signals due to differences in the response time of the switches, or asymmetries in the construction of the filters, or in the PCB routings.

Fig. 17 illustrates the QR controller structure used for the VSC. The equivalent transfer function of the controller, $G_{vc}(s)$ (26), describes the two resonances at the frequencies of 50 Hz and 150 Hz, with ω_c as the center frequency for each resonance, and B as the allowed bandwidth (2 Hz).

$$\begin{aligned} G_{vc}(s) &= \frac{d_v}{e_v}(s) \\ G_{vc}(s) &= K_v \cdot \left[H_{PI_v}(s) + H_{150_v}(s) + H_{50_v}(s)\right] \end{aligned} \tag{26}$$

Where,

$$H_{PI_v}(s) = \frac{u_{PI_v}}{e_v}(s) = K_{P_v}\frac{(1 + T_{i_v}s)}{T_{i_v}s}$$

$$H_{150_v}(s) = \frac{u_{150_v}}{e_v}(s) = \frac{K_{150_v}\, B\, s}{s^2 + Bs + \omega_{c150}^2}$$

$$H_{50_v}(s) = \frac{u_{50_v}}{e_v}(s) = \frac{K_{50_v}\, B\, s}{s^2 + Bs + \omega_{c50}^2}$$

The controller's parameters K_v, K_{P_v}, T_{i_v}, K_{150_v}, and K_{50_v}, are designed through the system's frequency response analysis. First, the system's Loop Gain $T_v(s)$ is required, which

TABLE 3. VSC Plant and Feedback Parameters

Voltage Source	Value
DC Link voltage	400 V
Switching frequency	100 kHz
LC-RC filter	L1 = 640 uH; C1 = 1 uF Cd = 2.85 uF; Rd = 15 Ω
Feedback bandwidth	25 kHz

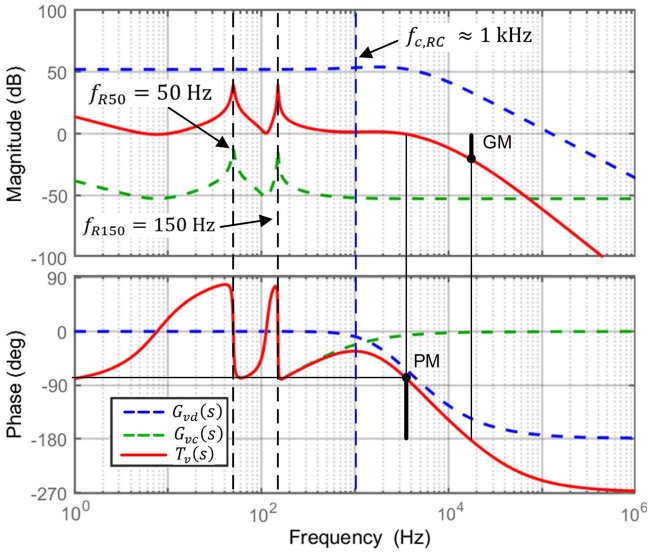

FIGURE 18. Bode diagram of the voltage source plant $G_{vd}(s)$ (blue), controller $G_{vc}(s)$ (green), and Loop Gain $T_v(s)$ (red). ($GM = 20$ dB, $PM = 107°$).

represents the cascaded behavior of all the stages involved in the VSC loop (27).

$$T_v(s) = G_{vd}(s) \cdot G_{vc}(s) \cdot H_{fb_v}(s) \tag{27}$$

Where, $G_{vd}(s)$ (28) is the control-to-output transfer function of the voltage source. $G_{vc}(s)$ (26) is the transfer function of the QR controller. $H_{fb_v}(s)$ (29) represents the frequency response of the voltage sensor, in this case a first-order low-pass filter with a cut-off frequency set at $f_{c_{fb}} \approx 25$ kHz for a given sampling frequency $f_s = 50$ kHz [27].

$$G_{vd}(s) = \frac{V_{BA}}{d_v}(s) = V_{DC1} \cdot H_{LC-RC}(s) \tag{28}$$

$$H_{fb_v}(s) = \frac{\omega_{c_{fb}}}{s + \omega_{c_{fb}}}; \quad \left(f_{c_{fb}} < \frac{f_s}{2}\right) \tag{29}$$

After substituting the parameters from Table 3 into equation (28), the open-loop frequency response of the system, $G_{vd}(s)$, is obtained and represented in blue in the Bode diagram in Fig. 18. The QR controller $G_{vc}(s)$ is tuned to ensure that the Loop Gain response of the VSC, $T_v(s)$, achieves a Gain Margin (GM) of at least 10 dB and a Phase Margin (PM) of no less than 60°. Its frequency response, $G_{vc}(s)$, is represented in green in Fig. 18 and exhibits significant attenuation

TABLE 4. VSC Controller Parameters

Controller	Value
Gain	$K_v = 2.3 \cdot 10^{-3}$
Proportional-Integral	$K_{P_v} = 1$; $T_{i_v} = 0.03$ s
Resonant	$K_{150_v} = 100$; $K_{50_v} = 100$; $B = 2$ Hz

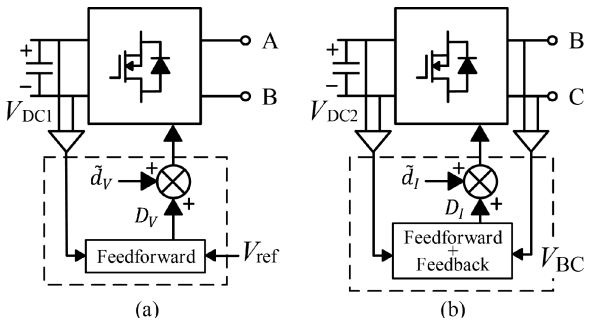

FIGURE 19. Different Positive Feedforward (PFF) strategies applied for each source control: (a) Voltage Source Control (VSC). (b) Current Source Control (CSC).

(−52 dB) for all frequencies except at the resonance peaks of 50 Hz and 150 Hz, each with narrow bandwidths of 2 Hz.

The resulting response for $T_v(s)$ is shown in the Bode diagram in red, presenting a gain margin of 20 dB and a phase margin of 107°, thus meeting the design criteria and ensuring small-signal stability. At the frequencies of 50 Hz and 150 Hz, the obtained gain is 40 dB for a 1% tracking error under VSC. Assuming a pure 150 Hz sinusoidal reference, the VSC closed loop response expects nearly 0 dB deviation of the output voltage V_{BA}, while ensuring no distorting of the 50 Hz component. Finally, the parameters used in this work for the VSC QR controller, $G_{vc}(s)$, are detailed in Table 4.

C. CURRENT SOURCE CONTROL

Similarly, for the second inverter implementing a Current Source Control (CSC), the control signal d_I combines two components. Firstly, a low-frequency component D_I to set the operating point of the inverter, and secondly, a high-frequency component $\tilde{d}_I$ for the reference tracking.

Despite the similarities in between the control strategy across the two inverters, the CSC differs from the VSC in its feedforward approach for obtaining the low-frequency component D_I. As depicted in Fig. 19, the VSC implements a PFF for the input voltage V_{DC1} while the CSC includes one additional feedback on the line voltage V_{BC} apart from the input voltage V_{DC2}. Reviewing each source connections with the PDL from Fig. 2 it is observable how, in contrast to the voltage source where the in-series A-B connection makes the V_{BA} addition independent from any grid distortion, the parallel connection B-C of the current source inside the MF Bus tides the output current I_{CB} (30) to depend on the V_{BC} line voltage variances $\tilde{v}_{BC}$. Calculating the operating point for D_I (31) from the ratio between the measured MF line voltage and

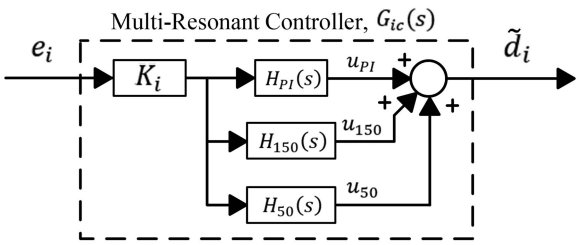

FIGURE 20. Structure of the Current Source Multi-Resonant controller $G_{ic}(s)$: Proportional-Integer-Resonant (PIR).

the input voltage V_{DC2} results in a Positive Feedback (PFB) [35] that sets the zero-current injection point over which the reference tracking from $\tilde{d}_I$ can regulate the desired output current I_{CB}. This approach endows the CSC a superior robustness against line voltage harmonics.

$$i_{CB}(s) = \frac{V_{H2}(s) - (V_{BC} + \tilde{v}_{BC})}{H_{LLCL-RC}(s)} \tag{30}$$

$$D_I = \frac{(V_{BC} + \tilde{v}_{BC})}{V_{DC2}} \tag{31}$$

Continuing with the description of the reference tracking controller for CSC, Fig. 20 depicts a similar QR structure for $\tilde{d}_I$ as the one from the VSC. The controller's equivalent transfer function $G_{ic}(s)$ (32) includes the two resonant peaks for 150 Hz and 50 Hz, with bandwidths B of 2 Hz.

$$G_{ic}(s) = \frac{d_i}{e_i}(s)$$

$$G_{ic}(s) = K_i \cdot \left[H_{PI_i}(s) + H_{150_i}(s) + H_{50_i}(s)\right] \tag{32}$$

Where,

$$H_{PI_i}(s) = \frac{u_{PI_i}}{e_i}(s) = K_{P_i}\frac{(1 + T_{i_i}s)}{T_{i_i}s}$$

$$H_{150_i}(s) = \frac{u_{150_i}}{e_i}(s) = \frac{K_{150_i}\, B\, s}{s^2 + Bs + \omega_{c_{150}}^2}$$

$$H_{50_i}(s) = \frac{u_{50_i}}{e_i}(s) = \frac{K_{50_i}\, B\, s}{s^2 + Bs + \omega_{c_{50}}^2}$$

Now, following the same design procedure for the VSC based on the system's response frequency analysis, the CSC system's Loop Gain $T_i(s)$ is obtained (33) to determine the controller's parameters K_i, K_{P_i}, T_{i_i}, K_{150_i}, and K_{50_i}.

$$T_i(s) = G_{id}(s) \cdot G_{ic}(s) \cdot H_{fb_i}(s) \tag{33}$$

Where, $G_{id}(s)$ (34) is the control-to-output transfer function of the current source. $G_{ic}(s)$ (32) is the transfer function of the QR controller. $H_{fb_i}(s)$ (35) represents the low-pass frequency response of the current sensor with a cut-off frequency set at $f_{c_{fb}} \approx 25$ kHz.

$$G_{id}(s) = \frac{I_{CB}}{d_i}(s) = V_{DC2} \cdot H_{LLCL-RC}(s) \tag{34}$$

TABLE 5. CSC Plant and Feedback Parameters

Current Source	Value
DC Link voltage	400 V
Switching frequency	100 kHz
LLCL-RC filter	L2 = 1 mH; Lf = 20 uH; Cf = 125 nF L3 = 160 uH; Cd = 2.85 uF; Rd = 15 Ω
Feedback bandwidth	25 kHz

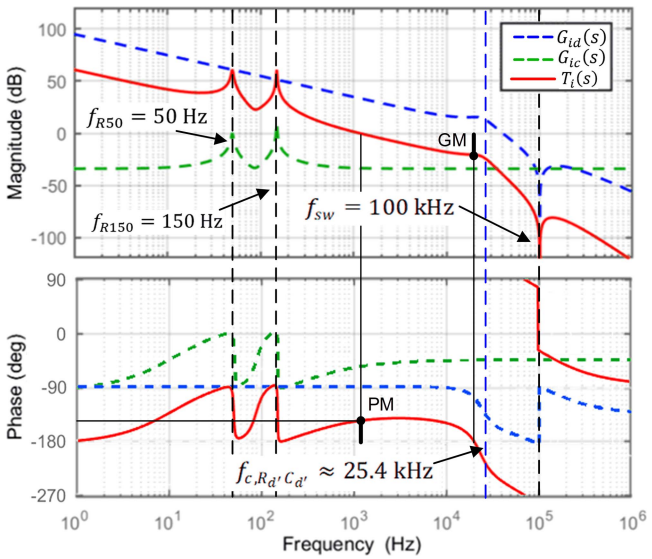

FIGURE 21. Bode diagram of the current source plant $G_{id}(s)$ (blue), controller $G_{ic}(s)$ (green), and Loop Gain $T_i(s)$ (red). (GM = 21 dB, PM = 68°).

$$H_{fb_i}(s) = \frac{\omega_{c_{fb}}}{s + \omega_{c_{fb}}} \tag{35}$$

The system's plant $G_{id}(s)$ is obtained by substituting the parameters from Table 5 into equation (34). The corresponding frequency response is depicted in blue in the Bode diagram from Fig. 21. Note that the plant's crossover frequency is about 40 kHz, too close to the sampling frequency of 50 kHz. A conservative design would usually place this crossover frequency one decade below, at about 5 kHz.

The QR controller, $G_{ic}(s)$, is tuned to ensure that the Loop Gain response of the CSC, $T_i(s)$, achieves a Gain Margin (GM) of at least 10 dB and a Phase Margin (PM) of no less than 60°. Placing the crossover frequency at about 1.2 kHz results in a good compromise between the closed-loop gain and phase margin. Its frequency response, $G_{ic}(s)$, is represented in green in Fig. 21, presenting big attenuation (-33 dB) for all frequencies except at the resonance peaks of 50 Hz and 150 Hz, each with narrow bandwidths of 2 Hz.

The resulting response for $T_i(s)$ is shown in the Bode diagram in red, exhibiting a gain margin of 21 dB and a phase margin of 68°, thus ensuring small-signal stability. The 60 dB gains of the resonant peaks result in a 0.1% tracking error of the 150 Hz sinusoidal output current reference for I_{CB} while

TABLE 6. CSC Controller Parameters

Controller	Value
Gain	$K_i = 0.01$
Proportional-Integral	$K_{P_i} = 2;\ T_{i_i} = 0.03$ s
Resonant	$K_{150_i} = 300;\ K_{50_i} = 100;\ B = 2$ Hz

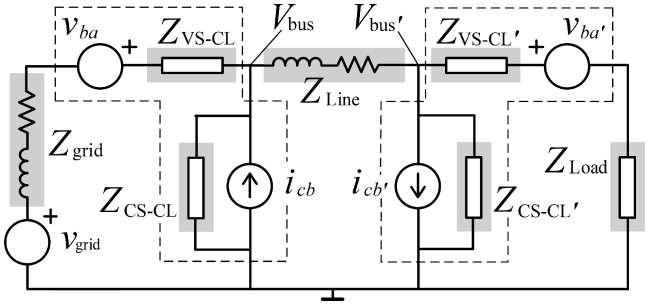

FIGURE 22. Microgrid structure under test.

ensuring the rejection of the 50 Hz perturbations. Finally, the parameters used in this work for the CSC QR controller, $G_{ic}(s)$, are detailed in Table 6.

Once the design procedures for the parameters of the different blocks of the control structure defined in Fig. 14 are completed, their equivalents in the z-domain are obtained for experimental implementation on a DSP.

For embedding the resulting control into the destiny board from Texas Instruments (Launchpad XL_F28379D), PSIM software environment is selected for its wide configuration capabilities and its automated code generation tool.

As the dual inverter control both sources together, the VS and the CS, and the time execution for the shared control DSP needs to ensure the completion of all the necessary calculations inside one sampling period. To achieve so without reducing the switching frequency f_{sw}, the sampling frequency for the Analog-to-Digital Converters (ADC) is reduced to $f_{sw}/2$. This modification provides a greater sampling period without affecting the system's performance as the frequencies of 50 Hz and 150 Hz are far below f_{sw}.

IV. STABILITY ANALYSIS

After completing the design of the inverters, the system's stability can be evaluated through impedance analysis under specific operating conditions, considering the effects of grid connection, line impedance, and load type. To this purpose, the configuration shown in Fig. 22 is analyzed.

This structure presents the equivalent impedance of a grid connection Z_{grid} (36) [36] on the left side; two dual inverters separated by the line impedance equivalent model, Z_{Line} (37); and the load impedance on the right side, Z_{Load}.

$$Z_{grid} = R_g + L_g s \tag{36}$$

$$Z_{Line} = R_L + L_L s \tag{37}$$

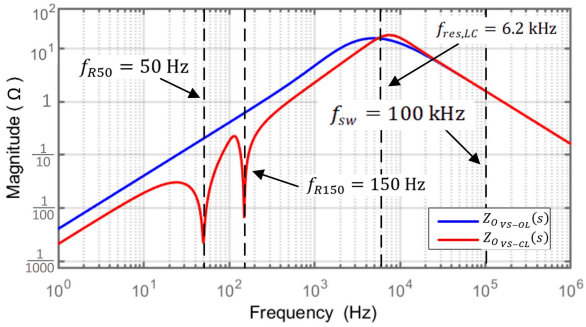

FIGURE 23. Bode diagram of the voltage source output impedance in Open Loop $Z_{O\,VS-OL}(s)$ (blue), and Closed Loop $Z_{O\,VS-CL}(s)$ (red).

To model the equivalent impedance circuit for the voltage sources of each dual inverter, a Thevenin equivalent circuit introduces an ideal voltage source v_{ba} in series with the inverter's equivalent output impedance in closed loop $Z_{O\,VS-CL}(s)$ (39).

Fig. 23 presents the Bode diagram depicting the frequency response for the voltage source inverters' impedance in open and closed loop configurations. The two traces intersect at the corner frequency of 6.2 kHz, where the total impedance reaches 15 Ω, corresponding to the corner frequency of the RC-branch of the output filter. Below this frequency, the effect of the closed-loop control results in a significantly reduced impedance compared to the open-loop case. Within this range, the impedance is particularly low at the frequencies of 50 Hz and 150 Hz, facilitating the operation at these frequencies. This behavior aligns with the intended frequency response of a 150 Hz sinusoidal voltage source [37].

$$Z_{O_{VS-OL}}(s) = \frac{v_{C1}(s)}{i_o(s)} = \\ = \frac{L_1 C_d R_d s^2 + L_1 s}{L_1 C_1 C_d R_d s^3 + (C_1 + C_d) L_1 s^2 + C_d R_d s + 1} \tag{38}$$

Then closing the loop,

$$Z_{O\,VS-CL}(s) = \frac{Z_{o\,VS-OL}(s)}{1 + T_v(s)} \tag{39}$$

To model the equivalent impedance circuit for the current sources of each dual inverter, a similar process is followed. This time, a Norton equivalent circuit introduces an ideal current source i_{cb} in parallel with the inverter's equivalent output impedance in closed loop $Z_{O\,CS-CL}(s)$ (42) as the inverse of the closed-loop admittance $Y_{O\,CS-CL}(s)$ (28). This admittance is obtained from the small-signal model by considering the open-loop output current response $\hat{i}_{L3}$ dependance on the voltage variations at its output $\hat{v}_{cb}$ (40), to later close the loop by adding the loop gain effect $T_i(s)$ (33).

The Bode diagram from Fig. 24 illustrates the frequency response for the current source inverters' impedance in open and closed loop configurations. The current source inverter

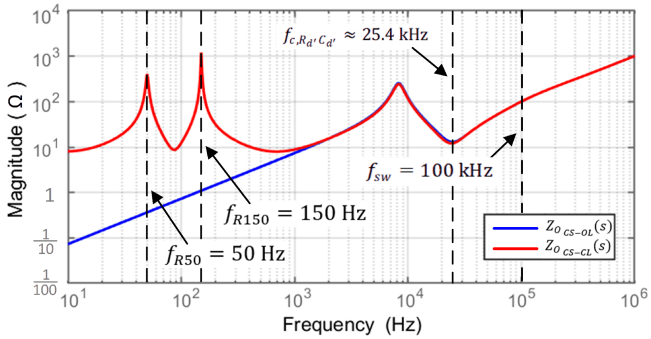

FIGURE 24. Bode diagram of the current source output impedance $Z_o(s)$ in Open Loop (blue), and Closed Loop (red).

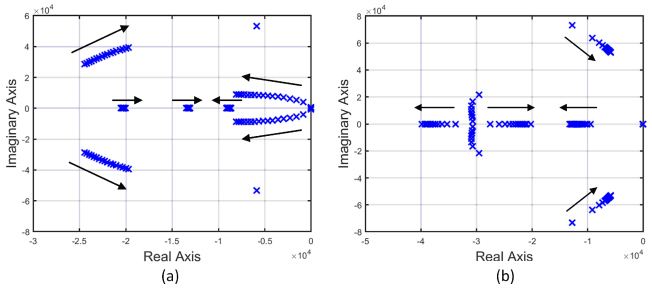

FIGURE 25. Root locus diagram of dominant poles for different load impedance, $Z_{load}(s)$, values: (a) capacitive-type ($\Omega + \mathbf{mF}$); (b) inductive-type ($\Omega + \mathbf{mH}$).

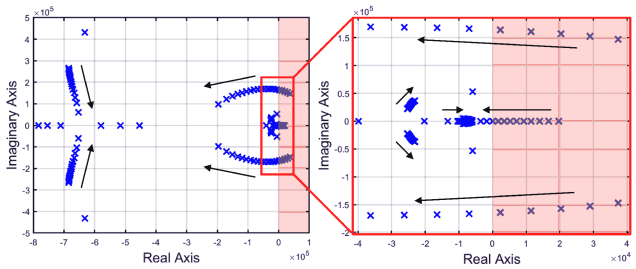

FIGURE 26. Root locus diagram of dominant poles for different load impedance, $Z_{load}(s)$, resistive values (Ω).

shows control capability across all frequencies below the corner frequency of the RC-branch, approximately 25.4 kHz. In this range of frequencies, the closed-loop impedance surpasses the open-loop in magnitude, aligning with the intended behavior of a current source [37]. At the operating frequencies of 50 Hz and 150 Hz the system exhibits high impedance. As expected for higher frequencies above the control bandwidth, the impedance increases and matches with an open-circuit behavior.

$$Y_{O\ CS-OL}(s) = \frac{i_{L3}(s)}{v_{cb}(s)} = \\ = \frac{\alpha\, s^4 + \beta s^3 + \gamma s^2 + C_d R_d s + 1}{a\, s^5 + b\, s^4 + c\, s^3 + d\, s^2 + (L_2 + L_3)\, s} \tag{40}$$

where,

$$\begin{aligned} \alpha,\ a &= L_2 L_3 L_f C_f C_d \\ \beta &= C_f C_d R_d (L_2 + L_f) \\ \gamma &= \left(L_2 C_f \left(C_f + C_d\right) + L_f C_f\right) \\ b &= C_f C_d R_d \left(L_2 L_3 + L_2 L_f + L_3 L_f\right) \\ c &= L_2 L_3 \left(C_d C_f\right) + C_f L_f \left(L_2 + L_3\right) \\ d &= C_d R_d \left(L_2 + L_3\right) \end{aligned}$$

Then closing the loop,

$$Y_{O\ CS-CL}(s) = \frac{Y_{o\ CS-OL}(s)}{1 + T_i(s)} \tag{41}$$

To finally obtain the closed-loop impedance,

$$Z_{O\ CS-CL}(s) = \frac{1}{Y_{o\ CS-CL}(s)} \tag{42}$$

The small-signal model from the structure presented in Fig. 22 is completed by substituting the derived impedances from equations (36), (37), (39) and (42). The resulting system of equations is shown in (43). To analyze stability, the system's characteristic equation is derived from any of the transfer function obtained from (43), for instance $\frac{V_{bus}}{I_{cb}}(s)$, assuming no zero-pole cancellation and therefore that all the closed-loop poles are observable. The system stability is determined by its poles position under a set of specific operating conditions [38], [35], as introduced in the following paragraphs. Moreover, the use of LTI methods in this stability analysis simplifies interpretation enabling root locus diagrams [39].

$$\begin{cases} I_{cb} = \frac{V_{bus}}{Z_{CS-CL}} + \frac{V_{bus}}{Z_{VS-CL}+Z_{grid}} + \frac{V_{bus}-V_{bus'}}{Z_{Line}} \\ \frac{V_{bus}-V_{bus'}}{Z_{Line}} = \frac{V_{bus'}}{Z_{CS-CL'}} + \frac{V_{bus'}}{Z_{VS-CL'}+Z_{Load}} \end{cases} \tag{43}$$

The first test analyses the effects of the load type over the system's stability considering a capacitive load. The system's pole locus diagram is presented in Fig. 25(a) with arrows pointing in the direction of the poles displacement. The load impedance, Z_{Load}, is varied for its capacitive component from 1 μF to 1 mF, with a fixed resistive component of 0.1Ω. The dominant poles at the lowest frequencies move from right to left indicating improved stability and better dynamic performance. However, increasing the impedance too much can have the opposite effect, as evidenced by the conjugate poles shifting from left to right. A similar response is obtained for the second test in Fig. 25(b), conducted with an inductive RL-type load. In this case, Z_{Load} varies in its inductive component from 1 μH to 1 mH, while the resistive component remains fixed at 0.1Ω. The poles displacements indicate a stable behavior throughout the variation.

For the third test, purely resistive loads are tested by varying Z_{Load} from -30Ω to 60Ω. The pole locus diagram in Fig. 26 initially exhibits unstable behavior caused by the negative values of Z_{Load}, reminding the linearized equivalent impedance

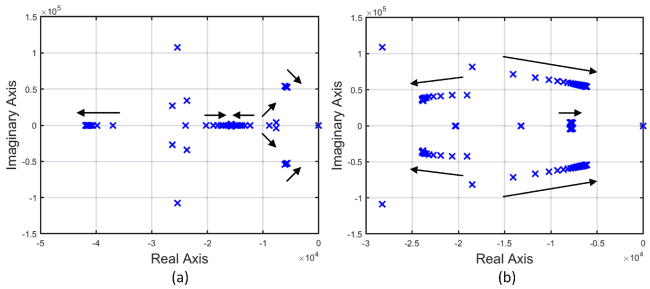

FIGURE 27. Root locus diagram of dominant poles for different values of: (a) Grid impedance $Z_{grid}(s)$ ($\Omega + \mathbf{mH}$); (b) Line impedance $Z_{Line}(s)$ ($\Omega + \mathbf{mH}$).

TABLE 7. Parameters for the Equivalent Impedances

Parameter	Distance	Value
Grid impedance, Z_{grid}	100 m	$R_g = R_L = 469\ \mu\Omega/\text{m}$
Line impedance, Z_{Line}	500 m	$L_g = L_L = 238.7\ \text{nH/m}$

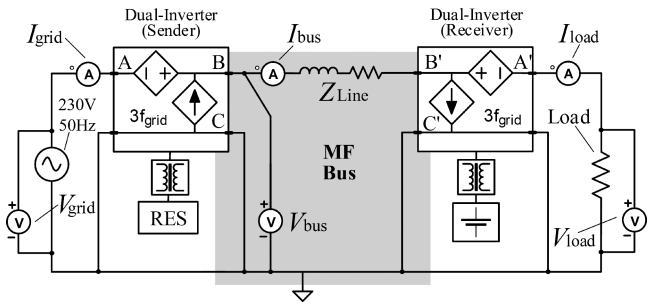

FIGURE 28. Simulation Schematic circuit of a single-phase microgrid (230 V, 50 Hz) with two dual-inverter structures.

of a constant power sink. Stability is restored once the dominant poles cross the real axis to the left, which occurs when a positive resistive value is applied to Z_{Load}.

The grid connection can also affect stability when considering a wide range of possible distances considering a constant resistive load, for this study $Z_{Load} = 10\Omega$. This case is depicted in Fig. 27(a), where the grid impedance (Z_{grid}) – both its real and positive imaginary components – is increased proportionally with the connecting cable length, ranging from 25 m to 500 m (see Table 7). The corresponding poles locus shows strong stability and limited displacement of poles. The same considerations can be applied for the line distance in between the two dual inverters, testing different values for Z_{Line} in Fig. 27(b) with similar results.

This study concludes that stability is ensured for all values of Z_{grid}, Z_{Line}, and Z_{Load} excluding power-sink behavior loads. Additionally, only overly big cable lengths affect the dynamic performance of the system. Consequently, stability and dynamic performance is improved with shorter distances.

V. SIMULATION RESULTS

The circuit shown in Fig. 28 is simulated in PSIM to verify the effectiveness of the dual-inverter structure in a point-to-point power transfer and to validate the designs outlined in the previous section. The circuit replicates the structure presented in Fig. 22, implementing a microgrid with one resistive load and two dual-inverter structures that link one RES to a storage system. The grid voltage is set to 230 V_{rms} at 50 Hz, and the resistive load is set to 10 Ω. The grid source impedance Z_{grid} and line impedance Z_{line} are defined as in Table 7. The two dual-inverter structures are configured according to the specifications in Table 3–6.

Fig. 29 shows the voltages and currents in the microgrid during the execution of a point-to-point power transfer from the RES to the storage system. The simulated sequence includes the operating states of start-up, active transfer, and stop of the dual-inverter structures. At 20 ms, the dual inverters are activated synchronously. The signals shown before this activation correspond to the interaction between the resistive load and the microgrid, exhibiting only 50 Hz voltage and current components on the multifrequency bus. Upon activation, the sender voltage source generates a 76.6 V_{rms}, 150 Hz component V_{BA} (Fig. 29(b), red). Simultaneously, the sender current source injects a 14 A_{rms} component I_{CB} in-phase with the additional 150 Hz channel (Fig. 29(b), green) to achieve a 1 kW point-to-point power-transfer. To receive the injected power, the receiver current source absorbs a matching 180° phase-shifted current component $I_{CB}{}'$ (Fig. 29(b), blue). Finally, the receiver voltage source compensates the added 150 Hz voltage component with $V_{BA}{}'$ (Fig. 29(b), black). The power transfer continues for 100 ms until a stop command is issued at 120 ms. During the active power transfer interval, the MF bus contains voltages and currents at both the fundamental 50 Hz frequency and the additional frequency 150 Hz (Fig. 29(c)). After 120 ms, the dual-inverter structures are deactivated, and the inverters are disconnected from the microgrid.

The power exchanges in the microgrid during this period are illustrated in Fig. 30. The grid power shows a 5.091 kW contribution P_{grid} at 50 Hz (Fig. 30(a)), matching the load consumption P_{load} of 4.924 kW (Fig. 30(b)). The dual-inverter systems exchange power at 1 kW level at 150 Hz, with the sender injecting 1.068 kW (P_{Sender}) (Fig. 30(c)) and the receiver extracting 1.053 kW ($P_{Receiver}$) (Fig. 30(d)). This results in a power exchange efficiency of 98.6% , with the remaining 1.4% attributed to line losses.

To assess the system's feasibility within a microgrid distribution, the THD in the load-side voltage V_{load} (Fig. 29(d), red) and grid current I_{grid} (Fig. 29(a), blue) are measured during the point-to-point power transfer, showing a THD of 1.59% in V_{load} and 1.54% in I_{grid}. These results are satisfactory, considering the allowable THD limit of 8% for voltages (in accordance with NE 50160, "Voltage Characteristics of Electricity Supplied by Public Distribution Networks") and 5% for currents (as per IEC 61000-3-2 and IEC 61000-3-4 standards for Electromagnetic Compatibility). The same measurements are repeated for a set of line distances (25, 250, and 500

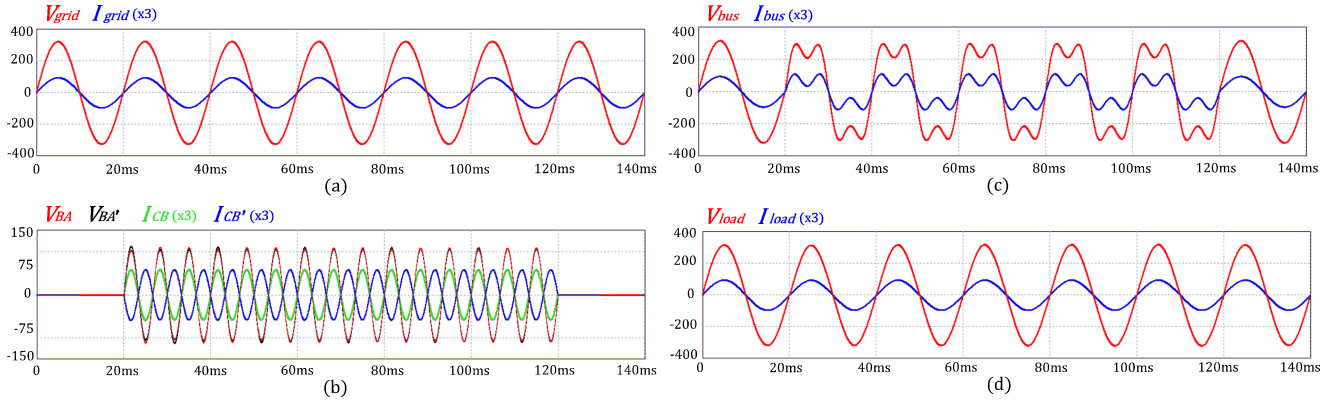

FIGURE 29. Simulation results of the microgrid with two dual-inverter structures performing a point-to-point power transfer.

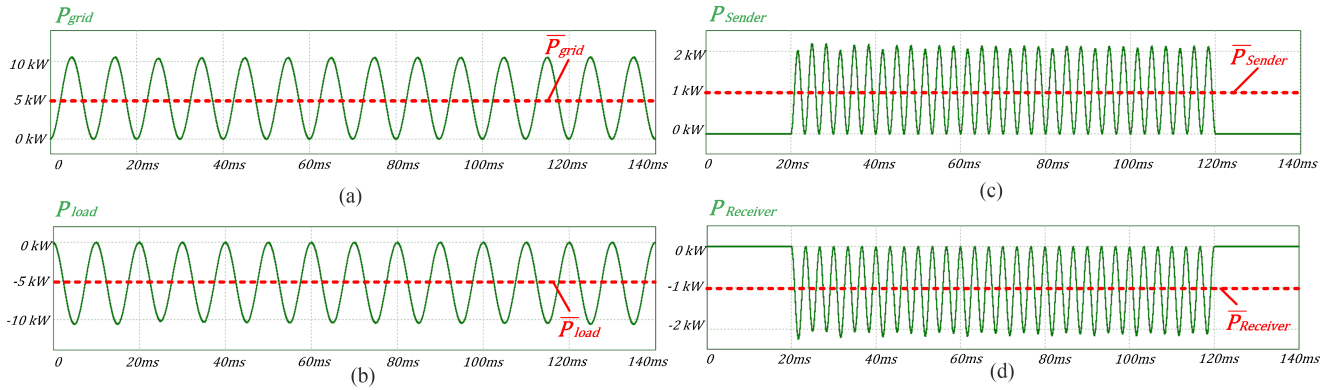

FIGURE 30. Power exchange in simulation in the microgrid with two dual-inverter structures performing a point-to-point power transfer. Power transfer.

TABLE 8. Load Voltage V_{load} THD for a Set of Power Levels And Line Distances.

Power / Distance	25 m	250 m	500 m
1 kW	0.11%	0.56%	1.59%
2 kW	0.14%	1.04%	2.08%
3 kW	0.17%	1.56%	3.12%

TABLE 9. Grid Current I_{grid} THD for a Set of Power Levels and Line Distances

Power / Distance	25 m	250 m	500 m
1 kW	0.22%	0.55%	1.52%
2 kW	0.31%	1.02%	2.04%
3 kW	0.40%	1.54%	3.07%

meters) and power levels (1, 2, and 3 kW), with the quantified THD obtained summarized in Tables 8 and 9, respectively.

The results compliance with the THD limits is demonstrated across all tested power levels and line distances, with the highest observed THD values being 3.12% for V_{load} and 3.07% for I_{grid}, recorded during a 3-kW power transfer over a 500 m line. The greater line impedance and the operation with greater currents exacerbate non-linear effects in the transmission line and switching components, further amplifying harmonic content. Consequently, these results confirm that while the system's THD remains well within acceptable limits, the influence of line distance and power levels on harmonic distortion may become a limitation for higher ranges.

VI. EXPERIMENTAL RESULTS

The experimental demonstrator for the dual-inverter structure presented in [10] has been upgraded accordingly with the control and hardware designs reviewed in this work. As shown in Fig. 31, the hardware updates are illustrated. The demonstrator now includes newly designed output filters, as described in Section II-B, positioned between the full-bridge structures and the connections points A-B-C. The voltage source's filtering circuits have been updated from LC-type to LC-RC type, while the current source's filter, previously an L-type, is now an LLCL-RC type. To ensure symmetry, each inductor has been split, making the inductive paths symmetrical for both polarities. Reducing conducted EMI propagation paths has been shown to be effective in significantly decreasing the THD of output currents, particularly in LCL-type circuits [40]. If required, further symmetry can be achieved by also splitting the capacitors [41].

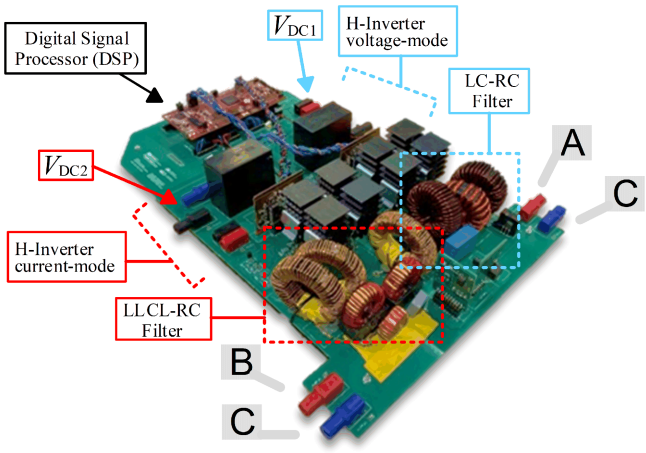

FIGURE 31. Proof-of-concept prototype of the dual-inverter source/sink with upgraded output filters (22 cm x 40 cm).

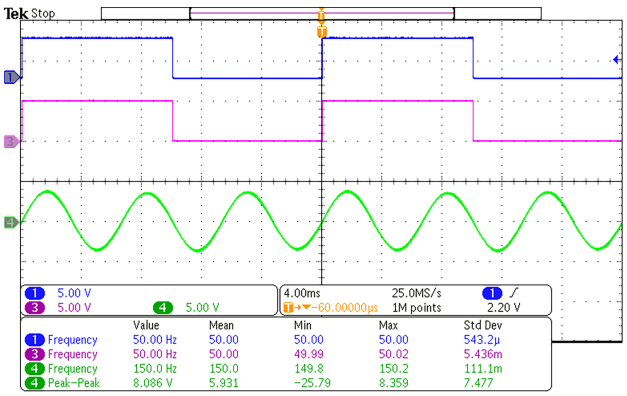

FIGURE 32. 3HRG Signals: grid frequency (blue); square waveform 50 Hz filter input signal (pink); sinusoidal 150 Hz filter output signal (green).

The power stage description continues similarly as in [10]. Each of the two H-bridge inverters employs a total of eight C3M0120090D Silicon Carbide MOSFETs (900 V, 23 A, 120 mΩ) with individual heat sinks. Four IR2110 dual-driver devices control the four inverter legs, while four IL611 digital isolators provide the PWM signals from the controller. The two four-quadrant bypass switches use IPW60R041C6 MOSFETs (650 V, 49 A, 41 mΩ). Voltage sensing for V_{BA}, V_{BC}, V_{AC}, V_{DC1}, and V_{DC2} is accomplished via the ACPL-C79B-000E differential-mode isolation amplifier, and current sensing for I_{AB} and I_{CB} is achieved with the LEM HO 25-P current transducer. Several ISE1515 and ISE1505 low-power DC/DC isolated converter modules supply the drivers, control, and sensing circuits.

The system includes a Digital Signal Processor (DSP) board, one Texas Instruments Launchpad XL-F28379D, to control the inverters. The programming code is generated using the PSIM and Code Composer Studio.

Firstly, the experimental validation of the 3HRG is presented. In Fig. 32, a 150 Hz sinusoidal output waveform (green) is obtained after processing the captured 50 Hz grid

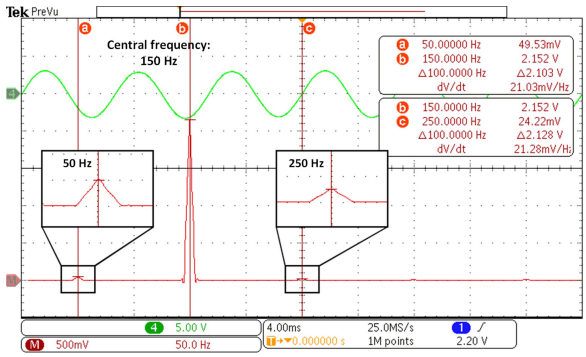

FIGURE 33. FFT in linear scale: 150 Hz filter output signal (green); corresponding FFT (red).

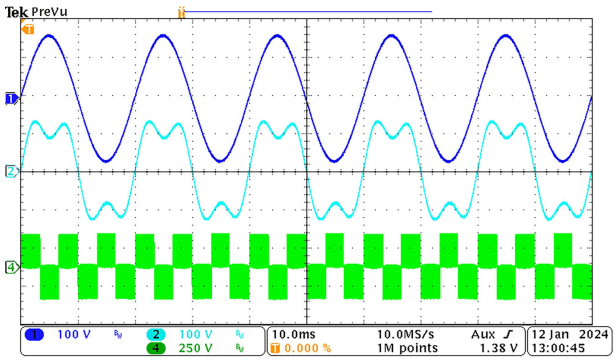

FIGURE 34. Voltage source's waveforms after the activation of the dual-inverter structure. (CH1) V_{AC} line voltage at 50 Hz; (CH2) V_{BC} internal voltage of the MF Bus; (CH4) V_{H1} output voltage of the voltage source before the LC-RC filter.

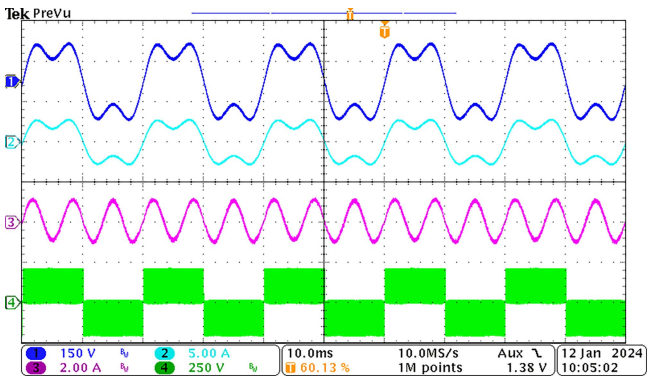

FIGURE 35. Current source's voltage and current waveforms after the activation of the dual-inverter structure. (CH1) V_{BC} internal voltage of the MF Bus; (CH2) I_{Bus} internal current of the MF Bus; (CH3) I_{CB} generated current component at 150 Hz; (CH4) V_{H2} output voltage of the current source before the LLCL-RC filter.

frequency in a square waveform (pink). Fig. 33 illustrates the FFT of the obtained 3HRG output signal, quantifying the impact of the contiguous harmonics at 50 Hz and 250 Hz (see Fig. 16), demonstrating a low total harmonic distortion THD

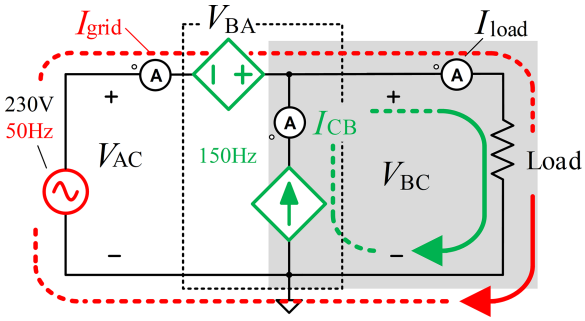

FIGURE 36. Proposed distribution diagram of the validation test for one dual-inverter structure.

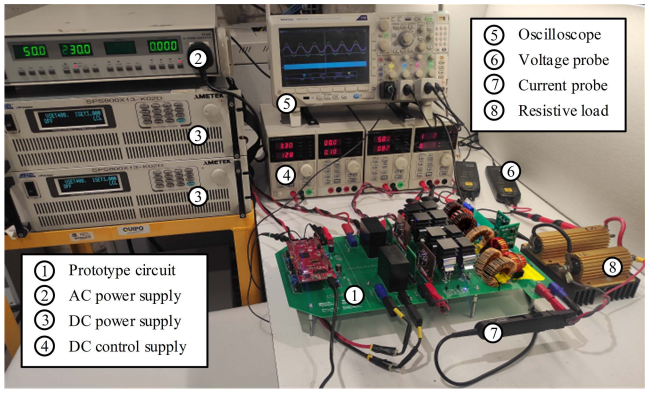

FIGURE 37. Experimental setup to test one dual-inverter structure with an AC voltage source and one resistive load.

of 2.56% . Additionally, the observed in-phase synchronization with the grid frequency confirms the 3HRG as a reliable reference generator for the dual inverter.

Fig. 34 demonstrates the generation of the additional voltage component V_{BA} by use of the modified unipolar PWM technique, replacing the bipolar one used in [10]. In this configuration, V_{AC} represents the grid voltage prior to adding V_{BA} , and V_{BC} denotes the internal voltage of the MF Bus. The output voltage V_{H1} of the voltage source full-bridge inverter, before the LC-RC filter, switches in the positive range (0 V to $+V_{DC1}$) during the positive half-cycle of V_{BA} and in the negative range ($-V_{DC1}$ to 0 V) for the negative half-cycle of 150 Hz. In the oscillograms, from Fig. 34 onwards, Vdc has been configured to 200 V for safety reasons.

To verify the I_{CB}current generation with the unipolar modulation technique, Fig. 35 shows the output voltage V_{H2} of the current source full-bridge inverter before the LLCL-RC filter. Unlike the voltage source inverter, the current source inverter is connected in parallel with the MF bus. Thus, the inverter's positive switching range, between 0 V and $+V_{DC2}$, is observed throughout the positive half-cycle of I_{Bus} (50 Hz grid voltage) and in the negative range ($-V_{DC2}$ to 0 V) during the negative half-cycle. The resulting voltage and current signals indicate an in-phase addition of V_{BA} and injection of I_{CB}.

To validate experimentally this proof-of-concept prototype, the Sender test depicted in Fig. 36 is performed. In the shown schematic distribution, an AC source (230 V, 50 Hz) is connected between the A and C points of the demonstrator to emulate the microgrid voltage. Between B and C points, a resistor (100 Ω) is the chosen load to interact with the microgrid signals at the multifrequency side.

By adding the voltage component V_{BA}, the resistive load will induce a current distortion at 150 Hz that will flow through the grid AC source. To validate the system capability to limit the presence of multifrequency components to only the inside of the multifrequency designated region, activating the current source compensates the 150 Hz current component demand by injecting I_{CB}, thus avoiding distorting the microgrid signals.

Fig. 37 shows a photograph of the corresponding experimental setup. For the AC voltage source, an APS FC200 AC

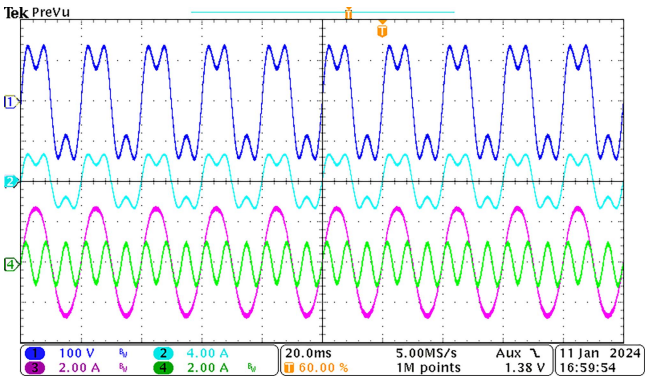

FIGURE 38. Voltage and current waveforms after the activation of the dual-inverter structure. (CH1) V_{BC} load voltage; (CH2) I_{load} current across the load; (CH3) I_{grid} grid's current contribution; (CH4) I_{CB} current injection at 150 Hz.

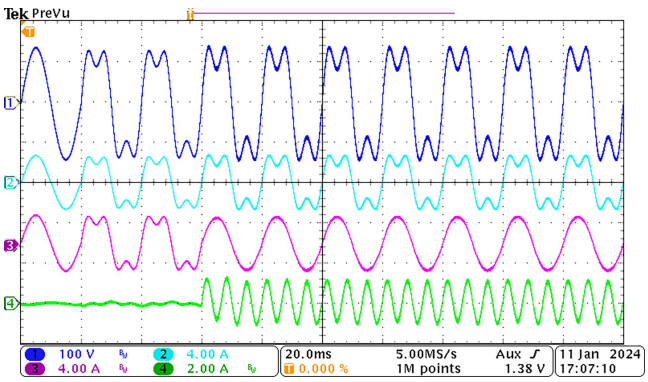

FIGURE 39. Voltage and current waveforms during a sequential activation of the dual-inverter structure. (CH1) V_{BC} load voltage; (CH2) I_{load} current across the load; (CH3) I_{grid} grid's current contribution; (CH4) I_{CB} current injection at 150 Hz.

power supply (1 kW, 300 V rms, 45-500 Hz) is used at 50 Hz and 230 V_{rms}; two Ametek SPS800X13-K02D.

DC power supplies (1.2 kW, 800 V, 150 A) provide the DC voltage to each inverter DC input V_{DC1} and V_{DC2}; and two TENMA 72-10505 (90 W, 30 V, 3 A) are used to supply

the control circuits. To measure and capture the electrical variables, the setup includes: a Tektronix MDO3014 (100 MHz, 2.5 GS/s) oscilloscope; three Tektronix THDP0200 (200 MHz, 1500V) differential probes; and one Tektronix TCP2020 (20 A rms) current probe. Fig. 38 shows the resulting signals in the circuit during this test. The observed signals follow the expected behavior represented in Fig. 36, where the grid's current follows the red path controlled by the grid voltage source, while the third-harmonic currents follow an inner path in between the load and the dual-inverter structure.

Additionally, Fig. 39 shows a test where the additional voltage and current sources are activated with an intentional delay. From instant 0 to 0.02 seconds the dual-inverter structure is inactive, the circuit signals are at 50 Hz with null I_{CB} current injection. From 0.02 to 0.06 seconds, the voltage source is activated, applying the additional voltage component V_{BA} to the load. During this period, the resulting current distortion in I_{grid} persists until 0.06 seconds, when the current source is activated, supplying the corresponding 150 Hz component. As a result, the grid current returns to an undistorted 50 Hz waveform.

VII. CONCLUSION

This paper has presented a detailed design and experimental evaluation of a dual-inverter structure tailored for a point-to-point multifrequency power transfer within microgrid structures. The proposed system combines hardware and control enhancements that allow for independent voltage and current modulation at different frequencies, demonstrating promising capabilities for decentralized power distribution applications.

The key advantages of the dual-inverter design include its ability to inject specific frequency components into the multifrequency bus without impacting the remaining grid signals outside the multifrequency region. By effectively isolating voltage and current contributions, the system supports advanced functionalities such as active filtering and harmonic compensation, which could improve power quality and the integration of nonlinear loads. Moreover, the implementation of high-performance filtering circuits, such as the LLCL-RC for the current source, has proven effective in mitigating EMI and maintaining harmonic distortion within allowable limits, even as line distance and power levels vary.

Additionally, various studies conducted in this work confirm the system's reliability, achieving high transfer efficiencies and stable operation, which reinforces its suitability for selective power transfer applications. However, potential limitations were identified, particularly regarding harmonic propagation when larger sections of the microgrid are involved or when distorted loads are connected to the MF bus, highlighting the need for additional filtering stages.

In summary, the dual-inverter structure offers a flexible solution for multifrequency power transfer in microgrids, with potential applications beyond point-to-point systems. Future work should include the measurement of system efficiency, with a detailed analysis of energy losses across the switching, filtering, and transformer components, which were not addressed in this proof-of-concept phase. Optimizing the system for configurations with multiple sender-receiver pairs and larger power transfer capacities remains a key task for future investigations. Additionally, further research could explore the application of this technology in different fields, as its versatility in enabling individual control over voltage and current components have a wide path in the field of microgrids power quality and active filtering.

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