IEEE Open Journal of
Power Electronics

Received 7 March 2025; revised 3 April 2025; accepted 9 April 2025. Date of publication 16 April 2025;
date of current version 15 May 2025. The review of this article was arranged by Associate Editor Liangzong He.

Digital Object Identifier 10.1109/OJPEL.2025.3561671

Coupled-Inductors Boost Converter With Quasi-Square-Wave Zero-Voltage-Switching

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This work was supported in part by the Universitat Rovira i Virgili and Diputacion de Tarragona under Grant Marti Franques 2019 PMF-PIPF-95 and Grant PID2021-124229NB-I00 funded by MCIU/AEI/10.13039/501100011033 and in part by the "ERDF/EU".

ABSTRACT In this article, the Quasi-Square-Wave (QSW) mode with Zero-Voltage Switching (ZVS) in the Coupled Inductors Boost (CIB) converter is thoroughly analyzed to provide design guidelines and compare the obtained performance with the QSW-ZVS boost converter. The studied mode is used to enforce output voltage regulation employing a nested loop architecture with an inner current loop and an outer voltage loop providing the reference for the inner loop. The current controller is an innovative hysteresis control in which the upper limit compares the secondary inductor current with the reference provided by the outer loop and the lower limit compares the primary inductor current with a constant value defined to ensure ZVS. This configuration allows the elimination of the right-half-plane zeros inherently widening the bandwidth of the frequency response. As it is demonstrated, the CIB exhibits two times faster dynamic response in front of load perturbations at the cost of a small reduction of the efficiency at high power loads and the inclusion of two additional components. Theoretical predictions and feasibility of the QSW-ZVS CIB are confirmed by means of simulated and experimental results.

INDEX TERMS DC-DC power converters, zero-voltage-switching (ZVS), soft switching, fast dynamics, boost converter.

I. INTRODUCTION

Nowadays, power electronics converters play a main role in different technology industry such as: electric vehicle (EV), solid-state transformer (SST), data center and even space applications. Mainly, those applications requirements are highly sensitive, starting from the fault tolerant to fast dynamic and high efficiency. The last two features are critical, especially in some application like data center wherein the processor can have abrupt changes from low load to full load. These fast changes should be compensated and need a power supply with faster response. Moreover, efficiency is a critical feature due to those applications should not be switched off and keep running with the lowest power loss for long time.

PWM boost converter is a canonical DC-DC step-up circuit used in widespread of applications from the lower-portable devices to high-power systems [1], [2], [3], [4], [5], [6], [7]. The most used operation mode is the continuous conduction mode (CCM), where the converter operates with a continuous input current. This mode of operation is preferred in front of the discontinuous conduction mode (DCM) because of the load dependent voltage gain, high current ripple and low efficiency at DCM operation. This topology suffers from a closed-loop bandwidth limitation because of the right half plane (RHP) zero in the control to output voltage transfer function, giving a non-minimum phase characteristic. Also, its hard-switching operation mode cause lower efficiency, especially in high voltage/power applications.

There are several methods to mitigate the effects of a RHP in a boost converter. Operate the system in DCM moves the RHP zero to higher frequencies at a cost of higher peaks and current ripples, which imply efficiency degradation [1]. In [8], authors combines the equivalent series resistance (ESR) of

the output capacitor and a leading edge modulation to send the RHP zero to the left hand plane (LHP). However, this implies the uses of high ESR values that varies with aging and generates high output voltage ripple and power losses. To reduce the value of the ESR for RHP zero mitigation purposes, the inductor-current based feedback (ICF) strategy is proposed in [9], where the inductor current is added to the output voltage to generate a new controlled variable, without RHP zero in its control-to-output transfer function. However, this method provokes a stationary error in the output voltage regulation [10]. A deeper study of the ICF strategy is done in [11], where no advantages are seen respect of using a PID control applied to output voltage regulation.

On the other hand, regarding a modification of the circuit topology, a tri-state forward converter topology is proposed in [12] that, similarly to DCM operation, moves the RHPZ to higher frequencies. Later, the use of magnetic coupling has been successfully used for RHP elimination in boost [12], [13], [14], [15], [16], and buck-boost topologies [17], [18]. In spite of introducing some losses, inductor coupled converters offer good efficiency and perfect output voltage and input/output current regulation in different applications[13], [14], [17], [18], [19], [20], [21].

Soft switching techniques have arisen as the more useful strategy for reducing switching losses in power conversion systems. These techniques are divided into auxiliary and non-auxiliary circuit-based techniques [22]. Auxiliary circuit-based techniques include Series/Parallel/Series-Parallel Resonant (SR/PR/SPR), Multi-Resonant (MR), RT and Quasi-Resonant (QR). Non-auxiliary circuit-based techniques include Single-Phase-Shift (SPS) and Dual-Phase-Shift (DPS) in case of isolated converters. However, in non-isolated converters, this non-auxiliary circuit-based techniques applied only for control-only technologies [23], regarding basic soft-switching modulation strategies: discontinuous conduction mode (DCM), critical conduction mode (CRM), and triangular current mode (TCM). Auxiliary-circuit-based techniques increase conduction losses due to the circulating currents in the auxiliary components. They also increase the size and cost of the system. In case of synchronous conduction converters, the inductor current can flow between positive and negative values, allowing MOSFET junction capacitor discharge achieving zero-voltage switching (ZVS) capability. This is the operational principle of the quasi square-wave mode with zero voltage switching (QSW-ZVS) [24], also known as triangular current mode (TCM) [25]. A dc-dc synchronous boost converter with QSW-ZVS operation is presented in [26], where three different modes of operation are analyzed: Typical CCM operation with large inductance and constant switching frequency, QSW-ZVS with constant operating frequency and low inductance value but high reactive current, and QSW-ZVS with variable switching frequency to decrease reactive current and increase efficiency. QSW-ZVS with variable switching frequency optimizes and fixes the minimum absolute value of the inductor current regardless of operating point and has higher efficiency. Solutions based on digital control compute time delays and/or switch-on and switch-off times every switching period. These digital strategies present large computational complexity and need expensive digital devices for their implementation [27]. A simple and cost-effective variable hysteresis implementation of QSW-ZVS applied to bidirectional buck and boost converters is presented in [28]. The proposal is compared with previous implementations in terms of efficiency and simplicity of implementation, demonstrating the feasibility of the proposed solution.

Using magnetic-coupled techniques to eliminate the RHP effects allows the use of the control law to achieve soft-switching operation and guarantee output voltage regulation. A comparative presented in [15] and [16] show that main differences between [13] converter are related to switch and diode voltage stress. In [15] and [16] the MOSFET voltage stress is reduced at expenses of increasing diode voltage stress. However, [13] presents lower number of added components and the same switch waveforms of the classical boost converter, which makes it a candidate to apply QSW-ZVS techniques. Despite the CIB converter with soft switching techniques has been previously studied [29], it has not been yet analyzed using QSW-ZVS.

The aim of the article is to design a cost-effective and simple implementation of a QSW-ZVS CIB converter obtaining higher efficiency and faster response than previous solutions. Therefore, a fair comparison must be done in terms of dynamic response and efficiency with a QSW-ZVS boost converter [28]. Following comparison rules presented in [30], both converters are designed with the same power and switching frequency. Input current and output voltage ripple of both converters is similar. Also, the same components and material types are used for their experimental implementation. However, in our case, there is no need to use cost functions to compare them because we have a trade off between obtaining faster dynamics response or a little bit lower cost.

The rest of the article is organized as follows: Section II analyzes and establishes QSW-ZVS design conditions. Control design of CIB and boost converter under QSW-ZVS are studied in Section III. Experimental results of both converters are shown and analyzed in Section IV.

II. ANALYSIS AND DESIGN

A. CONDITIONS FOR QUASI-SQUARE-WAVE ZERO-VOLTAGE-SWITCHING

Fig. 2(a) shows the CIB converter with two-MOSFETs switch realization. Effective terminal capacitances in the MOSFETs and the coupled inductors are included. These parasitic capacitances must be taken into account to analyze the QSW-ZVS mode. Fig. 2(b) shows the simplified circuit we have used to analyze the switching intervals. In Fig. 2(a), coupled inductors have been represented by an equivalent circuit which includes a transformer, with $1:n$ turns ratio, a magnetizing inductance referred to the primary side L_m, and an uncoupled inductor in series with the primary side L_p. The following formulas relate

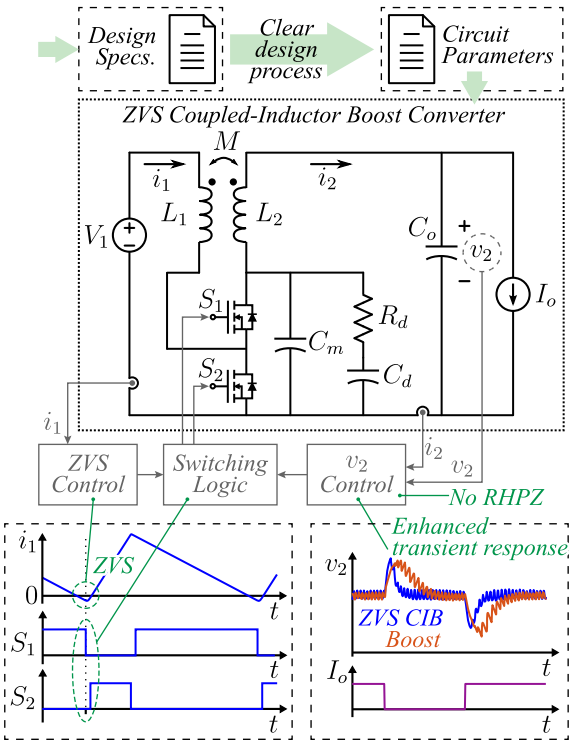

FIGURE 1. CIB converter: a boost converter with *LC* output filter and with its two inductors coupled together.

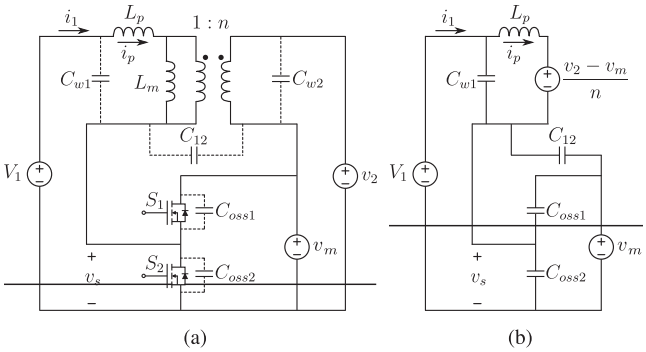

FIGURE 2. (a) CIB converter with two-MOSFETs switch realization. The coupled inductors have been replaced by an equivalent circuit with a transformer. MOSFESTs and coupled inductor parasitic capacitances are included. This is a simplified circuit assuming that v_m and v_2 are constant, valid during switching. (b) Simplified circuit valid for analyzing resonance during dead time.

the two set of coupled inductor parameters:

$$L_1 = L_m + L_p,\ M = nL_m,\ L_2 = n^2 L_m \tag{1}$$

$$L_p = \left(1 - k^2\right) L_1,\ L_m = k^2 L_1,\ n = \frac{1}{k}\sqrt{\frac{L_2}{L_1}} \tag{2}$$

where $k = M/\sqrt{L_1 L_2}$ is the coupling coefficient.

Large capacitors, C_m and C_o, keep their voltages (v_m and v_2) almost constant during the switching intervals and they can be replaced by ideal voltage sources for analyzing purposes.

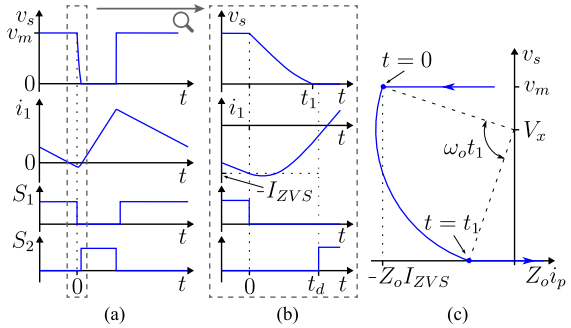

FIGURE 3. (a) Waveforms in mode QSW-ZVS of switching node voltage, v_s, input current, i_1, and input signals of the MOSFETs, S_1 and S_2. (b) Time axis zoom around $t = 0$ showing the resonance during dead time. (c) Trajectory in the $Z_o i_p$-v_s plane.

We assume that MOSFET drivers are ideal and then gate-to-source voltages are perfect square waves. Gate-to-drain and drain-to-source capacitances can be combined in one output capacitance $C_{oss} = C_{gd} + C_{ds}$.

If the input turn-off time is short enough then the small capacitances maintain near-zero voltage conditions during the switch turn off, mitigating turn-off losses. On the other hand, a dead time with the two MOSFETs switched off is mandatory to avoid catastrophic short circuits. With both MOSFETs off, the inductor current may force the body diode to turn-on. Therefore, if we switch on the MOSFET associated to that body diode, then a ZVS occurs and losses at switch turn-on are also mitigated. To also turn on in ZVS conditions the other MOSFET, the inductor current must reverse before the next dead time. With ZVS conditions in both MOSFETs, i_1 changes sign twice every switching period and the switch voltage shapes as a QSW. Fig. 3(a) shows switching node voltage v_s, input current i_1, and input signals of the MOSFETs waveforms in mode QSW-ZVS. The absolute value of i_1 in the opposite direction of power flow must be the needed minimum, to not unnecessarily increase current stress.

During the dead-time interval, a resonance involving L_p and parasitic capacitances occurs. Fig. 2(b) shows the simplified version of CIB converter represented in Fig. 2(a) which used to analyze the resonance. Initial conditions and duration of dead time must be assigned correctly to ensure ZVS. The switch-on will be at zero voltage only if the output capacitance is completely discharged before raising the input signal. Fig. 3(b) shows the desired behavior of the signals during the dead time interval.

Differential equations that corresponds to the circuit of Fig. 2(b), using inductor current i_p and low-side MOSFET drain-to-source voltage v_s as state variables, and assuming constant V_1, v_m and v_2, are

$$L_p \frac{di_p}{dt} = V_x - v_s \tag{3}$$

$$C_r \frac{dv_s}{dt} = i_p \tag{4}$$

where V_x equals to $V_1 - (v_2 - v_m)/n$ and

$$C_r = C_{w1} + C_{12} + C_{oss1} + C_{oss2} \tag{5}$$

Solutions of the system (3)–(4) are:

$$v_s(t) = V_x + \Re\left[V_y\, e^{j\theta}\, e^{j\omega_o t}\right] \tag{6}$$

$$i_p(t) = -\frac{\Im\left[V_y\, e^{j\theta}\, e^{j\omega_o t}\right]}{Z_o} \tag{7}$$

where $V_y\, e^{j\theta}$ is a phasor whose value depends on initial conditions, ω_o is $1/\sqrt{L_p C_r}$ and Z_o is $\sqrt{L_p/C_r}$. If the initial conditions are $i_p(0) = i_1(0) = -I_{ZVS}$ and $v_s(0) = v_m$, then $V_y\, e^{j\theta}$ equals to $v_m - V_x + j\, Z_o\, I_{ZVS}$. In this case, the solution is shown in Fig. 3(c) as a trajectory in the $(Z_o\, i_p)v_s$-plane. In this plane, it has the shape of a circular arc whose subtended angle is $\omega_o t$. From geometrical considerations over this figure, sufficient conditions for ZVS are

$$t_d = \frac{\pi}{2\omega_o} = \frac{\pi}{2}\sqrt{L_p C_r} \tag{8}$$

$$I_{ZVS} = \frac{V_x}{Z_o} = V_x\sqrt{\frac{C_r}{L_p}}. \tag{9}$$

B. STEADY-STATE ANALYSIS

1) DIRECT MODE

We begin the steady-state analysis with the case of $I_o > 0$ or direct mode. To found simplified relationships we assume that t_d is zero and the current valley value of i_1 is $-I_{1,v} = -V_y/Z_o$. A system of differential equations that corresponds to the circuit of Fig. 1, without damping network C_d - R_d, using input i_1, output i_2 coupled inductor currents, the intermediate capacitor voltage v_m and the output capacitor voltage v_2 as state variables, is

$$L_1\frac{di_1}{dt} - M\frac{di_2}{dt} = V_1 - v_m(1-u) \tag{10}$$

$$M\frac{di_1}{dt} - L_2\frac{di_2}{dt} = v_2 - v_m \tag{11}$$

$$C_m\frac{dv_m}{dt} = i_1(1-u) - i_2 \tag{12}$$

$$C_o\frac{dv_2}{dt} = i_2 - I_o \tag{13}$$

where $u = 1$ corresponds to MOSFETs S_1-off, S_2-on, and $u = 0$ corresponds to MOSFETs S_1-on, S_2-off.

Replacing u by the duty cycle D and assuming I_1, I_2, V_m, and V_2 are the average values of the state variables in steady state, we obtain the boost converter DC voltage transfer function (V_2/V_1), equals to 1/(1-D).

Assuming the switching frequency and capacitances C_m and C_o are large enough that the ripple values of v_m and v_2 are much smaller than their average values, then i_1 and i_2 have an essentially constant slope during each interval. From (10)–(11) and $v_m = v_2 = V_2$, we get that current slopes in steady-state are

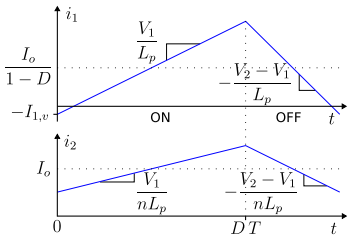

FIGURE 4. Ideal waveforms of currents in steady-state.

$$\frac{di_1}{dt} = n\frac{di_2}{dt} = \begin{cases} \frac{V_1}{L_p} & \text{ON} \\ -\frac{(V_2 - V_1)}{L_p} & \text{OFF} \end{cases} \tag{14}$$

Fig. 4 shows the ideal waveforms of the currents in steady-state, with DC values and slopes. If $v_m = v_2 = V_2$ then

$$I_{ZVS,v} = \frac{V_1}{Z_o} \tag{15}$$

$$I_{1,v} = \frac{\sqrt{(V_2 - V_1)^2 + V_1^2}}{Z_o}. \tag{16}$$

From Fig. 4, the switching period T is

$$T = \frac{2\left(I_o + I_{1,v}\, V_1/V_2\right) L_p}{V_1\, D\,(1-D)}. \tag{17}$$

The expression (17) can be used to design L_p from a switching period specification, but extreme duty cycles are not allowed.

The transformer magnetizing current in Fig. 2(a) is $i_m = i_1 - n\, i_2$. Using (14) we conclude that this magnetizing current has essentially no switching ripple and then the transformer core losses could be small. On the other hand, the DC component of i_m is

$$I_m = \frac{I_o}{1-D} - nI_o = I_o\left(\frac{V_2}{V_1} - n\right). \tag{18}$$

If $n = V_2/V_1$, then the magnetic flux in the transformer core will be zero and the transformer size can also be small. Defining the converter voltage gain as $G = V_2/V_1$, voltage variations lead to a range of converter voltages gains $G_{\min} \le G \le G_{\max}$. If I_o can be maximum for any G, the best choice for minimizing transformer size is

$$n = \frac{G_{\min} + G_{\max}}{2}. \tag{19}$$

Assuming that the ripple of v_m has a triangular shape, its peak-to-peak value is

$$\Delta v_{m,pp} = \frac{I_o\, D\, T}{C_m} = \frac{2\, I_o\left(I_o + I_{1,v}\, V_1/V_2\right) V_2\, L_p}{{V_1}^2\, C_m}. \tag{20}$$

If $I_{1,v}\, V_1/V_2 \ll I_{o,\max}$, the maximum relative ripple is

$$\frac{\Delta v_{m,pp,\max}}{V_2} = \frac{2\,{I_{o,\max}}^2\, L_p}{{V_{1,\min}}^2\, C_m}. \tag{21}$$

Finally, the ripple in v_2 is approximately

$$\Delta v_{2,pp} = \frac{\Delta i_{2,pp}\, T}{8\, C_o}. \tag{22}$$

Expressions (21) and (22) can be used to obtain C_m and C_o from ripple specifications.

2) REVERSE MODE

When $I_o < 0$, the QSW-ZVS analysis is very similar. Deadtime duration condition is also (8), the initial condition is now a positive current

$$I_{ZVS,p} = \frac{V_2 - V_1}{Z_o} \tag{23}$$

and the peak current is $I_{1,p} = I_{1,v}$ (16). Then, the expression for the switching period is equation (17) again, using the absolute value of I_o. Note, the rest of the steady-state expressions do not change.

C. IDEAL OUTPUT CURRENT CONTROL

The main feature of the CIB converter is its ability to tightly control its output current. Concerning dynamics behavior, the CIB converter is a fourth-order converter similar to a buck converter with an *LC* input filter. When the CIB converter is controlled by a high gain feedback loop of the output current error, the internal voltage v_m can oscillate, in a similar way that can the input voltage filter of the buck converter, if it is not well damped. In order to avoid oscillation a damping network is added. Therefore, to design the damping network, we will use the sliding-mode control method to analyze the system dynamics when the converter is controlled by an ideal output current feedback loop [31].

1) SLIDING-MODE CONTROL OF CIB CONVERTER

Defining the sliding control surface as

$$s(t) = i_r(t) - i_2 = 0 \tag{24}$$

where $i_r(t)$ represents the external current reference value and, using the following control law 24 guarantees an ideal sliding-mode regimen with $i_2 = i_r(t)$ [31].

$$u = \begin{cases} 1 & \text{if } i_2 < i_r(t) \\ 0 & \text{if } i_2 > i_r(t) \end{cases} \tag{25}$$

If $i_r(t) = I_o$ then the linearized dynamics around the equilibrium point ($v_2 = v_m = V_2$; $i_1 = I_o V_2/V_1$ and $i_2 = I_o$) is second order and has the characteristic polynomial

$$p_1(s) = s^2 + a_1\, s + a_0 \tag{26}$$

where

$$a_1 = \frac{I_o\left(L_m V_1\, n - L_m V_2 - L_p V_2\right)}{C_m L_m V_1 V_2\, n} \tag{27}$$

$$a_0 = \frac{V_1}{C_m L_m V_2\, n}. \tag{28}$$

It should be noted that $p_1(s)$ (26) and the numerator of the transfer function (4) in [13] have the same coefficients. Thus,

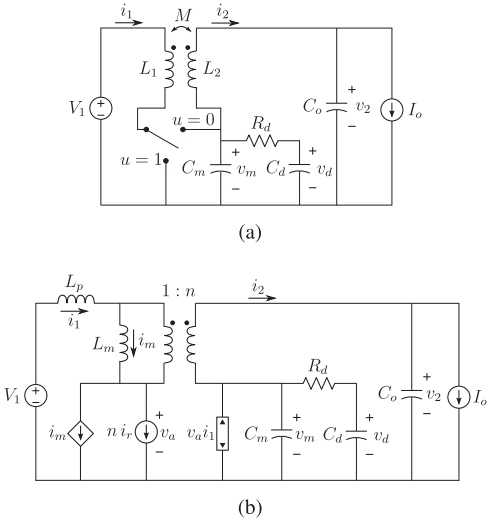

FIGURE 5. (a) CIB converter with $R_d - C_d$ damping network. (b) Nonlinear circuit representing its ideal sliding-mode dynamics with the control law (25).

the output current can be controlled in ideal sliding-mode only if the control-to-output small-signal transfer function has no right half-plane zeros (RHPZ). Stability conditions of this ideal sliding-mode control dynamics guarantees the control-to-ouput transfer function of the CIB converter has a minimum phase characteristic.

For (26) to be stable, the coefficient a_1 (27) must be positive. If I_o is always positive, it can be achieved by choosing the parameters properly, but not if the energy flow can be reversed. Also, if the output current is close to zero, for any way to choose the parameters, the dynamics are very poorly damped. For those reasons, a damping circuit $R_d - C_d$ is added in parallel with C_m, as shown in Fig. 5(a).

2) SLIDING-MODE CONTROL OF THE CIB DAMPED CONVERTER

Fig. 5(b) shows the ideal sliding-mode dynamics of the damped CIB converter with the control law (25). When $i_r(t) = I_o$, the characteristic polynomial corresponding to linearized dynamics around the equilibrium point ($v_2 = v_m = v_d = V_2$; $i_1 = I_o V_2/V_1$ and $i_2 = I_o$), is

$$p_2(s) = s^3 + a_2\, s^2 + a_1\, s + a_0 \tag{29}$$

where

$$a_2 = \frac{I_o\left(L_m V_1\, n - L_m V_2 - L_p V_2\right)}{C_m L_m V_1 V_2\, n} + \frac{C_d + C_m}{C_d C_m R_d} \tag{30}$$

$$a_1 = \frac{I_o\left(L_m V_1\, n - L_m V_2 - L_p V_2\right)}{C_d C_m L_m R_d V_1 V_2\, n} + \frac{V_1}{C_m L_m V_2\, n} \tag{31}$$

$$a_0 = \frac{V_1}{C_d C_m L_m R_d V_2\, n}. \tag{32}$$

Parameters must be chosen carefully to ensure enough damping for all levels of voltages and currents. We will obtain the restrictions of the parameters in three steps:

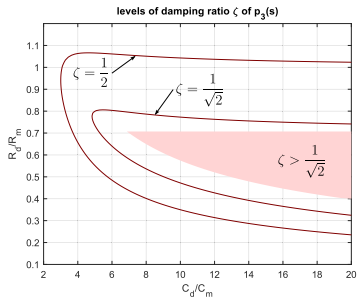

FIGURE 6. Contour lines of damping ratio $\zeta(k_{Cd}, k_{Rd})$ of the complex roots of $p_3(s)$ (33) for constant levels of ζ. The shaded region has $\zeta > 1/\sqrt{2}$ in all their points and is delimited by $\sqrt{3(1+k_{Cd})}/k_{Cd} \le k_{Rd} \le 1/\sqrt{2}$.

1) First, setting $I_o = 0$ to get design expressions for C_d and R_d.
2) Next, finding a condition for the case of fixed voltage gain $G = n$.
3) And last, checking that the extreme cases are also well-damped.

The minimum damping ratio ζ of the complex roots of the characteristic polynomial is the damping indicator we use. Our design criteria is $\zeta > 1/\sqrt{2}$.

1) We will give expressions for C_d and R_d in a way that the dynamics be well-damped for all the voltages gains between G_{min} and G_{max} when $I_o = 0$. Using the frequency (ω_m) which equals to $1/\sqrt{G\,n\,L_m\,C_m}$, and resistance $R_m = \sqrt{G\,n\,L_m/C_m}$, polynomial $p_2(s)$ (29) with $I_o = 0$ can be written as

$$p_3(s) = s^3 + \frac{\omega_m\,(k_{Cd}+1)}{k_{Cd}\,k_{Rd}}\,s^2 + {\omega_m}^2\,s + \frac{{\omega_m}^3}{k_{Cd}\,k_{Rd}} \tag{33}$$

where $k_{Cd} = C_d/C_m$ and $k_{Rd} = R_d/R_m$. A change of scale of the complex variable, $s = s_m\,\omega_m$ in $p_3(s)$, does not affect the damping ratio ζ of the complex roots, then ζ depends only on k_{Cd} and k_{Rd}. Fig. 6 shows the contour lines of $\zeta(k_{Cd}, k_{Rd})$ for constant levels of ζ. The shaded region in Fig. 6 has $\zeta > 1/\sqrt{2}$ in all their points and is delimited by

$$\frac{\sqrt{3\,(1+k_{Cd})}}{k_{Cd}} \le k_{Rd} \le \frac{1}{\sqrt{2}}. \tag{34}$$

To satisfy the last inequality in (34) we choose

$$R_d = \frac{R_{m,\min}}{\sqrt{2}} = \sqrt{\frac{n\,G_{\min}\,L_m}{2\,C_m}} \tag{35}$$

and then, the first inequality in (34) holds if

$$C_d = 3\,g_r\left(1 + \sqrt{1 + \frac{2}{3\,g_r}}\right)C_m \tag{36}$$

where $g_r = G_{\max}/G_{\min}$.

2) We assume now that I_o is free but the voltages are fixed with the gain $G = n$. Using expressions (35) and (36) to replace parameters R_d and C_d, polynomial $p_2(s)$ (29) becomes

$$p_4(s) = s^3 + b_2\,s^2 + b_1\,s + b_0 \tag{37}$$

where

$$b_2 = \omega_m\left(-\lambda + \frac{k_{Cd}+1}{k_{Cd}\,k_{Rd}}\right) \tag{38}$$

$$b_1 = {\omega_m}^2\left(\frac{-\lambda}{k_{Cd}\,k_{Rd}} + 1\right) \tag{39}$$

$$b_0 = \frac{{\omega_m}^3}{k_{Cd}\,k_{Rd}}, \tag{40}$$

$k_{Rd} = 1/\sqrt{2}$, $k_{Cd} = 3 + \sqrt{15}$, and $\lambda = I_o L_p/V_1\sqrt{L_m\,C_m}$.

The damping ratio ζ of the complex roots of polynomial $p_4(s)$ (37) is a function of the parameter λ. The condition to have a well-damped dynamics is $\lambda \le 0.2$. To meet this condition in the worst-case ($I_o = I_{o,\max}$ and $V_1 = V_{1,\min}$) we choose

$$\frac{1}{\sqrt{L_m\,C_m}} = \frac{0.2\,V_{1,\min}}{I_{o,\max}\,L_p}. \tag{41}$$

This equation sets the product of L_m and C_m, and it can also be fulfilled for a small L_m if C_m is large, and vice versa.

3) Finally, using expressions (19), (35) and (36) to replace parameters n, R_d ans C_d, and applying restriction (41), we have calculated roots of $p_2(s)$ (29) in the four extremes of the region $-I_{o,\max} \le I_o \le I_{o,\max}$, $G_{\min} \le G \le G_{\max}$, and we have checked that they are also well-damped provided that C_m is not too small, or equivalently, L_m is not very large. We set the limit

$$L_m \le L_p. \tag{42}$$

The designer will choose C_m and L_m taking into account the physical size of C_m, C_d and L_m and also the power losses at R_d. Power dissipation at damping resistor, P_{Rd}, in steady-state, is approximately [17]

$$P_{Rd} \approx \frac{(\Delta v_{m,pp})^2}{12\,R_d}. \tag{43}$$

This expression sub-estimates the losses at R_d. If large transients are frequent, P_{Rd} has low-frequency components that must be taken into account.

The previous analysis of damping and the derived design expressions are general and not restricted to the QSW-ZVS mode. Nevertheless, using expression (21) for the ripple of v_m, valid only in QSW-ZVS, allows seeing better the design trade-offs. Using (21), the design condition (41) becomes

$$\frac{L_m}{L_p} = 12.5\,\frac{\Delta v_{m,pp,\max}}{V_2} \tag{44}$$

and the limit (42) is equivalent to

$$\frac{\Delta v_{m,pp,\max}}{V_2} \le 0.08. \tag{45}$$

Guideline for designing a stable QSW-CIB converter is summarized in Table 3, where CIB and inner current control parameters are depicted with their corresponding design equations.

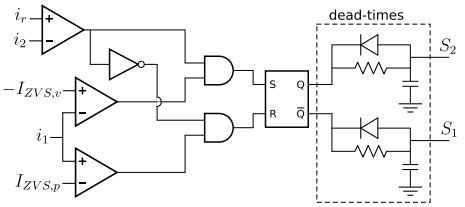

FIGURE 7. Inner current control scheme that works in both direct and reverse directions of power flow. A variable-width hysteretic analog control with two current sensors. Current i_2 follows the reference i_r with high bandwidth, while current i_1 is only there to assure ZVS.

III. CONTROL DESIGN

Fig. 1 depicts a block diagram of the converter two-loop control strategy. A high bandwidth inner current control, which also guarantees QSW-ZVS, has been designed to validate the theoretical analysis of the CIB converter. In addition, an outer voltage control loop ensures output voltage regulation. Simulation results are analyzed and compared with those obtained from an equivalent QSW-ZVS boost converter.

A. CURRENT CONTROL LOOP

Fig. 7 shows the schematic of the selected current controller for the CIB converter that generates MOSFETs activation signals, S_1 and S_2. It is a variable-width hysteretic analog current control [28] adapted to the CIB converter, with two current sensors, for i_1 and for i_2. Uses -$I_{ZVS,v}$ as valley current reference value of the input current i_1, in case of direct operating mode, and $I_{ZVS,p}$ as the peak reference, in reverse, as required for ZVS. It also includes circuitry to set the required duration of dead times. On the other hand, current i_2 is compared with current reference i_r to control the peak in direct operating mode and the valley in reverse, which allows controlling i_2 with high bandwidth, as required for sliding-mode analysis.

B. VOLTAGE CONTROL LOOP

The voltage control loop is a proportional-integral voltage controller with a high-frequency pole,

$$G_C(s) = K_p\left(\frac{1+\omega_I/s}{1+s/\omega_h}\right), \tag{46}$$

whose output is the current reference value i_r. With ideal sliding-mode current control, the transfer function from current reference to output voltage, assuming a resistive load $R_o = V_2/I_o$, is the same as we found in a buck converter [31]:

$$Gv_2i_r(s) = \frac{0.5R_o}{sC_oR_o+1} \tag{47}$$

This small-signal model is only valid for frequencies well below the switching frequency. Due to (47) is a minimum phase transfer function, the bandwidth of the voltage loop can be large, but will be limited by the switching frequency and the small-signal assumption. Therefore, the minimum switching frequency, ω_s, will be a specification required to design the voltage controller. We choose the 0 dB crossover frequency of the loop gain to be $\omega_c = \omega_s/\pi$. Calculating $G_c(s)$ coefficients

TABLE 1. Voltage Controller Parameters

	CIB	Boost
ω_s	$2\pi\, f_{s,min}$	
ω_z		$\frac{{V_{1,min}}^2}{L\,V_2\,I_{o,max}}$
ω_c	ω_s/π	$\omega_{RHPZ}/4$
K_P	$C_o\,\omega_c$	$\frac{V_2\,C\,\omega_c}{V_{1,min}}$
ω_I	$\omega_c/4$	$\omega_c/4$
ω_h	$4\,\omega_c$	$4\,\omega_c$

TABLE 2. Converter System Specifications

Variable	Specification
DC output voltage	$V_2 = 200\,\text{V}$
Output voltage ripple	$\Delta v_{2,pp} \le 0.3\,\text{V}$
Peak to peak ripple in C_m	$\Delta v_{m,pp,max} \le 12\,\text{V}$
Input voltage	$80\,\text{V} \le V_1 \le 120\,\text{V}$
Output current	$-1.5\,\text{A} \le I_o \le 1.5\,\text{A}$
Switching frequency	$\ge f_{s,min} = 50\,\text{kHz}$

according to the criteria shown in Table 1 for CIB converter, the phase margin will be higher than 60°, and the gain margin will be infinite [31].

C. EQUIVALENT BOOST CONVERTER DESIGN

We want to compare the CIB converter with a typical boost converter, with the same operating specifications [30], also controlled in QSW-ZVS mode. Current control is implemented following the same schematic in Fig. 7, but using the inductor current in place of both currents i_1 and i_2. Controlling the inductor current in sliding mode, the small signal transfer function from current reference to output voltage is [31]:

$$Gv_2i_r(s) = 0.5\left[\frac{R_o(1-D)^2 - sL}{(1-D)(sCR_o+2)}\right] \tag{48}$$

The presence of an RHPZ in (48) limits the bandwidth of the voltage control loop that can be robustly achieved. Therefore, in this case, the 0 dB crossover frequency of the loop gain, ω_c, must be a quarter of the minimum frequency value of the RHPZ, ω_{RHPZ}, which is minimum when the input voltage has its lowest value and the load current is maximum. We use the same voltage controller (52) with coefficients calculated according to the right-hand column formulas in Table 1.

D. SIMULATION RESULTS

A CIB and a boost converter, with operating specifications shown in Table 2, are designed by following equations presented in Sections II and III. A list of converters and ZVS parameters in addition to their corresponding equations is depicted in Table 3. To make the comparison fairer [30], it will be done for the same switching frequencies, the same input current ripple, and the same capacitors. Therefore, L and C components of the boost converter are chosen as follows:

$$L = L_p \tag{49}$$

TABLE 3. Converters Simulation and Experiment Parameters for CIB, Boost and Current Control

Parameter	Value	Units	Eq No
CIB			
L_p	94	µH	(17)
L_m	9.8	µH	(44)
C_r	2.4	nF	(5)
C_o	20	µF	(22)
C_d	27	µF	(36)
C_m	2.7	µF	(21)
R_d	2.5	Ω	(35)
n	2		(19)
Boost			
L	94	µH	(49)
C_r	2.4	nF	(5)
C	49.7	µF	(50)
Current Control			
t_d	503	ns	(8)
$I_{ZVS,v}$	0.6	A	(15)
$I_{ZVS,p}$ (Simulation)	2.4	A	(23)

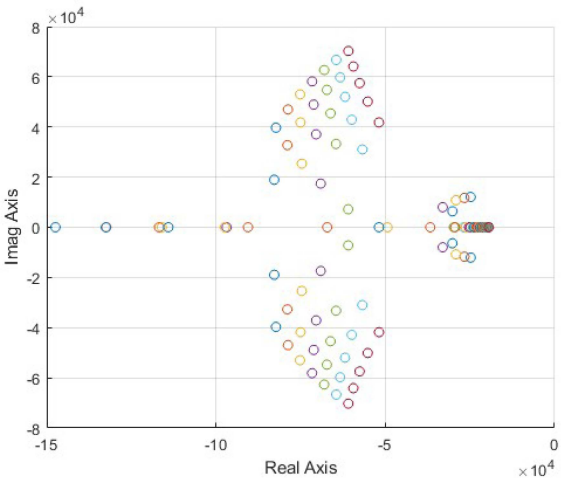

FIGURE 8. Zero maps of the CIB damped converter for I_o and V_1 ranges shown in Table 2.

$$C = C_m + C_d + C_o \tag{50}$$

With this choice, CIB converter and boost converter can be built with the same components except for the 1:n transformer, the R_d resistor and the extra current sensor required for i_2 measurement.

In Fig. 8, the depicted zero maps for equation (29), representing the characteristic polynomial of the damped CIB converter according to the converter specifications of Table 2, show the elimination of RHPZ.

The voltage controller for the CIB converter results from Table 1 as follows:

$$G_C(s) = 3\left(\frac{1 + 37500/s}{1 + s/600000}\right), \tag{51}$$

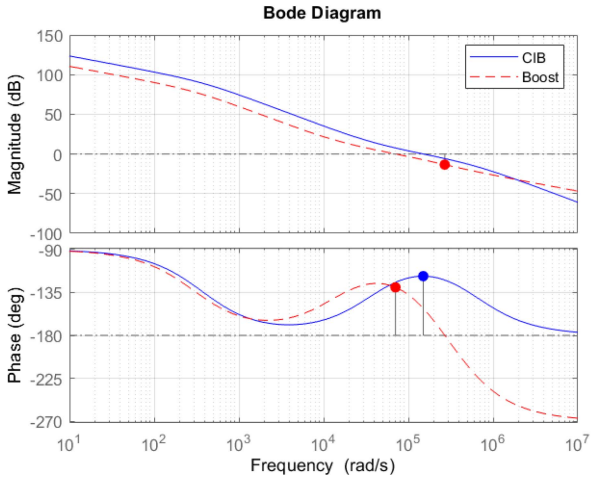

FIGURE 9. Voltage loop gain Bode plots for CIB and boost converters.

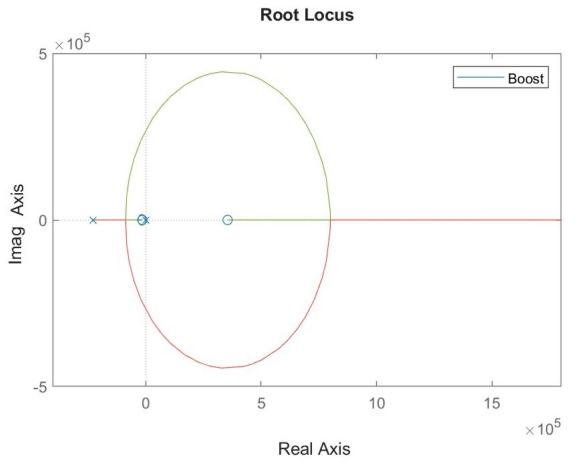

FIGURE 10. Voltage loop root locus diagram for the boost converter.

Similarly, the voltage controller for the boost converter is obtained from Table 1 as:

$$G_C(s) = 7.05\left(\frac{1 + 14184/s}{1 + s/226950}\right), \tag{52}$$

The Bode voltage loop gain plot of both converters is shown in Fig. 9 and the corresponding root locus diagrams for the boost and CIB converter are shown, respectively, in Figs. 10 and 11. In these three figures, we can see the RHPZ in the case of the boost converter and the minimum phase characteristic of the CIB converter due the absence of RHPZ. As a consequence, as shown in Fig. 9, this allows the design of a larger voltage control loop bandwidth in the case of the CIB converter.

Fig. 12 shows the simulation waveforms for the CIB converter. The top subplot shows the input current i_1 with valley current value -$I_{ZVS,v}$ and peak current value $I_{ZVS,p}$ that guarantee ZVS respectively in forward and reverse modes of operation. Shows the two operation modes of the bidirectional

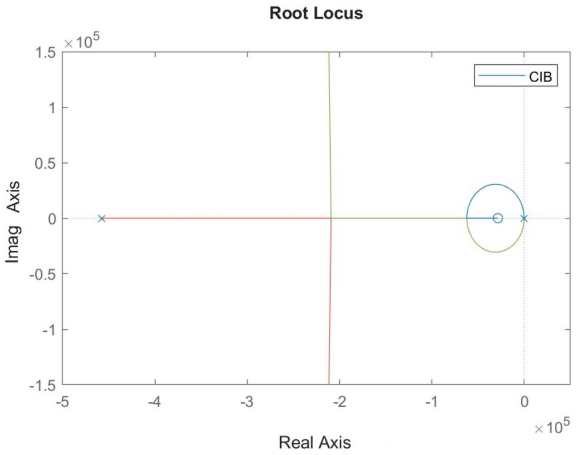

FIGURE 11. Voltage loop root locus diagram for the CIB converter.

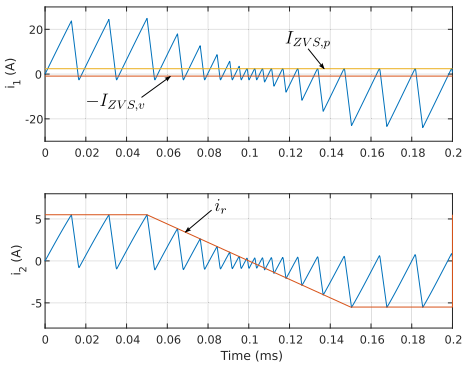

FIGURE 12. Simulation waveforms for current i_1 and current i_2 of a CIB converter with the control of Fig. 7. The ZVS is maintained while i_2 follows the reference i_r with bidirectional power flow.

power flow. The hysteretic current controller guarantees that the input current i_1 has always enough negative/positive current for ZVS operation regardless of the power flow sense. Fig. 12 bottom subplot shows the current i_2 with the reference current i_r to set its absolute peak value for voltage regulation. Fig. 13 shows the waveforms of the load transient simulation results for both converters at a 100 V input voltage. The CIB converter is in unidirectional power flow operation, wherein the top subplot is the output voltage and the bottom one is the output current. Both transients have approximately 100 µs of settling time for the CIB converter. The typical boost converter also operates in unidirectional power flow operation. However, the same load transients in this converter have a settling time of 200 µs. This makes the response time of the boost converter twice as long as the response time of the CIB converter for the same load transient. This is due to the limitation in the bandwidth of the boost converter voltage control caused by the RHPZ.

IV. EXPERIMENTAL VERIFICATION

To validate the theoretical formulation and the simulation results, several experiments have been developed in our

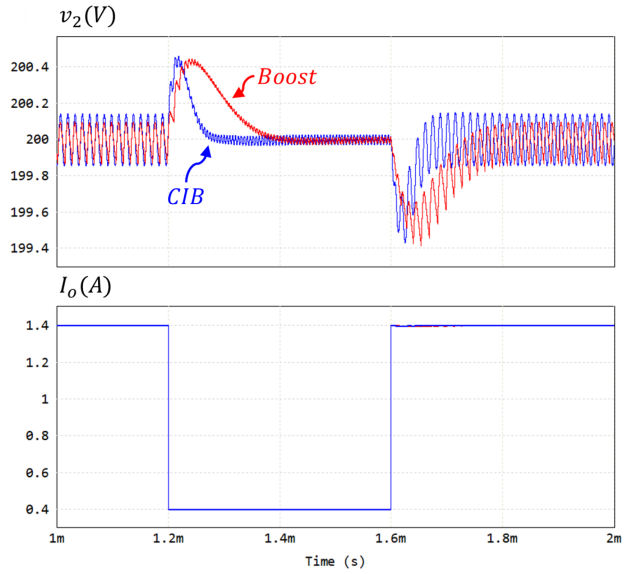

FIGURE 13. Comparison of output voltage responses to the same step load changes for CIB converter and boost converter. The response time of the boost converter is twice that of the CIB converter.

laboratory. The converter prototype and the experimental set-up are described in detail to facilitate replication.

A. CONVERTER PROTOTYPE AND EXPERIMENTAL SET-UP

A configurable prototype able to select either the CIB or boost converter topologies has been implemented in the laboratory considering the parameters in Table 3. A circuit schematic of the experimental CIB converter implementation is shown in Fig. 15. The power stage consists of two series connected inductors (Wurth Electronics 74435584700) configuring L_p, a configurable transformer (CoilCraft HPH6-0121) obtaining the coupled inductor using two paralleled coils for the primary side and two series connected coils for the secondary side, one film capacitor C_o (VISHAY MKP383547063JPM4T0), one film capacitor C_m (PANASONIC ECW-FD2J275K), one electrolytic capacitor C_d (Chemi-Con EKXJ501ELL270MK40S), four paralleled 10 Ω resistances (BI TECHNOLOGIES BPC10100J) forming R_d, and two MOSFET (INFINEON IPx60R160C6). Selection of the converter topology (CIB or boost) for validation tests is performed using fuses which alow a fair comparison between them [30]. The inductor currents i_1 and i_2 are measured using Hall-effect current sensors (LEM LAH25-NP) with unitary gain fed by isolates sources (MURATA NMH0515SC), while the output voltage is sensed using a resistive voltage divider with a gain 0.03. The gate signals for MOSFETs are applied by means of two opto-isolated drivers (HCPL-3120) fed by two isolated converters (XP Power ISH0515A). RCD filters which delay turn-on but not turn-off transition in each one of both switches are used to introduce the desired dead time t_d. The current control loop has been implemented by means of a hysteresis comparator composed of one flip-flop (HEF4027BP), two comparators (LM319N) and three NAND gates (HEF4093BP). The voltage

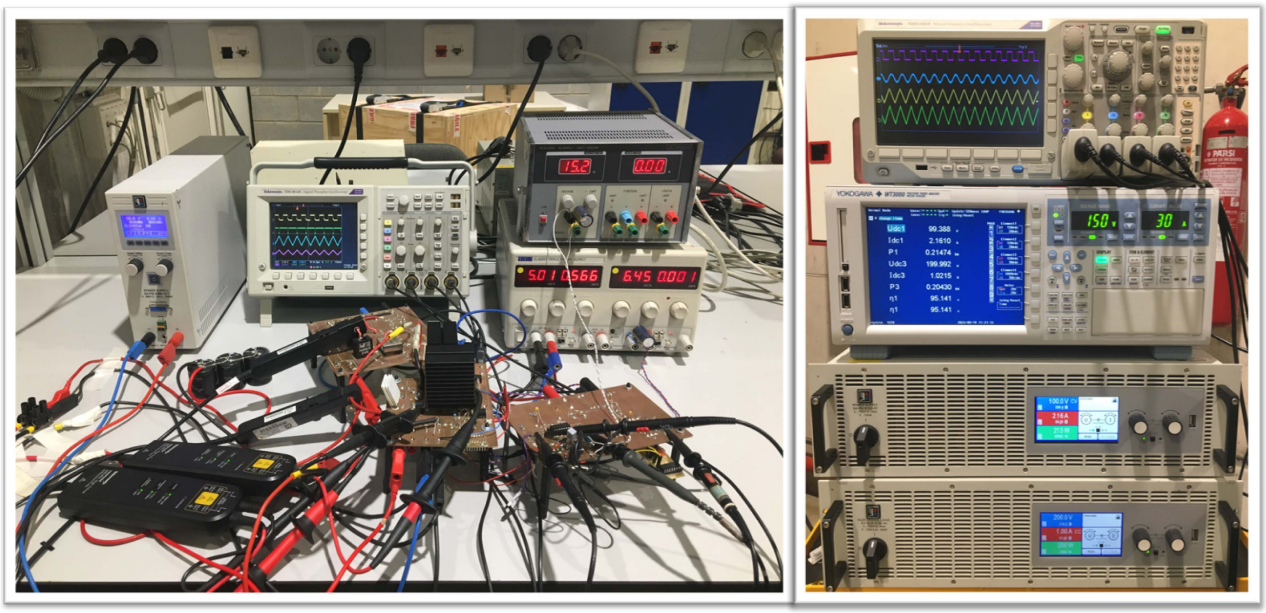

FIGURE 14. Laboratory experimental setup and converter prototype.

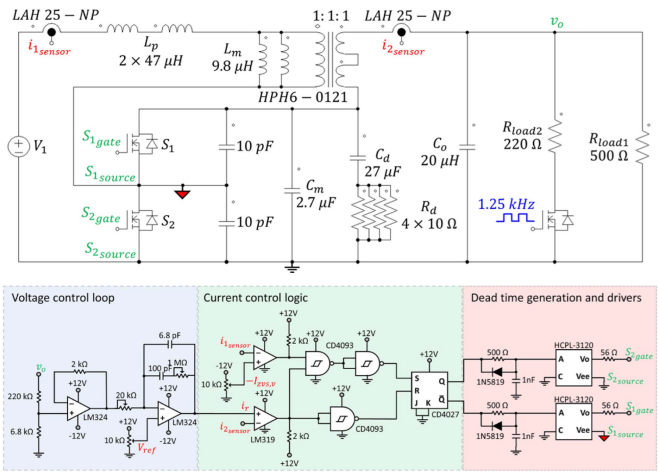

FIGURE 15. Schematic diagram of the power converter and control circuit.

controller has been implemented using a high precision operational amplifier (OPA277P). The reference for the voltage loop is provided by a precision potentiometer.

The instruments used for measurements in the experimental set-up and depicted in Fig. 16 are: a digital phosphor oscilloscope (Tektronix TDS3014 C) and a mixed domain oscilloscope (Tektronix MDO3014), two isolated current probes (Tektronix TCP0030 A), two differential voltage probes (Tektronix THDP0200) and a precision power analyzer (YOKOGAWA WT3000). The control system is fed by two power sources (Aim-TTi EL302RT and Promax FAC-3638). The input port of the power converter is fed by one programmable power source (ELEKTRO-AUTOMATIK EA PSI-9750-40) and the output port is connected to the programmable electronic load (ELEKTRO-AUTOMATIK EA ELR-9750-44) to obtain steady-state results. For the transient response test in the output load, a set of power resistances has been used, one fixed resistance of 500 Ω and another resistance of 220 Ω switched in parallel at 1.25 kHz using a power MOSFET (INFINEON IPx60R160C6) which has a gate signal provided by a function generator (GW Instek MFG-2260M). A photography of the experimental set-up and prototype is depicted in Fig. 14.

B. EXPERIMENTAL RESULTS

Fig. 16 displays load transients from 0.4 A to 1.4 A and vice-versa with nominal input voltage of 100 V for both converters. The first waveform is the output voltage v_2 with an AC coupling to remove the average value, the second waveform is the input current i_1 and the third waveform is the output current I_o. Fig. 16(a) shows a load transient response with deviations of 0.4 V recovering the steady-state in approximately 100 μs. Fig. 16(b) shows the transient for the typical boost converter which shows a similar voltage deviation recovering the steady-state in 200 μs. In this test, the typical boost converter has almost double the response time compared to the CIB converter, making the CIB converter have faster dynamics than the typical boost converter.

Fig. 17 shows load transients from 0.4 A to 1.4 A and vice-versa with minimum and maximum input voltages of 80 V and 120 V for the CIB converter. Fig. 17(a) shows the load transient at 80 V input voltage, which is considered as the worst-case scenario for the converter, where the response time facing the disturbance slightly increases with respect to the 100 μs obtained at nominal input voltage. Fig. 17(b) shows the load transient at 120 V input voltage, where the response time slightly decreases with respect to the 100 μs for both transient cases.

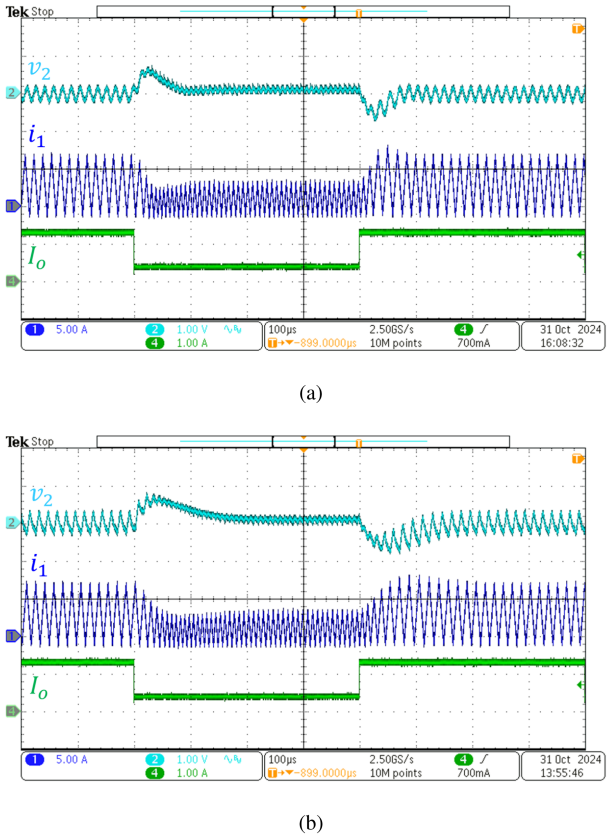

FIGURE 16. Experimental waveforms for load disturbances with input voltage of 100 V of (a) CIB converter. (b) Boost converter.

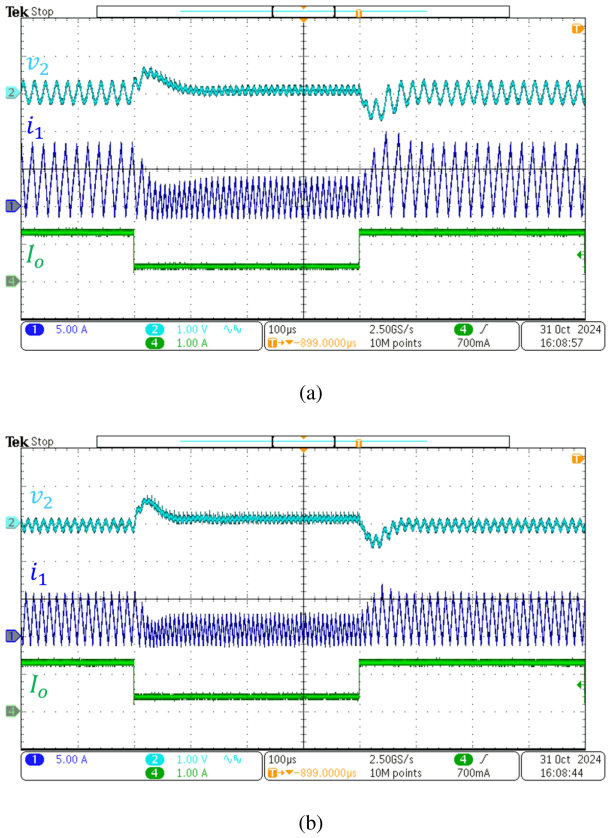

FIGURE 17. CIB experimental waveforms for load disturbances at input voltage of (a) 80 V. (b) 120 V.

In Figs. 16 and 17, the input current i_1 waveform displays a negative valley current value even during transient operation, thanks to the robustness of the hysteresis control, which guarantees ZVS operation in all operating points, transients, and different input voltages. To emphasize the ZVS operation, switching period waveforms of input current i_1, drain-source voltage v_s, and gate-source voltage v_{gs} for converter switches S_1 and S_2 are also depicted in Fig. 18. It is evident that when the gate-source voltage v_{gs} turns on, the drain-source voltage v_{ds} is zero. When the gate-source voltage v_{gs} turns off, the drain-source voltage v_s is also zero. This demonstrates the ZVS operation in both the turn-on and turn-off periods. The zoom provided in sub-figures (b), (c), (d), and (f) of Fig. 18 allows to appreciate the effect of the applied dead time during switching transitions.

C. EFFICIENCY ANALYSIS

Considering that CIB and boost converters have differences with respect to the number of components, it make sense to compare the efficiency behavior of both converters to confirm that the cost of the advantages obtained with the CIB is reasonable. The efficiency has been measured using the precision power analyzer YOKOGAWA WT3000 for a constant input voltage of 100 V, a regulated output voltage of 200 V and steps of 0.1 A in the load from 0.2 A until 1.8 A. To do that, the power converter prototype has been fed by one programmable power source ELEKTRO-AUTOMATIK EA PSI-9750-40 and the load has been represented by means of one programmable electronic load ELEKTRO-AUTOMATIK EA ELR-9750-44 operating in constant current mode. The results presented in Fig. 19 show that both converters have efficiencies above 90% for almost the entire range of operation and the CIB converter has a slightly lower efficiency with a difference of no more than 0.25 % in the worst case. Due to n = 2 the magnetizing current has no switching ripple and the transformer losses must be small. Therefore, most of the efficiency differences between both converters are expected to be due to power losses in the CIB damping network. From Fig. 16(a) we approximately obtain Io = 1.3 A, D = 0,5 and T = 15 µs. Applying equations (20) and (43) the corresponding power losses at R_d for an output power P_o = 260 W are $P_{R_d,260}$ = 0.4582 W. In Fig. 19 the efficiency difference between both converters at P_o = 260 W is equal to 0.4603 W, thus validating CIB efficiency assumptions.

V. CONCLUSION

The work has presented the design procedure and analysis for ensuring QSW-ZVS operation applied to Coupled Inductor Boost converters. A variable-width hysteretic analog current controller is responsible for controlling the absolute valley

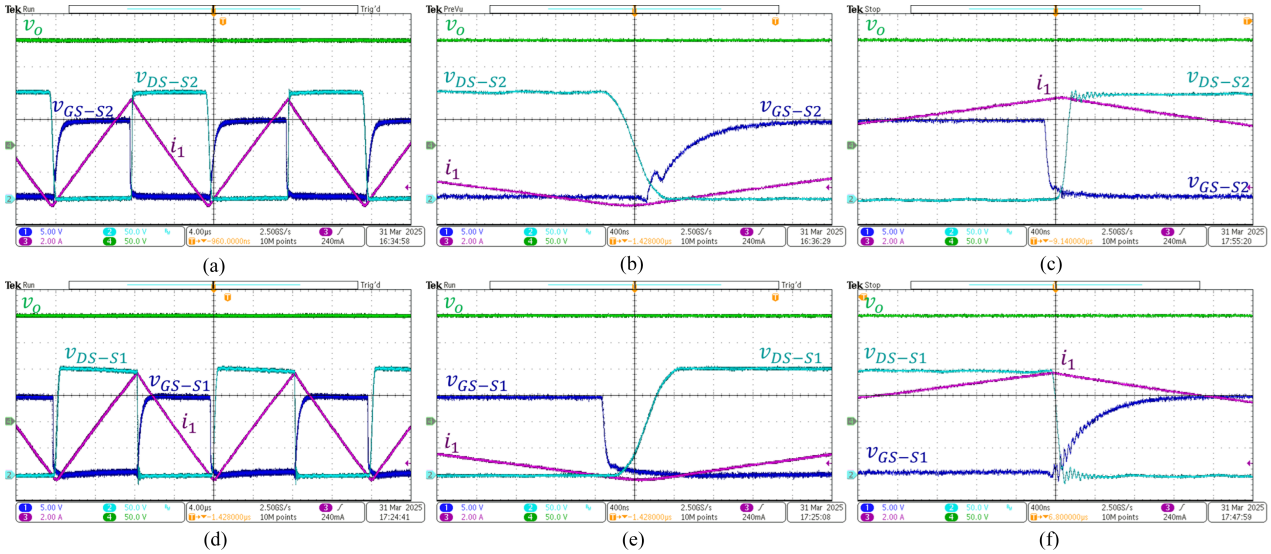

FIGURE 18. Experimental results detailing the switching events in the MOSFETs of the converter: (a) steady-state waveforms for S_2, (b) turn-on transition for S_2, (c) turn-off transition for S_2, (d) steady-state waveforms for S_1, (e) turn-off transition for S_1 and (f) turn-on transition for S_1.

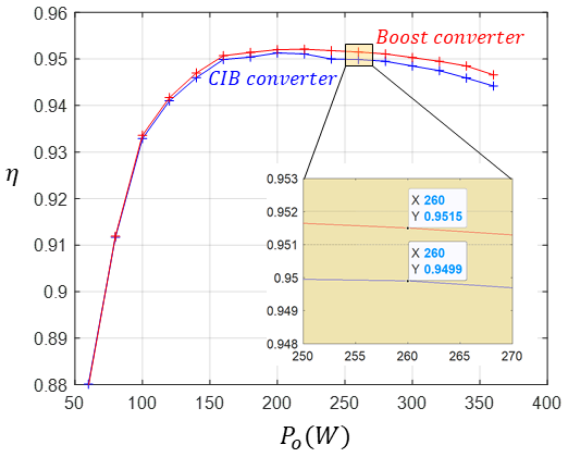

FIGURE 19. Experimental measurement of efficiency comparing the CIB and boost converters.

value of the input current i_1 guaranteeing QSW-ZVS in every operating condition. Besides, the absolute peak current value of i_2 is used to guarantee output voltage regulation. An outer voltage control loop is the responsible to supply this peak current reference. All the theoretical predictions have been validated by means of simulation and experiment showing the feasibility of the proposal. A comparison with an equivalent QSW-ZVS boost converter is realized. Simulation and experimental results show the CIB converter presents a faster transient behavior response to load perturbations because of the absence of RHPZ in the current reference to output voltage transfer function. CIB converter requires two current sensors, one more than the boost converter, and two additional components, a transformer and a damping resistor. However, high and similar efficiency values are obtained in both converters for all operating range. Not significant efficiency differences between both converters are due to power losses in the CIB damping network. Therefore, a trade-off between CIB and boost converter, both operating under QSW-ZVS conditions, should be done depending whether we want a faster converter response at a little bit higher cost.

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