Series Loss-Free Resistor as Stabilizing Active Damping of Constant-Power Load Systems

M. Sebastià-Rullo, A. Cid-Pastor, H. Valderrama-Blavi,
A. El Aroudi and L. Martínez-Salamero

***Abstract*— This paper presents the detailed design of an active damping system for the stabilization of an open-loop boost converter in constant-power load (CPL) operation. The reported work analyzes the steady-state regime of the interconnection of a boost converter supplying a CPL, and a loss-free resistor (LFR) in series with the converter input port (SLFR) performing the active damping. The LFR behavior is obtained by peak current mode control (PCMC) imposing proportionality between the steady-state average values of current and voltage in the SLFR input port. The isolated SEPIC fulfills the topological constraints of the interconnection and is selected to implement the SLFR. Finally, PSIM simulations and measurements from a 500 W prototype are in good agreement with the theoretical predictions and illustrate the system stabilization around the specified steady-state operating point for different values of the CPL power.**

***Index Terms*— Constant power load, series loss-free resistor, steady-state converters interconnection**

I. INTRODUCTION

CONSTANT-POWER load (CPL) regime is a usual operating mode in the multi-converter systems of electric vehicles (EVs), microgrids and power supplies for telecommunications [1]. A tight voltage regulation in the cascade connection of two power converters results in constant power operation, in which the first converter acts as source converter and the second one as load converter absorbing constant power. In EVs, CPL operation is reached under certain driving conditions, the most frequent being the result of a simultaneous operation at both constant speed and torque. The demand of mechanical constant power in the motor axis is transmitted backwards to the EV powertrain, so this effect can be modelled as a nonlinear one-port device absorbing constant electric power in the output port of the powertrain converter.

It is well-known that supplying constant power from dc-dc switching converters in open-loop and continuous conduction mode (CCM) results in unstable behavior [2], and therefore these systems must use an appropriate closed-loop control [3]-[5] to counteract their intrinsic instability. Stabilization can be also obtained for either open- or closed-loop operation by adding adequate passive [6] or active dampers.

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M. Sebastià-Rullo, A. Cid-Pastor, H. Valderrama-Blavi, A. El Aroudi and L. Martinez-Salamero are with the Group of Automatic Control and Industrial Electronics (GAEI), Rovira i Virgili University, Department of Electrical, Electronic and Automatic Control Engineering, School of Electrical and Computer Engineering, Campus Sescelades, 43007 Tarragona, Spain.

e-mail: max.sebastia@urv.cat, angel.cid@urv.cat hugo.valderrama@urv.cat, abdelali.elaroudi@urv.cat and luis.martinez@urv.cat.

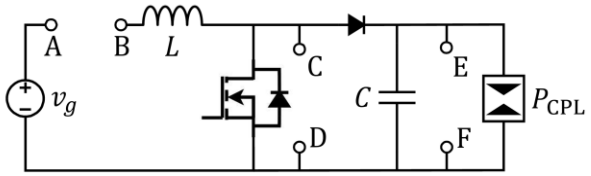

Fig. 1. Circuit diagram of a boost converter supplying a CPL with different insertion points for active dampers.

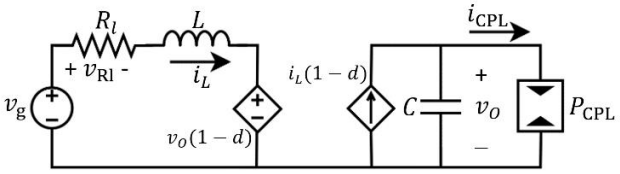

Fig. 2. Averaged circuit diagram of a boost converter, with a series resistor in the input port, supplying a CPL.

Several active damping approaches exist in the microgrid literature, most of them being based on the emulation of a passive element by means of an appropriate control strategy. This is the case of the work reported in [7]-[12], where damping is introduced by the control law without modifying the power stage topology. The latter is altered in [13] by the insertion of one-port device acting as virtual capacitor in an intermediate connection point between a source converter and a load converter. Similarly, a capacitor emulated by a bidirectional converter modifies the original topology of a microgrid when the virtual capacitor is connected in series with a CPL as explained in [14].

Unlike the mentioned active dampers, we investigate in this paper an alternative solution based on the insertion of a two-port circuit in the topology of a power converter supplying a CPL. The objectives of the insertion are:

(i) To stabilize the CCM open-loop operation of the converter with the minimum waste of energy.

(ii) To recycle the stabilizing energy in other parts of a multi-converter system.

If we consider a unidirectional boost converter representing the core of a multi-converter system, the insertion of the input port of an active two-port damper can be performed between nodes A and B, C and D or E and F as illustrated in Fig. 1. If the damper input port is a virtual resistance, a simple calculation will reveal that the minimum stabilizing energy will correspond to the A-B connection. For example, for an input voltage of 200 V, a CPL absorbing 500 W and an output voltage of 400 V, the minimum power that a virtual resistance between A and B would absorb is 0.45 W, while

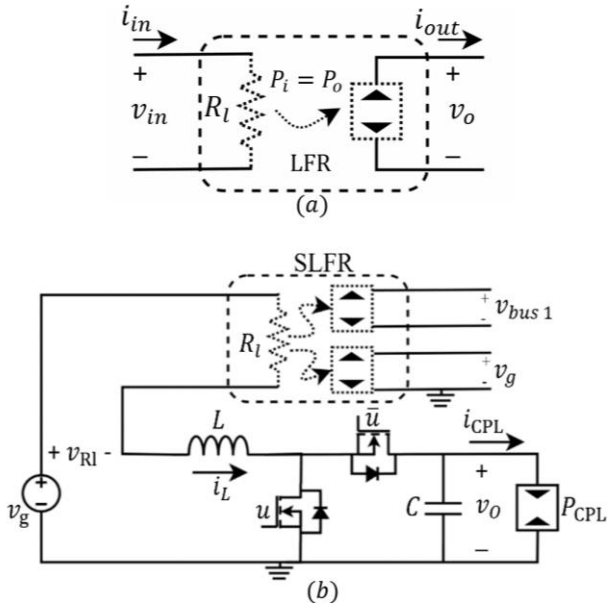

Fig. 3. Emulation of the virtual resistance of Fig. 2. (a) LFR model (b) Series connection of the LFR and the boost converter in the input port and reinjection of energy to the battery or to a secondary bus.

between C and D and E and F would require at least 250 W and 500 W respectively.

The CPL operation in a boost converter in open-loop and CCM can be analyzed using the averaged circuit model depicted in Fig. 2. In that figure, *d* represents the converter duty cycle, the nonlinear load is the CPL, and R_l represents the emulated resistance in the damper input port connected between nodes A and B of Fig. 1. Therefore, the input port of the two-port damper must be connected in series with the input port of the boost converter and exhibits resistive characteristics. Both requirements point out that the two-port damper must be a series loss-free resistor (SLFR) whose interconnection with the boost converter is illustrated in Fig. 3. It can be observed in the figure that the input port of the SLFR is modelled by a virtual resistor R_l, and the output port is represented by a power source that supplies the power absorbed in the input port to any load connected at the output terminals.

The underlying idea is inserting the necessary damping to stabilize the main converter and reinjecting the energy absorbed by the virtual resistor to other part of the electrical architecture of the system, this including the input battery or a secondary bus as shown in Fig. 3.

The rest of the paper is organized as follows. The application of the concept of loss-free resistors (LFR) in power electronics is reviewed in Section II and the selection of the converter topology for SLFR implementation is justified in Section III. The operating conditions for the series connection of the input port of the boost converter and the SFLR are studied in Section IV together with the analysis of the interconnected system as a single topology. The stability analysis of the SLFR is carried in Section V. Simulation and experimental results are given in Section VI. Next a discussion about the applications of the presented implementation is provided in Section VII. Finally, conclusions are summarized in Section VIII.

II. Review of LFR Applications

LFRs have been used to compensate resistive losses in power supplies for lasers [15] or to stabilize the oscillations produced by ferroresonant phenomena in medium voltage transformers [16]. In both cases, LFRs are based on the buck-boost converter operation in discontinuous conduction mode (DCM) [17], [18]. Besides, combining DCM and interleaving can lead to LFR characteristics in flyback converters as reported in [19].

Moreover, the synthesis of LFRs with the input port connected in parallel with the external energy source was reported in [20] and extended in [21] to a 3-phase system. In both cases, sliding-mode control (SMC) [22] imposes proportionality between the steady-state values of input current and voltage in a power converter in continuous conduction mode (CCM), and allows the LFR application in the maximum power point tracking of photovoltaic systems (PVs) and in the power factor correction (PFC) of voltage rectifiers and pre-regulator power stages.

Based on that synthesis, impedance matching in photovoltaic (PV) generators is attained by means of interfacing converters with LFR characteristics as reported in [23]. In addition, maximum power point tracking in PV generators is obtained when the inner loop of the cascade control of the matching converter imposes LFR behavior to the power stage [24].

PFC in interleaved operation of two boost converters is the result in [25] of a discrete-time SMC-based PWM approach that imposes LFR on each converter. It is also the consequence of SMC application in a boost converter [26] yielding LFR behavior or the result of adaptive current control as reported in [27]. More recently, it has been demonstrated that transferring energy from a dc source to a generic nonlinear static load can be successfully performed using a boost converter with SMC-based LFR behavior [28].

A first proposal of SLFR has been presented in [29] and consists of an LFR whose virtual resistance is connected in series between the input and output ports of a power stage, and its power source is connected in parallel with the external energy source as illustrated in Fig. 4. In that work, the SLFR is implemented using a power converter operating in DCM, and is applied to compensate losses in the activation circuitry of the power devices of a push-pull converter. The latter SLFR notion is extended in [30] to a power converter in CCM operation whose LFR behavior is imposed by a dedicated current loop.

The goal of this paper is to demonstrate that a new type of SLFR can be designed by imposing proportionality between current and voltage in its input port by means of an appropriate control in CCM operation, where the current reference is generated proportionally to the input voltage. The input port of the proposed SLFR is connected in series with the main power stage feeding a CPL in open-loop in order to emulate a resistor and introduce an appropriate damping for stabilization. The output port of the proposed SLFR must have galvanic isolation with respect to the input port to avoid short-circuits between terminals of different voltage, and hence the power absorbed by the emulated resistor

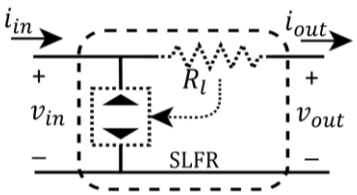

Fig. 4. Schematic circuit diagram of the source-side SLFR-based two-port network proposed in [29].

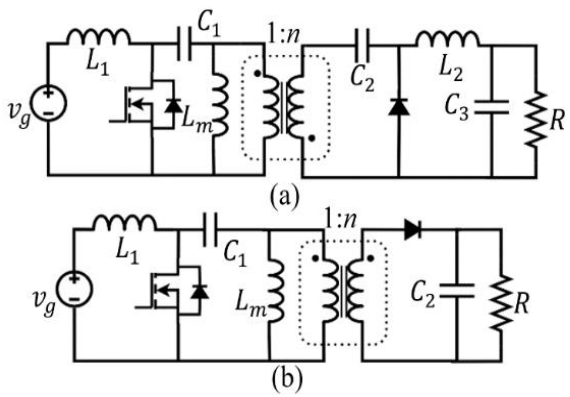

Fig. 5. Circuit schematics of the galvanic-isolated power converters with an inductor in the input port (a) Isolated Ćuk (b). SEPIC.

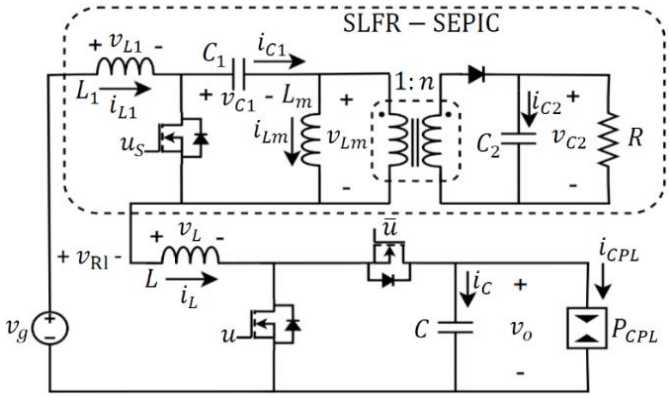

Fig. 6. Implementation of the SLFR of Fig. 3 by means of a SEPIC and reinjection of energy to a secondary bus.

can be easily transferred to a secondary bus or even reinjected to the input energy source (Fig. 3 (b)).

Therefore, the work here reported solves the design problems caused by the series connection of the input ports of a boost converter and a SEPIC, the latter being selected to implement the SLFR with the required galvanic isolation. On the one hand, the interconnection requires a synchronous operation of both converters, which implies a pulse width modulation (PWM)-based control for both of them, and identical switching frequency and duty cycle. On the other hand, the design has to take into account the constraints ensuring the stability of the boost converter.

III. SLFR Topology

It has to be pointed out that the candidates for SLFR must have an inductor in series with the input voltage in order to impose proportionality between current and voltage in that port in steady-state using an appropriate control strategy as explained in [20]. This topological constraint in the input port is because controlling the input inductor current leads to a stable equilibrium point in most hard switching converters. On the other hand, to ensure the versatility of the output port of the active damper, the SLFR requires galvanic isolation to facilitate the connection to any secondary bus. Note, for example, that the reinjection of energy from the SLFR output port to the boost input port wouldn't be possible in the absence of galvanic isolation. From the topological classification in [31]-[32], we can select at least two converters meeting the requirements of series inductor in the input port and galvanic isolation; namely, the isolated Ćuk converter and the SEPIC. We have selected SEPIC due to the lower number of components as illustrated in Fig. 5. The damping system based on SLFR will be implemented by means of the SEPIC stage interconnected with the boost converter as illustrated in Fig. 6. The energy absorbed by the emulated resistor of the active damper will be reinjected to a secondary bus loaded with a resistor *R*.

In addition, since both converters will have the same input current, the design of the interconnection must ensure that the operation of the SLFR does not affect the operation of the boost converter. For that reason, the switching frequency of the SEPIC and the boost converter will be equal which eventually will imply the simultaneity of states ON and OFF, CCM, and the same duty cycle in steady-state.

Notice that the waveform of the input current and its ripple is directly affected by the switching frequency and the duty cycle of both converters. Any mismatch in switching frequency will drive the system into a multi-state scenario resulting in unpredictable behavior. For this reason, the clock signal that sets the start and end of the switching period must be the same in both converters.

On the other hand, any mismatch in the duty cycle can lead to two possible situations. Considering that the boost converter works in open-loop and therefore the duty cycle is constant, the two possible scenarios correspond to the duty cycle of the SEPIC being higher or lower than that of the boost converter. In any of these cases, a time subinterval appears in which the non-simultaneity of states in the converter causes the appearance of an interval in the waveform of the input current ripple that precludes the separated analysis of the two converters and complicates the design process due to the impossibility of studying the independent operation of the converters.

IV. Design Constraints

The design of the interconnection has to take into account the effect of the resistance R_l of the emulated resistor in the steady-state output voltage of both SEPIC and boost converter as well as in the resulting stability margin of the latter. The characteristic polynomial corresponding to the linearized averaged model of the boost converter depicted in Fig. 2 is

$$s^2 + \left(\frac{R_l}{L} - \frac{P_{CPL}}{V_o^2 C}\right)s - \frac{1}{LC}\left((1-D)^2 - \frac{P_{CPL}\cdot R_l}{V_o^2}\right) \quad (1)$$

where *D* is the value of the duty cycle. It can be concluded from (1) that the boost converter will be stable if R_l satisfies the following inequality

$$\frac{P_{\mathrm{CPL}} L}{V_o^2 C} < R_l < \frac{V_o^2 (1-D)^2}{P_{\mathrm{CPL}}} \quad (2)$$

On the other hand, the steady-state average value of the output voltage of the boost converter will be given by

$$V_o = \frac{1}{2\cdot(1-D)}\left(V_g + \sqrt{V_g^2 - 4P_{\mathrm{CPL}}R_l}\right) \quad (3)$$

Besides, the steady-state input voltage of the SEPIC can expressed as

$$V_{Rl} = R_l \cdot I_L \tag{4}$$

where current I_L is the steady-state averaged value of the input current in the boost converter and can be obtained as follows

$$I_L = \frac{P_{\mathrm{CPL}}}{(1-D)V_o} \tag{5}$$

In addition, the steady-state value of the SEPIC output voltage is

$$V_{C2} = \frac{D \cdot n \cdot V_{\mathrm{Rl}}}{(1-D)} \tag{6}$$

where D is the steady-state value of the duty cycle and n is the transformer ratio of the SEPIC. Introducing (4) and (5) into (6) yields

$$R_l = \frac{(1-D)^2 \cdot V_{C2} \cdot V_o}{D \cdot n \cdot P_{\mathrm{CPL}}} \tag{7}$$

which is the constraint on the resistance of the emulated resistor imposed by the SEPIC. Finally, solving for R_l in (3) leads to the constraint on R_l introduced by the steady-state operation of the boost converter.

$$R_l = \frac{V_g \cdot V_o \cdot (1-D) - (1-D)^2 \cdot {V_o}^2}{P_{\mathrm{CPL}}} \tag{8}$$

Finally, if a resistive load is selected for the SEPIC the following expression must be taken into account.

$$R = \frac{{V_{C2}}^2}{{I_L}^2 R_l} = \frac{n^2 D^2 R_l}{(1-D)^2} \tag{9}$$

Therefore, for given values of V_g, V_o and P_{CPL}, we must verify that there is a pair (D, R_l) that satisfies simultaneously the steady-state constraints of SEPIC and boost converter, and also corresponds to a stable design. That pair corresponds to point P in Fig. 7 (a) for the set of parameters $V_g = V_{C2} = 200$ V, $V_o = 400$ V and $P_{\mathrm{CPL}} = 500$ W. Note that P is located in the stability reg

ion given by inequality (2), which is shaded in the plane $D-R_l$. A second situation is presented in Fig. 7 (b) for the set of parameters $V_g = 50$ V, $V_o = V_{C2} = 100$ V and $P_{\mathrm{CPL}} = 200$ W.

The stability region and hence the appropriate design zone is the volume corresponding to the stable zone in the 3-D representation of Fig. 8, in which besides the duty cycle and damping resistance, the value of the CPL has been considered as an independent variable. If the design conditions leading to point P in Fig. 7 are satisfied, the interconnection behaves like a single converter with five state variables provided that the magnetic transformer is modelled by a first-order circuit based on the magnetization inductance L_m and an ideal transformer. Note that both converters have the same input inductor current, i.e. $i_{L1} = i_L$, and therefore the interconnection has the four state variables of the SEPIC plus the one added by the capacitor voltage of the boost converter. In that case, the ideal steady-state waveforms of inductor voltages and capacitor currents in CCM plus the corresponding transistor activation signal $u(t)$ can be represented as depicted in Fig. 9.

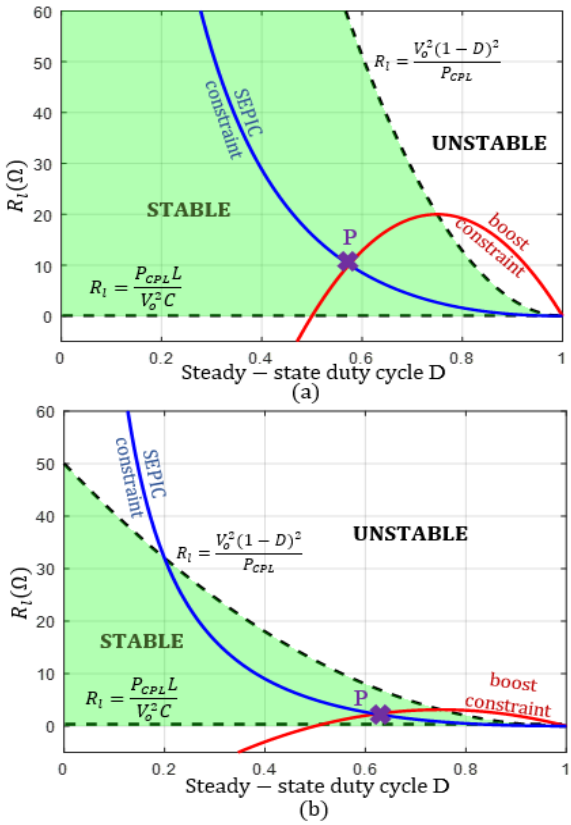

Fig. 7. Operating point of the interconnection within the stability region. (a) $V_g = V_{C2} = 200$ V, $V_o = 400$ V, and $P_{\mathrm{CPL}} = 500$ W. (b) $V_g = 50$ V, $V_o = V_{C2} = 100$ V and $P_{\mathrm{CPL}} = 200$ W.

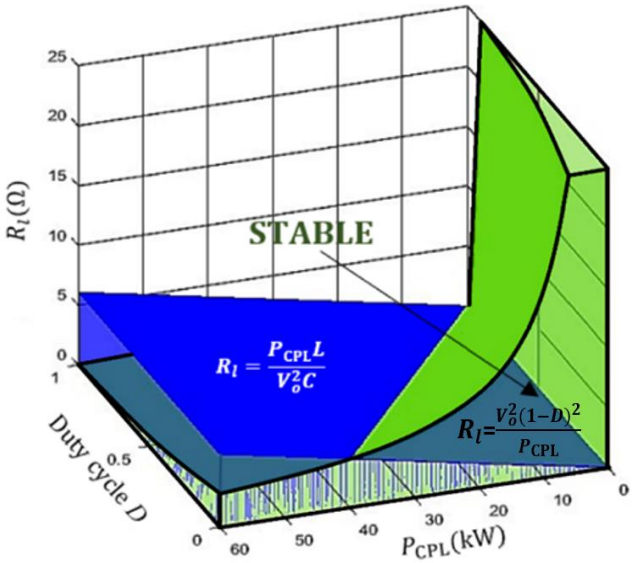

Fig. 8. Stability region of the boost converter supplying a CPL in the parametric space $(D, P_{\mathrm{CPL}}, R_l)$ for $V_g = V_{C2} = 200$ V and $V_o = 400$.

V. SEPIC SLFR Stability Analysis

Peak current mode control (PCMC) is used to emulate a resistive behavior in the input port of the SEPIC [33]. With this aim, input current $i_{L1}(t)$ tracks the reference $i_{\mathrm{ref}}(t)$, which is proportional to the converter input voltage $v_{\mathrm{Rl}}(t)$ as illustrated in the block diagram of Fig. 10, in which a compensating ramp has been

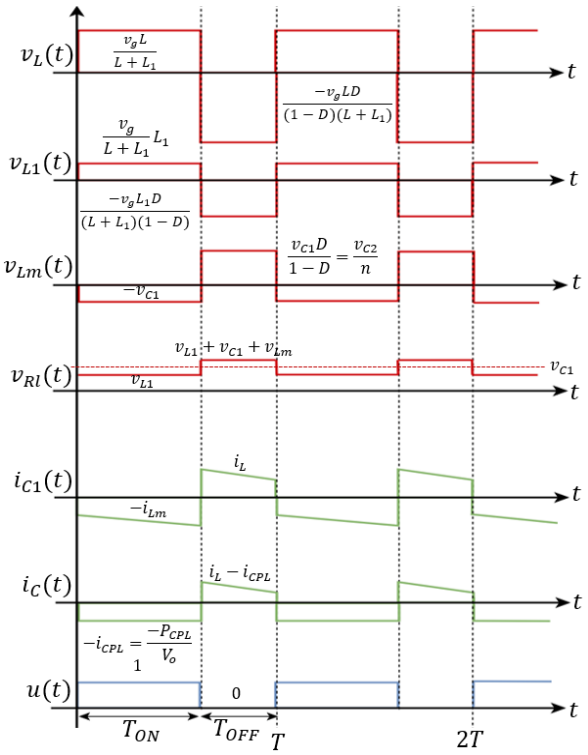

Fig. 9. Theoretical steady-state waveforms of the resulting interconnection within the stability region.

included to avoid subharmonic oscillations for duty cycles higher than 0.5. The SET signal provided by the clock is synchronized with the compensating ramp to ensure that the transistor is activated at the beginning of the switching period and therefore the flip-flop enables the control signal $u_s(t)$ and the ON state starts. When $i_{L1}(t)$ reaches the reference, given by i_{ref} minus the compensating ramp, a reset signal is sent to the flip-flop, $u_s(t)$ is disabled and the OFF state begins. The waveforms of $i_{L1}(t)$ and its effective reference including the compensating ramp are illustrated in Fig. 11 for one switching cycle. With the described control system, under transient conditions, for which $i_{L1}(0) \neq i_{L1}(T)$, the averaged expression of the inductor current $\langle i_{L1}(t)\rangle$ can be expressed in terms of the inductor current slopes m_1, m_2 and compensating ramp slope m_a as follows

$$\langle i_{L1}\rangle = \langle i_{ref}\rangle - m_a T d - \frac{m_1 T d^2}{2} - \frac{m_2 T(1-d)^2}{2} \quad (10)$$

where d is the duty cycle corresponding to the SEPIC SLFR.

If we consider each variable as the sum of its dc value and its ac small signal value and we keep only the first order ac small signal terms, (10) can be arranged as follows.

$$\hat{d} = \frac{1}{M_a T}\left(\hat{\imath}_{\text{ref}} - \hat{\imath}_L - \frac{T}{2}[D^2\hat{m}_1 + (1-D)^2\hat{m}_2]\right) \quad (11)$$

where D is the steady-state value of d.

It has to be pointed out that the small signal perturbation of the slope of the compensating ramp is considered null ($\hat{m}_a = 0$), and furthermore, that in steady-state operation one has $DM_1 = (1-D)M_2$, where M_1 and M_2 stand for the equilibrium values of m_1 and m_2 respectively. Replacing the current perturbed slopes by their expressions given in (12) obtained for the SEPIC, the small signal duty cycle $\hat{d}$ can be expressed as in (13) whose coefficients can be found at TABLE I.

$$\hat{m}_1 = \frac{\hat{v}_{Rl}}{L_1}, \qquad \hat{m}_2 = -\frac{\hat{v}_{Rl} - \hat{v}_{C1} - \hat{v}_{C2}/n}{L_1} \quad (12)$$

$$\hat{d} = F_m\left(\hat{\imath}_{\text{ref}} - \hat{\imath}_L - \hat{v}_{Rl}F_g - (\hat{v}_{C1}n + \hat{v}_{C2})F_v\right) \quad (13)$$

Note that since we are implementing an LFR, the input voltage should be proportional to the input current, and $\hat{\imath}_{ref}$ is replaced by $\hat{V}_{Rl}(s)\cdot C(s)$, the factor $C(s)$ being a transfer function that ensures the proportionality of the mentioned averaged variables and introduces additional dynamics to the system. Also, each variable can be replaced by the effect that a disturbance in the duty cycle or in the input voltage causes in it, as expressed in (14), (15) and (16).

$$\hat{I}_L = G_{ig}(s)\hat{V}_{Rl} + G_{id}(s)\hat{D} \quad (14)$$

$$\hat{V}_{C1} = G_{v1g}(s)\hat{V}_{Rl} + G_{v1d}(s)\hat{D} \quad (15)$$

$$\hat{V}_{C2} = G_{v2g}(s)\hat{V}_{Rl} + G_{v2d}(s)\hat{D} \quad (16)$$

Using the previous expressions, the block diagram small signal model shown in Fig. 12 is obtained. It is observed that this model depends on the transfer functions $G_{ig}(s)$, $G_{v1g}(s)$ and $G_{v2g}(s)$, that relate the input voltage $\hat{V}_{Rl}$ with $\hat{I}_L$, $\hat{V}_{C1}$ and $\hat{V}_{C2}$ respectively. It also depends on $G_{id}(s)$, $G_{v1d}(s)$ and $G_{v2d}(s)$ that relate the duty cycle $\hat{D}$ with the same state variables. These transfer functions can be easily obtained from the averaged model of the SEPIC operating in continuous conduction mode and have the general expression $G_{XY}(s)$ given in (17), and whose coefficients are shown in TABLE II and TABLE III.

$$G_{YX}(s) = \frac{N_O(s)}{D_E(s)} = K\frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (17)$$
$$Y = \{i, v_1, v_2\}; \quad X = \{d, g\}$$

Once the previous transfer functions have been detailed, it is possible to obtain a model that relates the state variables of the SEPIC with PCMC and the system inputs. Expression (18) relates the small-signal variations of the input inductor current with the small-signal variations of the input voltage once the described control is implemented in closed loop.

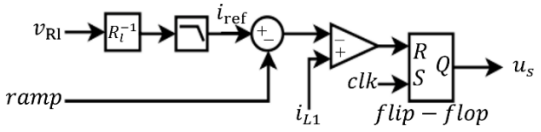

Fig. 10. Block diagram of the PCMC.

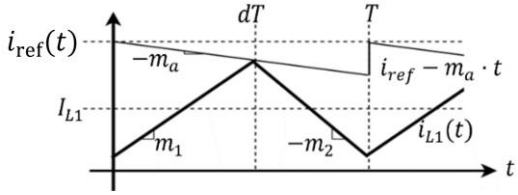

Fig. 11. Waveforms of the controlled current and its reference including the effect of the compensating ramp.

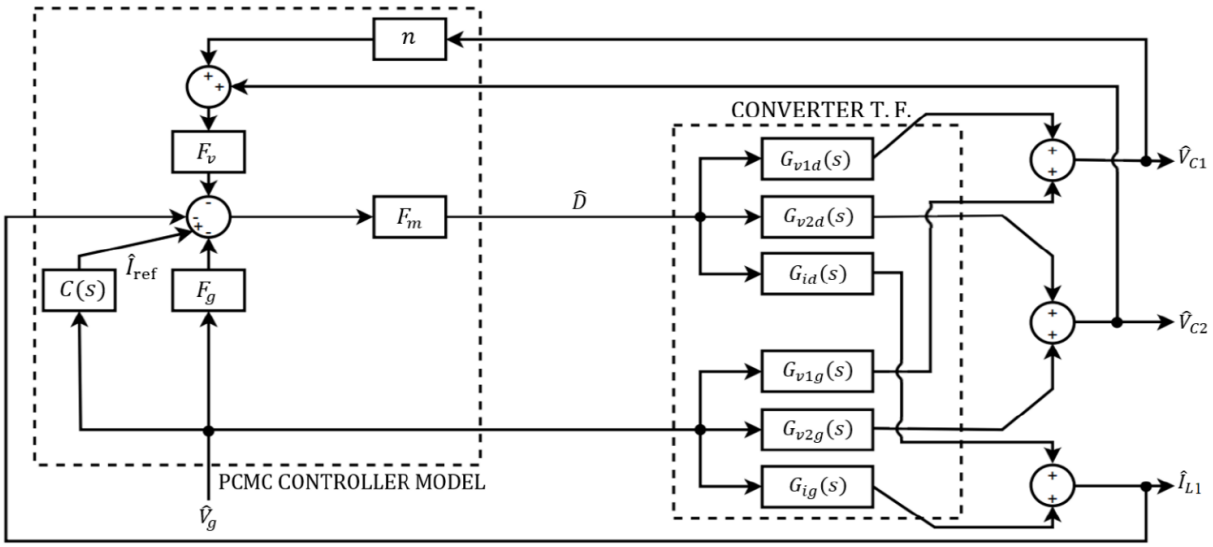

Fig. 12. Block diagram of the SEPIC with peak current mode control imposing the LFR behavior.

$$G_{ig\ closed\ loop}(s) = \frac{F_m G_{id}\left(C - G_{ig} - F_g - F_v[G_{v1g}\cdot n + G_{v2g}]\right) + (1 + F_m(G_{id} + F_v[G_{v1d}\cdot n + G_{v2d}]))G_{ig}}{1 + F_m(G_{id} + F_v[G_{v1d}\cdot n + G_{v2d}])} \quad (18)$$

TABLE I
PCMC SMALL SIGNAL GAINS FOR THE SEPIC

F_m	F_g	F_v
$\frac{1}{m_a T}$	$\frac{T}{2L_1}(2D-1)$	$\frac{T}{2nL_1}(1-D)^2$

TABLE II
COEFFICIENTS OF THE DENOMINATOR OF THE TRANSFER FUNCTIONS OF THE SEPIC IN CCM

$$b_3 = \frac{1}{C_2 R}$$
$$b_2 = (1-D)^2\left(\frac{1}{C_1 L_1} + \frac{1}{C_1 L_m} + \frac{1}{C_2 L_m n^2}\right) + \frac{D^2}{C_1 L_m}$$
$$b_1 = \frac{1}{C_1 C_2 R}\left(\frac{(1-D)^2}{L_1} + \frac{D^2}{L_m}\right)$$
$$b_0 = \frac{(1-D)^2}{C_1 C_2 L_1 L_m n^2}$$

TABLE III
COEFFICIENTS OF THE NUMERATOR OF THE TRANSFER FUNCTIONS OF THE SEPIC IN CCM

	K	a_3	a_2	a_1	a_0
G_{ig}	$\frac{1}{L_1}$	1	$\frac{1}{C_2 R}$	$\frac{D^2}{L_m C_1} + \frac{D'^2}{L_m C_2 n^2}$	$\frac{D^2}{C_1 C_2 L_m R}$
G_{id}	$\frac{V_g}{D' L_1}$	1	$\frac{Dn^2}{RC_1} + \frac{D+1}{C_2 R}$	$\frac{D(C_2 R^2 + L_m n^2)}{C_1 C_2 L_m R^2}$	$\frac{2D}{C_1 C_2 L_m R}$
G_{v1g}	$\frac{D'}{C_1 L_1}$	0	1	$\frac{1}{C_2 R}$	$\frac{D'}{C_2 L_m n^2}$
G_{v1d}	$\frac{-DV_g n^2}{D'^2 R C_1}$	1	$-\frac{RD'^2}{L_1 D n^2} - \frac{RD'}{L_m n^2} + \frac{1}{C_2 R}$	$\frac{(D' L_m - 2DL_1)D'}{DC_2 L_1 L_m n^2}$	0
G_{v2g}	$\frac{D'}{C_1 L_1}$	0	1	0	$\frac{D}{C_1 L_m}$
G_{v2d}	$\frac{-V_{C2}}{D' R C_2}$	1	$-\frac{R(L_1+L_m)D'^2}{L_1 L_m n^2 D}$	$\frac{D}{C_1 L_m}$	$\frac{V_g}{Dn^2 L_1 L_m C_1}$

The goal now is to approach the stability analysis of the system. Observe that the denominator of the transfer function $G_{ig\ closed\ loop}(s)$, can be interpreted as the characteristic polynomial of a closed –loop negative feedback system, in which F_m is a constant multiplying the loop gain $\boldsymbol{T}(s)$.

$$1 + F_m \cdot \boldsymbol{T}(s) = 0 \quad (19)$$

where $\boldsymbol{T}(s)$ is given by the following expression

$$\boldsymbol{T}(s) = G_{id}(s) + F_v(G_{v1d}(s)\cdot n + G_{v2d}(s)) \quad (20)$$

Since F_m is inversely proportional to slope m_a of the compensating ramp, the root-locus of the system can be eventually represented as a function of slope m_a. This is illustrated in Fig. 13 (a), in which the plots corresponding to four different values of m_a and the set of parameters $V_{Rl} = 29.5\,V$, $R = 460.45\,\Omega, R_l = 3.2\,\Omega$, $L_1 = 84$ µH, n = 5 $C_1 = 30$ µF and $C_2 = 10$ µF. Furthermore, Fig. 13 (a) confirms the stability of the LFR since all the poles of the system are located in the left half-plane.

Note that given the implementation of the system, to ensure the proportionality between the input current and voltage in the SLFR, the amplitude of the compensating ramp must be minimal. It should also be considered that to avoid subharmonic phenomena that PCMC can induce when the duty cycle is greater than 0.5, the slope must meet certain restrictions. Therefore, in order to guarantee stability of the system for all the values of the duty cycle the following inequality must be satisfied [17]:

$$m_a \geq -\frac{1}{2} m_2 \quad (21)$$

Fig. 13 also shows the PSIM simulation of the input inductor current response to 1 V step variations of the input voltage for four different values of m_a. It can be observed that the smaller the amplitude of the compensating ramp is, the more damped the

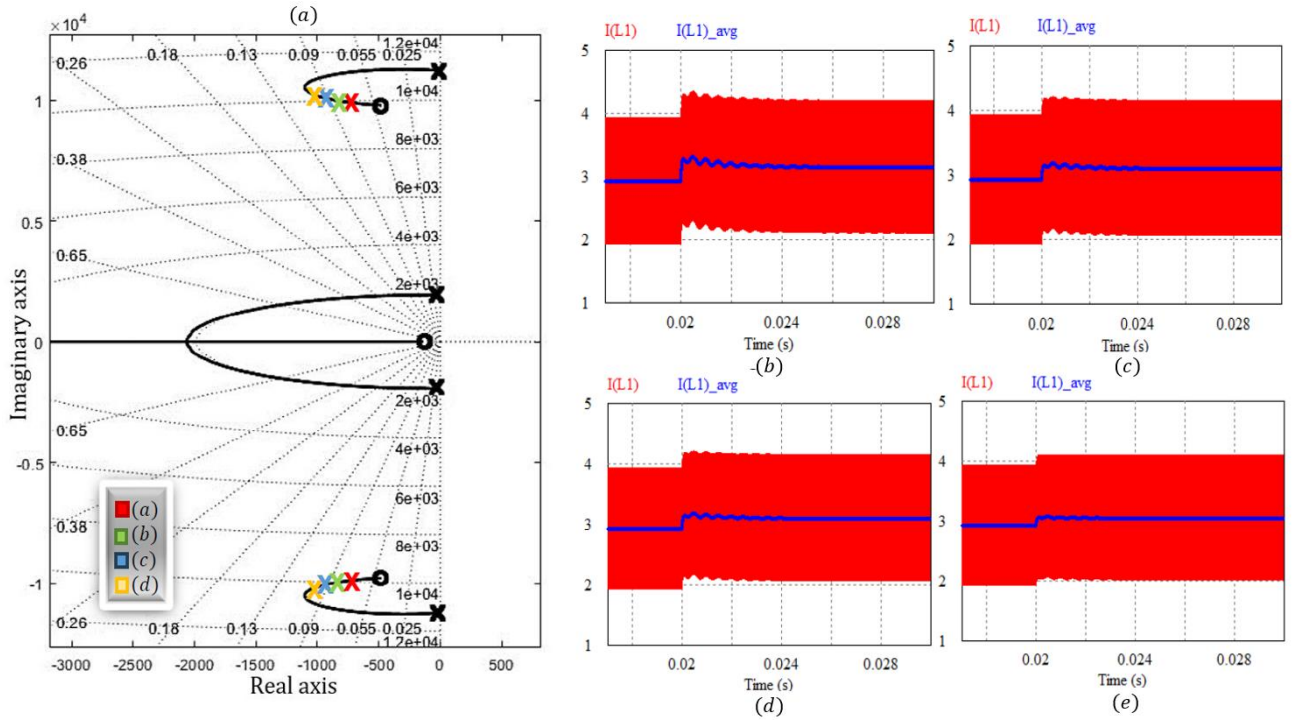

Fig. 13. (a) Root loci of the characteristic polynomial (19) and time response to step variations of the input voltage for (b) $m_a = -4\,m_2$, (c) $m_a = -2\,m_2$ (d) $m_a = -\,m_2$ and (e) $m_a = -0.5\,m_2$.

voltage. In addition, it can be observed that the transfer function (18) predicts accurately the behavior of the system as it can be verified by a quick inspection of the blue line in the time-domain responses of Fig. 13.

VI. Simulations and Experimental Results

An experimental prototype has been implemented to validate the theoretical predictions. The input voltage supplied by a battery is 200 V, the boost converter output voltage is 400 V while the SEPIC ideally delivers 200 V to a secondary bus. The experimental parameters and results obtained from the implemented prototype are summarized in TABLE IV both for the isolated operation of the SLFR and for two different experiments carried out with both converters interconnected.

The experimental setup is illustrated in Fig. 14 and is composed of a Tektronix MD0314 Mixed Signal Oscilloscope, an ISO-TECH IDM 205 RMS precision multimeter, a TTI EX354T DC voltage supply for the control board, a GW INSTEK-MFG-2260M multi-channel function generator, an Ametek SPS800x13-K02D supply for the power circuit and the Elektro-Automatik EA-EL 9750-75 HP electronic load.

The schematic diagram of the power circuit for the boost converter and SEPIC is depicted in Figs. 15 (a) and 15 (b) respectively, while the control circuit is represented in Fig. 16.

The laboratory prototype of the SEPIC-based LFR has been implemented using an inductor with inductance L_1 = 84 µH, a transformer, implemented in a ferrite Pot Core 36/22, with a magnetizing inductance of 60 µH and a turns ratio n = 5 and thin film capacitors with capacitances C_1 = 30 µF and C_2 = 10 µF. Finally, IRFP27N60KPBF MOSFETS and C4D02120E silicon carbide Schottky diodes have been also used in both the

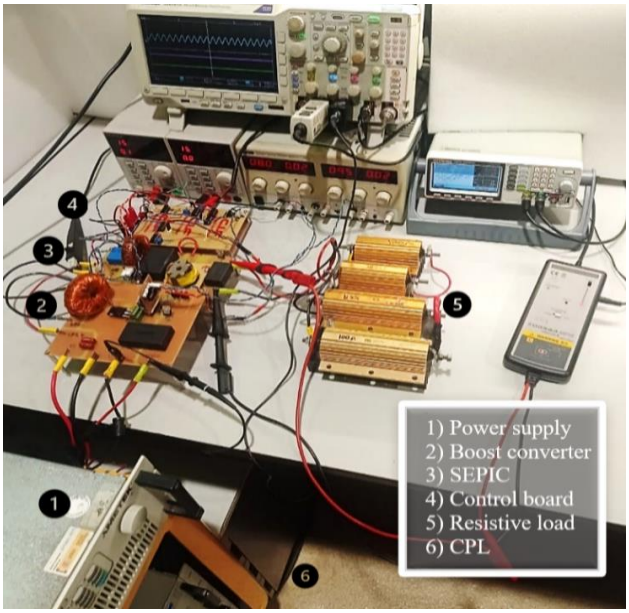

Fig. 14. Experimental setup.

TABLE IV
System Parameters and Experimental Results

	Isolated SLFR	BOOST + SLFR Experiment 1	BOOST + SLFR Experiment 2
V_g	-	200 V	50 V
v_{Rl}	8 V	30 V	12 V
R_l	4 Ω	11 Ω	2.7 Ω
V_o	-	400 V	100 V
V_{C2}	40 V	178 V	100 V
P_{CPL}	-	500 W	200 W
R	100 Ω	450 Ω	150 Ω

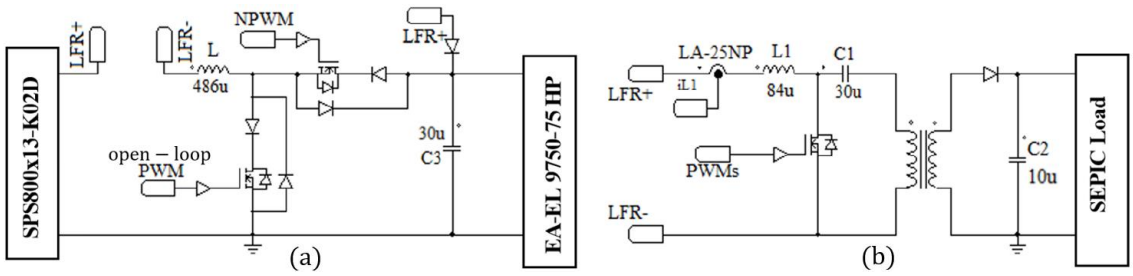

Fig. 15. Schematic circuit diagram of the implemented power stages of the experimental prototype (a) boost converter (b) SEPIC.

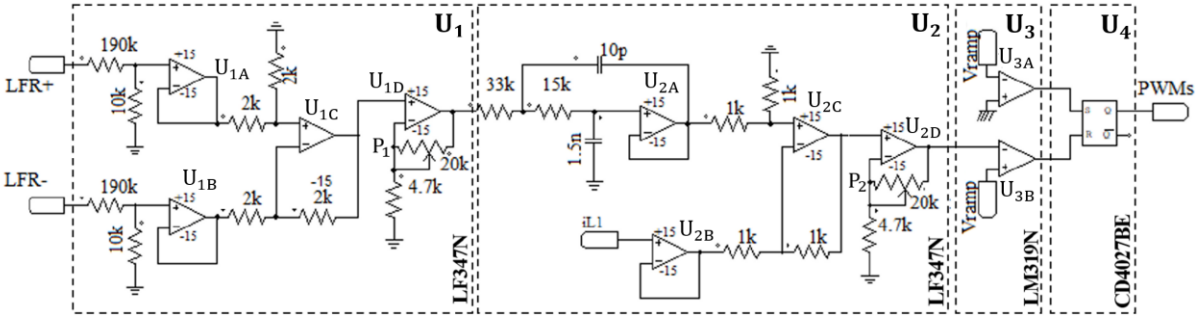

Fig. 16. Schematic circuit diagram of the implemented control of the experimental prototype.

SEPIC and the boost converter. These diodes have been added to the boost converter to ensure the bi-directionality of the prototype, and the initial charge the output capacitor of the boost converter to the input voltage, to obtain a smoother start-up. On the other hand, the laboratory prototype of the boost converter, has been implemented with an inductance L = 486 µH and a thin film capacitor with capacitance C = 30 µF. A PWM modulator based on the LM319N (U_3) comparator and the CD4027BE (U_4) flip-flop acting as a set/reset bistable activates the boost converter.

The operational amplifiers contained in the LF347N (U_1, U_2) integrated circuit with the mentioned comparator and flip-flop impose the LFR behavior to the SEPIC using a peak current control with a compensating ramp of slope m_a = 0.24 V/µs. A classical design of the controller [17] ensures the stability of the SLFR.

Note that, using U_{1A} and U_{1B} of the stage U_1 in Fig. 16, the input voltage of the LFR is differentially sensed. These two voltages are then subtracted at U_{1C} to obtain -v_{Rl}. Next, the value of this voltage is inverted and multiplied by the gain given by the potentiometer P_1 to obtain a reference value of v_{Rl}/R_l at the output. In the next stage, the ripple in the SLFR input voltage is filtered using the second-order Sallen-Key filter implemented in U_{2A}. The signal from the current sensor is processed in U_{2B} and both are subtracted in U_{2C}. Finally, the result is multiplied by the gain value given by the second potentiometer P_2.

The next stage generates the activation (SET) and deactivation (RESET) signals required by the SLFR MOSFET driver. The SET signal is the result of comparing a high-frequency periodic sawtooth signal with a small offset voltage in U_{3A}. The RESET signal results in U_{3B} from the comparison of the output of stage U_2 with the mentioned sawtooth signal that implements here the effect of the compensating ramp.

For comparison purposes, the ideal operation of the SEPIC implementing a LFR with the mentioned control law is illustrated through PSIM simulations. The waveforms obtained from the experimental prototype are shown in Figs. 17-21 together with the simulated results.

A. Simulations and experiments for the SEPIC LFR

To check the proper functioning of the SEPIC-based LFR, a disturbance in the input voltage is simulated in order to validate that the input current follows the imposed proportionality and therefore the input port behaves like a resistor.

The SEPIC input voltage v_{Rl} supplied by an external supply is 8 V initially and the emulated resistance is $R_l = 4\ \Omega$. At this operating point the SEPIC ideally delivers 40 V to a secondary bus and demands 1.95 A to the source. In this case, its load is a 100 Ω resistor. In Fig. 17 (a) we can observe the simulated transient response due to an increase of 4 V in the input voltage. At this new point of operation, the output voltage is 67 V and the input current is 3.6 A.

It can also be seen that the results obtained with the small-signal averaged model, match perfectly with the switched model results, and with the measured results from the experimental prototype, hence validating the theoretical predictions of Section IV.

The resulting efficiency of the implemented SLFR drops to 82 % with respect to 100% assumed in the simulation mainly due to the magnetic losses of the converter. As can be seen in Fig. 17 (b), which was obtained using the same set of parameter values as the PSIM simulation, the input voltage and the input current match perfectly with the simulation but the output voltage drops to 33 V in the first part of the experiment and to 60 V after the transient.

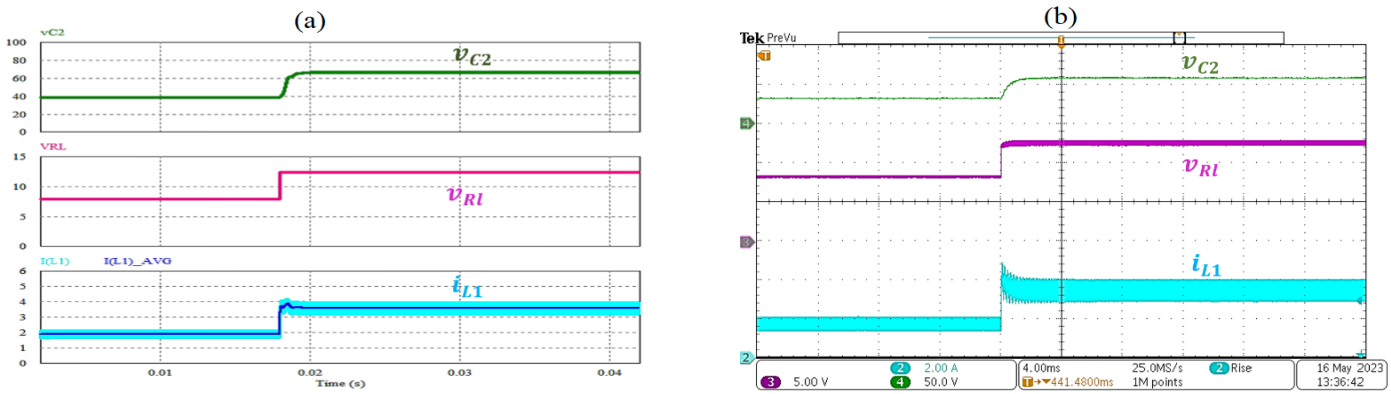

Fig. 17. Results of the waveforms of a 4 V disturbance in the input voltage of the SEPIC-based LFR for $R_l = 4\ \Omega$ and $R = 100\ \Omega$. (a) numerical simulations, (b) experimental mesaurements.

B. Simulations and experiments for the open-loop boost with CPL stabilized by the SLFR

In this section, experimental results for two different operating points are presented. In the first part the input voltage supplied by a battery is 200 V, the open loop boost converter provides 400 V while the SEPIC ideally delivers 200 V to a secondary bus loaded with a 460 Ω resistor. The results presented correspond to the parameters shown in the caption of Fig. 7 (a).

The PSIM simulation results shown in Fig. 18 illustrates the stabilizing effect of the SEPIC acting as an SLFR. The open-loop boost converter loaded with a 500 W CPL is initially unstable and the instability is eliminated when the SLFR is connected. Considering ideal behavior, the absorbed power by the SEPIC is 87 W while the delivered power by the battery is 587 W and the transferred power to the load is the required constant power of 500 W. The emulated resistance is $R_l = 11\ \Omega$ matching the graphical result shown in Fig. 7 (a).

The measured efficiency of the implemented SLFR matches with the one estimated in the previous section, in which the SEPIC was operating independently. Measurements for the same input voltage and CPL power P_{CPL} ranging from 300 W to 500 W result in an efficiency between 94 % and 96 % for the whole system.

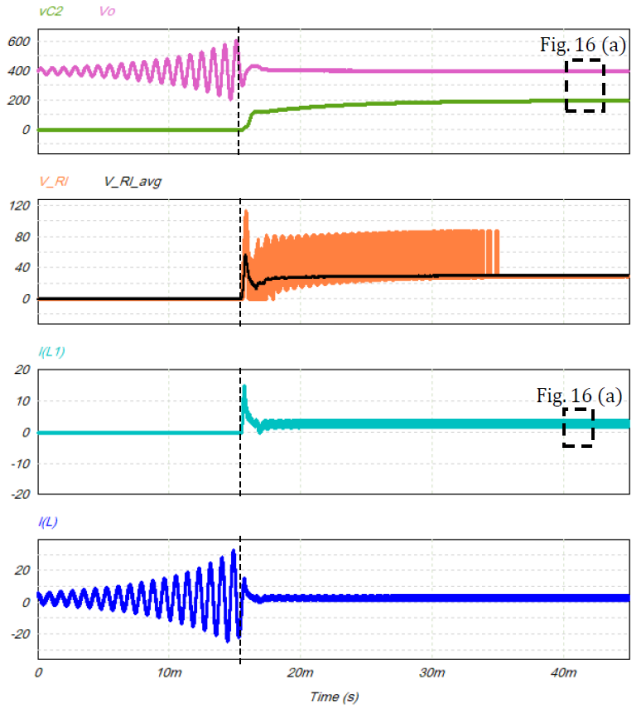

Fig. 18. Response of the boost converter showing the stabilizing effect of the SLFR which is connected at t = 15 ms for $V_g = 200$ V, $R = 460.45\ \Omega$ and $P_{\mathrm{CPL}} = 500$ W.

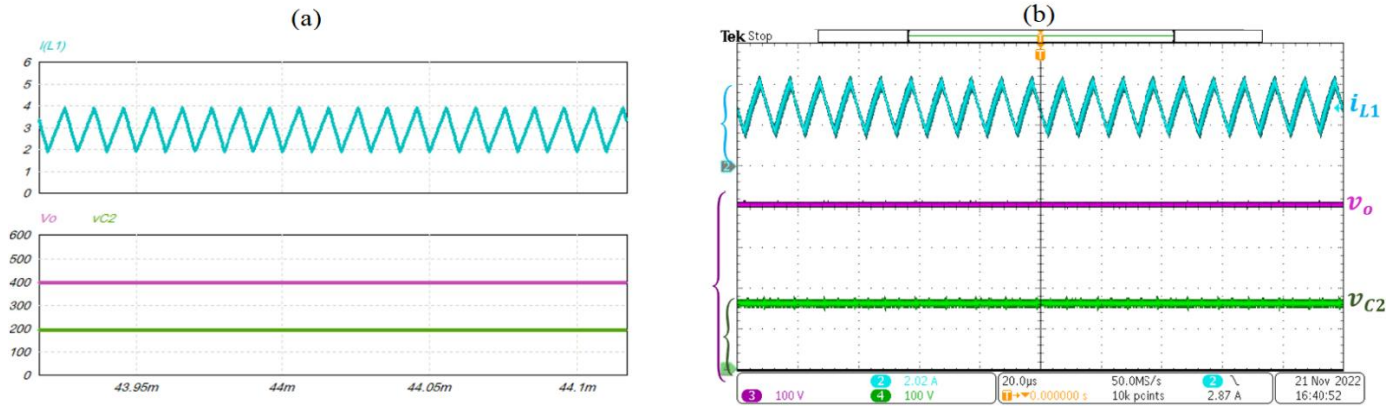

Fig. 19. Steady-state waveforms corresponding to the interconnection of the boost converter and the SEPIC-based SLFR, for $V_g = 200$ V, $R = 450\ \Omega$, and $P_{CPL} = 500$ W being (a) numerical simulations, (b) experimental measurements.

The interconnected converters operate with a switching frequency of 100 kHz. The steady-state measurements corresponding to the simulated waveforms in Fig. 19 (a) are depicted in Fig. 18 (b), in which a good agreement with the simulations can be observed taking into account the mentioned losses.

The second set of experiments focuses on the dynamic behavior of the system. Therefore, a step variation in the input voltage and in the power of the CPL are performed. In this case the operating point corresponds to Fig. 7 (b) in which the input voltage supplied by the battery is 50 V, and both, the boost converter and the SEPIC, provide 100 V. The power demanded in the boost converter is 200 W and the SEPIC is feeding a 150 Ω resistive load.

In Fig. 20 (a) are shown the simulation results in the output voltage of both converters and the input current after a step of -5 V in the input voltage. These results are depicted experimentally in Fig. 20 (b) where it can be observed a perfect agreement between the numerical simulations and the experimental measurements from the laboratory the prototype.

Equivalently, Fig. 21 (a) shows the simulated response of the interconnected system when the output power of the boost converter undergoes a variation of 20 W. The corresponding experimental response is depicted in Fig. 21 (b) in which the results are replicated for the output voltage of both converters and its input current.

VII Discussion

In this section, potential applications of the proposed SLFR are discussed together with the limitations of the implemented design.

A. Potential applications of the implemented design

The interconnected architecture proposed in this paper can be useful in the context of the EV, for example, where the boost converter could work in the vehicle powertrain and the output port of the SLFR damper could be used to charge the 12 V onboard battery that supplies the communication and multimedia bus of the vehicle [34].

In other applications, the insertion of feedback in the implementation of the virtual resistance could regulate the output voltage of the main converter. In the previous sections, the system is designed around a fixed value of the stabilizing resistance R_l. Considering the described system, if an external disturbance affects the input voltage or the output power demand, the output voltage of the boost converter changes. This is the expected behavior of the presented implementation since the boost converter is operating in open loop. An option to avoid this effect is to close the loop in the actively damped boost converter loaded with CPL in order to regulate its output voltage.

To illustrate this preliminary idea, we have modified the emulated conductance of the SLFR in order regulate the boost converter output voltage. A slower outer feedback loop has been been introduced in the implementation of the SLFR conductance in the PCMC controller.

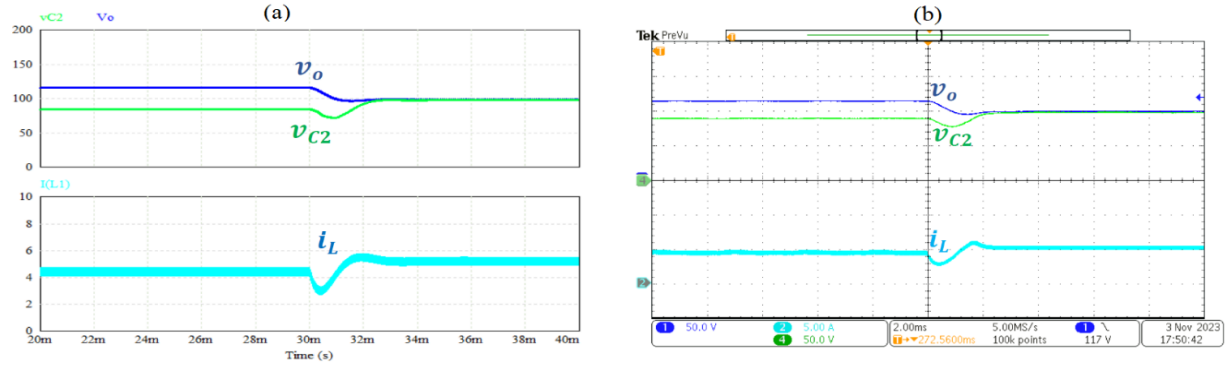

Fig. 20. Results of the interconnection, of the boost and the SLFR, for a step variation of -10% in the input voltage, $V_g = 50$ V, R = 150 Ω and $P_{CPL} = 200$ W being (a) numerical simulations, (b) experimental measurements.

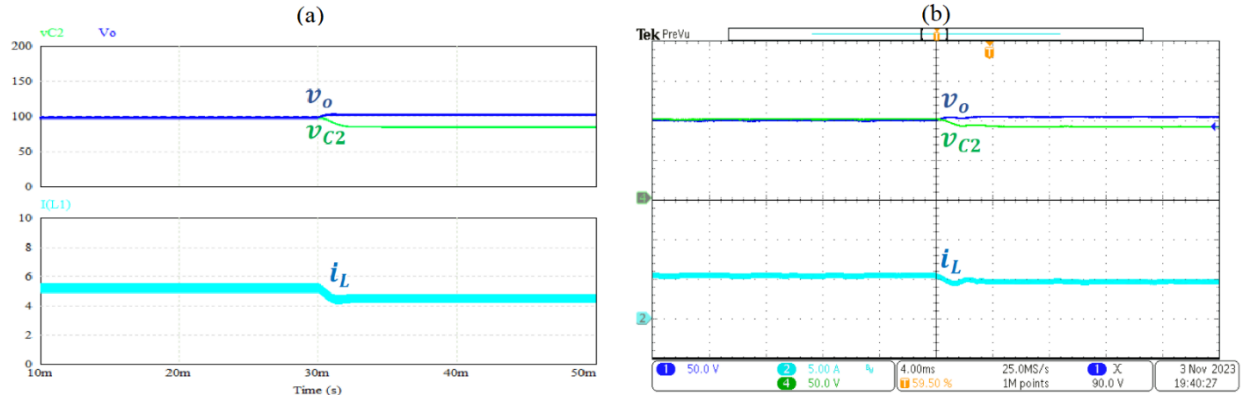

Fig. 21. Results of the interconnection, of the boost and the SLFR, for a step variation of -10% in the output power, $V_g = 50$ V, R = 150 Ω and $P_{CPL} = 200$ W being (a) numerical simulations, (b) experimental measurements.

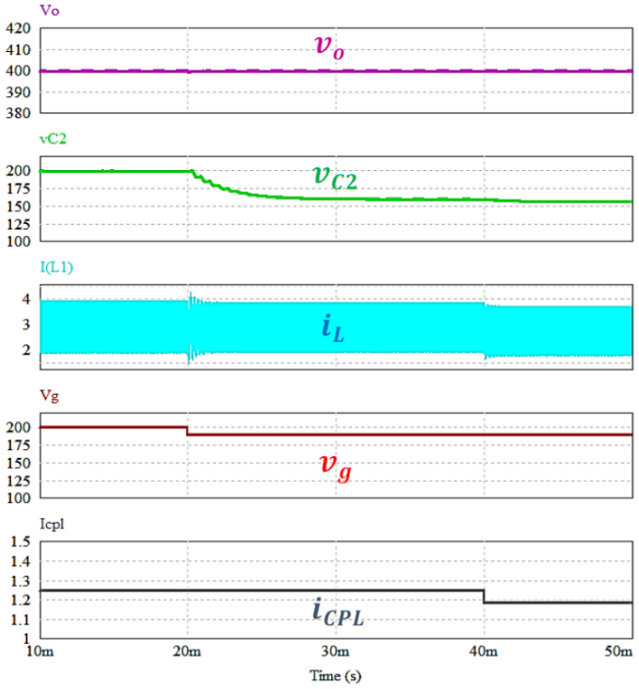

Fig. 22. Simulation results showing the regulation of the output voltage of the boost by means of a feedback to modify the emulated resistance R_l in the SLFR, for $R = 460.45\ \Omega$ and $P_{\mathrm{CPL}} = 500$ W.

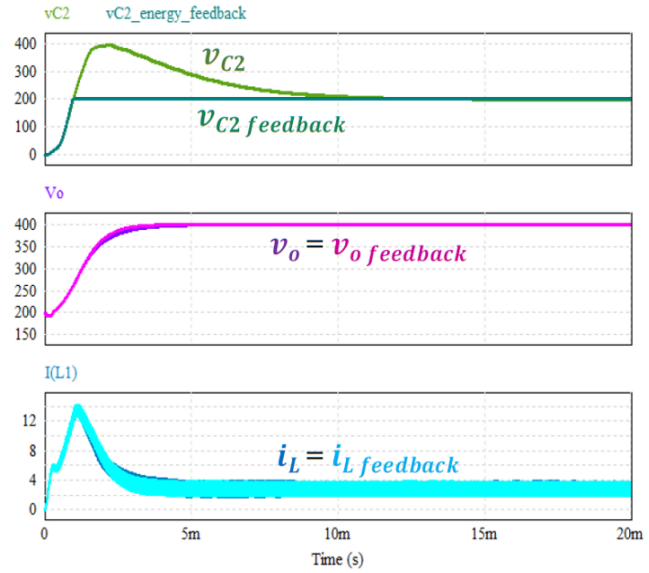

Fig. 23. Simulation results showing the reinjection of the SLFR output voltage to the input battery, for $V_g = 200$ V, $V_o = 400$ V and $P_{\mathrm{CPL}} = 500$ W.

Namely, the output voltage of the boost converter is sensed, compared to a reference that ensures the output voltage to be 400 V, and compensated with a PI controller. Finally, the output of the compensator is multiplied by the input voltage of the SLFR, hence the value of the emulated conductance of the SLFR is adapted. In this case, if the input voltage of the boost converter is increased, the value of the emulated conductance will also decrease to compensate the output voltage of the boost converter. On the other hand, the value of the emulated conductance will increase if the input voltage of the boost converter is reduced.

In Fig. 22 the simulation results corresponding to a 5% step change in the input voltage of the system at t = 20 ms, and a 5% step change in the output power of the boost converter at t = 40 ms are shown. In both cases, the output voltage of the boost converter is regulated to 400 V.

On the other hand, if feedback between the ports of the power stages of SEPIC and boost converter is considered, the output energy of the SLFR could be reinjected to the input battery in order to recover the energy wasted in the stabilization. In this case, this reinjection is performed by means of a diode connected between the output port and the battery in order to prevent the current to flow in the opposite direction. More analysis and experiments have to be carried out with this proposal, but it is expected that, in case of having a regulated voltage output in the SLFR, the stability of the system will not be affected. In this sense, it can be observed in Fig. 23 that the start-up dynamics of the system with and without energy reinjection is the same. With this approach, the design is more flexible since it allows eliminating the condition imposed by the output voltage of the SLFR. In this case, since the output voltage of the SLFR is already set by the application, a wide range of values for the stabilization resistance R_l and the duty cycle D can be obtained within the stability zone, which allows the system to provide the desired output voltage of the boost converter loaded with CPL.

B. Limitations of the implemented design

The advantages of the proposed active damping based on SLFR with respect to a passive solution are illustrated in TABLE V in terms of power losses and system efficiency for the same value of stabilizing resistance and identical operating point P of Fig. 7 (a). It can be observed in the TABLE V that the implemented solution based on SLFR has almost 10 points of higher efficiency due to much smaller stabilizing power losses.

Nonetheless, the design presents a series of limitations that has to be taken into account.

First of all, the input port of the SLFR has to be connected in series with an inductor of the main power converter.

In addition, the interconnected converters have to operate in CCM with the same frequency and duty cycle. Therefore, the parameters of the final design of the damper will depend on the topology of the main converter that has to be stabilized.

On the other hand, the selection of the operating point can affect the stability region of the system in Fig. 7. Note that the nominal values of input voltage, CPL power and stabilizing resistance are related by the following inequality , which can be directly derived from (3) and introduces a new restriction:

$$V_g \geq \sqrt{4P_{\mathrm{CPL}}R_l} \tag{22}$$

Notwithstanding, the design procedure introduced in Section IV can be perfectly adapted to stabilize other power converters. For instance, the potential extension of the

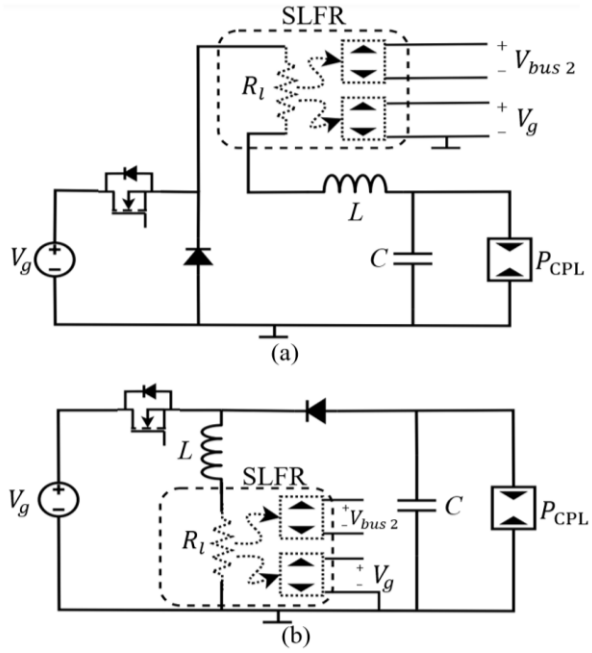

Fig. 24. Interconnection of the proposed SLFR and other elementary converters. a) buck converter b) buck-boost converter.

TABLE V
SUMMARY OF THE GLOBAL RESULTS FOR $R_l = 11\ \Omega$.

	Passive damped boost (Fig. 2)	Ideal SLFR damped boost (Fig. 19)	Implemented SLFR damped boost (Experiment 1)
Boost ouptut voltage	400 V	400 V	400 V
SLFR ouptut voltage	0 V	200 V	178 V
Power losses in the damper	87 W	0 W	15 W
System efficiency	85%	100 %	94%

method to dc-dc buck or buck-boost converters is depicted in Fig. 24, the resulting characteristic polynomial being:

$$s^2 + \left(\frac{R_l}{L} - \frac{P_{CPL}}{V_o^2 C}\right) s - \frac{1}{LC}\left(1 - \frac{P_{CPL} \cdot R_l}{V_o^2}\right) \quad \text{buck} \qquad (23)$$

$$s^2 + \left(\frac{R_l}{L} - \frac{P_{CPL}}{V_o^2 C}\right) s - \frac{1}{LC}\left((1 - D)^2 - \frac{P_{CPL} \cdot R_l}{V_o^2}\right) \quad \text{buck-boost} \qquad (24)$$

Note that expressions (24) and (1) are identical while expressions (23) and (1) are similar, which allows predicting a straightforward design of the SLFR in both cases. Notwithstanding, in the case of CPL behavior caused by the cascaded connection of two buck converters with the source converter operating in open-loop, it should be taken into account additionally the effect of the feedforward current ripple that can be introduced by the converter load as reported in [35].

VII. CONCLUSIONS

This paper has shown that active damping of open loop dc-dc converters operating in CCM and loaded by a CPL is possible using a series-connected SLFR. It has been demonstrated that a SEPIC under a PCMC with compensating ramp can be used to synthesize the SLFR, and it has resulted effective in stabilizing an open-loop boost converter supplying a CPL. With the approach used no energy is wasted in the damper contrarily to what occurs with series-connected resistors frequently used in power electronics systems for damping purposes.

A systematic design that integrates the steady-state constraints of both SEPIC and boost converter plus the stability conditions of the latter has led to the appropriate coordinates of the interconnection operating point. The coordinates are given in terms of the SLFR resistance and the duty cycle of both converters. The interconnected converters have the same duty cycle and identical switching frequency. Their respective input ports are connected in series, but their corresponding loads are split, which ensures the versatility of the proposal.

Moreover, theoretical analysis, numerical simulation and experimental measurements have been provided on the operation of the SEPIC SLFR supplying a resistive load. The possibility of reinjecting the energy from the damper output port to another point of the boost converter has been studied by simulation. In this case, the energy is reinjected to the input port which leads to a less restrictive situation than in the case of an independent resistive load since the converter does not require a specific resistor value or any kind of regulation to ensure the desired voltage at its output port.

Future work contemplates the experimental validation of the voltage regulation feature that can provide the SLFR to the boost converter. It also considers the study of the reinjection of the SLFR output power to the input battery and the extension of the design of SLFR to stabilize other types of open-loop converters with CPL.

Finally, we are also working in the substitution of the resistance of some passive damping networks used in power electronics by means of an LFR or a SLFR. In particular, we are currently investigating the effect of these stabilizers on the *LC* input and output filters in some dc-dc converters and power inverters respectively.

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M. Sebastià-Rullo received the B. S. degree in Industrial Electronics and Automation Engineering and the B.S. degree in Electrical Engineering both in 2020 from the Universitat Rovira i Virgili, in Tarragona, Spain. He received the Master Engineering degree in Electric Vehicle Technologies in 2021 also from Universitat Rovira i Virgili. He joined in 2021 the Automatic Control and Industrial Electronics Research Group (GAEI), where he worked as a research technician supporting some GAEI research projects. In 2022, he joined the GAEI research team where he is working towards his Ph.D. His main research interests include DC-DC converters, power converter stabilization strategies such as active damping, renewable energies and electric vehicle technologies.

A. Cid-Pastor graduated as Ingeniero Técnico Industrial en Electrónica Industrial in 1999 and as Ingeniero en Automática y Electrónica Industrial in 2002 at Universitat Rovira i Virgili, Tarragona, Spain. He received the M.S. degree in Design of Microelectronics and Microsystems Circuits in 2003 from Institut National des Sciences Appliquées, Toulouse, France. He received the Ph.D. degree from Universitat Politècnica de Catalunya, Barcelona, Spain, and from Institut National des Sciences Appliquées, LAAS-CNRS Toulouse, France in 2005 and 2006, respectively. He is currently an Associated Professor at the Departament d'Enginyeria Electrònica Elèctrica i Automàtica, Escola Tècnica Superior d'Enginyeria, Universitat Rovira i Virgili, Tarragona, Spain. He is a member of the Research Group in Automatic Control and Industrial Electronics (GAEI). He currently serves as a Subject Editor of Electronics Letters for Power Electronics, Energy Conversion and Sustainability. His research interests are in the field of power electronics, power conditioning for electric vehicles, and renewable energy systems.

H. Valderrama-Blavi received the Ingeniero de Telecomunicación (Ms degree) and the PhD. degree from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1994 and 2001, respectively. In 2001 he got a post-doctoral position at the LAAS-CNRS (Laboratoire d'Analyse et Architecture des Systèmes of the Centre National de la Recherche Scientifique) of Toulouse, France where he remained for one year. Since 2003 he is a Associate Professor with the Department of Electrical, Electronics, and Automatic Control Engineering (DEEEA) of the Universitat Rovira i Virgili, Tarragona, Spain. From 2018 until February 2022 he has been the academic responsible of the master of electric vehicle technologies. From then, he is the director of the electronic engineering and automatic control department (DEEEA). From 2003 until now, he has been the main researcher (IP) of 5 research projects financed by the Spanish ministry of science and technologies, he has co-authored more than 40 journal-papers, and has got the full professor accreditation from ANECA since June 2022. He is working interests are: power electronics for renewable energy and distributed generation systems, efficient lighting, high voltage gain conversion, applications for silicon carbide devices, nonlinear control for power converters, active stabilization networks based on Loss Free Resistor (LFR), multifrequency AC-buses, and fast chargers and battery modeling for electrical vehicles.

A. El Aroudi received the bachelor's degree in physical science from the Faculté des Sciences, Université Abdelmalek Essaadi, Tetouan, Morocco, in 1995, and the Ph.D. degree (Hons.) in applied physical science from Universitat Politècnica de Catalunya, Barcelona, Spain, in 2000. He is currently a Full Professor with the Department of Electronics, Electrical Engineering and Automatic Control, University of Rovira o Virgili, Tarragona, Spain. His research interests include the field of dynamics, design and control of power conditioning for electric vehicles and renewable energy applications, power factor correction and battery modeling. He was an Associate Editor of the IET Circuits, Systems and Devices, the IET Power Electronics, and the IET Electronics Letters. He was also a Guest Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS ON CIRCUITS AND SYSTEMS in 2015, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS in 2018, and Energies from 2018 to 2019. From 2019 to 2023 he was a Topic Editor for Energies. He currently serves as an Associate Editor for International Journal of Circuit Theory and Applications.

L. Martínez-Salamero received the Ingeniero de Telecomunicación degree in 1978 and the Ph.D. degree in 1984, both at the Universidad Politécnica de Cataluña, Barcelona, Spain. From 1978 to 1992, he taught circuit theory, analog electronics and power processing at the Escuela Técnica Superior de Ingenieros de Telecomunicación de Barcelona, Barcelona, Spain. From 1992 to 1993, he was a visiting professor at the Center for Solid State Power Conditioning and Control, Department of Electrical Engineering, Duke University, Durham, NC. From 2003 to 2004, 2010 to 2011, and March-September 2018 he was a visiting scholar at the Laboratory of Architecture and Systems Analysis (LAAS), National Agency for Scientific Research (CNRS), Toulouse, France. Since 1995 he has been a full professor with the Department of Electrical Electronic and Automatic Control Engineering, School of Electrical and Computer Engineering, Rovira i Virgili University, Tarragona, Spain, where he managed the Research Group in Automatic Control and Industrial Electronics (GAEI) in the period 1998-2018. His research interests include structure and control of power conditioning systems, namely, electrical architecture of satellites and electric vehicles, as well as nonlinear control of converters and drives, and power conditioning for renewable energy. Dr. Martínez-Salamero has published a large number of papers in scientific journals and conference proceedings in the fields of modelling, simulation, and control of power converters, and holds a U.S. patent on dual voltage electrical distribution in vehicles. He was guest editor of the IEEE Transactions on Circuits and Systems Special Issue on Simulation, Theory and Design of Switched-Analog Networks (Aug. 1997). He organized in cooperation with the European Space Agency (ESA) the 5th European Space Power Conference (ESPC-98) in Tarragona and served during two terms (1996-2002) as a dean of the School of Electrical and Computer Engineering. He was president of Spanish Joint Chapter of the IEEE Power Electronics and Industrial Electronics Societies from 2005 to 2008, and distinguished lecturer of the IEEE Circuits and Systems Society in the period 2001-2002. He is currently distinguished professor of Rovira i Virgili University.