Fixed Switching Frequency Digital Sliding-Mode-Based Control of a Three-Phase Four-Wire AC–DC Rectifier With Power Factor Correction

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***Abstract*—This article presents a fixed-frequency digital sliding mode control (SMC) technique to perform power factor correction (PFC) for electric vehicle (EV) charging applications. A three-phase four-wire boost rectifier with split-capacitor topology is selected. Using system model, three decoupled sliding mode controllers are designed to achieve loss-free resistor (LFR) behavior in each phase for PFC. The control law and the dynamic model of the rectifier are obtained by imposing sliding-mode regime in discrete time. To obtain simple expression of the duty cycle for ease of digital implementation in natural frame, the discrete-time model of the system has been used with reasonable approximations. Despite the theoretical stability of the closed-loop system, practical implementation of the control law is limited by digital control delays. To mitigate this problem in practice, a modified control law is proposed to ensure stability by scaling the weighted error in the expression of the control law resulting from the ideal SMC. The combination of the topology and the control method in the natural frame shows improved performance compared to the existing literature. Theoretical predictions are validated by several numerical simulations of the switched model and experimental measurements under different practical scenarios.**

***Index Terms*—Digital signal processor (DSP), loss-free resistor (LFR), power factor correction (PFC), sliding mode control (SMC), three-phase four-wire ac–dc rectifier.**

I. Introduction

THE development of electric vehicle (EV) battery chargers has recently gained significant importance [1]. Typical EV battery chargers are two-stage systems consisting of a three-phase or an interleaved single-phase ac–dc rectifier in the first stage performing power factor correction (PFC) followed by a dc–dc converter which is responsible for the desired charging of the battery according to the required charging protocol (see Fig. 1). First, PFC is essential to minimize the reactive power drawn from the grid and to improve the overall efficiency of the system [2]. Second, achieving low total harmonic distortion (THD) for ac phase currents is crucial to meet international standards such as IEEE and IEC [3].

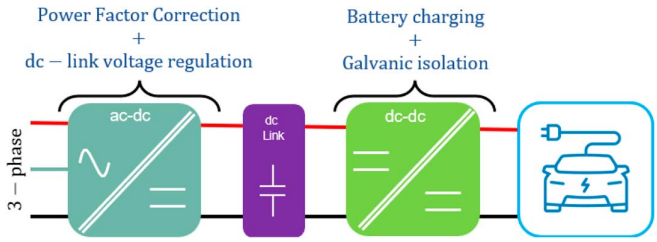

Fig. 1. Block diagram of a two-stage battery EV charger. The first stage is a three-phase ac–dc front-end rectifier for PFC and the second stage is a dc–dc converter for charging the EV battery.

The control of three-phase ac–dc rectifiers efficiently, properly, and reliably in PFC application presents several challenges that need to be addressed in the control design [4]. A large variety of control methods and circuit topologies have been developed and implemented to perform PFC in three-phase ac–dc rectifiers. The control system must be able to respond quickly to load changes and maintain the power factor (PF) and the THD within acceptable limits [5]. The traditional cascaded control strategy with either proportional integral (PI) controller in dq-frame [6], [7] or proportional resonant (PR) controller in abc-frame or $\alpha\beta$-frame [8] faces several issues, including high computational burden, modeling uncertainties, dependency on the operating point, the necessity for synchronization strategies [9], and complex optimal controller parameter tuning. These challenges make the control strategy unreliable, expensive, nonoptimal, and slow [10], particularly in EV charging applications that demand fast dynamic responses to fluctuating charging loads [11].

Other more advanced control techniques exist in the literature to address the PFC problem in three-phase ac–dc rectifiers. Among others, we can quote hysteresis control [12], sliding mode control (SMC) [13], and model predictive control (MPC)

Received 11 December 2024; revised 29 March 2025; accepted 30 April 2025. Date of publication 18 June 2025; date of current version 21 November 2025. This work was supported in part by the Spanish Ministerio de Ciencia e Innovación under Grant PID2023-150839OB-I00 funded by MICIU/AEI/10.13039/501100011033 and by "ERDF/EU." The work of Kuntal Mandal was supported by the Agency for Management of University and Research Grants (AGAUR) through the Ministry of Research and Universities of the Government of Catalonia under Grant 2020 BP 00260. *(Corresponding author: Seyedamin Valedsaravi.)*

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Digital Object Identifier 10.1109/TIE.2025.3569951

TABLE I
COMPARATIVE ANALYSIS OF DIFFERENT PFC CONTROL METHODS

Characteristics	PI Control	PR Control	Hysteresis Control	MPC	Adaptive SMC	Proposed Method
Steady-state switching frequency	Fixed	Fixed	Variable	Fixed/variable	Fixed	Fixed
Transient switching frequency	Fixed	Fixed	Variable	Variable	Variable	Fixed
Computation burden of the control	Moderate	High	Low	High	Moderate	Low
Difficulties in digital implementation	Moderate	High	Low	Moderate	Moderate	Low
Difficulties in bidirectional implementation	Moderate	High	Low	Low	Low	Low
Modeling uncertainties	High	High	Low	Low	Low	Low
Synchronization method	phase-locked loop (PLL)	PLL	Not required	Not required	Not required	Not required

[14]. These methods fall under the category of nonlinear control strategies and offer advantages such as reduced steady-state error, robustness to disturbances and modeling uncertainties, faster and more desirable transient response, and no requirement of modulator to produce the control signal for switches. However, they inherently suffer from variable switching frequency issues, which can increase switching and driver power losses, elevate electromagnetic interference (EMI), complicate filter design, degrade converter regulation performance, and reduce converter efficiency [15].

In MPC, the accuracy of the predictive model is crucial for achieving desirable control performance [16]. Although the switching frequency in MPC can be fixed through manipulation of the MPC objective function, this control method suffers from a high computational burden and the need for expensive processors. Additionally, the switching frequency can be fixed with adaptive hysteresis modulation (HM) techniques [13] applied to both hysteresis control and SMC. The steady-state frequency regulation in SMC method can be done using global fast terminal [17] and artificial intelligence-based techniques [18]. However, adaptive SMC methods also face issues with variable switching frequency when the operating point of the converter changes. During transients, the switching frequency can exceed twice the nominal frequency [19], which may jeopardize the EMI certification. Although the average steady-state frequency remains constant, there is a chattering effect, causing small frequency variations around the average value.

The SMC operates by driving the state of the system onto a suitable predefined sliding surface, ensuring that its trajectories remain on this surface during operation [20]. When combined with the loss-free resistor (LFR) approach, the SMC can provide additional benefits, particularly in simplifying PFC and enhancing overall control performance [21], [22]. Most of the sliding mode controllers are designed and implemented in the analog domain, which results in less flexibility. With advancements in digital control techniques and the development of digital signal processors (DSPs), more sophisticated and robust control strategies can be implemented in power converters, providing real-time monitoring and diagnostics.

On the one hand, the digital implementation of SMC in three-phase ac–dc rectifiers offers several advantages over analog implementations [23]. Some of these advantages include fixed switching frequency, precise and flexible control algorithms, easy parameter tuning, and integration of advanced control techniques [15], [16]. On the other hand, the digital implementation presents some challenges. The sampling rate and delay effects of the digital control system can impact not only the performance of the rectifier [24], [25] but also its stability. Careful consideration must be given to the design of the control algorithm to ensure accurate and timely control actions [26]. Additionally, the digital control system must be robust against noise and disturbances [27]. To implement a digital SMC technique with a fixed frequency, the equivalent duty cycle in each switching cycle must be determined. The controller can effectively drive the power switches using digital PWM to achieve the desired control objectives [28]. To do so, the model of the rectifier must be discretized. Therefore, the duty cycle is determined based on a discrete-time recurrent equation [29]. To address all these issues, the discrete-time SMC with digital pulse-width modulation (DPWM) switching technique is proposed to combine the advantageous features of nonlinear SMC with the predictability and ease of implementation associated with fixed-frequency operation. This can ease the adoption of the interleaving of single-phase and three-phase rectifiers in high-power EV ultra-fast charging applications. The comparative analysis of different PFC control methods is presented in Table I.

The contributions of this article are listed as follows: 1) a discrete-time SMC with fixed-frequency digital PWM is designed in natural frame to perform the PFC of a three-phase four-wire ac–dc rectifier for EV charging applications. The sliding surface is defined based on the emulation of a virtual LFR in parallel with the input voltage of three-phase ac–dc rectifier; 2) to avoid complex expressions of the duty cycles, the discrete-time model of the system has been obtained by using reasonable approximations. As a result, the obtained fixed-frequency control algorithm that adjusts the duty cycles is simple and can be easily implemented for each phase. In addition, it can be easily adopted to existing three-phase ac–dc rectifiers with a software upgrade and minor reconfiguration; and 3) due to computation delay effects by the DSP, the control law cannot be applied during the same switching cycle within which it is calculated. Therefore, a modified control law to ensure the stability is proposed by scaling the weighted error in the expression of the control law resulting from the ideal SMC. This approach is validated by several numerical simulations from the switched model of the system and experimental measurements on a 1 kW hardware prototype.

The remainder of this article is organized as follows. In Section II, the system description and mathematical modeling are addressed, and simple design-oriented reduced-order

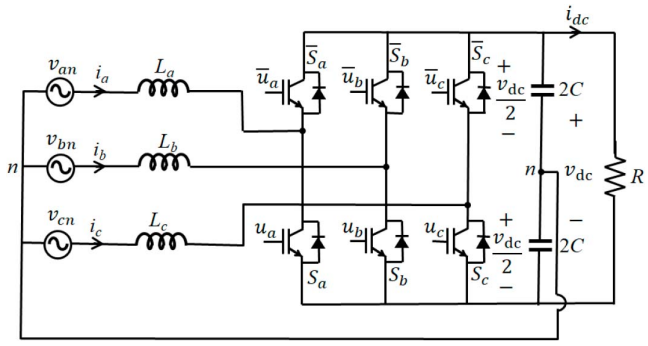


Fig. 2. Schematic circuit diagram of the studied three-phase four-wire boost type split-capacitor ac–dc rectifier with resistive load.

discrete time is obtained. Section III presents ideal digital SMC law. The effect of computation delay on the system's stability is revealed. It is demonstrated that the closed-loop system is marginally stable in the presence of such computation delay, and a modified control law to stabilize the system is proposed. In Section IV, the ideal SMC method based on the LFR approach is thoroughly elaborated. The numerical simulations and the experimental results are presented in Section V. Finally, the concluding remarks are provided in Section VI.

II. System Description and Discrete-Time Modeling

A. System Description

Fig. 2 illustrates the schematic circuit diagram of the three-phase four-wire ac–dc rectifier under study. The ac side is connected to a three-phase source which represents the grid. A resistive load is connected to the dc side. Although an inductor-capacitor (LC) or an inductor-capacitor-inductor (LCL) filter is usually used to enhance power quality and mitigate harmonics, in compliance with the IEEE standard [30], a simple inductor is integrated as a filter on the power grid side. For simplicity, the internal parasitic resistances in the inductors are neglected in the modeling. The midpoint of the dc link is connected to the neutral of the grid. The inclusion of a neutral conductor in a three-phase four-wire ac–dc rectifier makes the multiinput control system decoupled.

It should be noted that the model of a three-phase three-wire ac–dc rectifier in the *abc*-frame exhibits cross-coupling terms introduced by the neutral point voltage [13]. To calculate the three duty cycles, the coupled nonlinear equations must be solved, which is a time-consuming control task. To address these issues, a three-phase four-wire ac–dc rectifier is selected in this article. This approach decouples the control of each phase, simplifies digital implementation, and reduces costs. Additional advantages of the three-phase four-wire rectifier over three-phase three-wire rectifier include design modularity for interleaving methods, power quality improvement, harmonics reduction, ground fault protection or increased safety, improved EMI characteristics, reduced applied voltage to the power switches, and compatibility with single-phase as well as two-phase systems [31].

The three-phase grid voltages $v_{an}(t)$, $v_{bn}(t)$, and $v_{cn}(t)$ are considered sinusoidal and can be represented as follows:

$$v_{pn}(t) = V_{\text{rms}}\sqrt{2}\sin(\omega_g t + \varphi_p) \tag{1}$$

where $p = a, b, c$, $\varphi_p = 0$ for $p = a$, $\varphi_p = +2\pi/3$ for $p = b$, $\varphi_p = -2\pi/3$ for $p = c$, V_{rms} represents the rms value of the line-to-neutral balanced grid voltages and ω_g denotes the grid angular frequency. The dc-link output comprises two identical capacitors with capacitance of $2C$, each with a voltage of $v_{\text{dc}}/2$, where v_{dc} is the dc-link voltage.

B. Switched Model

By neglecting parasitic elements in the components and considering equal inductance values in each phase ($L_a = L_b = L_c = L$), the mathematical model of the three-phase four-wire ac–dc rectifier can be expressed as follows:

$$\frac{di_p(t)}{dt} = \frac{v_{pn}(t)}{L} + s_p\frac{v_{\text{dc}}(t)}{2L} \tag{2a}$$

$$\frac{dv_{\text{dc}}(t)}{dt} = -\frac{1}{2C}\sum_{p=a}^{c} s_p i_p(t) - \frac{v_{\text{dc}}(t)}{RC} \tag{2b}$$

where $i_p(t)$ represents the three-phase grid current in phase p and s_p is a square-wave signal taking values in the finite set $\{-1,1\}$. Note that $s_p = 1$ when the bottom switch S_p of leg p is closed and $s_p = -1$ when this switch is open [32]. It is related to the binary control signal $u_p \in \{0,1\}$ for the switch S_p by $s_p = 2u_p - 1$. In this article, a simple resistive load R is considered. This will represent the input port of the dc–dc stage in the complete EV charger (Fig. 1).

C. Simplified Discrete-Time Model

Although the exact and full-order discrete-time model of the three-phase four-wire ac–dc rectifier can be obtained by integrating the switched model within the switching period T_s, this would result in a complex expression for the model and for the control law. To avoid a complex model and consequently complex expressions of the duty cycles, the following assumptions are considered to obtain a simple design-oriented discrete-time model for the rectifier.

1) The parasitic parameters are ignored.
2) The switching ripple in the dc-link voltage v_{dc} is neglected and considered constant during a switching cycle. Therefore, its dynamics is not considered in the modeling, and consequently, the inductor current equations for each phase can be easily integrated resulting in simple model and control law.
3) Under balanced conditions, the $2\omega_g$ ac ripple will not be present in the dc-link voltage v_{dc}. However, with one or two faulty phases, a $2\omega_g$ ac ripple will appear in v_{dc}. For maintaining simplicity, this ripple will also be neglected for synthesizing the controller.

Based on the previous assumptions and from (2a), the discrete-time state equation for the inductor current in phase p can be

expressed as follows:

$$i_p[k+1] = i_p[k] + \frac{T_s}{L}\left(v_{pn}[k] + (2d_p[k]-1)\frac{v_{\rm dc}[k]}{2}\right) \tag{3}$$

where for $p = a, b, c$, $d_p[k]$ represents the duty cycle of the signal u_p of leg-down switch in phase p within the kth switching cycle. Also, $i_p[k] = i_p(kT_s)$, $v_{pn}[k] = v_{pn}(kT_s)$, and $v_{\rm dc}[k] = v_{\rm dc}(kT_s)$ represent the sampled inductor current in each phase, ac input voltage, and dc output voltage at the sampling instant kT_s, respectively, for the discrete time $k = 0, 1, 2, \ldots$. Depending on the modulation method, the samples in (3) taken at the start of the switching cycle can represent the peak values, the valley values, or the average values of the inductor current i_p. In this article, a double-edge modulation is employed, so the samples and averages at the start of each switching cycle are the same.

D. Quasi Steady-State Analysis at the Switching Scale

Under quasi steady-state operation at the switching scale, one has $i_p[k+1] \approx i_p[k]$ and therefore from (3), the following expression for $d_p[k]$ is obtained:

$$d_p[k] \approx -\frac{v_{pn}[k]}{v_{\rm dc}[k]} + \frac{1}{2}. \tag{4}$$

Using the fact that $0 < d_p[k] < 1$ in the previous equation, a necessary condition for the system to operate correctly is given as follows:

$$-\frac{v_{\rm dc}[k]}{2} < v_{pn}[k] < \frac{v_{\rm dc}[k]}{2}. \tag{5}$$

By performing a quasi steady-state analysis, it can be found that the inductor current ripple (peak-to-peak) varies according to the following equation:

$$\Delta i_p[k] = \frac{T_s}{L} v_{\rm dc}[k](d_p[k](1-d_p[k])) \tag{6}$$

where d_p is the duty cycle of the switch S_p. The phase current ripple Δi_p varies within the ac line cycle according to a quadratic function of the duty cycle d_p. The maximum value of the ripple (worst case) occurs when $d_p = 1/2$. For this worst case value of duty cycle, one has maximum inductor current ripple

$$\Delta i_{p,\max}[k] = \frac{T_s}{4L} v_{\rm dc}[k] \Rightarrow L = \frac{T_s}{4}\frac{v_{\rm dc}[k]}{\Delta i_{p,\max}[k]}. \tag{7}$$

Therefore, the value of the inductance L can be selected according to the maximum allowed value of the current in each phase.

E. Steady-State Analysis at the AC Time-Scale

To impose an LFR behavior on the three-phase four-wire rectifier, the ac voltage and current in each phase must have a resistive correlation [33] emulating in each phase a resistive behavior with resistance r_p, $p = a, b, c$. The power at each phase is completely delivered to the output port. The proposed PWM-based digital SMC is designed by imposing LFR behavior at the input side of the rectifier. To do so, the ac current in each phase is controlled in such a way to be proportional to the ac voltage in the same phase [34]. This implies that the input three-phase

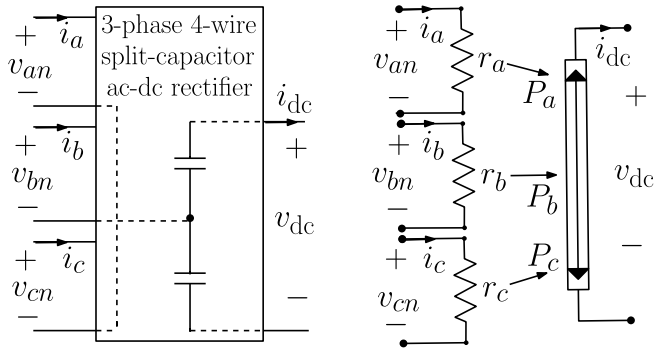


Fig. 3. Power flow model of the rectifier based on the LFR approach.

power can be modeled as three independent power flows in three resistors with conductance g_p, as shown in Fig. 3. Consequently, the three-phase four-wire rectifier can be regarded as three single-phase modules. Let P_a, P_b, and P_c be the input power of the modules connected to phases a, b, and c, respectively. The resistances $r_a = 1/g_a, r_b = 1/g_b$, and $r_c = 1/g_c$ are considered all equal: $r_a = r_b = r_c = r$ and $g_a = g_b = g_c = g$. Let G is the nominal value of g. Therefore, the equations for the input power $P_{\rm in}$ and the output power $P_{\rm out}$ under steady-state operation are as follows:

$$P_{\rm in} = P_a + P_b + P_c = 3GV_{\rm rms}^2 \tag{8a}$$

$$P_{\rm out} = \frac{V_{\rm dc}^2}{R} \tag{8b}$$

where $V_{\rm dc}$ is the steady-state value of $v_{\rm dc}[k]$. Under balanced operation, each half-bridge module delivers the same amount of power, i.e., $P_a = P_b = P_c = P_{\rm in}/3 = P_{\rm out}/3$ [34]. Therefore, the input power under steady-state operation can be expressed as follows:

$$P_{\rm in} = 3GV_{\rm rms}^2. \tag{9}$$

Therefore, the nominal value of the conductance can be determined in terms of system parameters as follows:

$$G = \frac{1}{3R}\left(\frac{V_{\rm dc}}{V_{\rm rms}}\right)^2 = \frac{P_{\rm out}}{3V_{\rm rms}^2}. \tag{10}$$

Therefore, for a given value of rms grid voltage and demanded output power (dc-link voltage and load resistance), a suitable value of G can be selected.

III. Digital SMC

A. Ideal Digital SMC Law

To perform PFC, the input port of each phase must exhibit a purely resistive impedance. It is worth to note from the model given in (3) that the system is decoupled in the sense that the current i_p in phase p is only affected by the control variable d_p corresponding to the same phase. This would not be the case if the four-wire structure was not used as in [13] where the system exhibits cross-coupling introduced by the voltage at the neutral point. Therefore, the desired reference $i_{p,\rm ref}[k]$ based on the LFR

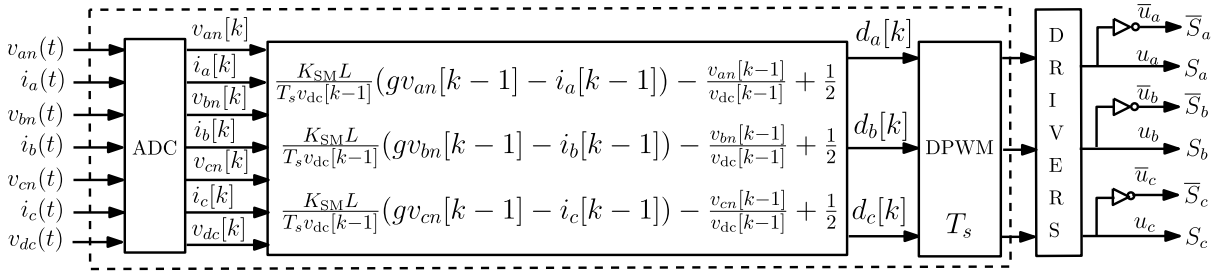


Fig. 4. Practical digital PWM-based SMC emulating an LFR in the rectifier input taking into account delay in the feedback loop.

approach is obtained as follows:

$$i_{p,\mathrm{ref}}[k] = g v_{pn}[k]. \tag{11}$$

Thus, to control the samples of the inductor current $i_p[k]$ to their desired reference $i_{p,\mathrm{ref}}[k]$, the following discrete-time sliding surface $S(x[k])$ in natural frame is used:

$$S(x[k]) = g v_{pn}[k] - i_p[k]. \tag{12}$$

In a fixed-frequency digital SMC of switching converters, the control variable $d_p[k]$ during a certain switching period is selected in such a way that the controlled variable is imposed to catch its reference one period later, i.e., $i_p[k+1] = i_{p,\mathrm{ref}}[k]$. Therefore, the duty cycle $d_p[k]$ is obtained by imposing the previous condition and solving for $d_p[k]$ in (3). In doing so, the following expression for the duty cycle is obtained for phase p:

$$d_p[k] = \frac{L}{T_s v_{\mathrm{dc}}[k]}(g v_{pn}[k] - i_p[k]) - \frac{v_{pn}[k]}{v_{\mathrm{dc}}[k]} + \frac{1}{2}. \tag{13}$$

From (13) and (3), we obtain the following:

$$i_p[k+1] = g v_{pn}[k] = i_{p,\mathrm{ref}}[k]. \tag{14}$$

In the discrete z-domain

$$K(z) = \frac{I_p(z)}{I_{p,\mathrm{ref}}(z)} = \frac{1}{z}. \tag{15}$$

It can be observed that (14) and (15) are equivalent descriptions of a first-order *deadbeat* response, i.e., the controlled signal reaches the reference in one sampling period.

B. Practical Control Law Due to Delay Effect

Due to the computation delay in the experimental system, the value of duty cycle cannot be applied in the same switching period within which it is calculated. The delay effect in the feedback system cannot be neglected, as this will strongly affect its dynamics and its stability. Taking into account one switching cycle delay, the control law (13) is modified as follows:

$$d_p[k+1] = \frac{L}{T_s v_{\mathrm{dc}}[k]}(g v_{pn}[k] - i_p[k]) - \frac{v_{pn}[k]}{v_{\mathrm{dc}}[k]} + \frac{1}{2}. \tag{16}$$

Particularizing (16) in (3) yields

$$i_p[k+1] = i_p[k] + \frac{T_s}{L} v_{pn}[k] + \frac{v_{\mathrm{dc}}[k]}{v_{\mathrm{dc}}[k-1]}(g v_{pn}[k-1] - i_p[k-1]) - \frac{T_s v_{\mathrm{dc}}[k]}{L v_{\mathrm{dc}}[k-1]} v_{pn}[k-1]. \tag{17}$$

Let $i_{p,\mathrm{ref}}[k-1] = g v_{pn}[k-1]$. Assuming $v_{\mathrm{dc}}[k-1] \approx v_{\mathrm{dc}}[k] = V_{\mathrm{dc}}$, expression (17) simplifies to

$$i_p[k+1] = i_p[k] - i_p[k-1] + i_{p,\mathrm{ref}}[k-1] + \frac{T_s}{L}(v_{pn}[k] - v_{pn}[k-1]). \tag{18}$$

After performing a small-signal analysis of (18), the following z-domain $i_{p,\mathrm{ref}}$-to-i_p transfer function is obtained:

$$K_i(z) = \frac{I_p(z)}{I_{p,\mathrm{ref}}(z)} = \frac{1}{z^2 - z + 1}. \tag{19}$$

Likewise, the v_{pn}-to-i_p transfer function is obtained as follows:

$$K_v(z) = \frac{I_p(z)}{V_{pn}(z)} = \frac{T_s}{GL}\frac{z - 1 + \frac{GL}{T_s}}{z^2 - z + 1}. \tag{20}$$

Note that with one switching cycle time delay, the system order has been increased by one compared to (15). It can be deduced from (19) that the current $i_p[k]$ will present a forced sinusoidal component proportional to reference $v_{pn}[k]$ plus another sinusoidal component introduced by the system due to the poles of unitary modulus $z_{1,2} = 1/2 \pm j\sqrt{3}/2$. This leads to a marginally stable system. Therefore, another modification in the control law is needed.

C. Modified Control Law for System Stabilization

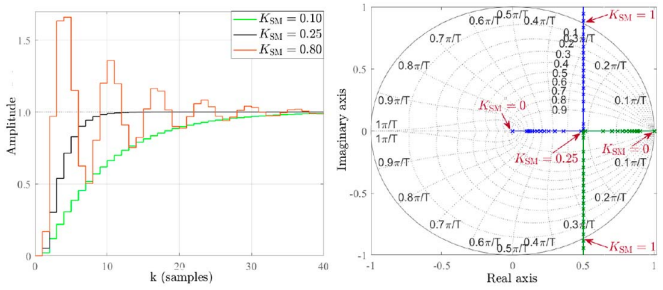
To eliminate the sinusoidal oscillation added by the system, a compensating factor K_{SM} is introduced by multiplying the tracking error as illustrated in the block diagram of Fig. 4. Therefore, the new $i_{p,\mathrm{ref}}$-to-i_p transfer function will be given by

$$K_i(z) = \frac{I_p(z)}{I_{p,\mathrm{ref}}(z)} = \frac{K_{\mathrm{SM}}}{z^2 - z + K_{\mathrm{SM}}}. \tag{21}$$

The new poles becomes

$$z_{1,2} = \frac{1}{2}\left(1 \pm \sqrt{(1 - 4K_{\mathrm{SM}})}\right). \tag{22}$$

For these poles to be located within the unit circle and consequently the system to be stable, the condition $|z_{1,2}| = \sqrt{K_{\mathrm{SM}}} < 1$ must hold implying that $0 < K_{\mathrm{SM}} < 1$. For $1/4 < K_{\mathrm{SM}} < 1$, the settling time t_s of the system due to a step change in the conductance g or equivalently in the current reference $g v_{pn}[k]$ is given by $t_s = -4T_s/\ln|z_{1,2\max}|$, where $z_{1,2\max}$ is the eigenvalue with maximum modulus. By particularizing the expression of $\ln|z_{1,2\max}|$, the settling time can be expressed in terms of the



(a) (b)

Fig. 5. (a) Normalized step response (assuming hold between samples) of the closed-loop current transfer function (21) with different values of K_{SM}. The sample time period is $T_s = T = 50\ \mu$s. (b) Change of poles position (21) with the variation of K_{SM}.

control parameter K_{SM} as follows:

$$t_s = \begin{cases} -\dfrac{4T_s}{\ln\left(\dfrac{1}{2}\left(1+\sqrt{1-4K_{SM}}\right)\right)} & \text{for } 0 < K_{SM} < \dfrac{1}{4} \\ -\dfrac{8T_s}{\ln(K_{SM})} & \text{for } \dfrac{1}{4} < K_{SM} < 1. \end{cases} \tag{23}$$

For $K_{SM} = 0.25$, the transient response will exhibit critical damping and the sinusoidal reference $gv_{pn}[k]$ will be practically attained after a settling time given by $t_s = -4T_s/\ln(0.5)$, i.e., approximately after six sampling periods, in a clear-cut contrast with the ideal *deadbeat* behavior given by (14). According to the transfer function (21), the stability of the system depends on the control parameter K_{SM}. In Fig. 5, the step response and the evolution of the poles of the system are shown.

IV. Ideal Sliding Dynamics

Under digital SMC, the inductor current reaches its steady state in few switching cycles, and its dynamics is much faster than the dc-link voltage dynamics. In this case, the average currents i_p are in phase with their corresponding phase voltages v_{pn} and therefore are identical to their desired references, i.e., $i_p = gv_{pn}$. Also, v_{pn} is a slowly varying signal, and g is practically constant, and their derivative can both be considered zero. Under these conditions, the switched signal s_p in (2a) and (2b) can be replaced by the equivalent control which in turns can be derived solving (2a) for s_p, hence getting the following:

$$s_{p,\text{eq}} = -\frac{2v_{pn}}{v_{\text{dc}}}. \tag{24}$$

By substituting s_p by $s_{p,\text{eq}}$ and i_p by gv_{pn} in (2b), one gets the following:

$$\frac{dv_{\text{dc}}}{dt} = \frac{g}{C}\sum_{p=a}^{c}\frac{v_{pn}^2}{v_{\text{dc}}} - \frac{v_{\text{dc}}}{RC}. \tag{25}$$

Accordingly, and because

$$\sin^2(\omega_g t) + \sin^2\left(\omega_g t - \frac{2}{3}\pi\right) + \sin^2\left(\omega_g t + \frac{2}{3}\pi\right) = \frac{3}{2}$$

TABLE II
Parameters for Numerical Simulation and Experiment

Parameters	Symbol	Value
Grid voltages (rms)	$V_{an} = V_{bn} = V_{cn}$	50 V, 50 Hz
Inductance	$L_a = L_b = L_c = L$	1.768 mH
DC-link capacitance	C	1024 μF
Nominal load resistance	R	40 Ω
Switching frequency	f_s	20 kHz
Nominal control gain	K_{SM}	0.25

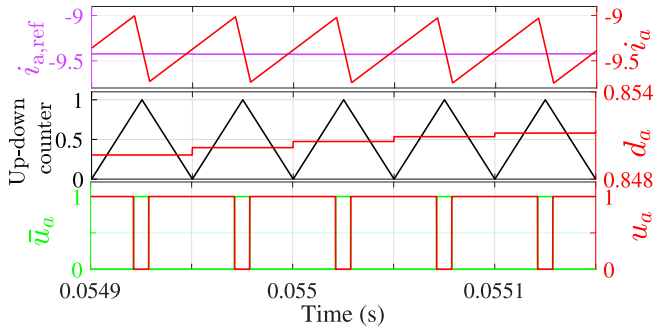


Fig. 6. Waveforms of typical control signals of double-edge modulation realized by DPWM and current for phase a.

the ideal sliding mode dynamics (25) corresponding to the dc-link voltage v_{dc} can be expressed as follows:

$$v_{\text{dc}}\frac{dv_{\text{dc}}}{dt} + \frac{v_{\text{dc}}^2}{RC} = \frac{3GV_{\text{rms}}^2}{C}. \tag{26}$$

This is a nonlinear equation in v_{dc}, but it is linear in v_{dc}^2. Indeed, by defining $Z = v_{\text{dc}}^2/2$, (26) can be written as follows:

$$\frac{dZ}{dt} + \frac{2Z}{RC} = \frac{3GV_{\text{rms}}^2}{C}. \tag{27}$$

The steady-state value of Z is the forced solution of (27) and is given by

$$Z_{\text{ss}} = \frac{3GRV_{\text{rms}}^2}{2}. \tag{28}$$

Therefore, the steady-state value V_{dc} of the output voltage v_{dc} is given by

$$V_{\text{dc}} = \sqrt{2Z_{ss}} = \sqrt{3GRV_{\text{rms}}^2} = V_{\text{rms}}\sqrt{3GR}. \tag{29}$$

This is exactly the prediction given by (10) on the basis of power conservation equations.

V. Numerical Simulations and Experimental Validation

To validate the previous theoretical results, numerical simulations using PSIM© software and experimental measurements from a hardware prototype will be presented in this section. With the parameters given in Table II, both the numerical simulation and the experimental tests are performed.

A. Simulation Results for Validating the Control Law

First, the performance of the system under the developed control technique is checked by numerical simulations. Fig. 6 shows

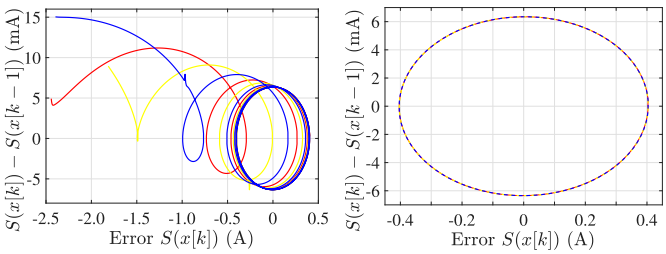


Fig. 7. Phase plane diagram of the error and the difference of the error for three phases. (a) Before reaching steady state. (b) Steady state. All are overlapped.

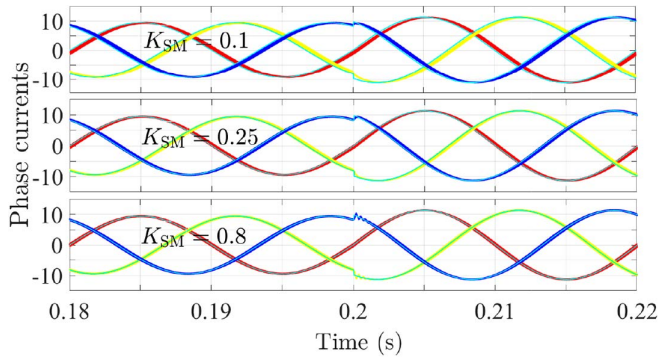


Fig. 8. Three-phase currents for different values of K_{SM} after applying a step change (20% increase) in three-phase voltages at $t = 0.2$ s. The reference currents gv_{pn} for all phases are also shown.

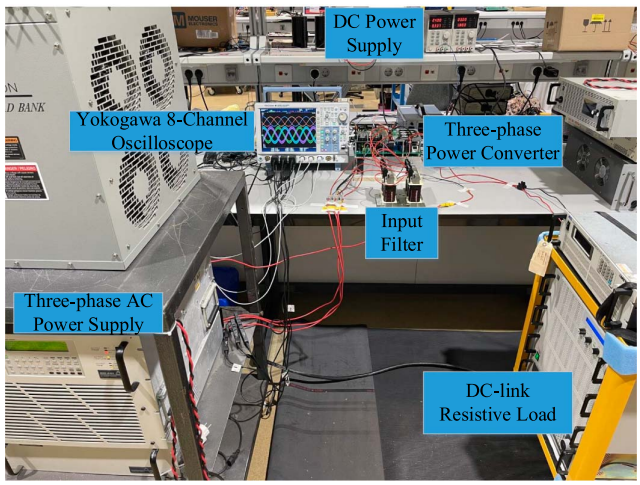


Fig. 9. Photograph of experimental setup with measuring instruments.

the control signals and current for phase a illustrating the proper operation after implementing the digital SMC on the selected topology. Fig. 7 shows the phase portrait of the error signals, and the differences in error signals among the three phases. In Fig. 8, the effect of 10% change (increase) in three-phase voltages is shown in three-phase currents for different values of K_{SM}.

B. Testing of Control Law Under Normal Scenario

In this section, to validate the previous theoretical results, both numerical simulations using PSIM© software and experimental measurements from a hardware prototype are given for ease of comparison.

TABLE III
HARDWARE SPECIFICATIONS OF EXPERIMENTAL SETUP

Hardware	Type
Switches	SKIIP 23AC12T4V1
Drivers	ACPL-331J
Current sensors	LA 25-NP
Voltage sensors	ACPL-C79B
DSP microcontroller	F28M35H52C
Three-phase ac supply	360AMX Pacific Power Source
Electronic load	EA-EL 9750-75 HP
Oscilloscope	YOKOGAWA DLM3000 MSO Series

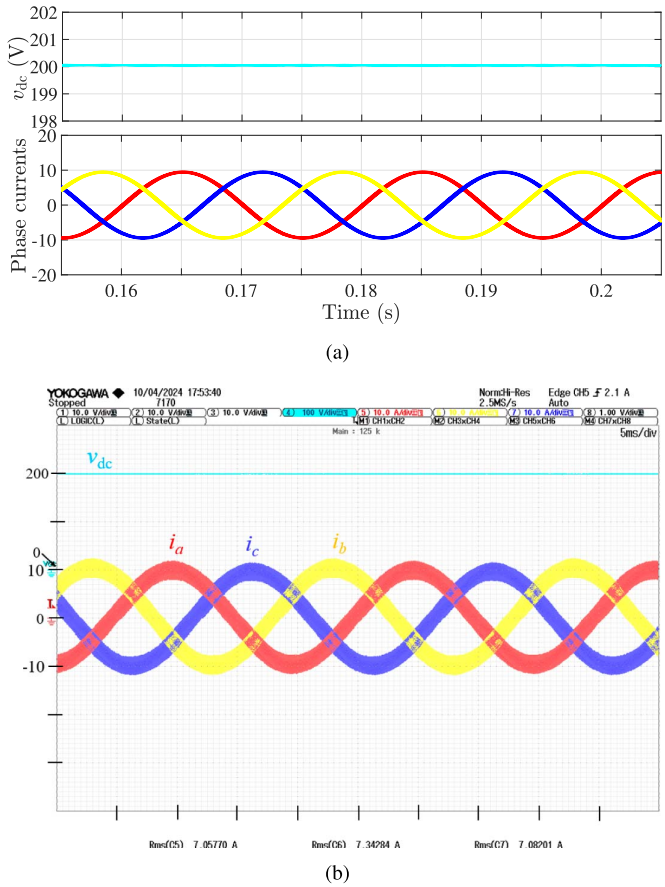


Fig. 10. Phase currents and dc-link voltage in steady-state operation. (a) Numerical simulations. (b) Experimental measurements. Time axis: 5 ms/div. Color code—phase a: red, phase b: yellow, phase c: blue.

The photograph of the experimental setup is given in Fig. 9. The rectifier consists of six switches with insulated-gate bipolar transistor (IGBT) modules rated at 1200 V and 25 A, using IGBT 4 technology. Inductors in three phases are rated at 20 A. Control computation of sensed three-phase voltages, currents, and dc-link voltage is performed through the F28M35H52C DSP. More details on the experimental setup and hardware specifications are presented in Tables II and III, respectively.

To avoid saturation in the duty cycles at start-up, a software-controlled precharge circuit (precharge relays with resistors and bypass relays) is employed to charge the capacitors appropriately at no load to reach $V_{dc,min} = 2\sqrt{2}V_{rms}$ [35]. Fig. 10 shows the

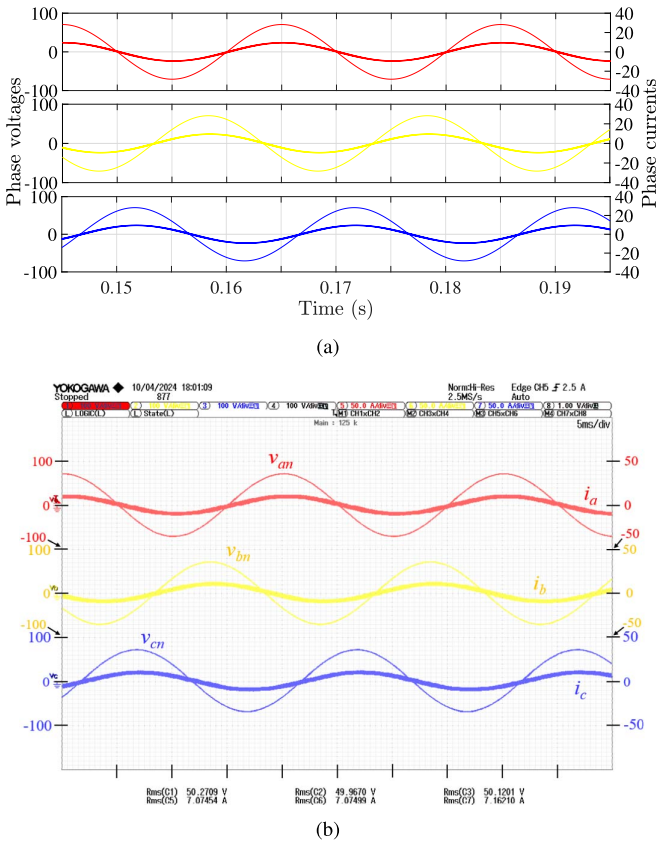


Fig. 11. Waveforms of the ac–dc rectifier input voltages and currents for three-phase operation showing PFC. (a) Numerical simulations. (b) Experimental measurements. Time axis: 5 ms/div.

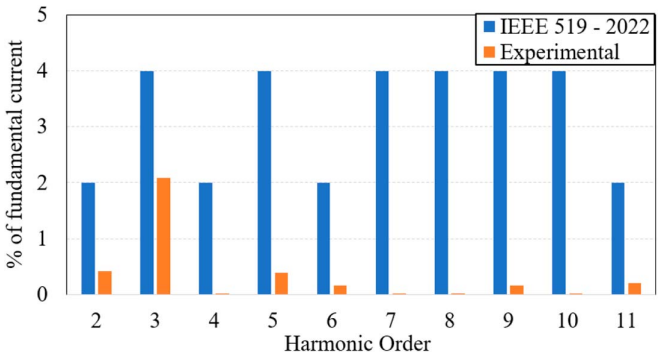


Fig. 12. Harmonic content together with IEEE 519-2022 standard limits for phase *a* current in Fig. 10.

three-phase current waveforms and the dc-link voltage in steady state. It can be observed that the input currents are sinusoidal and in phase with the input voltage, hence the system correctly performs PFC as detailed in Fig. 11. The THD and PF for simulations and experimental results are calculated using the following expressions [36]:

$$\mathrm{THD} = \sqrt{\left(\frac{I_{\mathrm{rms}}}{I_{1,\mathrm{rms}}}\right)^2 - 1} \tag{30}$$

$$\mathrm{PF} = \cos(\theta_v - \theta_i)\sqrt{\frac{1}{1+\mathrm{THD}^2}} \tag{31}$$

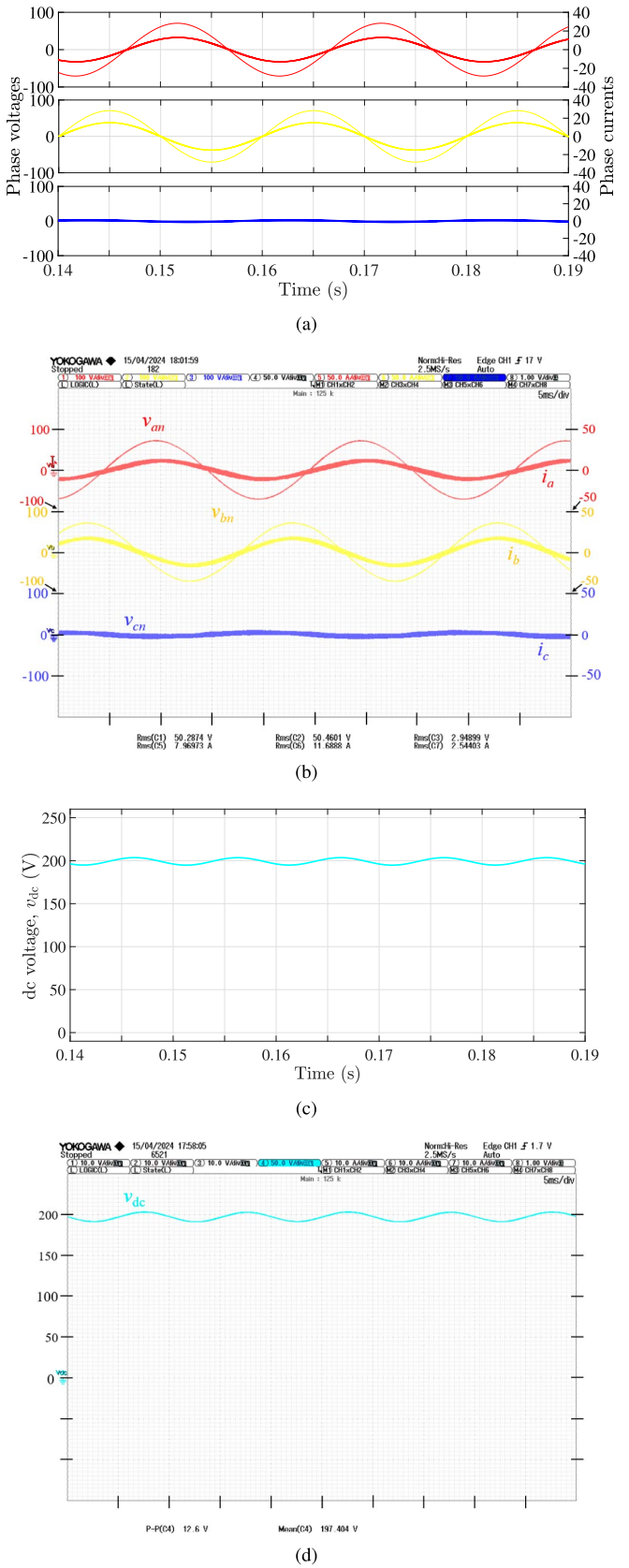


Fig. 13. Waveforms of the ac–dc rectifier input voltages and currents for two-phase operation showing PFC. (a) Numerical simulations. (b) Experimental measurements. DC-link output voltage (c) numerical simulations (d) experimental measurements. Time axis: 5 ms/div.

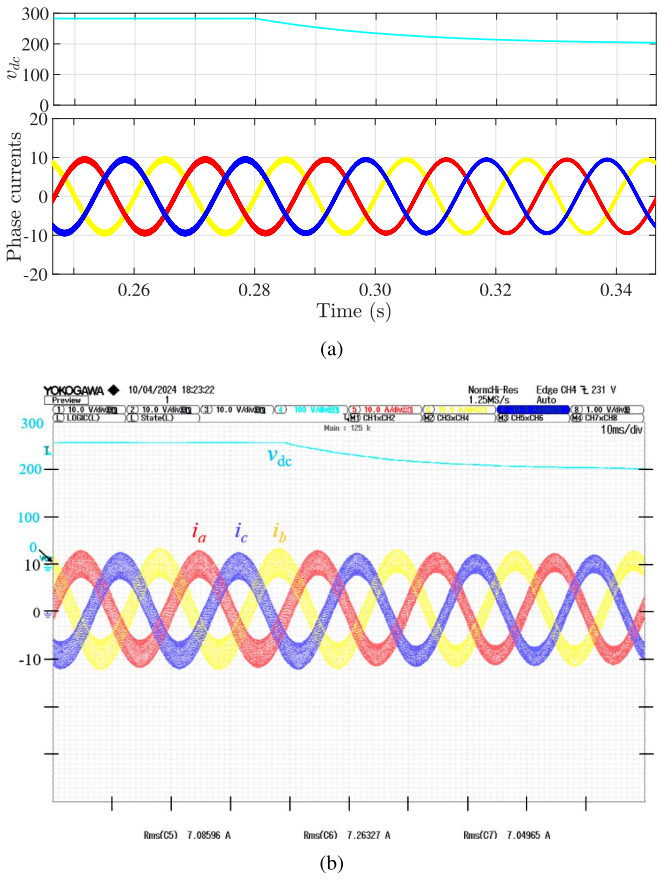


Fig. 14. Waveforms of the input currents and dc-link voltage for three-phase operation under 50% change in load resistance (80 to 40 Ω). (a) Numerical simulations. (b) Experimental measurements. Time axis: 10 ms/div.

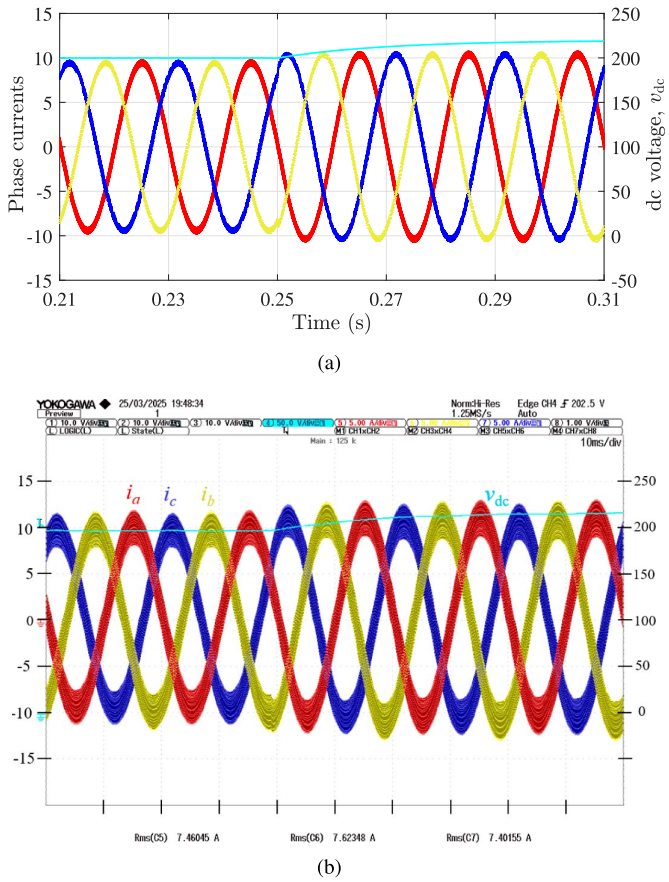


Fig. 15. Waveforms of the input currents and dc-link voltage for three-phase operation under 10% change (increase) in input voltages (50 to 55 V) at $t = 0.25$ s. (a) Numerical simulations. (b) Experimental measurements. Time axis: 10 ms/div.

where I_{rms} and $I_{1,\text{rms}}$ are rms values of the total current including switching ripple and fundamental current at 50 Hz, respectively. The phase difference between fundamental voltage and current is denoted by $\theta_v - \theta_i$.

For calculating the previous quantities from the experimental results, the data of the waveforms are first captured and then processed using a computer program and then pass-band filtered using a 20-Hz filter bandwidth centered at 50 Hz. The same filtering process was applied to the results from the numerical simulation. For the calculation of THD, current sensor bandwidth of 150 kHz is used. The obtained PF and THD calculated for phase a are 99.87% and 0.70% respectively from the numerical simulations while they are 99.12% and 2.42% respectively from the experimental data. In Fig. 12, harmonic contents of the phase a current are shown where third harmonic contributes most. The results comply with IEEE standard [3].

C. Testing of Control Law Under Different Scenarios

The performance of the rectifier in two-phase mode of operation, in case of a shortage in one phase, is shown in Fig. 13. It can be observed from this figure that the rectifier can also work effectively in this mode of operation and correctly perform the PFC, which is desirable in case of any faulty condition in one of the input phases. The PF values corresponding to phases a and b in two-phase mode of operation are 99.23% (simulation 99.90%) and 99.36% (simulation 99.96%). The THD values for the same phases are 2.23% (simulation 0.60%) and 1.72% (simulation 0.44%). Furthermore, the output dc voltage is still satisfactory, although there is a small $2\omega_g$ ripple on it due to the time-variant term of instantaneous power in nonbalanced two-phase system. From this figure, it can be concluded that the rectifier can work effectively in two-phase and three-phase modes of operation under the proposed digital control strategy. Therefore, it is suitable, reliable, and flexible for a wide range of applications such as EV charging, dc microgrids, interconnection of multisource microgrids, solid-state transformers, and so on.

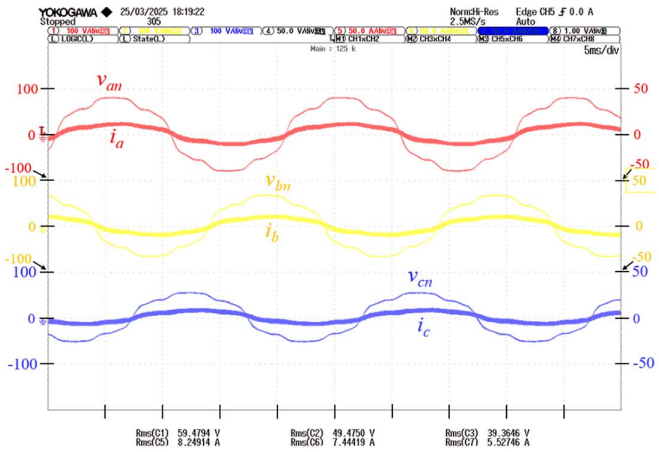
The performance of the rectifier under the proposed control strategy is also validated in front of a 50% load resistance step change. Fig. 14 shows the performance of the rectifier under this load resistance change both by numerical simulations and experimental measurements. It can be seen from this figure that the rectifier can perform well after a change in the output load resistance. Moreover, the simulation results and the experimental measurements are in good agreement.

In Fig. 15, the effect of the 10% step change (increase) in the three-phase voltages is shown in the three-phase currents both by numerical simulations and experimental measurements. The current is regulated after the step change along with the desired PF and THD.

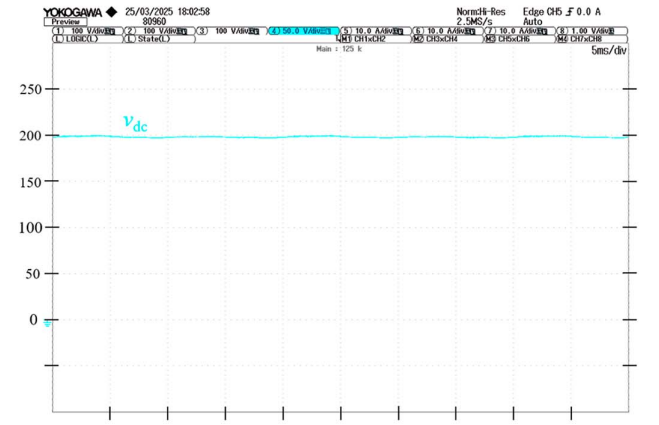
TABLE IV
COMPARATIVE ANALYSIS OF PROPOSED CONTROL METHOD WITH LITERATURE

Ref.	Converter	Controller	SW Tech.	No. SW	Control Process	f_s (kHz)	Trans. f_s	Filter-mH	THD (%)	PF	Power (kW)
Wong et al. [37]	SWISS rectifier	Cascaded PI	MOSFET	12	TMS320F28335	Fixed-40	Fixed	*LC*-0.7	2.50	0.993	1.2
Muhlethaler et al. [38]	3ϕ 3-wire	Cascaded PI	IGBT 4	6	DSP-N/A	Fixed-8	Fixed	*LCL*-2.54	3.86	0.998	10
Guo et al. [39]	CAC-ZVS[1]	Cascaded PI	N/A	7	DSP28335	Fixed-10	Fixed	*L*-20	3.80	0.991	1.2
Abdel-Aziz et al. [40]	B8 rectifier[2]	MPC	MOSFET	8	DSP-N/A	Fixed-8	Variable	*L*-3	4.47	N/A	1.0
Guo et al. [41]	CAC-ZVS	MPC	N/A	7	TMS320F28335	Fixed-10	Fixed	*L*-50	2.20	0.995	1.2
Rathore et al. [42]	Conventional 1ϕ	Adaptive SMC	N/A	3	OPAL-RT	Fixed-N/A	Variable	*L*-1.6	3.42	0.999	0.2
Mejia-Ruiz et al. [43]	Semi-bridgeless	Adaptive SMC	GaN	6	TMS320F28379D	Fixed-50	Variable	*L*-1.6	3.20	0.998	1.0
Proposed	3ϕ 4-wire	Digital SMC	IGBT 4	6	F28M35H52C	Fixed-20	Fixed	*L*-1.76	2.42	0.991	1.0

Note: [1]Compound active clamp zero voltage switching. [2]Two-leg neutral point diode-clamped rectifier. Switch (SW), Metal Oxide Semiconductor Field-effect Transistor (MOSFET), Not Available (N/A), Gallium Nitride (GaN).

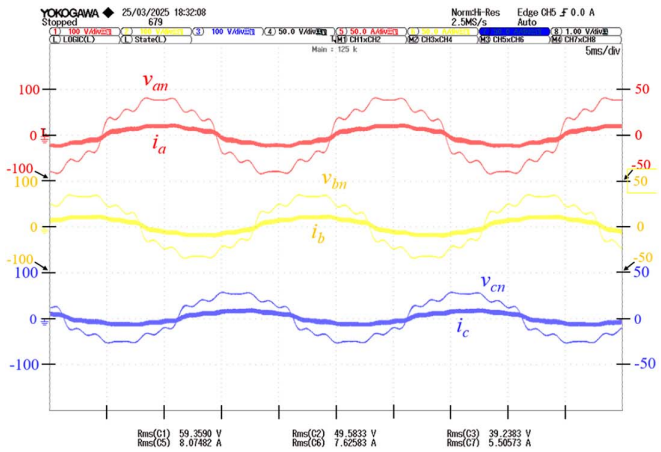


(a)

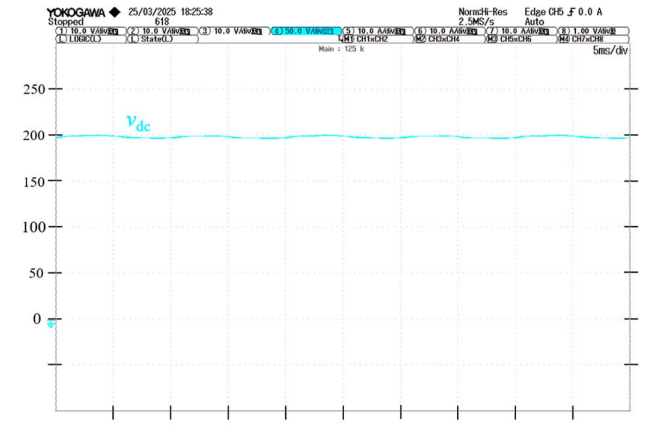


(b)

Fig. 16. (a) Phase currents and (b) dc-link voltage under unbalanced grid voltage with many harmonic contents. Three-phase voltages of unequal amplitude ($V_{an} = 50\,\text{V}+20\%$, $V_{bn} = 50\,\text{V}$, $V_{cn} = 50\,\text{V}-20\%$) contain mainly third, fifth, and seventh harmonics. Time axis: 5 ms/div.



(a)



(b)

Fig. 17. (a) Phase currents and (b) dc-link voltage under unbalanced grid voltage with many harmonic contents. Three-phase voltages of unequal amplitude ($V_{an} = 50\,\text{V}+20\%$, $V_{bn} = 50\,\text{V}$, $V_{cn} = 50\,\text{V}-20\%$) contain mainly third, fifth, and seventh harmonics. Time axis: 5 ms/div.

Finally, the proposed control is tested under unequal amplitude of three-phase voltages with harmonics in two cases. As shown in Figs. 16 and 17, the system can still maintain the desired PF and THD in each phase. However, small ripples appear in the dc-link voltage (less than 1%).

The comparative analysis between the proposed control method and those from the literature is shown in Table IV. From this table, it can be seen that the cascaded PI control strategy used in [39] exhibits higher input filter component values and THD values compared to the proposed control method, while the PF is the same and the power levels of the converters are approximately equal. Additionally, the proposed method achieves lower THD than adaptive SMC methods with approximately the same value of input inductance. A key advantage of the proposed method is its fixed switching frequency across the entire operation profile, whereas adaptive SMC methods have variable switching frequencies during transients, potentially jeopardizing the EMI certification of the power converter. It

should be noted that the MPC method in [41] shows a better THD compared with the proposed method; however, it has a significantly higher inductance value.

VI. Conclusion

This article proposed a fixed-frequency digital SMC-based control technique for an ac–dc three-phase four-wire unity PF rectifier using LFR approach. The control algorithm employs three decoupled sliding mode controllers to achieve LFR behavior in each phase, enabling the PFC. A DSP is utilized to implement the control algorithm, facilitating real-time control. The use of DSP can simplify the implementation of SMC with more control freedom and possibility of using advanced control methods. This article has also investigated the effect of computation delay on the stability of the system under the ideal digital SMC and has proposed a modified control law to ensure stability in the real-time control system in the presence of unavoidable computation delay. Through the proposed modified control method, the ac–dc rectifier can still perform PFC and maintain high-quality phase current waveforms. This makes the rectifier a suitable candidate for different applications such as EV battery charging. The numerical simulations and the experimental results show close agreement with the theoretical analysis, affirming the effectiveness, feasibility, and accuracy of the proposed digital control technique based on SMC and LFR approach. The advantages of the proposed control method are listed below.

1) Fixed-frequency digital SMC based on the LFR approach.
2) Increased reliability under unbalanced conditions with capability of operating in single- and two-phase systems.
3) Feasible, efficient, cheap, and simple control technique which is appropriate for EV battery charging, solid-state transformer, and bidirectional application.
4) Capability of combining the control method with more advanced and complex techniques.
5) Needless of conventional mathematical transformations for the control of three-phase rectifiers in the stationary or synchronous reference frames.
6) Needless of phase-locked loop (PLL) control.
7) Easy implementation in existing rectifiers with only a software upgrade and minor hardware reconfiguration.

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