A Novel PV Microinverter With Submodule-Level Balancing and Active Power Decoupling

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***Abstract*—Conventional photovoltaic (PV) systems suffer from mismatch losses at the PV submodule level, which reduce energy yield and create hot spots. Hence, the reliability and lifetime of both the PV module and the microinverter are critical for the commercial viability of residential systems. To improve the reliability and longevity of both, this article proposes a novel PV microinverter architecture that integrates a series-stacked buffer converter (SSBC) for active power decoupling (APD) at the dc bus level and submodule-integrated converters (subMICs) for mismatch mitigation at the submodule level. Although the SSBC has previously been used for APD in the literature, it typically requires a dedicated input energy storage capacitor and a corresponding voltage regulation loop. Also, it demands additional sensors compared to other APD circuits, increasing system cost and complexity. The novel integration of the SSBC and subMICs in a two-stage microinverter brings three main advantages. First, the isolated-port capacitor of the subMICs, originally used for power balancing, is repurposed as the input energy storage for the SSBC, eliminating a redundant capacitor. Second, because the isolated port is well regulated by the subMICs, the need for a separate SSBC control loop is removed, simplifying and enhancing control robustness. Third, the isolated-port voltage can be adjusted according to the PV module's power level, optimizing SSBC efficiency under varying conditions. This article focuses on the modeling and control of the integrated power stages, with emphasis on simplifying SSBC control. The proposed concept has been validated experimentally with a 300-W microinverter prototype connected to a 180-W, 72-cell commercial PV module. The proposed approach has achieved a 1.2% voltage ripple on the dc bus with a 20-μF film capacitor.**

***Index Terms*—Active power decoupling (APD), modeling and control, photovoltaic (PV) system, series-stacked buffer converter (SSBC), submodule-level balancing, two-stage microinverter.**

I. Introduction

SINGLE-PHASE dc–ac and ac–dc converters with high power factor on the ac side require a power pulsation decoupling stage to compensate for the instantaneous power mismatch between the ac and dc sides [1], [2], [3]. This requirement is critical in grid-connected applications, such as photovoltaic (PV) inverters, LED drivers, fuel cell inverters, and battery chargers. In such systems, the twice-line-frequency power ripple on the dc side negatively affects reliability and efficiency. Specifically, in PV microinverters, this ripple propagates to the PV module side, degrading the accuracy of maximum power point tracking (MPPT) and reducing energy yield [4].

In addition, residential PV microinverters are affected by submodule level imbalances caused by partial shading, temperature variations, dust accumulation, and manufacturing tolerances or aging effects [5], [6], [7], [8], [9]. These undesired conditions can significantly impact the overall efficiency and performance of the PV system. Research has shown that submodule integrated converters (subMICs) can effectively mitigate these mismatches by employing differential power processing architectures (i.e., PV-to-isolated-port) [5], [6], which enhance energy capture and prevent issues like hot-spot formation [7]. Moreover, subMICs can mitigate long-term cell degradation, potentially extending the lifespan of a PV module by 5–10 years beyond its nominal 25-year lifetime [8], [9]. However, conventional microinverters typically lack the ability to address submodule-level mismatch, leaving associated energy losses and hot-spot risks unaddressed.

Traditionally, power pulsation decoupling relies on electrolytic capacitors due to their high energy density [1], [2], [3]. However, they suffer from high power losses, limited ripple current handling capability, low reliability, and shorter lifetime in high-temperature environments such as PV systems [10]. To reduce the size of the dc bus capacitor and improve power density and reliability, active power decoupling (APD) circuits have been proposed, as highlighted in *Google* and *IEEE* jointly sponsored "little box challenge" [11].

The APD approaches are broadly classified as dependent and independent power decoupling. The independent APD circuits operate separately from the inverter and rectification stage [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], and they are further divided into parallel-connected [12], [13], [14], [15] and series-connected APD circuits [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. In parallel-connected APD circuits, the main energy storage capacitor is connected across the dc bus through a bidirectional converter, using full-bridge and half-bridge buck [12], [13], boost [14], and split-capacitor types [15]. The voltage stress in these circuits is at least the dc bus voltage and is often higher in boost-type converters. This high voltage stress, combined with limitation of using low-switching transistors, hinders compact design

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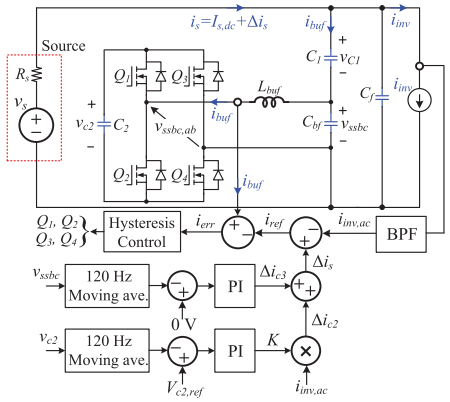

Fig. 1. DC–AC inverter with SSBC and its feedback control loops [19], [20].

and leads to increased losses, reduced efficiency, and low power density [16].

To overcome these drawbacks, series-connected APD converters with different insertion points have been proposed [17], [18]. They employ an H-bridge converter with voltage stress corresponding to the ripple presented on the main energy storage capacitor. However, in [17] and [18], the ripple voltage on the main energy storage capacitor is limited, as its minimum voltage needs to be higher than the inverter output or grid voltage for proper operation of the power stage. Thus, the reduction in size of the main energy storage capacitor is limited. In [19], [20], [21], [22], [23], [24], [25], [26], and [27], a series-stacked buffer converter (SSBC) depicted in Fig. 1 is presented. The SSBC is placed in series with the main storage capacitor, C_1, thus processing only a fraction of the total power. This alleviates the efficiency penalty, achieving peak efficiencies of 99.4%, comparable to its passive counterpart [19]. A plethora of research has been conducted, focusing on its optimal design and operation [21], [22], [23], cost [24], and control approaches [19], [20], [25], [26], [27], [28].

However, controlling the SSBC demands more voltage and current sensors than other APD converters. In [19] and [20], a hysteresis current mode control (CMC) has been proposed using two voltage and two current sensors for SSBC operation (Fig. 1). This method does not require a plant model of the SSBC; however, it introduces challenges like increased design complexity due to variable switching frequency operation. Additionally, the inherent inaccuracies of hysteresis CMC method result in a dc offset in the SSBC output voltage, which must be corrected with an additional control loop. This control loop introduces a dc correction term, Δi_{C3}, to eliminate the dc offset from the current. If not addressed, this issue can cause drift in the main storage capacitor voltage, v_{C1}, and disrupt system operation. Besides, in practice, SSBC is lossy, which needs a compensation term, Δi_{C2}, to regulate the voltage on the input energy storage capacitor, introducing an undesirable small ripple voltage at the dc bus. In addition, the voltage mode control (VMC) method has also been proposed in [25], [26], and [27]. However, this method still requires three isolated voltage sensors. Moreover, the SSBC in [19], [20], [21], [22], [23], [24], [25], [26], and [27] requires a dedicated input energy storage capacitor, a voltage regulation loop, and its precharge mechanism to ensure proper SSBC operation.

In modern PV systems, two-stage microinverters are preferred due to their higher MPPT efficiency, flexibility in handling wide voltage and power variations, and ability to decouple twice-line-frequency power ripple at the dc bus level [1], [3]. Numerous two-stage microinverters have been presented in the literature [28], [29], [30], [31], [32], [33], [34], [35], including commercial ones from Texas Instruments [33], UBIK S350 [34], and STMicroelectronics [35]. However, these microinverters typically exhibit low reliability and limited lifetime, as they employ passive power decoupling using electrolytic capacitors. Moreover, they do not address shading effects at the PV submodule level, which can lead to mismatch losses and hot-spot formation.

To address the challenges faced by microinverters in residential systems—namely mismatch losses, power decoupling, and control complexity of the APD circuits—this article proposes a novel two-stage microinverter architecture, as depicted in Fig. 2. The core innovation lies in the integration of SSBC at the dc bus level and subMICs at the PV submodule level. A comparison with existing technologies is provided in Table I. The distinguishing features of the novel architecture, combined with the proposed fixed-frequency CMC for the SSBC, are summarized as follows.

1) *Reuse of Existing Capacitor C_{sec}:* The isolated-port capacitor of the subMICs, originally used for power balancing, is repurposed as the input energy storage for the SSBC, eliminating a redundant capacitor.
2) The isolated-port voltage is well-regulated by the subMICs, thereby eliminating the need for a dedicated SSBC voltage regulation loop and simplifying its overall control.
3) The isolated-port voltage can be dynamically adjusted based on the PV module's power output, reducing voltage stress on the SSBC and enhancing its efficiency under varying environmental conditions.
4) A small-signal model and a fixed-frequency proportional-resonant (PR) controller are proposed to ensure accurate sinusoidal current tracking by the SSBC, preventing dc offset, and further simplifying SSBC implementation.

The integration of APD in a microinverter enables the use of long-lifetime ceramic and/or film capacitors, improving its reliability. Simultaneously, the subMICs mitigate submodule-level mismatch, improving PV module's performance and extending its lifetime. These two functionalities are crucial for the commercial viability of residential microinverters.

The remainder of this article is organized as follows. Section II describes the operation and design guidelines of the proposed two-stage microinverter. Section III presents the small-signal modeling and control of IIBC, SSBC, and subMICs. Simulation and experimental results are discussed in Sections IV and V, respectively. Section VI concludes this article.

II. Proposed Microinverter Architecture

The main circuit diagram of the proposed two-stage microinverter architecture, which integrates SSBC with subMICs for APD and introduces a novel CMC for SSBC, is

TABLE I
COMPARISON OF THE PROPOSED MICROINVERTER WITH EXISTING TWO-STAGE MICROINVERTERS AND THE SSBC

Topologies and its main characteristics	Mismatch Mitigation Capability at PV Submodule Level	Active Power Decoupling at the DC Bus Level	Simplified Control of SSBC	Simplified Circuit of SSBC	Improved PV Energy Yield	Reliability	Avoiding Hot-Spot Formations in PV Module	Lifetime Enhancement of PV Module & Microinverter	THD (< 3 %)
Other two-stage micro-inverters [28]-[32]	No	No	–	–	No	Low	No	No	–
Commercial two-stage microinverters [33]-[35]	No	No	–	–	No	Low	No	No	≅ 5 % 2.6 % 4.8 %
DC-AC inverter with SSBC [19]-[20]	–	YES	Require two current and two voltage sensors	Require dedicated energy storage port and its pre-charging	–	High	–	–	–
Proposed microinverter	YES	YES	Require only two current sensors	Do not require dedicated energy port	YES	High	YES	YES	2.42 %

SSBC→Series-Stacked Buffer Converter, PV→Photovoltaics, THD→Total Harmonic Distortion.

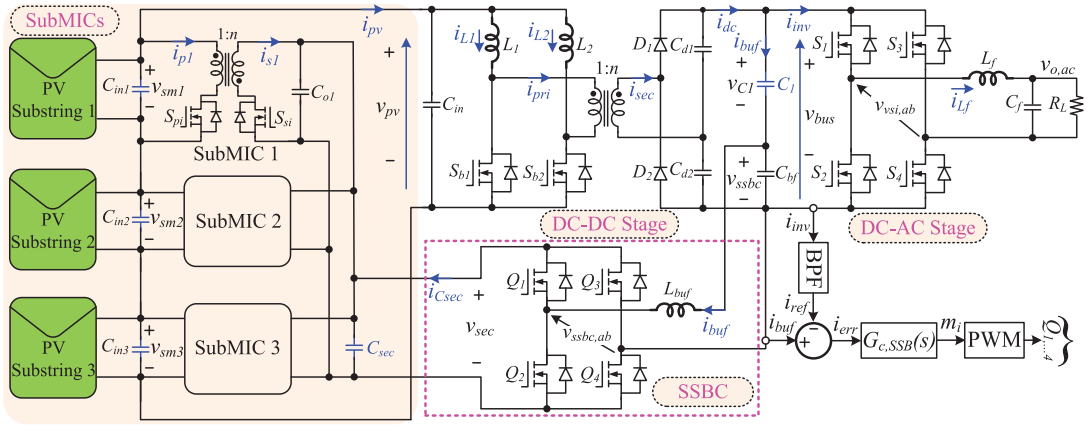

Fig. 2. Proposed microinverter architecture integrating SSBC at the dc bus level with subMICs at the submodule level in PV applications.

depicted in Fig. 2. The two-stage architecture assumes a PV module with three submodules (or substrings) and consists of subMICs, an interleaved isolated boost converter (IIBC), an H-bridge voltage-source inverter (VSI), and the H-bridge SSBC.

The IIBC is used to boost the low input voltage of the PV while maintaining the PV module near the maximum power point, and it provides galvanic isolation with a high-frequency (HF) transformer. On the right-hand side, the SSBC is connected in series with the energy storage capacitor C_1 at the dc bus level, while on the left-hand side, it is connected to the secondary side (isolated-port) capacitor C_{sec} of the subMICs. Note that capacitor C_{bf} is a small decoupling capacitor that attenuates switching noise from v_{ssbc}.

In the sequel, a step-by-step power stage design and a steady-state analysis of the proposed microinverter are discussed.

A. Interleaved Isolated Boost Converter

The IIBC is a well-known topology used to step up the low input voltage of the PV module to the high output voltage of the dc link. It minimizes the input current ripple at the PV source, which is particularly sensitive to current fluctuations. The circuit diagram, including a voltage-doubler rectifier and an MPPT control loop, is shown in Fig. 3. The PV module is modeled as a current source. The converter consists of an input decoupling capacitor (C_{in}), two boost inductors (L_1, L_2), two low-side MOSFETs (S_{b1} and S_{b2}), an HF transformer with a $1:n$ turns ratio, and the voltage-doubler rectifier (D_1, D_2, C_{d1}, and C_{d2}). Stray resistances (r_{L1} and r_{L2}) account for windings and MOSFETs ON-resistances. The gate signals of the switches are phase-shifted by 180° and duty cycles are always greater than 0.5.

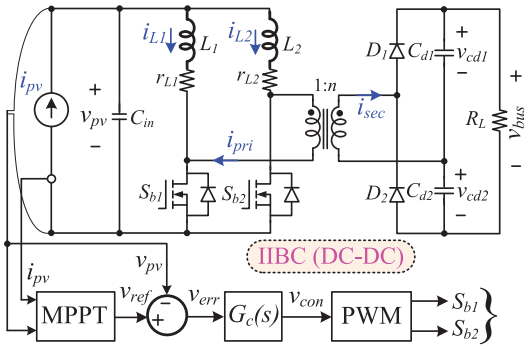

Fig. 3. IIBC with MPPT control loop.

The voltage-doubler rectifier reduces the required turns ratio of the HF transformer, thereby lowering secondary winding conduction losses. The maximum secondary voltage, v_{cd1} or v_{cd2}, is equal to half of the dc bus voltage (v_{bus}). The number of secondary turns (N_s) is determined based on the maximum flux density (B_m), switching frequency ($f_{sw,iibc}$), and the core cross-sectional area (A_e) as follows:

$$N_s \geq \frac{V_{\text{bus,max}}}{4B_m A_e f_{sw,iibc}} \tag{1}$$

where $V_{\text{bus,max}}$ is the maximum average dc bus voltage. The primary number of turns is then given by $N_p = N_s/n$.

TABLE II
CIRCUIT PARAMETERS OF THE PROPOSED MICROINVERTER

Parameters	Values/Units
Microinverter power rating: P_m	300 W
PV module rated current: I_{pv}	5 A
PV module voltage: V_{pv}	[21, 39] V
PV nominal voltage	30 V
DC bus nominal voltage: V_{bus}	360 V
IIBC - Transformer turns ratio: n	1 : 1.9
IIBC - Inductors: L_1, L_2	410 µH
IIBC - Doubler capacitors: C_{d1}, C_{d2}	10 µF
IIBC - Inductor resistances: r_{L1}, r_{L2}	100 mΩ
IIBC - Switching frequency: $f_{sw,iibc}$	50 kHz
SSBC - Main storage capacitor: C_1	20 µF
SSBC - Output filter: L_{buf}, C_{bf}	[400 µH, 680 nF]
SSBC - Inductor resistance: r_{buf}	100 mΩ
SSBC: Switching frequency: $f_{sw,ssbc}$	50 kHz
SSBC: Power processed: p_{ssbc}	7 % of P_m
Inverter: AC side filter: L_f, C_f	[2.4 mH, 330 nF]
Inverter: Switching frequency: $f_{sw,inv}$	50 kHz
SubMICs: Submodule voltage range: $v_{sm,i}$	[7, 13] V
SubMICs: Nominal submodule voltage: V_{sm}	10 V
SubMICs: Max. secondary port voltage: V_{sec}	60 V
SubMICs: Duty cycle: D_{sub}	[0.01, 0.5]
SubMICs: Transformer turns ratio: n_{sub}	1 : 7
SubMICs: Primary inductance of xformer: L_m	13.3 µH
SubMICs: Primary capacitors: $C_{in,i}$	45 µF
SubMICs: Secondary capacitor: C_{sec}	232 µF
SubMICs: Switching frequency: $f_{sw,sub}$	50 kHz

The boost inductor values can be calculated using

$$L_1 = L_2 = \frac{v_{\text{bus}}/2n \cdot (1 - D_b) D_b T_{s,iibc}}{\Delta i_L} \tag{2}$$

where D_b is the duty cycle, $T_{s,iibc}$ is the switching period, and Δi_L is the allowable inductor current ripple (i.e., 20% of I_L). Finally, applying the volt-second balance condition to either L_1 or L_2, the voltage gain of the IIBC is obtained as

$$\frac{V_{\text{bus}}}{V_{\text{pv}}} = \frac{2 \cdot n}{1 - D_b} \tag{3}$$

where the factor $2 \cdot n$ accounts for both the transformer turns ratio and the voltage-doubler rectifier gain. Following these design guidelines, the values of L_1, L_2, and the transformer turns ratio for a given dc bus and PV voltage are summarized in Table II.

B. Series-Stacked Buffer Converter

The SSBC is a full-bridge bidirectional dc–ac converter, as shown in Fig. 2. Its primary function is to source and sink the twice-line-frequency power ripple occurring at the dc bus. To achieve this, the SSBC monitors and compensates for the instantaneous current difference between the dc-side current (i_{dc}) and the inverter input current (i_{inv}), as illustrated in Fig. 2. The inverter input current is a phase-shifted sinusoidal waveform with an average value equal to I_{dc}. Thus, the relationship between i_{inv} and buffer converter current i_{buf} is given by

$$i_{\text{inv}} = I_{\text{dc}} + I_{\text{dc}} \sin(\omega t) \tag{4}$$

$$i_{\text{dc}} = i_{\text{buf}} + i_{\text{inv}} \tag{5}$$

$$i_{\text{buf}} = -I_{\text{dc}} \sin(\omega t) \tag{6}$$

where $i_{\text{dc}} = I_{\text{dc}} + i_{\text{dc},r}$, $i_{\text{dc},r}$ is a small ripple on I_{dc}, $\omega = 2 \cdot \omega_{\text{line}}$, and $\omega_{\text{line}} = 2\pi \cdot 60$ rad/s for a line frequency of 60 Hz. The SSBC must source and sink i_{buf} as defined in (6). Additionally, the charge stored in the main energy storage capacitor C_1 is determined by i_{buf}. This capacitor instantaneously stores and releases the twice-line-frequency charge (q_{C1}), leading to a corresponding voltage ripple given by

$$q_{C1} = \int i_{\text{buf}} dt = -\frac{I_{\text{dc}}}{\omega} (-\cos(\omega t)) = \Delta q_{C1} \tag{7}$$

$$v_{C1,r} = \frac{\Delta q_{C1}}{C_1} = \frac{I_{\text{dc}}}{\omega C_1} \cos(\omega t) = \Delta v_{C1,pk} \cos(\omega t). \tag{8}$$

By source/sinking the current in (6), the SSBC generates a controlled output voltage (v_{ssbc}), which is exactly out of phase and equal in magnitude to the peak-to-peak voltage ripple of C_1 (Δv_{C1}), i.e., $\Delta v_{C1} = -\Delta v_{\text{ssbc}}$. Consequently, the dc bus voltage is $v_{\text{bus}} = v_{C1} + v_{\text{ssbc}}$. Since the ripple voltages cancel each other, the resulting v_{bus} is ripple free and equal to V_{bus}. It should be noted that the voltage on C_1 is the dc voltage plus the ac ripple on it, as $v_{C1} = V_{\text{bus}} + v_{C1,r}$.

The capacitance of C_1 is obtained from (8). A higher allowable voltage ripple on C_1 reduces its required capacitance but increases the voltage stress on the SSBC. This tradeoff must be carefully considered to minimize the overall size of the SSBC. The maximum voltage ripple on C_1 is limited to 33% of the dc bus voltage, following the guidelines in [36]. Design guidelines for the isolated-port capacitor C_{sec} are provided in Section II-C.

The SSBC filter inductor L_{buf} is designed based on ripple current analysis, similar to L_f in the VSI as discussed in [38]. A small decoupling capacitor C_{bf} is included to mitigate switching frequency noise at the SSBC output. The SSBC filter operates at a fundamental frequency of 120 Hz, while the VSI operates at 60 Hz.

C. Submodule Integrated Converters

A bidirectional flyback converter is used in the PV-to-isolated-port architecture for submodule-level voltage balancing (v_{sm1}, v_{sm2}, and v_{sm3}), as shown in Fig. 2. The topology is chosen for its electrical isolation, bidirectional power transfer, high step-up ratio, and simple structure [9], [36]. Each of the three subMICs ($i = 1, 2, 3$) consists of input decoupling capacitors ($C_{\text{in},i}$), MOSFET switches on both the primary ($S_{p,i}$) and secondary sides ($S_{s,i}$), and an isolated-port capacitor (C_{sec}). Under mismatch conditions, the flybacks process only a fraction of the power imbalance between PV submodules, transferring energy to or from C_{sec}. In balanced conditions, they remain off, solely turning on to regulate V_{sec}.

The flybacks are series-connected on the PV side and parallel-connected on the secondary side. Thanks to electrical isolation, the isolated-port voltage can be regulated independently, enabling SSBC integration for APD. The subMICs set V_{sec} high enough to cancel the ripple voltage of capacitor C_1 at the dc bus. For example, with a 360-V dc bus and a 33% ripple, the peak ripple $\Delta v_{C1,pk}$ is 59.4 V, requiring $C_1 = 11.2\ \mu$F for a 180-W PV module, according to (8). To ensure proper SSBC operation, v_{sec} must exceed 59.4 V to fulfill $v_{\text{sec}} > v_{\text{ssbc}}$.

Since the ripple on C_1 depends on the power processed by the microinverter, V_{sec} is adaptively adjusted to reduce the voltage stress on the SSBC. This adaptive approach can enhance SSBC efficiency across varying PV generation levels.

The isolated port of the subMICs serves as a dc link for the SSBC; however, it does not directly supply net energy from C_{sec}. Instead, C_{sec} buffers the twice-line-frequency power ripple at $4 \cdot f_{line} = 240$ Hz. Its capacitance is designed as

$$C_{sec} = \frac{p_{ssbc}}{(2\pi \cdot 240) V_{sec} \Delta v_{sec}} \tag{9}$$

where $p_{ssbc} = 7\% \cdot P_{dc}$ is the power processed by SSBC ($p_{ssbc} = v_{ssbc} \cdot i_{buf}$), V_{sec} is the isolated-port voltage, and Δv_{sec} is the allowable 240 Hz ripple on C_{sec} given in Table II.

Similar to the dc link ripple, excessive ripple on v_{sec} introduces 240-Hz harmonics into the SSBC output, undermining ripple cancellation. Ideally, v_{ssbc} should be a pure sinusoid with no dc offset. A ripple of only 1% on C_{sec} is chosen, though up to 3% is permissible, aligning with the conditions for dc bus voltage in grid-connected inverter standards. Additionally, Δv_{sec} should be attenuated at the subMICs control level, but this is discussed in Section III-C.

The subMICs only process the energy lost in the SSBC to maintain v_{sec} to its average regulated value of V_{sec}, ensuring that $v_{sec} > v_{ssbc}$ without compromising overall system efficiency. Unlike other APD designs, which require an additional energy port and precharging mechanism, this approach reduces the control complexity.

The power rating of the subMICs depends on the number of submodules or substrings (n_{st}) and their power rating: $P_{sub} = (n_{st} - 1/n_{st})P_{st}$, where P_{st} is the substring power rating. For the PV module of 180 W, $n_{st} = 3$, and $P_{st} = 60$ W such that the subMICs power rating is $P_{sub} = 40$ W. The flybacks operate in discontinuous conduction mode (DCM), providing a sufficiently good efficiency at this power level and simplifying the dynamic response.

D. Voltage Source Inverter

A conventional H-bridge dc–ac VSI performs the inversion, as shown in Fig. 2. It consists of MOSFET switches and a low-pass filter to attenuate switching noise. The switches operate under unipolar SPWM. The grid frequency and phase are assumed to be known through a standard phase-locked loop, though its implementation is beyond the scope of this work. The dc bus voltage is regulated via inverter control, as detailed in Section III-D.

E. Efficiency Considerations

Although some aspects of the proposed architecture can improve SBBC efficiency, this work focuses on control topics, rather than demonstrating microinverter efficiency.

First, the SSBC, as an APD circuit, has been demonstrated not to compromise efficiency in the literature. In this article, the SSBC processes a maximum of 7% of the PV rated power, minimizing its impact on the microinverter efficiency.

Similarly, subMICs do not introduce significant losses. They remain off when PV submodules are balanced and only regulate the isolated-port voltage by compensating for minor power losses in the SSBC. Since the SSBC operates with high efficiency, the additional power processed by the subMICs is negligible.

III. Small-Signal Modeling and Control Design of the Proposed Microinverter

This section presents the small-signal modeling and control design for the IIBC, SSBC, subMICs, and VSI in the proposed microinverter. Although the control strategies for the SSBC and subMICs introduce novel approaches, the VSI control follows a conventional design. The primary contribution lies in the small-signal model and fixed-frequency PWM controller for the SSBC, as well as the modified controller design for the subMICs, which are detailed in a step-by-step manner in Sections III-A–III-D.

A. IIBC Modeling and Control

Despite the advantages of the IIBC in high conversion ratio applications, its small-signal modeling and controller design have not been demonstrated with experimental results [37]. A conventional small-signal averaged model has been derived, and an appropriate controller has been designed, as detailed.

The IIBC operates in four modes as in [37]. According to Fig. 3, in mode 1, S_{b1} is off and switch S_{b2} is on. Mode 3 is identical to mode 1, except for inverted gate signals. These modes correspond to energy delivery. Conversely, in modes 2 and 4, both switches are on, allowing the inductors to store energy.

Given these operating conditions, the state-space model of the IIBC considers three instead of four intervals. Averaging the equations over one switching period and linearizing them results in the general state-space model in the matrix form

$$\begin{cases} \dfrac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) \\ \hat{y}(t) = C\hat{x}(t) + D\hat{u}(t). \end{cases} \tag{10}$$

The state matrices yield the small-signal model of the converter as (11), shown at the bottom of the next page.

Finally, using the parameters in Table II, the control-to-output transfer function $G_{vd}(s)$ is obtained as follows:

$$G_{vd}(s) = \frac{\hat{v}_{pv}(s)}{\hat{d}(s)} = \frac{-8.1245 \times 10^8 (s + 832)}{(s + 238)\left((s + 211)^2 + 3770^2\right)} \tag{12}$$

where $\hat{v}_{pv}(s)$ is the input voltage of the IIBC and $\hat{d}(s)$ is the control input duty cycle.

From Fig. 3, it can be seen that the variable of interest for regulation is the PV module voltage, v_{pv}. This voltage must follow v_{ref}, which is the output of an MPPT block. Since changes in the reference voltage depend on environmental conditions such as temperature, they are slow over time, meaning that the loop gain does not need a high crossover frequency. For this reason, a controller $G_c(s)$ consisting of a proportional gain plus two poles at different frequencies meets the application requirements.

1) The proportional term increases the dc magnitude of the loop gain and reduces the steady-state error.
2) A low-frequency pole ensures the desired crossover frequency of the loop gain.
3) A high-frequency pole attenuates the switching frequency noise in the feedback loop.

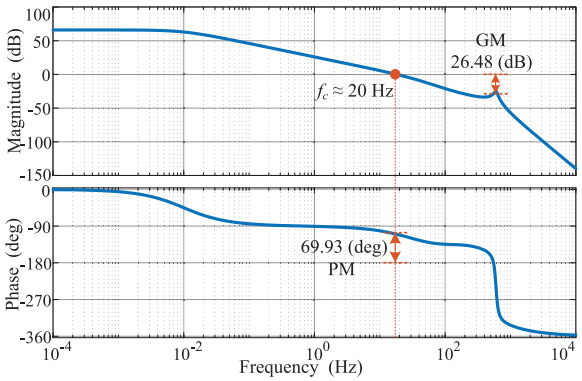

Fig. 4. Bode plot of the loop gain of the IIBC.

Therefore, the s-domain transfer function of the proposed controller is

$$G_c(s) = \frac{-K_p}{\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)} \tag{13}$$

where K_p is the proportional gain and $\omega_{p1} = 2\pi \cdot f_1$ and $\omega_{p2} = 2\pi \cdot f_2$ are the pole frequencies.

The Bode plot of the loop gain $G_{vdc}(s) = G_{vd}(s) \cdot G_c(s)$ is shown in Fig. 4. It can be observed that the phase margin (PM) is approximately 70° at a crossover frequency of about 20 Hz, whereas the gain margin (GM) at 600 Hz is greater than 26 dB.

B. SSBC Modeling and Control

The simplified SSBC circuit is shown in Fig. 5(a), including the stray resistance r_{buf} of the inductor L_{buf}. Under unipolar modulation, the state equations for the ON and OFF states during $d(t)T_{s,\text{ssbc}}$ and $(1 - d(t))T_{s,\text{ssbc}}$, respectively, are

$$\begin{cases} \dfrac{di_{\text{buf}}(t)}{dt} = -i_{\text{buf}}(t)\, r_{\text{buf}} + v_{\text{ssbc}} - V_{\text{sec}} \\ \dfrac{di_{\text{buf}}(t)}{dt} = -i_{\text{buf}}(t)\, r_{\text{buf}} + v_{\text{ssbc}} + V_{\text{sec}}. \end{cases} \tag{14}$$

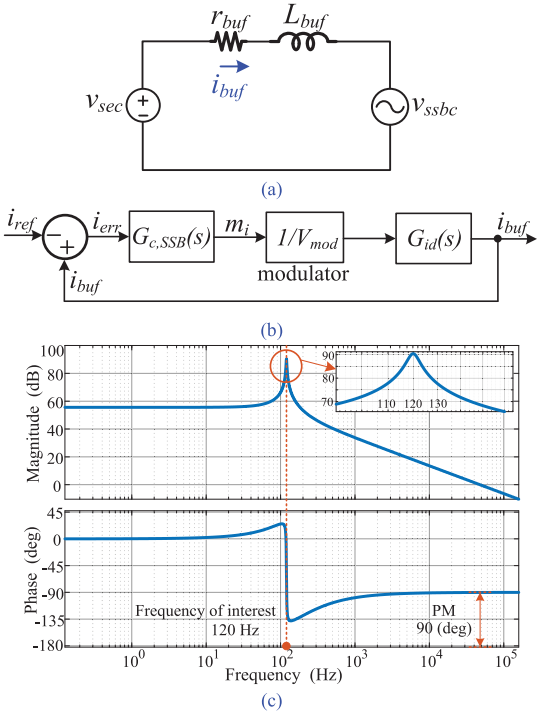

Fig. 5. (a) Simplified equivalent circuit of the SSBC, (b) proposed control loop block diagram, and (c) Bode plot of the loop gain of the SSBC.

Averaging over one switching period and linearizing yields the small-signal model of the converter. The control-to-output transfer function is

$$G_{id}(s) = \frac{\hat{i}_{\text{buf}}(s)}{\hat{d}(s)} = \frac{V_{\text{sec}}/r_{\text{buf}}}{1 + s(L_{\text{buf}}/r_{\text{buf}})} \tag{15}$$

where $\hat{i}_{\text{buf}}(s)$ is the regulated output and $\hat{d}(s)$ is the control input. V_{sec} is the input source voltage of the SSBC, which is regulated by the subMICs. In the bipolar modulation case, the numerator in (15) is modified to $2V_{\text{sec}}/r_{\text{buf}}$.

The proposed SSBC control loop in the microinverter, shown in Figs. 2 and 5(b), requires two current sensors: one for the inverter input current i_{inv} and another for the SSBC inductor current i_{buf} sensing. The inverter current i_{inv} is filtered using an analog bandpass filter (BPF) to generate the reference

$$A = \begin{bmatrix} 0 & -1/C_{\text{in}} & -1/C_{\text{in}} & 0 & 0 \\ 1/L_1 & -R_L & 0 & 0 & (D_b - 1)/nL_1 \\ 1/L_2 & 0 & -R_L & (D_b - 1)/nL_2 & 0 \\ 0 & 0 & -(D_b - 1)/nC_{d1} & -1/R_L C_{d1} & -1/R_L C_{d1} \\ 0 & -(D_b - 1)/nC_{d2} & 0 & -1/R_L C_{d2} & -1/R_L C_{d2} \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & 1/C_{\text{in}} \\ \dfrac{-i_{\text{pv}}(R_L + D_b^2 R_L - n^2 r_{L1} + n^2 r_{L2} - 2D_b R_L)}{4n^2 L_1 (D_b - 1)} & 0 \\ \dfrac{-i_{\text{pv}}(R_L + D_b^2 R_L + n^2 r_{L1} - n^2 r_{L2} - 2D_b R_L)}{4n^2 L_2 (D_b - 1)} & 0 \\ \dfrac{i_{\text{pv}}}{2nC_{d1}} & 0 \\ \dfrac{i_{\text{pv}}}{2nC_{d2}} & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad D = 0 \tag{11}$$

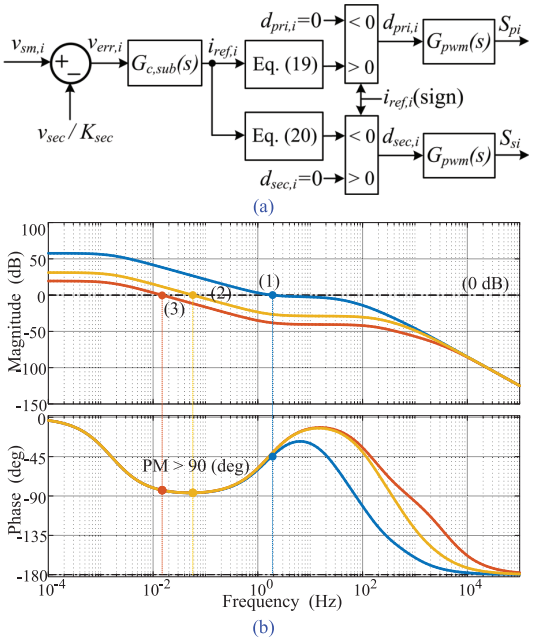

Fig. 6. (a) Control loop block diagram of the subMICs and (b) its Bode plot of the loop gain in: 1) constant current region; 2) MPP region; and 3) constant voltage region.

signal i_{ref}. The controller then computes the error signal as, $i_{\text{err}} = i_{\text{ref}} - i_{\text{buf}}$.

Since the reference signal is a sinusoid at twice the line frequency, a PR controller is employed to minimize the steady-state error between the ac component of i_{inv} and i_{buf}. To achieve minimal error, the resonance frequency of the PR controller should closely match the main harmonic frequency of the reference signal i_{ref}. The transfer function of the PR controller is given by

$$G_{c,\text{SSB}}(s) = \frac{s^2 + 2\omega_{pr1}s + \omega_{pr2}^2}{s^2 + \left(\frac{2\omega_{pr1}}{Q}\right)s + \omega_{pr2}^2} \tag{16}$$

where $\omega_{pr1} = \omega_{pr2} = 4\pi \cdot f_{\text{line}}$ and Q is the quality factor. The loop gain Bode plot in Fig. 5(c) shows that the PR controller provides an appropriate crossover frequency and a sufficiently high gain at the key frequency of $2 \cdot f_{\text{line}} = 120$ Hz, ensuring a negligible steady-state error. Moreover, the PM of 90° and the infinite GM confirm robust stability.

The controller is designed to be adaptable to grid frequency variations, as illustrated in the zoomed-in section of Fig. 5(c). This flexibility allows it to maintain performance even if slight deviations in grid frequency occur.

Additionally, the controller ensures precise tracking of the ac component of i_{ref}, preventing any dc component from affecting SSBC operation. This eliminates the need for an additional control loop previously adopted for dc correction of the SSBC output voltage, reducing both control complexity and implementation cost.

C. SubMIC Controller Design

The control block diagram for each subMIC is shown in Fig. 6(a). The voltages of the submodules (v_{sm1}, v_{sm2}, and v_{sm3}) and the secondary isolated-port voltage (v_{sec}) is sensed for control purposes. The error signal for each subMIC control loop is given by $v_{\text{err},i} = (v_{\text{sec}}/K_{\text{sec}}) - v_{sm,i}$, where K_{sec} is a positive scaling factor introduced to adapt the isolated-port voltage level to the power rating of the microinverter. This reduces voltage stress on the SSBC as power levels vary. The value of K_{sec} determines how many times v_{sec} is larger than the average of the submodule voltages v_{sm1}, v_{sm2}, and v_{sm3}. Given that the nominal voltage of the submodules at the MPP is approximately 10 V, K_{sec} and the corresponding range of v_{sec} are defined as

$$\begin{cases} 1 \le K_{\text{sec}} \le 7.5 \\ 10\ \text{V} \le V_{\text{sec}} \le 75\ \text{V}. \end{cases} \tag{17}$$

The lower bound of K_{sec} is set by the nominal value of the submodule voltages, whereas the upper bound is limited by the maximum allowable voltage ripple on C_1, which is 33% of the dc bus value. In the control realization, the microcontroller selects K_{sec} based on a lookup table generated using the sensed PV current and voltage, effectively adjusting K_{sec} as the PV power output varies.

The subMIC controller design follows the modeling approach in [9] but introduces key differences. Since the SSBC control generates a sinusoidal current i_{buf}, the secondary isolated-port voltage $v_{\text{sec}}(t)$ exhibits a sinusoidal ripple at four times the line frequency ($4 \cdot \omega_{\text{line}}$). The subMIC controller must filter out this disturbance while ensuring that the average value V_{sec} remains proportional to $V_{sm,i}$ and in accordance with K_{sec}.

To achieve this, a low-pass filtering pole ω_{sp1} is set at 10 mHz, resulting in a closed-loop crossover frequency below 1 Hz and a PM greater than 90°, particularly in the MPP region, as shown in Fig. 6(b). Thanks to this low bandwidth, the 240-Hz ripple in the isolated port is attenuated, preventing any impact on the submodule voltages. Despite the slow response of the subMICs, with a settling time in the order of seconds, this does not pose problems, as PV voltage variations due to irradiation, temperature, or mismatches change slowly.

The controller transfer function includes a zero at ω_{sz} and two poles at ω_{sp1} and ω_{sp2} with a gain K_{sm}

$$G_{c,\text{sub}}(s) = \frac{K_{sm}\left(\frac{s}{\omega_{sz}} + 1\right)}{\left(\frac{s}{\omega_{sp1}} + 1\right)\left(\frac{s}{\omega_{sp2}} + 1\right)}. \tag{18}$$

The outputs of these controllers are current References $i_{\text{ref},i}$ ($i = 1, 2, 3$), which can be positive for primary-to-secondary power flow and negative for the reverse. For $i_{\text{ref},i} > 0$, the duty cycle $d_{\text{pri},i}(t)$ of the primary switch $S_{p,i}$ is given by

$$d_{\text{pri},i}(t) = \frac{\sqrt{i_{\text{ref},i}(t)\, 2L_{m,\text{pri}}}}{v_{sm,i}(t)\, T_{s,\text{sub}}} \tag{19}$$

where $L_{m,\text{pri}}$ is the flyback primary inductance and $T_{s,\text{sub}}$ is the switching period. For $i_{\text{ref},i} < 0$, the duty cycle $d_{\text{sec},i}(t)$ of secondary-side switch $S_{s,i}$ is

$$d_{\text{sec},i}(t) = \frac{\sqrt{i_{\text{ref},i}(t)\, 2L_{m,\text{sec}}}}{v_{\text{sec}}(t)\, T_{s,\text{sub}}}. \tag{20}$$

It should be noted that switches on either side must be active for power transfer. The inactive MOSFETs rely on

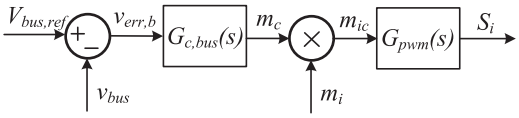

Fig. 7. Control loop block diagram of dc bus voltage regulation.

their body diodes for magnetizing inductance discharge. While synchronous rectification could improve efficiency, it has not been considered since these converters typically process low power.

D. Inverter Dc Link Voltage Regulation

The control block diagram of dc bus regulation is depicted in Fig. 7. Since the dc link voltage is an internal variable of the converter, it does not require tight regulation or exact tracking of the reference $V_{\text{bus,ref}}$.

A proportional–integral (PI) controller is employed to regulate the dc bus voltage [38]. The transfer function of the controller is given by

$$G_{c,\text{bus}}(s) = \frac{K_{\text{bus}}}{T_c}\left(\frac{1+sT_c}{s}\right) \tag{21}$$

where K_{bus} is the proportional gain and T_c is the time constant of the controller zero. It has been considered that $G_{pwm}(s) = 1$.

As it can be seen, the controller includes a pole at the origin and a zero at a very low frequency. Therefore, a high gain controller is not necessary to ensure a low steady-state dc error. Additionally, the output of the proposed controller (m_c) is used as the amplitude modulation index for the downstream inverter. It is multiplied by the modulating sinusoidal signal m_i, which has a magnitude of one and a frequency equal to that of the grid, yielding a sinusoidal modulating signal m_{ic}. This signal is then fed into the PWM block to generate the switching signals for the inverter (S_1–S_4).

IV. Simulation Results

A PSIM model has been developed to verify the performance of the novel architecture, with the proposed CMC of SSBC along with other control loops, also to regulate the isolated-port voltage to an optimal value with a step change in irradiance. The circuit parameters used in the simulation are given in Table II. A step change from 1000 to 0 W/m^2 is applied to the irradiance of one submodule; hence, power generated by the affected PV submodule is reduced. Despite the step change, the PV voltage regulation and the operation of the SSBC remain stable, and the subMICs mitigate the effects of submodule-level mismatch.

Fig. 8 presents the simulation results of the proposed microinverter. In Fig. 8(a), the dc bus voltage (v_{bus}) and the capacitor C_1 voltage (v_{C1}) are shown. At 100 ms, the step change in irradiance is applied, which causes a slight change in the dc bus voltage due to a change in power generated by the PV module. However, it quickly stabilized by the dc bus voltage regulation loop, as highlighted in the zoomed-in waveforms in Fig. 8(b). Additionally, the ripple voltage on v_{C1}, which is influenced by the microinverter power rating, exhibits a change after the 100-ms mark due to the reduction in irradiance. This change in ripple voltage is expected, as it is proportional to the power being processed by the microinverter, as given in (8), and decreases as the power generated by the PV module is reduced. Similarly, Fig. 8(c) illustrates the ripple voltage of C_1 ($v_{C1,r}$), the output voltage of the SSBC (v_{ssbc}), and the isolated-port capacitor C_{sec} voltage (v_{sec}). At 100 ms, when the power generated by the PV module decreases and the ripple voltage $v_{C1,r}$ changes, the isolated-port voltage v_{sec} adjusts accordingly, dropping from 60 to 45 V. This adjustment is done to optimize the voltage stress on the SSBC under varying environmental conditions. This optimization contributes to improving the overall efficiency of the SSBC as discussed in Section III-C. Fig. 8(d) provides a zoomed-in view of the waveforms from Fig. 8(c), clearly showing the change in the ripple voltage of C_1, followed by the adjustment in the SSBC output voltage. Thanks to the proposed CMC approach, this adjustment compensates for the ripple voltage on the dc bus and ensures stable operation of the SSBC. Furthermore, Fig. 8(e) shows the filtered waveforms for the inverter input, dc bus, SSBC filter inductor, and the isolated-port capacitor C_{sec} currents ($i_{\text{inv}}, i_{\text{dc}}, i_{\text{buf}}$, and $i_{C\,\text{sec}}$). As expected, the change in irradiance results in a reduction in the peak values of these currents, indicating the decrease in generated power. This also demonstrates that i_{buf} is exactly out of phase with i_{inv} and has no offset. Thanks to the proposed PR controller, which keeps the i_{buf} pure ac waveform even under fluctuating environmental conditions and, therefore, further simplifies the control of the SSBC by eliminating additional dc correction control loop. Moreover, Fig. 8(f) displays the PV module voltage and current (v_{pv} and i_{pv}). With the change in irradiance, the PV module output current decreases, while the voltage remains well-regulated at the 30-V reference set by the MPPT control loop. This shows the effectiveness of the MPPT control loop discussed in Section III-A.

Fig. 9(a) illustrates the output voltage and load current of the VSI, denoted as $v_{o,\text{inv}}$ and i_o, whereas Fig. 9(b) presents the output voltage and the filter inductor current of the SSBC (v_{ssbc} and i_{buf}). The waveforms show that both the inductor peak current and the output voltage decrease as the power generated by the PV module decreases. This indicates the excellent performance of the SSBC under the proposed CMC approach, effectively adapting to the changing power conditions. Fig. 9(c) depicts the power processed by SSBC (p_{ssbc}) both at full power and after the change in irradiance as well as the power generated by the PV module (P_{dc}). At 100 ms, when the irradiance drops and the PV power output decreases, the power processed by the SSBC also reduces accordingly from 4.4% to 2%, as demonstrated in Fig. 9(c). In addition to the low voltage stress in Fig. 8(c) and (d) after the step change in irradiance, the low power process leads to improved efficiency of the SSBC under varying environmental conditions. Note that the proposed CMC approach shows excellent dynamic adjustment of ripple cancellation on the dc bus with a step change in irradiance.

V. Experimental Results and Discussion

The hardware prototype of the proposed microinverter, which integrates subMICs and an SSBC for APD, has been

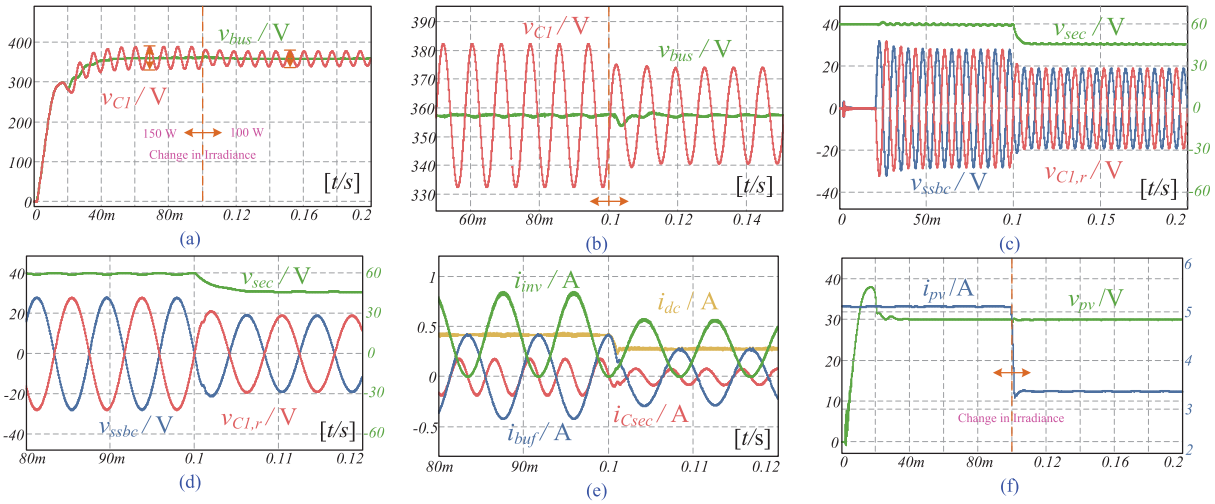

Fig. 8. Simulation results of novel microinverter with a step change in irradiance (a) dc bus and capacitor C_1 voltage (v_{bus}, v_{C1}); (b) zoom-in waveforms of (a); (c) ripple voltage of C_1 ($v_{C1,r}$), output voltage of SSBC (v_{ssbc}), and isolated-port capacitor C_{sec} voltage (v_{sec}); (d) zoom-in waveforms of (c); (e) filtered inverter input, dc bus, SSBC filter inductor, and C_{sec} currents (i_{inv}, i_{dc}, i_{buf}, and $i_{C\,\text{sec}}$); and (f) PV module voltage and current (v_{pv} and i_{pv}).

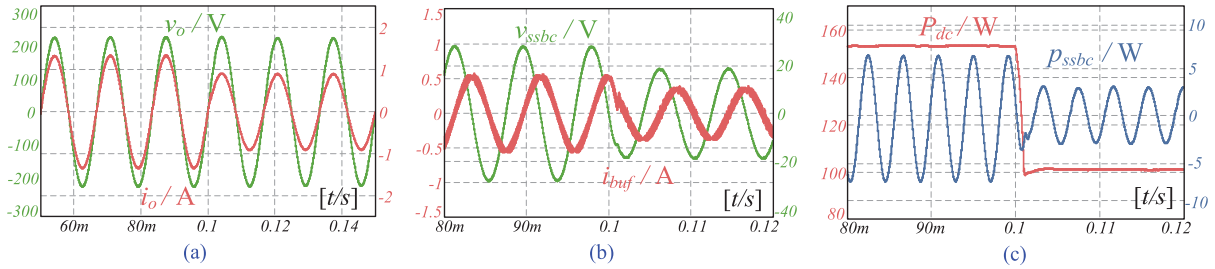

Fig. 9. Simulation results of novel microinverter with a step change in irradiance (a) VSI voltage and current ($v_{o,\text{inv}}$ and i_o), (b) SSBC output voltage and filter inductor current (v_{ssbc} and i_{buf}), and (c) PV generated power and power processed by SSBC (P_{dc} and p_{ssbc}).

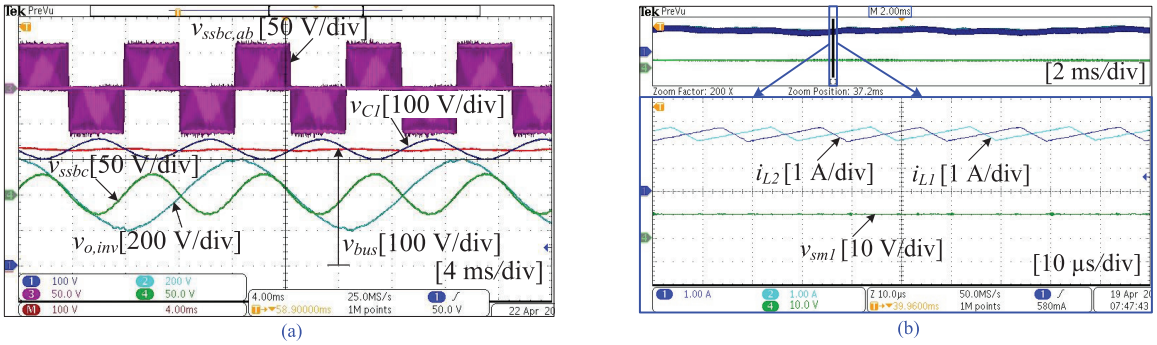

Fig. 10. Steady-state experimental results of the proposed microinverter (a) switching node voltage of SSBC ($v_{\text{ssbc},ab}$), capacitor C_1 voltage (v_{C1}), output voltage of SSBC (v_{ssbc}), dc bus voltage (v_{bus}), and inverter output voltage ($v_{o,\text{inv}}$), and (b) IIBC inductor currents (i_{L1} and i_{L2}) and submodule 1 voltage (v_{sm1}).

designed, built, and tested. The prototype is rated for a power of 300 W. However, the experiments were carried out with a commercial PV module (STP175S-24/ac) with a nominal power of 180 W. Indoor tests were performed with laboratory power supplies (EA-PS 2042-10B) operating as current sources emulating photogenerated currents. As previously mentioned, all the prototype parameters are listed in Table II. In addition, Table III provides the part numbers of the components.

A. Steady-State Experimental Results

Fig. 10(a) presents the steady-state experimental results of the proposed microinverter, where $v_{o,\text{inv}}$ is the output voltage of the VSI, v_{C1} is the main energy storage capacitor voltage, and v_{bus} is the dc bus voltage. Additionally, $v_{\text{ssbc},ab}$ and v_{ssbc} are the switching node and output voltage of the SSBC, respectively. Since the dc bus voltage is the sum of v_{C1} and v_{ssbc}, a mathematical operation in a Tektronix Mixed Domain Oscilloscope MDO3014 is used to compute the dc bus voltage and display it as the fifth waveform (in red). It can be observed that the ripple voltages of v_{ssbc} and v_{C1} are out of phase, following $\Delta v_{C1} = -\Delta v_{\text{ssbc}}$, which cancels out the ripple on the dc bus voltage, resulting in a nearly constant value.

In the experiment, an 18% ripple voltage on C_1 is observed. To satisfy the condition $v_{\text{sec}} > v_{\text{ssbc}}$, a value of $K_{\text{sec}} = 6$ is selected. Thus, $v_{\text{ssbc},ab}$ not only confirms the proper operation of the SSBC power stage but also reflects the peak value of v_{sec}, which is regulated by the subMICs to 60 V in this

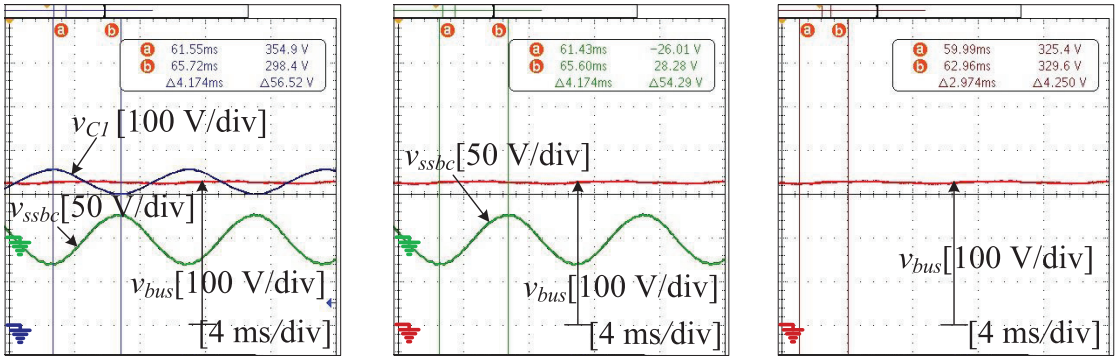

Fig. 11. Experimental results of peak-to-peak ripple of (a) main energy storage capacitor (v_{C1}), (b) output voltage of SSBC (v_{ssbc}), and (c) dc bus (v_{bus}).

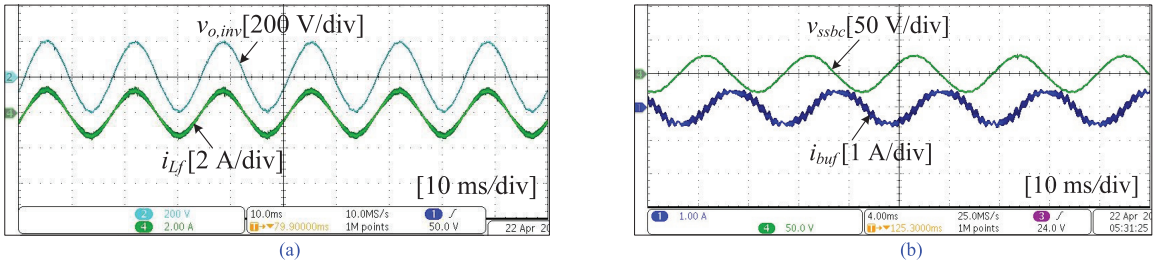

Fig. 12. Steady-state experimental results of (a) VSI filter inductor current and output voltage (i_{Lf} and $v_{o,\text{inv}}$) and (b) SSBC filter inductor current and output voltage (i_{buf} and v_{ssbc}).

TABLE III
PROTOTYPE COMPONENTS PART NO. OF THE PROPOSED MICROINVERTER

Parameters	Values/Units
PV Module	STP175S-24/AC
PV Emulators	EA-PS 2042-10B
Main energy storage capacitor (C_1)	C4AQHBW5200P3FJ
Isolated-port capacitor (C_{sec})	CKG57NX7S2A226M500JJ
Input capacitor of the subMICs ($C_{in,i}$)	C4532X7R1E156M250KC
Voltage doubler capacitors (C_{d1}, C_{d2})	R60IR51005040K
Current transducer	HO 6-P/SP33
Isolated voltage sensor	HCPL7520
Quad-opamp sensing $v_{sm,i}$	LM324AN
SubMICs transformer, SSBC inductor core	RM14, N97
IIBC transformer and inductors core	PQ3535, N97
IIBC power MOSFETs	IPP600N25N3
Rectifier diodes	VS-E5TH1506-M3
VSI MOSFETs	IPP65R190CFD7A
SSBC MOSFETs	IRF520NPbF
Texas Instruments microcontrollers	TMS320F28335

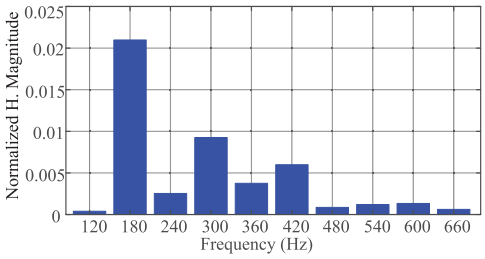

Fig. 13. Normalized THD spectrum of load current.

experiment. Moreover, the proposed PR controller for the SSBC ensures that the output of the SSBC maintains a purely sinusoidal waveform with zero dc offset.

Fig. 10(b) presents the experimental waveforms of the IIBC boost inductor currents i_{L1}, i_{L2}, and the submodule voltage v_{sm1}. The currents i_{L1} and i_{L2} are free of twice-line-frequency ripple, demonstrating that the proposed APD method effectively decouples the twice-line-frequency power ripple at the dc bus. Additionally, the IIBC input current exhibits ripple at twice the switching frequency, reducing the filtering effort required. Consequently, the PV module efficiency is enhanced due to the minimal current ripple. The average values of i_{L1} and i_{L2} are approximately 2.5 A, resulting in a total PV module current of $I_{\text{pv}} = i_{L1} + i_{L2} = 5$ A. Moreover, the zoomed-in waveform of v_{sm1} shows a constant dc value of 10 V, without any switching or power ripple. This proves that the subMIC controllers effectively prevent the propagation of the $4 \cdot \omega_{\text{line}}$ power ripple from the isolated port to the PV module side.

Fig. 11 presents the measurements of the peak-to-peak ripple of the main energy storage capacitor voltage v_{C1}, the peak-to-peak ripple voltage of the SSBC output v_{ssbc}, and the dc bus peak-to-peak ripple v_{bus}. As shown in Fig. 11(a), C_1 withstands the total dc bus voltage v_{bus} and exhibits a ripple voltage equal to 18% of the bus voltage. The measured peak-to-peak ripple voltage is 56.52 V, whereas the SSBC ripple voltage is 54.29 V, as shown in Fig. 11(b). The small difference of just 2.23 V confirms that the dc bus voltage ripple is significantly reduced due to the phase cancellation of these combined voltages. The proposed PR controller tightly tracks the reference signals, ensuring that no dc component is induced, which could otherwise cause drift in the SSBC output voltage. Thanks to the excellent performance of the PR controller, the dc bus voltage experiences a ripple of 4.25 V, as shown in Fig. 11(c). This corresponds to a 1.2% of the dc bus voltage, well below the dc bus voltage ripple of 3%, as explained in [36].

If electrolytic capacitors were used, the capacitance required would be approximately $C_{\text{dc}} = 320$ μF, for the same power rating and 1.2% dc bus ripple. This implementation would require four 100-μF/450-V electrolytic capacitors. However,

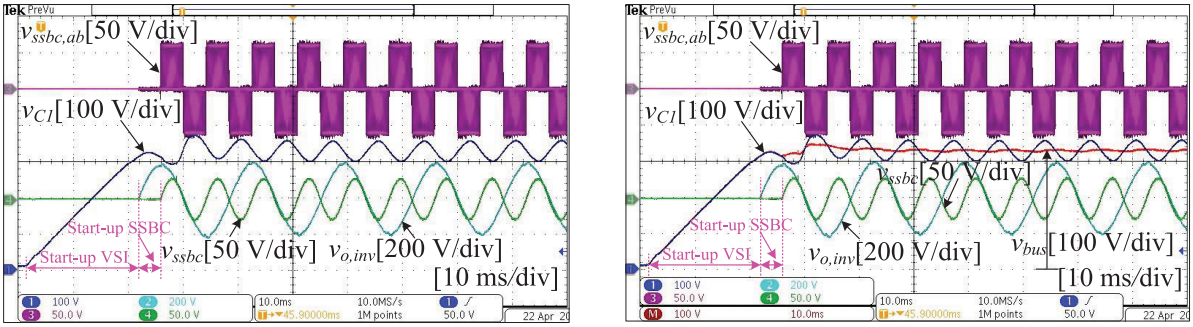

Fig. 14. Experimental waveforms of the proposed microinverter in start-up transient (a) switching node voltage of SSBC ($v_{\text{ssbc},ab}$), capacitor C_1 voltage (v_{C1}), output voltage of SSBC (v_{ssbc}), and inverter output voltage ($v_{o,\text{inv}}$), and (b) constant dc bus voltage (v_{bus}).

designers must consider the rms current rating, temperature rise limits, and the reduced lifetime of electrolytic capacitors in PV applications. This could lead to even a bulkier passive dc link solution.

Additionally, Fig. 12(a) presents the steady-state experimental results of the VSI filter inductor current i_{Lf} and the output voltage $v_{o,\text{inv}}$, while Fig. 12(b) shows the SSBC filter inductor current i_{buf} and the output voltage v_{ssbc}. The waveforms reveal that the frequency of i_{buf} and v_{ssbc} is twice that of i_{Lf} and $v_{o,\text{inv}}$. Also, i_{buf} corresponds to the current sourced and sunk by the SSBC to buffer the twice-line-frequency power ripple at the dc bus. The peak SSBC current is 200 mA, and the voltage stress is equal to the secondary isolated-port voltage of 60 V. As a result, the power processed by the SSBC is only a fraction of the total microinverter or PV module power rating.

The total harmonic distortion (THD) of the VSI output waveforms is experimentally measured using (22) and a Tektronix MDO3024 oscilloscope, yielding a THD value of 2.42%. The harmonic magnitudes up to the 10th order are normalized with respect to the fundamental component and plotted in Fig. 13

$$\text{THD} = \sqrt{\left(\frac{I_{\text{rms}}}{I_{1,\text{rms}}}\right)^2 - 1}. \tag{22}$$

B. Start-Up Transient Experimental Results

Fig. 14 presents the start-up experimental results of the proposed microinverter. Fig. 14(a) shows the switching node voltage of the SSBC $v_{\text{ssbc},ab}$, the capacitor C_1 voltage v_{C1}, the output voltage of the SSBC v_{ssbc}, and the inverter output voltage $v_{o,\text{inv}}$. Similarly, Fig. 14(b) displays the dc bus voltage v_{bus}, obtained using the oscilloscope's mathematical operation. The waveforms illustrate that the dc–dc converter, the dc–ac inverter, and the SSBC undergo a soft-start sequence. The startup is initiated by the subMICs microcontroller, followed by the main power stage microcontroller, as detailed in the next paragraph.

First, the IIBC is turned on in open loop with $D_b = 0.55$ to precharge the dc bus. Once the dc bus voltage reaches 120 V, an MPPT control loop is enabled to regulate the input voltage of the PV module. Second, the VSI modulation signal is synchronized with the reference signal once the dc bus voltage exceeds 300 V. As seen in Fig. 14(a) and (b), the VSI is activated a few milliseconds after the dc bus has reached the desired level, aligning with the start of its modulating signal cycle.

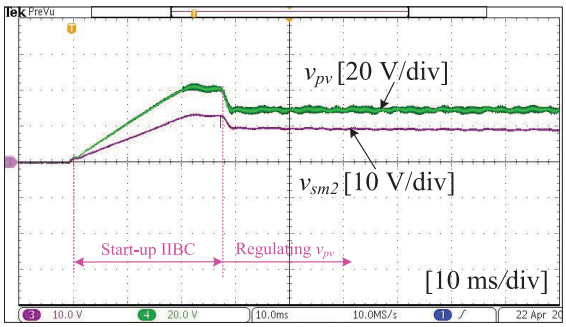

Fig. 15. Start-up transient experimental waveforms of the PV module voltage and the submodule 2 voltage (v_{pv} and v_{sm2}).

Third, the SSBC initially generates a zero vector using the inverse of the synchronization signal within the microcontroller to turn on switches Q_2 and Q_4, ensuring that its output remains at zero due to the shorted filter capacitor C_{bf}. This is evident in the waveforms of v_{ssbc} and $v_{\text{ssbc},ab}$ in Fig. 14, which remain at zero before the SSBC is turned on. During this brief period, C_1 temporarily acts as a conventional passive dc link. Shortly thereafter, the SSBC is synchronized with both its reference signal and the VSI synchronization signal. Once the SSBC is smoothly activated immediately after the VSI, the dc bus voltage stabilizes at a constant dc value, as shown in Fig. 14(b). These smooth transient waveforms highlight a well-coordinated soft-start sequence of each power stage in the proposed microinverter.

Similarly, Fig. 15 illustrates the start-up waveforms of the PV module input voltage v_{pv} and submodule 2 voltage v_{sm2}. The waveforms show that v_{pv} initially rises to the open-circuit voltage when the IIBC controller is inactive. Once the IIBC controller starts regulating the input voltage according to the reference generated by the MMPT block, v_{pv} closely tracks the reference and stabilizes at $V_{\text{pv}} = 30$ V. A similar behavior is observed for v_{sm2}, which is regulated to $V_{sm2} = 10$ V. The absence of ripple in the submodule voltage v_{sm2} demonstrates the excellent performance of the subMICs controller.

A picture of the hardware is depicted in Fig. 16, which shows a PV module along three current sources, IIBC, VSI,

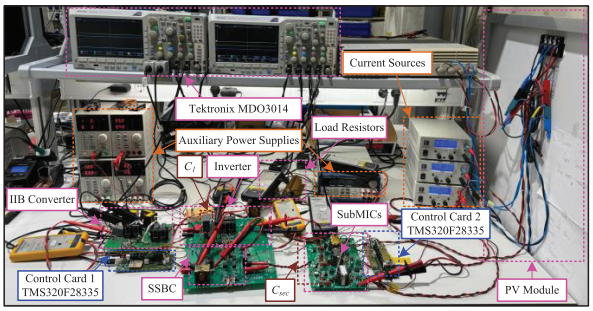

Fig. 16. Hardware prototype picture of the proposed microinverter.

SSBC, subMICs, and auxiliary power supplies. The part numbers of the prototype components are listed in Table III.

VI. Conclusion

This article has proposed a novel two-stage microinverter architecture that integrates subMICs with the SSBC for APD in PV applications. This novel integration introduces several key features in a two-stage microinverter, summarized as follows.

1) The integration of the SSBC for APD with the subMICs enables the well-regulated isolated-port capacitor C_{sec} to be used as an input energy port of the SSBC, eliminating a redundant capacitor and reducing the circuit cost.
2) The isolated-port voltage is well-regulated by subMICs; therefore, it eliminates the control loop previously adopted for the regulation of the SSBC input energy port, which makes the operation of the SSBC simple and robust.
3) The isolated-port voltage is dynamically adjusted based on power output of the PV module, reducing the voltage stress on the SSBC and enhancing its efficiency under varying environmental conditions.
4) A small-signal model and a fixed-frequency PR controller are proposed to tightly track the sinusoidal reference current, thereby effectively preventing dc offset in the SSBC output. This further simplifies the SSBC control implementation.
5) The SSBC enables the use of long-lifetime ceramic or film capacitors, enhancing microinverter reliability, while the subMICs mitigate submodule mismatch, improving PV module longevity—both functionalities are crucial for the commercial viability of residential microinverters.

The proposed microinverter was experimentally validated using a 180-W commercial PV module, achieving only 1.2% dc bus ripple with a 20-μF film capacitor.

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