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Organic Neuromorphic Circuits for Real-Time Biosignal Applications

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Organic neuromorphic circuits offer new opportunities for low-power, flexible electronics capable of real-time inference at the edge. In this work, we present a neuromorphic system based on organic thin-film transistors (OTFTs) that performs biosignal classification in a Bayesian framework. The spiking behavior of artificial OTFT neuron circuits are first characterized, showing how their dynamics can be tuned through circuit parameters. We then demonstrate how the circuits can infer information from real-world electroencephalography (EEG) data. When applied to epilepsy-related signal patterns, the system achieves excellent classification performance, while maintaining ultra-low power operation. These results highlight the potential of OTFT-based neuromorphic architectures for embedded medical diagnostics.

1. Introduction

Neuromorphic computing using organic materials has emerged as a promising platform for integration with biological systems.[1] Such materials can be integrated into soft, bendable and stretchable forms that can directly integrate with biology to enable sensing and making decisions. Current systems often integrate sensors into flexible substrates, but rely on traditional Si technology for light data preprocessing prior to sending information to external devices or the cloud for analysis.[2] Such architectures increase latency and raise privacy concerns. Inspired by the functioning of biological neural systems, the combination of neuromorphic concepts with organics can offer significant advantages in terms of energy efficiency, parallel processing, and real-time responsiveness, that can help overcome the inherent challenges due to speed and variability.

The most widely researched organic neuromorphic components are organic electrochemical transistors (OECTs).[3] The electrolytic gate, however, has potential drawbacks: its large capacitance can limit device speed and its relatively large gate current can increase power consumption. A possible alternative is organic thin film transistors (OTFTs) with organic dielectric gates and operation in the sub-threshold regime. These conditions offer potentially low power operation and compatibility with biological signals. Initial research investigating neuromorphic organic devices is promising,[4–6] but hampered by very low frequency response and significantly higher power consumption compared to oxide or Si technologies. Applications with OTFT neuron circuits for biosignals have not yet been considered.

Building on our prior simulation work,[7] we experimentally characterize and simulate Axon Hillock (AH) neuron circuits, depicted in **Figure 1a**, fabricated with printed OTFTs and demonstrate their application in biosignal processing. The devices were fabricated using the pilot line based on gravure printing at CEA-LITEN.[8] A fabricated circuit and a schematic of a single transistor is shown in Figure 1b,c. The AH circuit consists of a reset p-type OTFT and two inverters, each formed by a resistive load and a p-type OTFT. The transistor dimensions are chosen to be equivalent, thereby minimizing threshold voltage shifts associated with device scaling. Unlike more typical AH circuit implementations, which include a membrane capacitor extending from V_{mem} to ground, we deliberately exploit the intrinsic input capacitance of the first inverter, namely its gate and overlap capacitances, as the effective member capacitance C_m.[9] Extrinsic parasitic capacitances arising from pads, interconnects, the zero insertion force/flat flex cable (ZIF/FFC) and measurement fixtures

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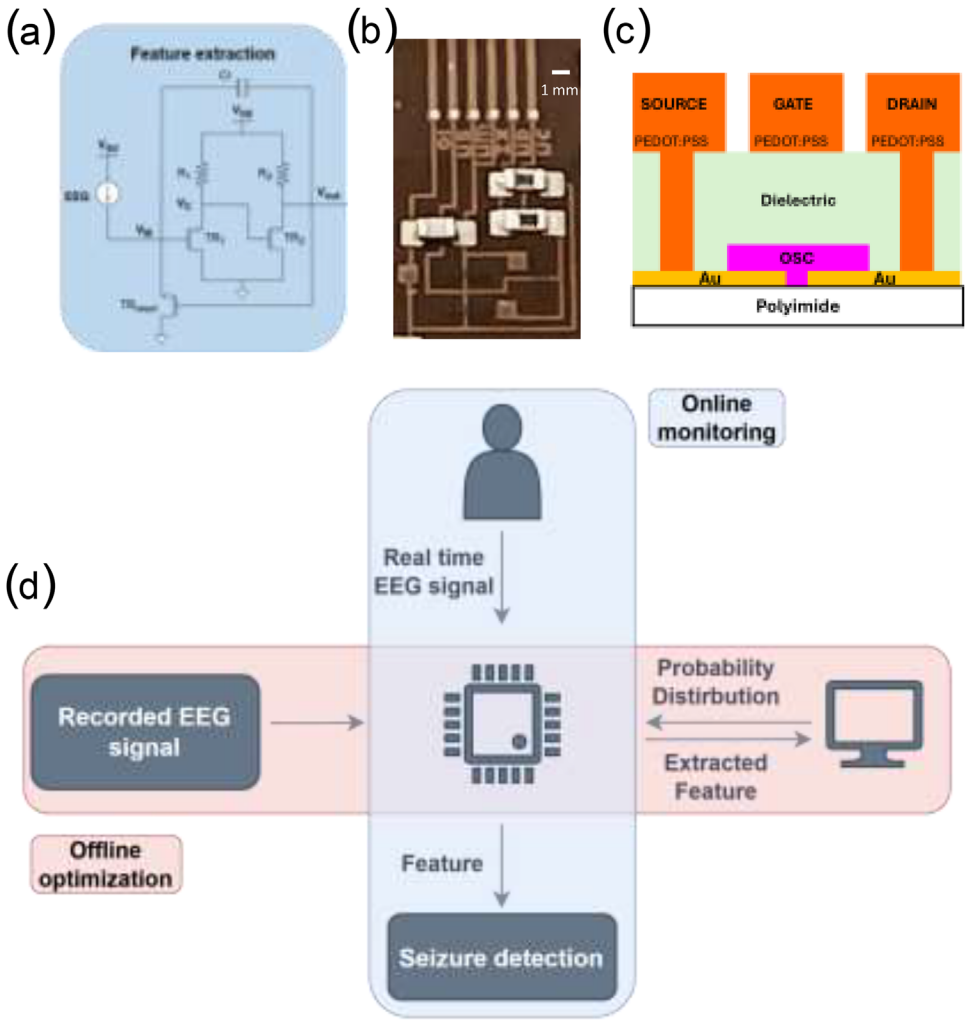


Figure 1. a) Schematic of the AH circuit used throughout the paper. b) Optical image of the realized circuit, c) Layout of OTFT transistor, further details of the materials and fabrication methods are provided in the methods section (OSC=organic semiconductor), d) Methodology of epileptic seizure detection.

are modeled separately as C_{ext}. This design enables a smaller circuit and increases energy efficiency. We use resistors instead of load transistors to improve circuit reliability by avoiding threshold voltage variability. Nevertheless, the load resistors are the primary source of power dissipation in the circuit. We therefore typically use 1 GΩ loads to limit static current ($P \approx V_{DD}^2/R$), and keep the power in the 100s nW range. The eventual implementation of a complementary circuit design could further minimize power consumption but was not available in the current large surface technology.

To show the circuit's utility for a practical biosignal task, we consider the detection of epileptic seizures. Figure 1d illustrates the overall methodology. The system operates in two stages: offline optimization and online monitoring. During the offline optimization, labeled prerecorded EEG signals are used to tune circuit parameters, notably the C_F and the conversion factor of the EEG voltage into input current (1 or 2×10^{-6} A mV^{-1}). This is analogous to the training phase of a supervised machine learning model. The online monitoring stage, equivalent to the test phase, then processes simulated real time EEG and determines whether a segment is a seizure or not.

The AH circuit is engineered so that non-seizure segments map to low spike-rates and seizure segments to higher spike-rates.[10] An additional post-neuron accumulator integrates output spikes on a capacitor C_A over an epoch length T_{epoch},. Brief high-amplitude signals that do not persist and signals that are too weak will not accumulate enough charge to trigger a decision. Only sustained spiking, as in seizures, will do so.

The voltage accumulated at C_A, denoted V_f for feature voltage, can be interpreted as the likelihood in a Bayesian framework. Bayes' rule states:

$$\mathrm{P}\ (\mathrm{C}|\mathrm{F}) = \frac{P\,(F|C)\,P\,(C)}{P\,(F)} \tag{1}$$

where $P(F|C)$ is the likelihood of observing a feature F of the EEG data for a category C, $P(C)$ is the prior probability of the category, and $P(F)$ is the marginal probability of the feature. A

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common method when in the presence of unbalanced classes, such as seizure detection, is to assume uniform priors to avoid biasing the classifier against rare events. Further, many hardware implementations of Bayesian inference neglect the normalization term, $P(F)$, because it is the same for all categories. Under these assumptions, classification can be performed directly on the likelihood. In our experimental implementation, we sum the spike voltages within an epoch, which is the discrete equivalent of the analog no-leak integrator. In simulations, we consider a full circuit where spikes accumulate on a downstream capacitor.

This framework allows us to extend these notions to include multiple features, which are also considered. Previous work has described related concepts as deterministic stochastic computing.[11] For clarity, we interpret this more broadly as *probabilistic computing*, that is, computing with probabilities, and specifically as *time-encoded probabilistic computing*. In our approach, spiking neurons generate time-encoded streams that represent probabilities. Two (or more) probability streams, each encoding as a spike train with rate $r_i \propto P(F_i|C)$, can be combined by a *coincidence accumulator*, consisting of an analog AND and a capacitor. The output integrates only overlapping events, yielding a signal $V_f \propto \prod_i P(F_i|C)$, under the assumption that the feature probabilities factorize independently given the class C. More generally, the same coincidence mechanism can be used to probe joint likelihoods, such as in our EEG example, where the accumulator estimates $P(F_1 \wedge F_2|C)$, the probability of both classes exhibiting coincident activity under class C.

To establish these concepts, we experimentally characterize printed OTFT Axon Hillock circuits and validate them through compact modeling and circuit simulation. We then demonstrate their utility in a biosignal task, showing that such circuits can implement probabilistic inference for seizure detection. These results motivate further exploration of printed neuromorphic circuits as building blocks for time-encoded probabilistic computing in biosignal applications.

2. Results

2.1. Characterization and Modeling of OTFTs

We fabricated and measured a series of AH circuits, each consisting of 3 transistors. In total 20 circuits with channel lengths ranging from 4 to 25 µm (1 mm width) were characterized but here we focus on one representative circuit with channel length of 10 µm. Each transistor was first measured individually, as described in the Methods and presented in Figure S1 and Table S1 (Supporting Information). **Figure** 2a,b shows sample electrical characteristics of the reset transistor in the AH circuit (Figure 1a). All transistors in the circuit exhibited hysteresis, resulting in a shift in the threshold voltage, V_{th}, and a change in the mobility.

The transistor data were fit to a compact model using the data taken at 1 NPLC (Number of Power Line Cycles), and a voltage step of 0.01 V. The OTFT model employs a DC and quasi-static charge model that solves Poisson's equation self-consistently, while also incorporating a hole transport model based on variable range hopping.[12] For each transistor we create two models, one to describe the forward sweep and a second for the reverse sweep. Sample fits are shown in Figure 2a,b. The fitting parameters reveal differences in the threshold voltages (V_{th}), leakage current (Ioff), and mobility. The parameters are then used to describe the device behavior in Verilog-A, enabling simulations of the circuits in Cadence Spectre (Cadence Design Systems, San Jose, CA, USA). The fitting parameters used in the simulations for this circuit are provided in Table S2 (Supporting Information) as well as for an additional AH circuit with 10 µm channel length. Table S3 (Supporting Information) provides a summary of the transistors' characteristics for both circuits.

We observe an important hysteresis in the sub-threshold characteristics and explore the variation with changes in step size and NPLC in Figure 2c–f. The hysteresis decreases with increasing step size and decreasing NPLC, as shown in greater detail in Table S3 (Supporting Information). Figure 2 shows that a change of V_{gs} of more than 3 V in 2 s (Figure 2e), would result in a hysteresis, whereas the same change in just 0.2 s (Figure 2f) would not. The measurements therefore suggest that the origin of the hysteresis is due to slow traps, and as previously analyzed in larger transistors sizes, present near the source/drain contacts.[7] Thus, if the output spikes from the AH circuit are sufficiently fast, the impact of hysteresis is likely to be minimal.

To explore this effect, we considered a series of measurements to understand the dependence on histroy. First measurements were performed following the order shown in Figure 2c–f and were subsequently repeated in reverse. Notably, the hysteresis observed in the final measurement condition (NPLC = 12) remained consistent with that of the initial measurement, demonstrating the reproducibility of the results (Figure S3, Supporting Information).

2.2. Circuit Characterization

Figure 3a presents the voltage transfer characteristics (VTC) of the first inverter, which has a transition voltage of ≈ −6.0 V. It also includes the fits to the compact model simulation for the reverse and forward sweeps. Due to the hysteresis of OTFTs, the threshold voltage and turn-on voltage depend on the sweep direction, which consequently affects the transition voltage of the inverter. The transition voltage increases during the reverse sweep by ∼1 V, which is consistent with the observed Vth shift (see Table S3, Supporting Information). Although TR_1 has twice the mobility of TR_2, hysteretic effects dominate so that the observed VTCs of the two inverters are very similar. In cascaded operation and for sufficiently fast switching, the lower-mobility transistor (TR_2) determines the overall response.

Experimental results of the AH circuit with 1 GΩ load resistors and a 1 pF C_F, operating at an I_{ex} of −1 nA is shown in Figure 3b. The measured firing rate is 1.3 Hz. The AH circuit was simulated using compact models fitted to each transistor in the circuit. Figure 3c shows the simulation result when an additional 20 pF parasitic capacitance was added to the simulation between the gate and source and gate and drain; while the intrinsic OTFT capacitance is only ≈ 0.2 pF, the larger value reflects extrinsic capacitance introduced by pads, interconnects, ZIF/FFC and measurement fixtures. We note that this contribution can be reduced by optimizing the experimental measurements.

The resulting firing rate closely matches the measured results, and the spike waveform exhibited a triangular shape, similar to

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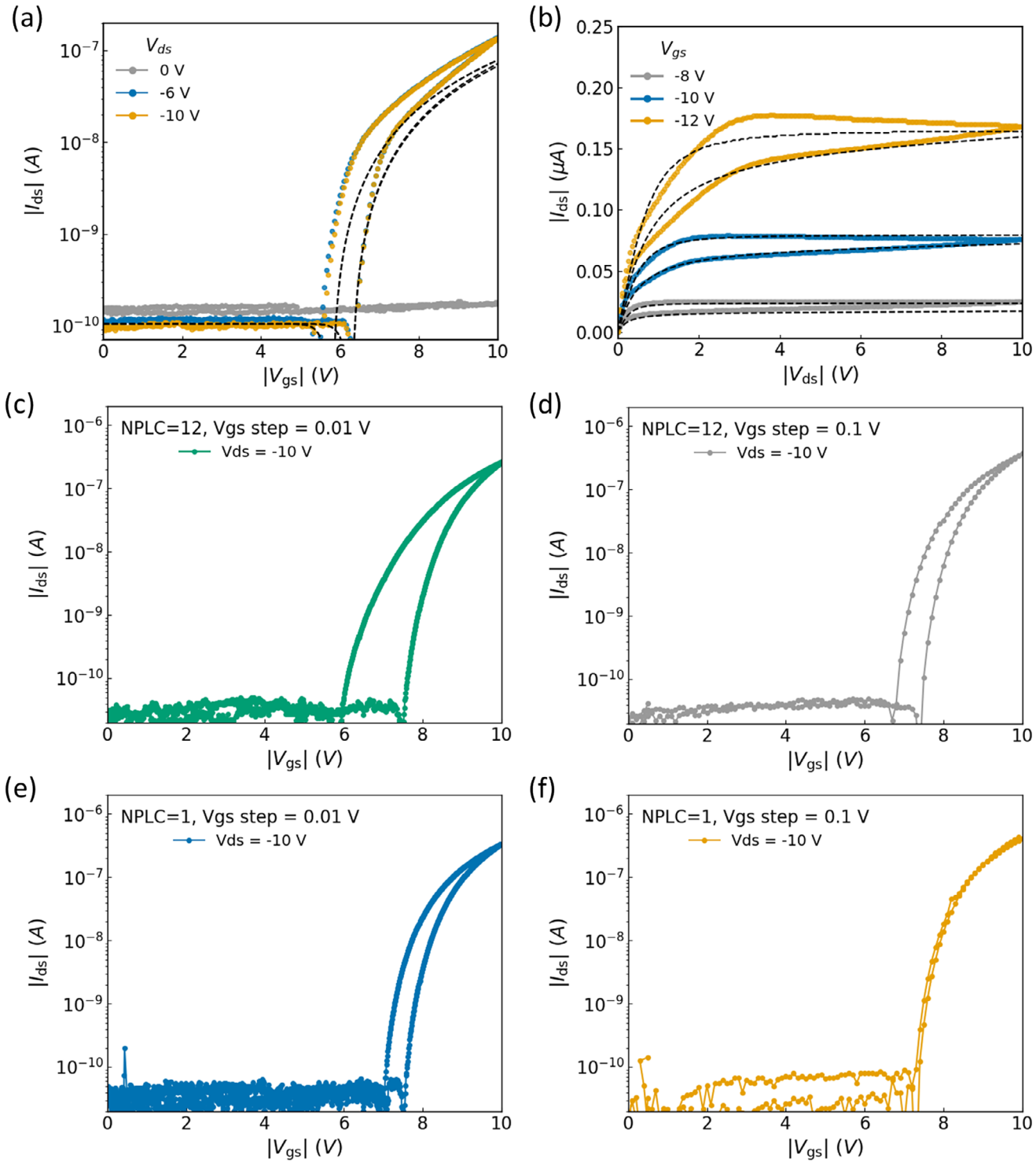


Figure 2. Measured (markers) and simulated (dashed black lines) a) transfer and b) output characteristics of the TR_{reset} in the AH circuit with a 10 µm channel-length OTFT. The limited separation between the $|I_{ds}|$ vs $|V_{gs}|$ curves at V_{ds} =−6 V and −10 V is attributed to series resistance as observed previously.[7] We include a representative $|I_g|$ trace (measured at V_{ds} = 0 V) to indicate gate-current levels; during acquisition we verified that $|I_g|$ did not increase appreciably with V_{ds} in this bias range (not shown). The data is fit to a compact model, shown in black solid lines. Hysteresis behavior of the TR_{reset} under the following measurement conditions: c) 12 NPLC, 0.01 V step size, d) 12 NPLC, 0.1 V step size, e) 1 NPLC, 0.01 V step size, and f) 1 NPLC, 0.1 V step size.

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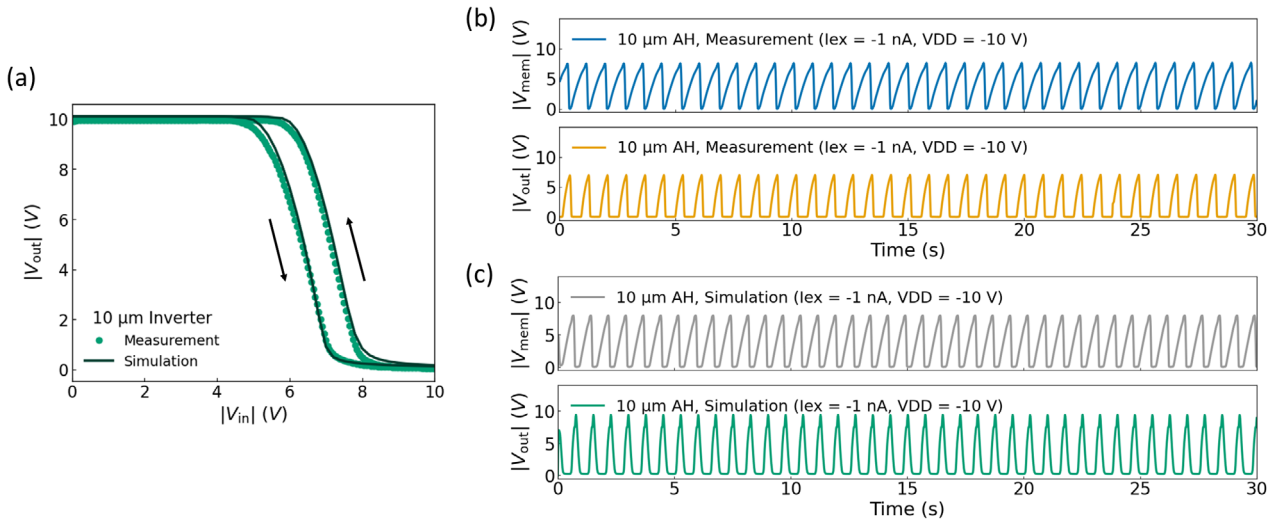


Figure 3. a) Voltage transfer characteristics (VTCs) of one of the inverters in the AH circuit under forward and reverse voltage sweeps with fitted compact model simulations. b) Measured time dependence of V_{mem} and V_{out} in a 10 µm channel length AH circuit with R1 = R2 = 1 GΩ, $V_{DD} = -10$ V, and under a constant input current of −1 nA. c) Simulated V_{mem} and V_{out} of a 10 µm channel length AH circuit under a constant input current of −1 nA and a parasitic capacitance of 20 pF.

the experimental observations. The firing rate is stable over time: across minute-scale recordings, but there is a variation due to the start of the measurement, found to be ≈ 0.05 Hz (1 GΩ load resistors, 1–2 Hz) and ≈ 0.5 Hz (60 MΩ load resistors, 10–20 Hz), i.e., ≈ 2.5–5% of the operating range. The firing rates are consistent for repeated sweeps hours apart (Figures S8, S9, Supporting Information). The slow firing rate, along with the triangular shape of the output waveform, can be attributed to a large external capacitance, which induces a significant RC delay. C_{ext} does not impact C_F because of the buffer circuit placed between V_{out} and the oscilloscope. This delay can be observed experimentally, shown in Figure S4 (Supporting Information), where the discharge of the C_F begins while V_{out} is still transitioning to a high state.

Gate leakage of the transistors can also modify the circuit behavior. Here, we observed gate leakage at $I_{ex} < 500$ pA. As shown in Figure S5 (Supporting Information), the large gate leakage in TR_1 prevents the return of V_{mem} to zero. Similar to the effect of the parasitic components, Vout consequently exhibits a triangular shape.

Figure 4a depicts the time-dependent response of the AH circuit. For the circuit with 1 GΩ load resistors, the non-linear firing rate is due to gate leakage at small I_{ex}. At high I_{ex}, saturation occurs due to C_{ext} that prevents the follower from discharging fast enough after each spike, as discussed above and seen in Figure S6 (Supporting Information). The effective I_{ex} range for firing is 10 nA.

To increase the firing rate, the load resistors were reduced to 60 MΩ (Figure 4b), enabling TR1 and TR2 to dominate over a wider voltage range. Theoretical considerations predict the observed linearity of the firing range, showing that the leakage current is no longer dominating the behavior. The effective I_{ex} range for firing is reduced to ≈ −6 nA but the frequency of the firing rate range is larger, extending from 2.5 to 20 Hz. Here the

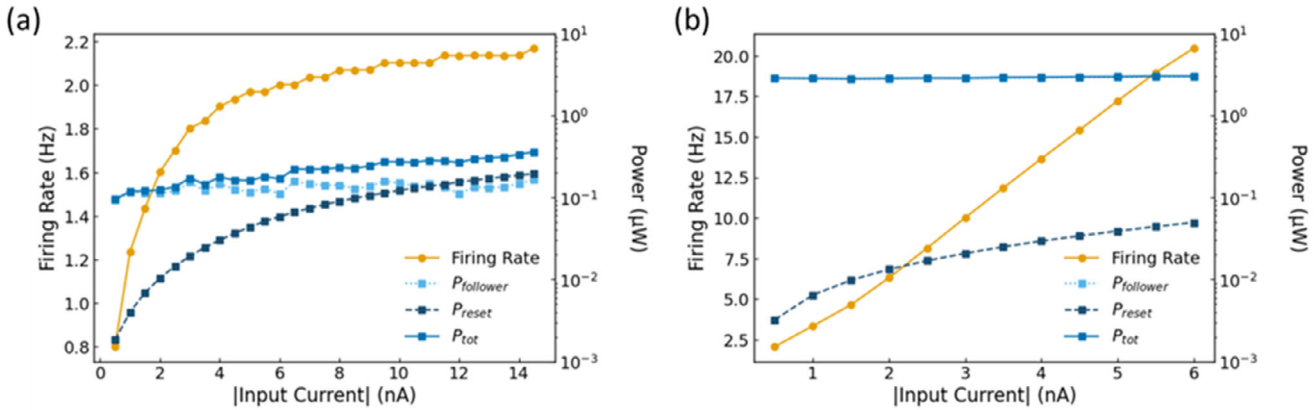


Figure 4. Firing rate and power consumption as functions of input current (I_ex) in AH circuits. As I_{ex} increases, the firing rate rises due to faster V_M charging, up to a limit where excessive current prevents proper reset. Power consumption is divided into $P_{follower}$, which remains relatively constant, and P_{reset}, which increases with firing rate. Results are shown for circuits with (a) 1 GΩ and (b) 60 MΩ resistors.

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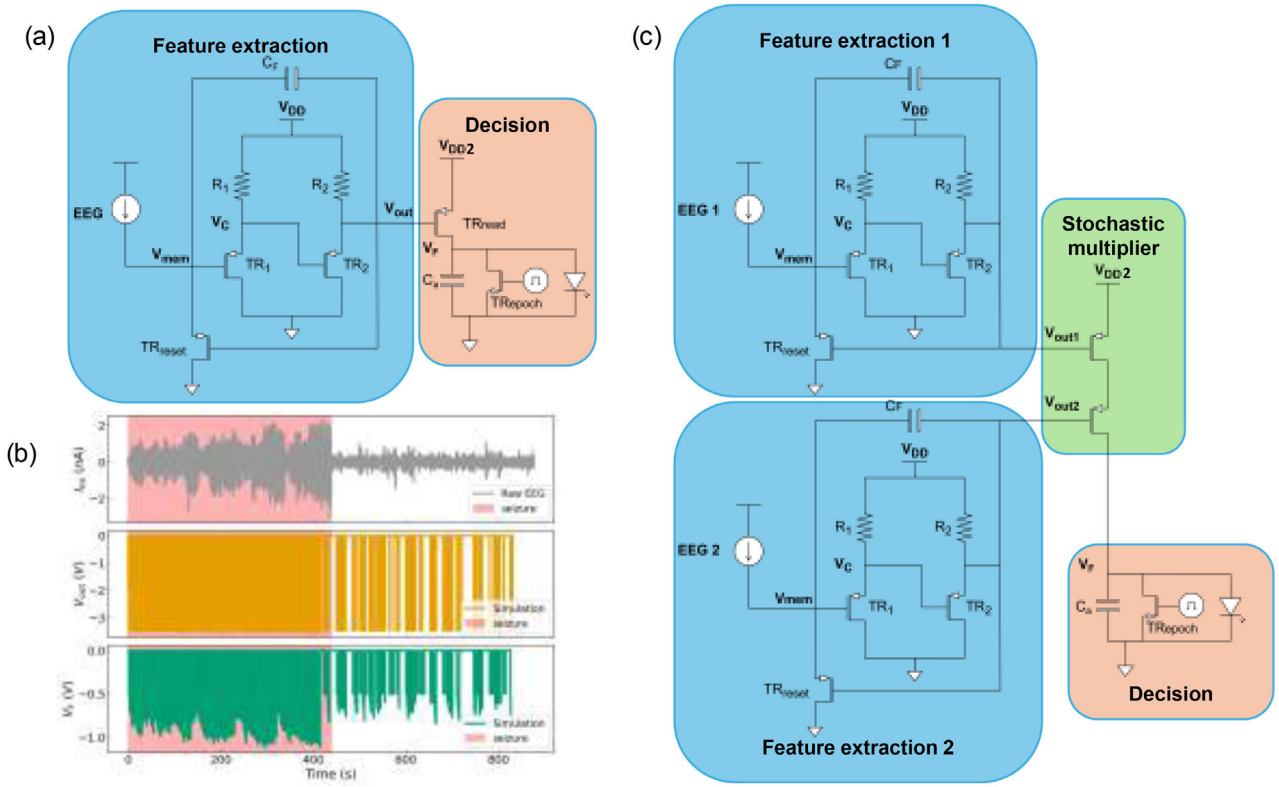


Figure 5. a) Circuit implementation of a single feature binary classification task, b) Sample EEG data from the EEG signal and simulations of the circuit output at Vout and Vf. Seizure data is indicated by the pink shaded background; c) Coincidence detection circuit to detect correlation between 2 EEG channels.

circuit stops firing for I_{ex} exceeding 6 nA because the voltage across the 60 MΩ resistors saturates, and the inverter cannot reset to trigger spiking. This could be remedied by increasing C_F.

We have quantified the firing rate stability by exploring how it changes over 30 seconds and how it changes when separated by several hours, shown in Figures S8 and S9 (Supporting Information). We find that the firing rate at the start of the current is slower (first 10s) by 2–5%, probably due to the response of the capacitors, and then stabilizes. After several hours we can reproduce the same curves.

The power consumption is also included in Figure 4. It consists of two components: that of the follower circuit ($P_{follower}$) and the reset transistor (P_{reset}) and is calculated using Equation (2). The total power consumption is dominated by $P_{follower}$, which remains nearly constant, dominated by the load transistor when an inverter is in the off state. In contrast, P_{reset} increases with firing rate, as it is proportional to the on-time of the reset transistor (TR_{reset}). Therefore, the more frequently the neuron fires, the higher the power consumed by the reset path. Under our measurement conditions, the total power consumption remains on the order of several hundred nW for the AH circuit with a 1 GΩ resistor, and a few μW for the configuration with a 1 MΩ resistor. Note that in Equation (1), P_{reset} is approximated as $I_{ex}V_{mem}$, which assumes the TR_{reset} is always on. However, in actual operation, TR_{reset} is activated only when the V_{out} exceeds a certain threshold. As a result, the actual power consumption is expected to be lower than the calculated value.

$$P \approx P_{follower} + P_{reset} \approx I_{DD}V_{DD} + I_{ex}V_{mem}$$

$$= \frac{V_{DD}^2}{\left(R_1 + R_{TR1}\left(V_{mem}\right)\right) \,||\, \left(R_2 + R_{TR2}\left(V_c\right)\right)} + I_{ex}V_{mem} \qquad (2)$$

2.3. Seizure Detection

We consider the use of the AH circuit for the classification of epilepsy using EEG data. We first simulate a full circuit implementation to demonstrate its viability and determine the necessary circuit parameters. **Figure** 5a shows the AH circuit connected to a decision circuit consisting of an OTFT and an accumulate capacitor C_a (10 pF) resulting in a VF that is proportional to the likelihood of the targeted feature, in the Bayesian sense (e.g., seizure activity). Concretely, during the initial training phase, C_F is chosen so that the spike rate of the AH circuit provides a measure of how probable it is that the observed EEG corresponds to that feature. The capacitor C_a is reset every epoch by a very slow additional counter neuron circuit that pulses at the end of each epoch.

The diode is included only to illustrate a possible hardware decision; it is not part of the circuit simulation. When V_F exceeds the turn-on voltage of the diode, the diode conducts,

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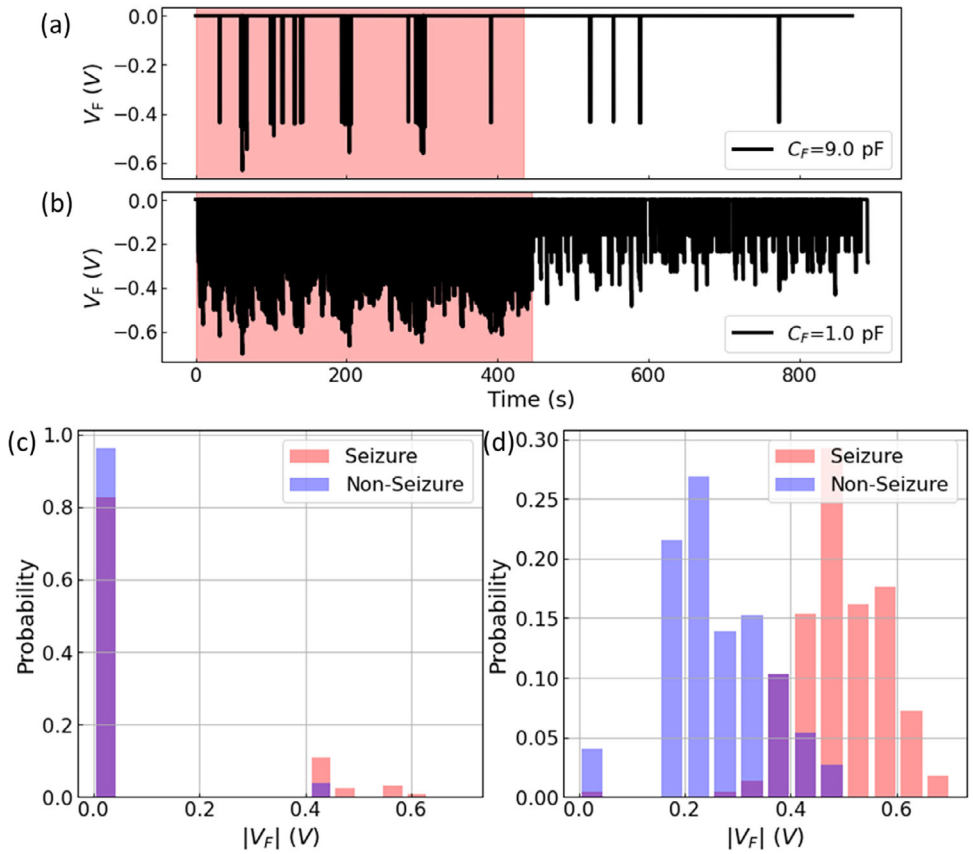


Figure 6. V_F versus EEG signal for a C_F of a) 9pF and b) 1 pF. Corresponding PD of seizure ($P(F|S)$) and non-seizure ($P(F|\bar{S})$) periods for C_F = 9pF c) with C_F = 1pF d).

providing a clear thresholded output that signals the presence of a seizure. This simple readout could, for example, monitor seizure episodes in infants or non-verbal patients with the illumination of an LED when a seizure is detected. For a wireless readout the diode output could instead modulate the impedance of a passive backscatter element (e.g. a Radio Frequency Identification(RFID) style antenna.[13] In this configuration, the output classification is encoded as a change in the reflected RF signal, enabling simple remote detection without active electronics. Importantly, this is not an amplitude threshold: the diode simply reports whether the epoch-averaged, rate-integrated decision variable V_F crosses a calibrated boundary, chosen in the offline stage to meet a desired sensitivity–specificity trade-off (e.g., fewer false positives or higher sensitivity).

We use labeled data from epileptic seizure EEG recordings from the publicly available Children's Hospital Boston dataset provided by PhysioNet.[14] We considered a single EEG channel for each of 24 cases, chosen by the highest potential for classification, as described in Section 5.4 and Section S4 (Supporting Information). Each one-hour EEG recording is segmented into 2s epochs (explained in Section S3, Supporting Information), and each epoch is labeled as either seizure or non-seizure, based on expert medical annotations. Initial explorations of the data determined the optimal circuit parameters.

We considered two circuit implementations. In the first, Figure 5a, the amplitude and rate of the most informative EEG channel activity of the single most informative EEG channel for each case were sufficient for classification. The rational here is that a seizure will incite larger brainwaves than a non-seizure and these should be detectable with our method. Sample input data and the simulated circuit response are depicted in Figure 5b. The pulse activity of Vout reflects characteristics of seizure (dense) or otherwise (sparse). The accumulator Ca sums these spikes over the epoch, yielding a smooth decision variable V_F that rises only with sustained activity and ignores brief excursions.

In the second method, we considered two EEG channels and target the correlation between them, capturing simultaneous large ampltudes of the two channels. We hypothesized that if seizure activity was located deep in the brain, larger amplitudes may not be visible on the scalp but correlations between nearby electrodes could be. Figure 5c shows how the latter can be realized in hardware. The coincidence accumulation of the two features uses an analog AND gate and a capacitor C_a, where charge accumulates by $\frac{Q_{spike}}{C_a}$ when both AH circuits emit spikes simultaneously.

Figure 6 illustrates the optimization for the circuit. The feature voltage (V_F), is extracted for different values of C_F, in Figure 6a, b and converted into probability distributions (PDs) in Figure 6c, d. The impact of changing C_F is clearly observable; when C_F = 9 pF a significant overlap exists between seizure and non-seizure

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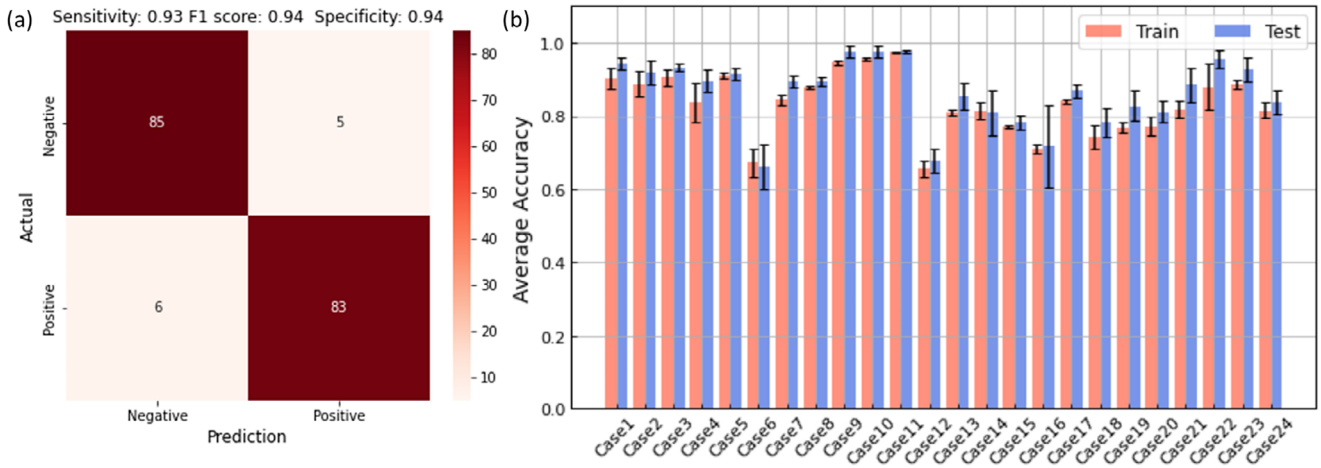


Figure 7. a) Confusion matrix for the test dataset of case 1. b) Average accuracy for training and test dataset for each case where bars correspond to the mean of five validation sets, and error bar is standard deviation.

PDs compared to when $C_F = 1$ pF. Once the optimal parameters are determined, an appropriate threshold for distinguishing seizure from non-seizure signals can be selected. For example, in Figure 6d, a threshold of approximately 0.4 V is suitable for classification.

2.4. Simulation Results

After the optimization process, seizure detection was performed for each case. We start with the simple single channel detection. To ensure robustness, the training datasets were balanced, and 5-fold cross-validation was employed, i.e., partitioning the dataset into five subsets, training on four and testing on the remaining one in turn, and then averaging all results. **Figure** 7a illustrates the detection for the test dataset of Case 1, which achieved the high performance metrics with a sensitivity of 0.93, F1 score of 0.94, and specificity of 0.94. For a more rigorous evaluation, Figure 7b presents the detection accuracy for all cases. The average train accuracy for all 24 cases was 0.833 ± 0.021. The average test accuracy was 0.864 ± 0.032.

Despite the high overall performance, certain cases, such as Cases 6, 12, and 16, showed relatively lower accuracy (< 0.75), suggesting that the second method might be beneficial. Nevertheless, the dataset, does not indicate information about the type of seizure so we cannot tell whether these cases are caused by a seizure deep in the brain, as was postulated for the second type of classification. We use the two most highly correlated EEG signals, as described in the Section S5 (Supporting Information).

We observed that correlated EEG channels were proximal but not necessarily the closest, indicating a likely dependence on the propagation of the seizure from deeper in the brain. **Figure** 8 illustrates the impact of using spike amplitude correlation of the two EEG channel on the detection performance. For these three cases, the specificity and overall accuracy metrics of the this classification consistently outperformed the single EEG classification.

2.5. Experimental Verification

We now verify experimentally the potential of the organic AH circuit to perform a classification. Since the circuit components

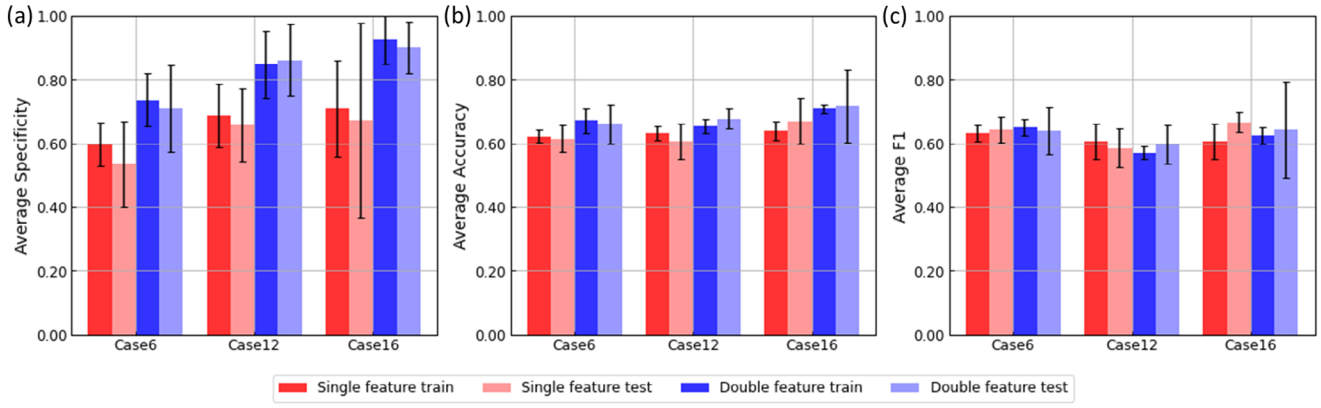


Figure 8. Detection accuracy of single EEG versus the two channel spike amplitude correlation classifications in terms of a) specificity, b) accuracy, and c) f1 score.

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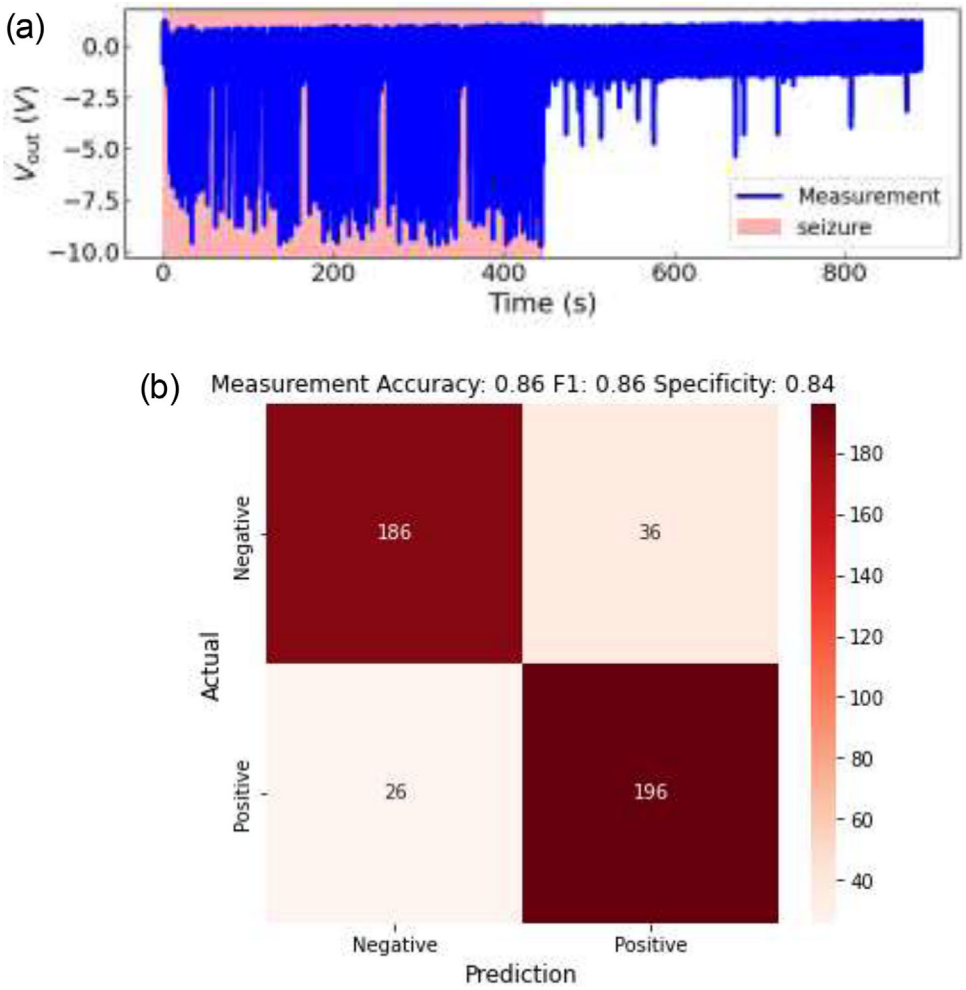


Figure 9. a) Experimental values of V_{out} from the AH circuit. The first half of the signals, with a pink background, consists of EEG seizure data and the other half non-seizure EEG data. b) Experimental classification result for case 1.

are fixed, the current levels were varied instead of C_F, (either 1 or 2×10^{-6} Amps/mV was used depending on the amplitude of the EEG case signal). While the sampling rate of the EEG data was 256 samples/s, the input data was reduced to 32 samples/s to accommodate the measurement capabilities and the speed of the circuit. VDD was set to −10 V, and the circuit was configured with R1 = R2 = 1 GΩ.

Figure 9a shows measurement results of V_{out} in response to sample EEG data. For signals corresponding to the seizure state, burst-like spiking activity was observed. During non-seizure EEG signals, however, the spikes failed to reach their full amplitude. This behavior originates from differences in the charging and discharging dynamics of V_{mem}. As discussed previously, when the charging current is insufficient, the rise in V_{out} is slow, preventing it from reaching the threshold required to activate the TR_{reset} As a result, V_{mem} is not fully discharged. Interestingly, this discrepancy is found to be beneficial for seizure detection. The circuit's sluggish response to low-amplitude inputs effectively filters out weak signals. Figure 9b shows the resulting experimental classification for case 1.

From these results, we can approximate the expected power consumption for a full circuit implementation. The most important component is due to the follower of the AH circuit. Additional power consumption in the decision circuit is expected to be ≈ 100 nW. Similarly, since the counter neuron has a slow spike rate, it is expected to consume less power than the feature selection circuit, and is also estimated to be ≈ 100 nW. For the classification part of the circuit, we thus find a power consumption of ≈ 500 nW. Nevertheless, the front-end electronics between the sensors and the classification circuit is necessary for a final circuit and is a burden for all such wearable systems. It is estimated to be ∼ 15 μW and would dominate compared to the power consumption of the classification.

2.6. Comparison with Software and Hardware

2.6.1. State-of-The-Art AI Algorithms

In this section, we compare our system with alternative software and hardware implementations. First, we compare the seizure

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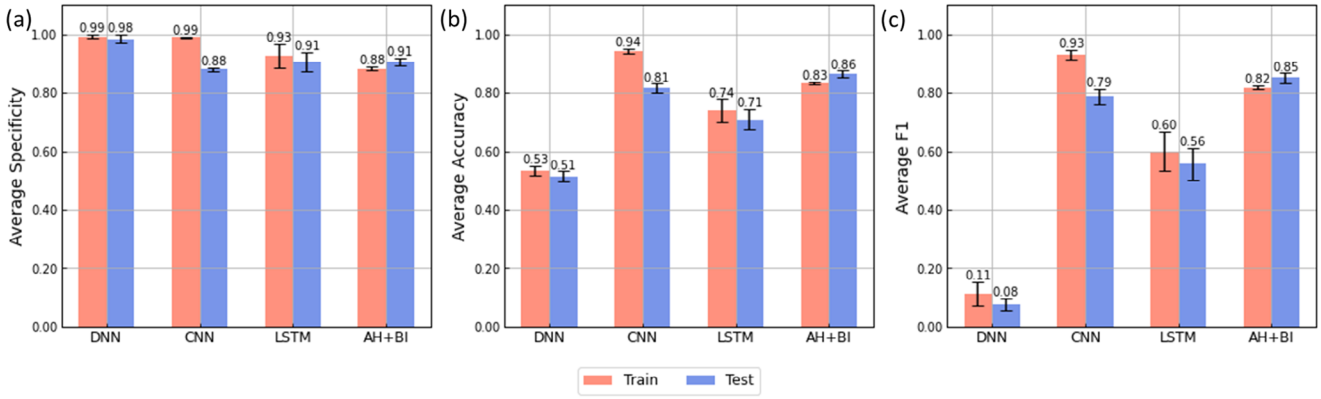


Figure 10. Comparison between epileptic seizure detection using our system (WH+BI) versus software AI algorithms for a) specificity, b) accuracy, and c) F1 score.

detection performance of our system (single EEG channel chosen to have the optimal information) against conventional AI models, including a Deep Neural Network, DNN, a Convolutional Neural Network, CNN, and Long Short-Term Memory, LSTM. The results are summarized in **Figure 10** and their implementation is described in more detail in the methods.

While the DNN model exhibits high specificity, indicating a strong capability to avoid false positives, its low overall accuracy and F1 score imply a high rate of false negatives and limited detection of true seizures. Aside from this anomalously high specificity in the DNN model, our system achieves the highest test accuracy across all evaluation metrics. This superior performance may be attributed to the explainability of our model, which is grounded in a simple, domain-informed hypothesis In essence, this method is able to extract more information from the same data than the AI algorithms. Notably, the software-based AI models appear to suffer from overfitting, likely due to their highly nonlinear architectures, which lack a solid physical or physiological basis. Interestingly, the CNN model outperforms both the DNN and LSTM models, which is somewhat unexpected given the temporal nature of EEG signals is traditionally well-suited to recurrent networks such as the LSTM.

The performance advantage of the CNN may stem from its structural resemblance to our hardware design. A 1D convolutional kernel in a CNN captures local temporal relationships between adjacent signal segments, which is analogous to the behavior of our circuit, where neighboring signals are accumulated and trigger spiking responses. In other words, the strong performance of the CNN may result from its structural alignment with domain-specific signal characteristics, similar to the probabilistic design implemented here.

2.6.2. Hardware

We compare our results with several recent approaches reported in the literature. This comparison is hindered by differences in benchmarks and the division of the data in the 3 other approaches. Nevertheless, we compare key performance indicators such as precision, sensitivity, specificity, power consumption, and explainability, along with patient applicability and hardware form factors. The results are summarized in **Table 1**. Note that the power consumption of our classification is negligible (1 orders of magnitude smaller) compared to the EEG front-end necessary to filter the signal from the EEG sensors that we have included in order to be comparable with the other works. In addition, our simulation accuracy indicates that the hardware can likely perform much better with an improved measurement setup that enables greater sampling rates.

3. Discussion

3.1. OTFT AH Circuits

The characterization and circuit modeling of the OTFT-based axon hillock (AH) neurons presented here offer insights into the practical implementation of organic spiking elements for neuromorphic applications. The compact model fit to the transistor data enabled circuit simulation in Cadence Spectre and reproduced the experimental behavior, underscoring the usefulness of this modeling approach for design and prediction. In particular, the ability to simulate forward and reverse sweeps separately provided a mechanism for understanding the impact of hysteresis on the circuit behavior.

Hysteresis in the OTFTs is present at slow bias sweeps, however, due to the comparatively abrupt changes in potential of the AH circuit, its manifestation is reduced. Its impact can be expected to be most significant at slower spiking rates, where the gate voltage evolves gradually and remains within the hysteresis window for extended periods. In this regime, hysteresis introduces a temporal dependence of the switching behavior of the inverters: the firing threshold becomes history-dependent, which can delay spiking or even inhibit it entirely if the membrane node does not charge or discharge sufficiently to overcome the altered threshold. However, in the current implementation, the effect of hysteresis appears to be minimal. This is attributed to the strong gate leakage at low I_{ex} in the first inverter stage, which dominates the voltage dynamics at the membrane node. As a result, the timing of spiking is governed primarily by the leakage current rather than the slow, history-dependent behavior typically associated with OTFT hysteresis. Consequently, the circuit operates in

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Table 1. Comparison with related work.[14,16] (–: not reported) The comparison includes the estimated front-end electronics, which dominates the number for the method reported here.

	Precision	Sensitivity	Specificity	False Alarm	Power	Method
This work	0.863	0.821	0.869	–	≈ 15 μW	Likelihood Estimation
Lin, S. K., et al [15] (2018)	0.926	–	–	0.527/h	55.89 mW	LDA
Zhan, T., et al [17] (2019)	–	0.925	0.801	–	110 μW	SVM

a regime where hysteresis plays a secondary role in setting the firing rate.

One challenges going forward is eliminating the external capacitance C_{ext}, (~pF), which induce significant RC delays and limit the firing rate and waveform shape. The consistency between simulated and experimental output waveforms, particularly the triangular spike profile and sub-Hz firing rates observed in high-resistance configurations, demonstrates that this parasitic component is the primary limitation on circuit speed. Based on our analysis of the circuit capacitance and the layout, we attribute Cext primarily to parasitic contributions from the measurement environment. Its elimination should enable higher firing rates in these devices while nevertheless keeping the power consumption the same due to the large resistive load of the followers. The observed saturation of firing rate with increasing excitation current is also directly linked to C_{ext}. As Iex increases, the follower transistor cannot discharge quickly enough between spikes, resulting in incomplete reset and loss of linearity in spike rate encoding. This effect has been confirmed both experimentally and through simulation and underscores the need to optimize possible parasitic components to extend the useful dynamic range.

Gate leakage effects, present at low excitation currents, were also found to distort Vout and introduce non-linearity in the firing rate. These effects were not present after the initial fabrication of the circuits. During the component assembly process, the OTFTs are subject to light, heat and oxygen, which can deteriorate their performance. It can thus likely be mitigated by adding an encapsulation. In addition, adjusting bias ranges and reducing resistor values can also provide a solution.

Despite these limitations, the ability to tune the firing rate by adjusting Cf, R1 and R2 demonstrates a pathway toward programmable temporal encoding. Transitioning from 1 GΩ to 60 MΩ load resistors allowed for a more extended dynamic range and linear response, with firing rates up to 20 Hz. This is a promising range for EEG-relevant signal processing and demonstrates that performance can be significantly improved by architectural choices without altering the active materials.

Importantly, the simulations not only reproduce circuit behavior but also support integration into larger probabilistic computing frameworks. In this context, the spiking output of the AH neuron can be interpreted as a time-encoded representation of a likelihood value, as used in maximum likelihood inference. The inclusion of power measurements shows that the neuron consumes sub-microwatt power in low-rate configurations, making it well suited for energy-constrained environments.

3.2. Classification Results

This work demonstrates the viability of organic AH circuits for implementing low-power, hardware-based biosignal classification using real-world data. The results illustrate how key circuit parameters such as Cf and the current levels strongly effect the classification performance, underscoring the importance of hardware-aware feature tuning. Additional modifications to the AH circuit can enable greater control of the feature selection. For instance, adding a leak transistor with an adjustable Vg in parallel with Iex. The input is then divided between the leakage transistor and the AH circuit, with the proportion of the input flowing through each path determined by the bias applied to the leakage transistor. As a result, this configuration raises the threshold at which the circuit begins to spike. By carefully adjusting the bias voltage, it is possible to control the firing in a way that neurons can spike preferentially for one class of data.

The probabilistic interpretation of the output voltage VF enables a maximum likelihood estimation, where optimal thresholds for distinguishing categories can be selected based on probability distributions derived from real EEG recordings. In this context, circuit behavior acts not only as a classifier but also as an analog preprocessor, inherently filtering signals through its integration and slow dynamical response. This dual role highlights the novelty of using a circuit to directly shape a probability distribution. This approach offers a promising path for probabilistic computing, with the potential to replace memory elements and significantly reduce implementation overhead.

Importantly, the simulations show that a single-feature classification strategy can be sufficient for many cases, achieving high average accuracy (0.86) across most patients. The improved accuracy for low performing cases that was seen with the coincidence implementation using two EEG channels, demonstrates how additional, weakly correlated features can enhance detection in ambiguous or difficult cases. This hardware-based implementation using a coincidence accumulator that is able to multiply probabilities aligns with Bayesian strategies for fusing evidence across modalities or signal sources.

Our experimental verification using fabricated OTFT-based AH circuits further confirms the ability of these systems to classify real EEG signals in a low-power regime. Although the devices operate at slow timescales, their sluggish response contributes to filtering out low-amplitude, non-seizure activity that can enhance the test accuracy. This phenomenon may be attributed to the explainability of our system, which stems from a well-founded hypothesis that EEG signals during seizure periods exhibit higher amplitude and frequency, leading to an increased firing rate. In addition, the system's explainability enables interpretability in decision confidence through the value of V_F. For example, as

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illustrated in Figure 6d, a V_F value of 0.6 suggests high confidence in classifying the epoch as a seizure period, whereas $V_F \approx 0.5$ indicates low confidence. Because of this knowledge, the threshold value fixed for a decision can be made based on specificity-sensitivity preference of the application.

Our system achieves a precision of 0.863, which is comparable to or slightly lower than[15] (0.926), yet higher than the results reported in[16] and,[17] which either do not report this metric or show inferior sensitivity. In terms of sensitivity, our approach (0.821) shows a balanced performance, below[16] (0.925) but significantly outperforming[17] (0.667), and superior to,[15] where the sensitivity is not reported. Importantly, our system achieves a specificity of 0.869 across all patients, whereas other methods are either limited to a few patients[15] or do not report this metric. This highlights the robustness and generalizability of our approach across patient variability.

Nevertheless, the main disadvantage of the technique is that it requires the tuning of circuit parameters to obtain the classification, and this can add significant challenges for more complex calculations. This adds setup time and can become challenging as systems scale to multiple features or classes because (i) the firing-rate map is sensitive to device variability and extrinsic capacitances, (ii) parameters interact non-linearly (changing voltages to currents, shifts the useful CF range and the optimal value for VF to make a decision), (iii) portability is limited—settings tuned on one subject/session may not transfer to another—and (iv) drift (temperature, humidity, aging) can move the operating point. In practice, many of these issues can be addressed by incorporating additional features into the circuit and will be explored in future work.

A significant advantage of our system is its ultra-low power consumption for the classification stage. The AH classifier itself consumes only ≈100s of nW, which is significantly less than other published classifiers[15] (55.89 mW),[16] (150 µW), and[17] (100 µW), For fairness, we note that additional the front-end circuitry (buffering, filtering and signal conversion from EEG voltage to current) is typically required, with an estimated consumption of ≈ 15 µW.[17] Ongoing work with OECT-based front ends aims to reduce this overhead.

The explainability of our methodology, which combines AH with a BI framework, is a distinct advantage over prior works based on black-box models such as LDA or SVMs, which lack interpretability. Additionally, our circuit is implemented on a flexible substrate, unlike the rigid form factors used in previous studies, further enhancing its applicability in soft bioelectronics systems.

4. Conclusion

Smart flexible devices that can monitor and interpret biosignals hold great promise for human health monitoring outside medical settings and significantly improving patient outcomes. Typical emerging devices currently focus on classifications on the cloud or edge devices based on well-established micron/nano fabrication techniques and von Neumann architectures. Our measurements demonstrate that OTFT-based spiking circuits can serve as low-power, probabilistic computing primitives. While the current design is constrained in speed and flexibility compared to digital or CMOS neuromorphic systems, its simplicity, low power, and compatibility with flexible substrates make it a compelling candidate for edge biomedical sensing platforms.

5. Experimental Section

Device Fabrication: The p-type OTFT transistors were realized using additive manufacturing techniques on the Pilot Line at CEA-LITEN.[18] The Au source/drain contacts consisted of 30 nm Au pads and are patterned by photolithography. They were subsequently functionalized with an self-assembled monolayer, pentafluorobenzene thiol dissolved in isopropanol and deposited by drop casting, to improve the injection from a work function point of view between the Au and the OSC. A 50 nm organic semiconductor (SP500 Lisicon polymer from Flexenable mobility of ≈2 $cm^2\ V\ s^{-1}$) and a 946 nm thick gate dielectric (Flexenable D320, dielectric constant of 2.2) were gravure printed. Interconnections between the source/drain and gate were achieved using vias. The vias are patterned by design, meaning that the layout of the dielectric layer included holes/areas where no dielectric will be deposited. The top gate electrode consisted of a screen printed conductive ink of PEDOT:PSS. Initial layouts of the axon-hillock circuit are 4 mm x 4 mm in size and include two discrete resistors and 1 discrete capacitor. With $\varepsilon_r \approx 2$, $t = 1$ µm, the inverter input intrinsic capacitance was estimated to be:

$$C_{mem} \approx C_{ch} + C_{ov,SG} + C_{ov,DG} \approx 0.18 + 0.18 + 0.18 \approx 0.54\,pF \quad (3)$$

where C_{ch} was the channel capacitance (W × L = 1 mm × 10 µm), and $C_{ov,XG}$ were the overlap of the source/drain-to-gate overlap capacitance arising from the PEDOT:PSS contact overlap over the gate dielectric (see Figure 1c for clarification for the device geometry).

The circuits were left in ambient conditions, and the discrete components were assembled using a silver-based epoxy glue and pick-and-place machine. Initial characterizations of the transistors prior to this assembly showed transistor thresholds around −3 V, as reported previously, and very low gate leakage currents (<1 pA).[7] Optimization of the assembly and encapsulation of the circuits are likely to improve the degradation and improve circuit performance in future fabrication.

For each transistor channel length in 5, 10, 15, 20, 25 µm, two circuits were fabricated and measured. We found that the 5 and 20 µm channel length circuits did not exhibit spiking, most likely because of large variations in V_{th}. The 10, 15, and 25 µm channel length circuits showed consistent spiking, with the firing rate decreasing for longer L and the effect of C_{ext} becoming less pronounced due the increase in C_{ch}. More detailed characterization of these devices will be reported in a separate study.

Simulation Parameters: The compact model was based on a DC and quasi-static charge model.[19] It solves Poisson's equation self-consistently using an appropriate density of states and a hole transport model based on variable range hopping. The ≈20 parameters for the model are found for each transistor based on the experimental data. The model does not directly account for the hysteresis. The challenge when fitting the model in its presence was that currents in the I_d -V_{ds} characteristics were often not consistent with the currents in the I_d -V_g characteristics at the same biasing conditions. To accommodate this, fits focused on matching the output characteristics as these were what were the most important for the AH circuits. The parameter extraction and fitting were done in *Matlab* (MathWorks, Natick, MA, USA) and the extracted parameters and final model were put into a Verilog-A code for simulations in *Cadence Spectre*.

To realize the classification in the OTFT technology, we used the following simulation parameters. The models were based on compact models developed for the individual transistors[12] and the forward hysteresis models were used. The transistors were taken to be 10 µm and assumed to be identical. The V_{dd} was −5 V and V_{dd2} was −4 V. The square wave voltage applied to reset the epochs consisted of a −5 V signal and a period of 2s. The duration of the reset pulse was 50 ns. In an experimental demonstration, the reset pulse duration was too fast and the epoch time and reset pulse would have to be revisited.

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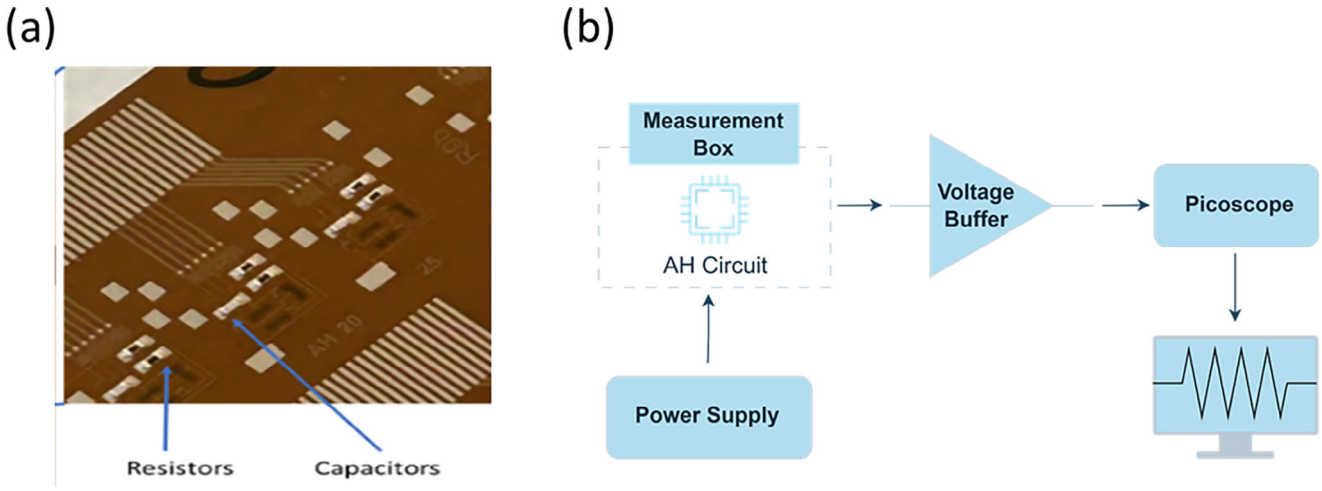


Figure 11. a) Photograph of AH circuits and b) experimental setup for measuring time-dependent response of AH circuits.

Experimental Setup: The electrical setup for measuring the AH circuits is illustrated in **Figure 11**. The AH circuit was placed inside a light-shielded box to eliminate undesired photo-induced effects on the organic materials. The circuit was connected to an external source measurement unit (SMU) via a ZIF connector inside the box. A Keithley 2636A System SourceMeter (Tektronix, Beaverton, OR, USA) was used to apply the required voltage and current to the circuit. The output signal from the AH circuit was then monitored through a voltage buffer amplifier (LMC6001) and recorded using a PicoScope 4000-series PC-based oscilloscope (Pico Technology, St Neots, UK).

To characterize each transistor in the AH circuits, voltages were applied to V_{mem}, V_c, V_{out}, and V_{DD}, and the transfer (I_{ds}–V_{gs}) and output (I_{ds}–V_{ds}) characteristics of the OTFTs were measured, as indicated in Figure S1 and Table S1 (Supporting Information). For TR_{reset}, characterization was performed by applying 0 V to V_c and V_{DD} while sweeping V_{mem} (as V_{ds}) and V_{out} (as V_{gs}). Similarly, TR_1 and TR_2 were characterized by applying 0 V to V_{out} and V_{DD} for TR_1, and to V_{DD} and V_{mem} for TR_2. Then, V_c (V_{ds}) and V_{mem} (V_{gs}) were swept for TR_1, and V_{out} (V_{ds}) and V_c (V_{gs}) for TR_2. Since the drain terminals of TR_1 and TR_2 were connected to resistors R_1 and R_2, respectively, the measured current includes the current flowing through these resistors (I_{R1}, I_{R2}). Therefore, to accurately determine the current flowing through the transistors, the current measured at I_c and I_{out} was compensated by subtracting the corresponding resistor currents, after first experimentally verifying them.

EEG Channel Selection: To evaluate and optimize our system, we use epileptic seizure EEG recordings from the publicly available Children's Hospital Boston dataset provided by PhysioNet.[14] This dataset includes EEG recordings of 22 patients with diverse ages and gender distributions, ensuring a representative sample of seizure patterns. In some cases, EEGs were recorded from the same patient at different ages, resulting in a total of 24 distinct cases. Each recording includes multiple EEG channels corresponding to different electrode placements on the scalp.

To design a compact and energy-efficient monitoring system, we perform channel selection to reduce the number of required transistors. Prior to channel importance analysis, all signals undergo a preprocessing step to eliminate irrelevant or noisy data. First, signals outside of the frequency range of 0 to 30 Hz are filtered out, as this range encompasses the major EEG bands such as Delta, Theta, Alpha, and Beta.[20] Next, each one-hour EEG recording was segmented into two second epochs, and each epoch was labeled as either seizure or non-seizure, based on expert medical annotations. For each epoch, two time-domain features were extracted from every channel like the number of peaks and average interval between the peaks. These features were chosen based on clinical observations that EEG signals typically exhibit burst activity during seizures, making them suitable for seizure characterization.

The correlation between these extracted features were then calculated and the seizure labels to determine the relative importance of each channel. This analysis helps identify the most informative channels for seizure detection, enabling to minimize circuit complexity while maintaining high classification accuracy. The complete details as to how this was accomplished was provided in Section S2 (Supporting Information).

Seizure Detection: Seizure detection performance was evaluated on a case-by-case basis. Twenty-four individual systems were individually trained, each tailored to the specific EEG characteristics. To ensure robustness, the training datasets are balanced, and 5-fold cross-validation was employed. Detection performance was quantified using the standard metrics: F1 score, precision, recall, specificity and accuracy.

For the experimental measurements, the data was divided in the following way. During the first 446 seconds, EEG data corresponding to the seizure state was applied, followed by non-seizure EEG signals for the remaining time. As a result, 223 values of V_F are obtained for each state. These V_F values are sorted according to their labels and voltage ranges, forming a Gaussian-like distribution. By normalizing the counts with the total number of epochs in each state, the corresponding PDs are derived.

Comparison Algorithms: To evaluate the detection capability of our system, we implement and compare three AI-based models: deep neural network (DNN), long-short term memory (LSTM) network, and convolutional neural network (CNN). Each model was designed to detect epileptic seizures on a per-time-window basis. To ensure fair comparison and robust evaluation, all models are trained and tested using the same EEG dataset, which contains an equal number of seizure and non-seizure segments. Due to the relatively limited number of seizure epochs, the training dataset was relatively small, making these data-driven models susceptible to overfitting. To mitigate this issue, dropout layers are incorporated into each network, and early stopping was applied during training. Consistent with the neuromorphic LIF-based system, we perform 5-fold cross-validation by dividing the dataset into five subsets.

The DNN consists of two hidden layers, each with 64 neurons, using a linear transformation followed by a leaky Rectified Linear Unit (ReLU) activation and dropout for regularization.

The 1D CNN comprises two convolutional layers: the first maps the input to 32 feature maps using a kernel size of 3 with padding, and the second increases the feature dimension to 64. Each convolutional layer was followed by ReLU activation and max pooling with a pool size of 2, effectively reducing the temporal resolution. A dropout layer with a rate of 0.5 was applied before passing the flattened output through two fully connected layers (128 units and 1 output unit). This architecture was suitable for binary classification of 1D signals.

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The LSTM model includes a single-layer LSTM with 16 hidden units, designed to process sequential data with an input size of 80. The output at the final time step was passed through a fully connected layer with 32 units and ReLU activation, followed by a final linear layer and a sigmoid function to produce a binary classification output. No dropout was applied in the LSTM.

All input data were normalized using min-max normalization. The dataset was divided into 5 subsets for cross-validation (4 for training, 1 for testing). Each model was trained using the AdamW optimizer with a learning rate of 1e-4. Training was terminated either when the maximum number of epochs (250) was reached or when early stopping criteria were met. The best-performing model (based on validation performance) was saved. A total of 24 models were trained, one for each independent case.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

artificial neuron circuits, circuit simulations, organic electronics, probabilistic computation

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