Loss-Free Resistors: An Alternative to Passive Damping in Power Topologies

M. Sebastià-Rullo, A. Cid-Pastor, *Member, IEEE*, H. Valderrama-Blavi, *Member*, *IEEE,*
A. El Aroudi, *Senior Member*, *IEEE* and L. Martínez-Salamero, *Life Senior Member*, *IEEE*

***Abstract*— This paper presents a systematic procedure based on the use of loss-free resistors (LFRs) to design active dampers for power converters with constant power load (CPL) in multi-bus power distribution systems. The proposed method is founded on the transformation of classical passive dampers into active ones by substituting their passive resistor by the emulated resistor of the LFR. The new active dampers preserve the dynamic behavior of the original passive networks without their power losses, because the power required for stabilization is recycled through the LFR to other uses in a multi-bus system. Considering the minimum power required for stabilization and the minimum increment of dynamic order after the LFR transformation, one passive network is selected out of five potential candidates and subsequently converted into an LFR-based active damper. The new active damper is used to stabilize the open-loop boost converter supplying a CPL and operating in continuous conduction mode. The LFR-based damper is also implemented by a boost converter that interfaces the input mesh of the main bus through a high-frequency transformer and a full-bridge rectifier. The stabilization power required by the main boost converter is reinjected into a DC load of the secondary boost converter. Theoretical predictions are verified by PSIM simulations and experiments in a prototype handling an input power of 200 W and using 6 W of that power for stabilization and recycling.**

***Index Terms*—Stability, constant power load, active damping, loss-free resistor, converters interconnection, multi-bus systems.**

I. INTRODUCTION

MULTI-CONVERTER systems are nowadays omnipresent in the electrical architecture of many power processing networks such as microgrids for renewable energy, powertrains in electric vehicles or power supplies for telecommunications. In such systems, switching power converters exchange energy through distribution buses acting either as sources when they transfer energy or as loads when they receive energy. The latter converters can behave as power sinks when they absorb constant power, which originates the notion of constant power load (CPL) [1].

CPL regime in power converters operating in continuous conduction mode (CCM) is inherently unstable [2], and therefore such converters must operate in closed-loop with an appropriate control strategy. This can be either of linear type, such as current control [3], or nonlinear, like boundary control [4] or sliding-mode control [5].

To reinforce the stability of the closed-loop system, passive or active damping is added to the converter. The insertion of active damping is carried out by the control system in some cases [6]–[11] or by the inclusion of an ad hoc one-port device that modifies the system topology [12]–[13]. The main purpose of this additional damping stage is to stabilize the open-loop operation of a power converter. In this work, the approach is applied to a boost converter loaded with a CPL, which is known to exhibit open-loop instability. This allows the control efforts to focus on providing other functionalities within an already stable system, which becomes easier to control by using well-known frequency-domain criteria such as desired bandwidth and phase margin.

In this context of topology modification, a two-port active damper was successfully implemented in [14] using the notion of loss-free resistor (LFR). This two-port damper exhibits a virtual resistor with emulated resistance R_d at the input port, ensuring proportionality between the input voltage v_{Rd} and input current i_{Rd}. The output port of the damper is a power source P_o, which ideally supplies a secondary bus v_{bus} with all the power absorbed by the input port P_i (Fig. 1a). As illustrated in Fig. 1b, the virtual resistor of the LFR is inserted in series with the input inductor to stabilize the open-loop boost converter loaded by a CPL with power P_{CPL}. The energy employed in the stabilization is recycled to a secondary bus of

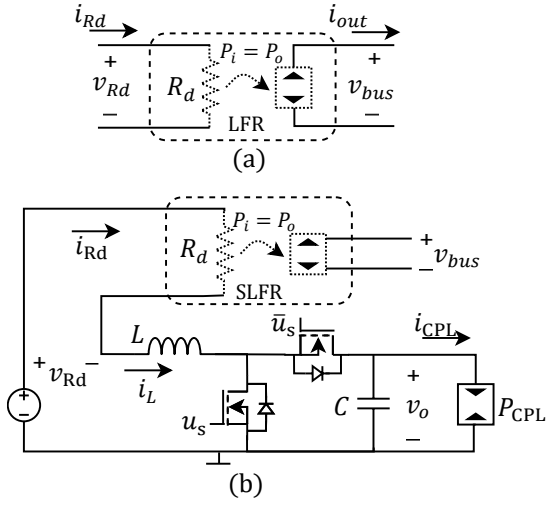

Fig. 1. (a) LFR model (b) Series connection of the LFR and the boost converter in the input port and reinjection of energy to a secondary bus.

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The authors are with the Department of Electrical, Electronic and Automatic Control Engineering, Rovira i Virgili University, 43007 Tarragona, Spain (e-mail: max.sebastia@urv.cat; angel.cid@urv.cat; hugo.valderrama@urv.cat; abdelali.elaroudi@urv.cat; luis.martined@urv.cat).

the multi-converter-system.

Since the virtual resistor was connected in series with the inductor of the boost converter the resulting damper was denominated series loss-free resistor (SLFR). Note that the latter SLFR shares the name with a different topology whose virtual resistance is connected in series between the input and output ports of a power stage, and its power source is connected in parallel with the external voltage source. That topology is implemented using a power converter operating in discontinuous conduction mode (DCM) and has been used to compensate losses in the activation circuitry of the power devices of a push-pull converter [15] and in the investigation of the charge conservation in the connection by an LFR of two identical capacitors with unequal initial charges [16].

The proposed method broadens the scope of [14], which utilized a single resistor connected in series with the inductor L, by extending the procedure to the rest of the passive dampers traditionally employed for stabilizing power converters with either resistive load [17]–[18] or a CPL [19].

Specifically, in this paper, we propose replacing the resistive element R_d in every of the five passive networks depicted in Fig. 2 with the virtual resistor of the LFR in order to reinject the absorbed energy to a secondary bus v_{bus}.

The rest of the paper is organized as follows. The steady-state and stability analyses of each damper in Fig. 2 are addressed in Section II. The topology selection for the best stabilizing LFR is carried out in Section III. The design of the LFR active damper based on the selected topology is studied in Section IV. Next, a control strategy for the stabilizer is proposed and verified through stability analysis in Section V. Theoretical predictions are validated through numerical simulations using the switched model presented in Section VI, and subsequently confirmed by experimental results obtained from a laboratory prototype described in Section VII. Section VIII discusses the scalability of the proposed method, and finally, Section IX summarizes the conclusions and outlines potential directions for future research.

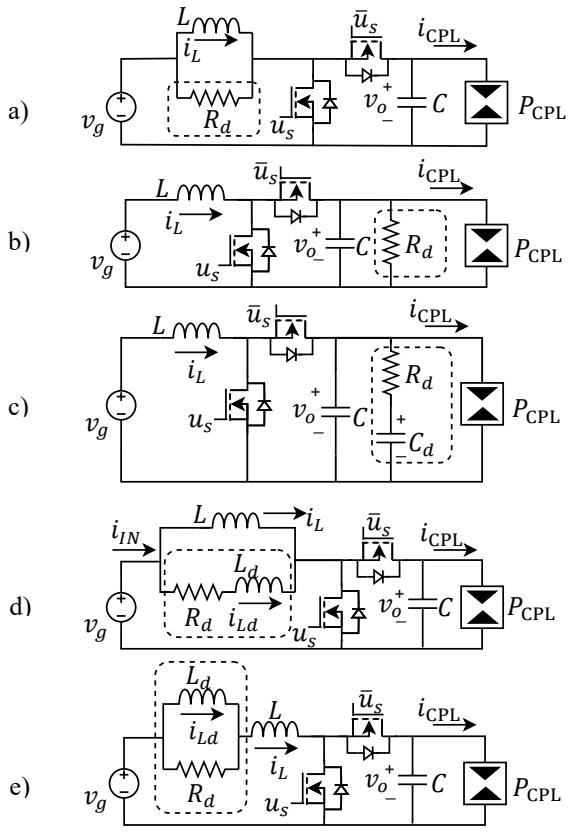

Fig. 2. Passive dampers integrated in a boost converter supplying a CPL. (a) R_d in parallel with L (b) R_d in parallel with C (c) R_d-C_d in parallel with C (d) R_d-L_d in parallel with L (e) R_d//L_d in series with L.

TABLE I

STABILITY MARGIN AND REQUIRED POWER FOR STABILIZATION OF THE PROPOSED TOPOLOGIES

Topology	Characteristic Polynomial	Stability Margin	Minimum Dissipated Power
R_d in parallel with L	$s^2+\left(\frac{1-D}{R_dC}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)s+\frac{(1-D)^2}{LC}$	$0<R_d<\frac{V_o^2(1-D)}{P_{\mathrm{CPL}}}$	$D\cdot P_{\mathrm{CPL}}$
R_d in parallel with C	$s^2+\left(\frac{1}{CR_d}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)s+\frac{(1-D)^2}{LC}$	$0<R_d<\frac{V_o^2}{P_{\mathrm{CPL}}}$	P_{CPL}
R_d-C_d in parallel with C	$s^3+\left(\frac{C+C_d}{CC_dR_d}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)s^2+\left(\frac{D'^2}{CL}-\frac{P_{\mathrm{CPL}}}{V_o^2CC_dR_d}\right)s+\frac{D'^2}{R_dLCC_d}$	$R_d<\frac{V_o^2(1+N_C)}{P_{\mathrm{CPL}}N_C}$ $\frac{1}{C}\left(\frac{(1+N_C)}{N_CR_d}-\frac{P_{\mathrm{CPL}}}{V_o^2}\right)\left(N_CCR_d-\frac{P_{\mathrm{CPL}}\mathrm{L}}{V_o^2D'^2}\right)>1$	$\frac{\left(\frac{T_sDP_{\mathrm{CPL}}}{2V_oC}\right)^2}{3R_d}$
R_d-L_d in parallel with L	$s^3+\left(\frac{R_d}{L_d}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)s^2+\left(\frac{D'^2(L_d+L)}{CL_dL}-\frac{P_{\mathrm{CPL}}R_d}{V_o^2CL_d}\right)s+\frac{R_dD'^2}{L_dLC}$	$R_d>\frac{LN_LP_{\mathrm{CPL}}}{CV_o^2}$ $L\left(\frac{R_d}{N_LL}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)\left(\frac{N_L+1}{R_d}-\frac{P_{\mathrm{CPL}}}{V_o^2D'^2}\right)>1$	$\frac{R_d\left(\frac{T_sDV_g}{2L_d}\right)^2}{3}$
R_d//L_d in series with L	$s^3+\left(\frac{R_d(L_d+L)}{L_dL}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)s^2+\left(\frac{D'^2}{LC}-\frac{R_dP_{\mathrm{CPL}}(L_d+L)}{L_dLV_o^2C}\right)s+\frac{R_dD'^2}{L_dLC}$	$R_d>\frac{P_{\mathrm{CPL}}LN_L}{CV_o^2(1+N_L)}$ $L\left(\frac{R_d(1+N_L)}{N_LL}-\frac{P_{\mathrm{CPL}}}{V_o^2C}\right)\left(\frac{N_L}{R_d}-\frac{P_{\mathrm{CPL}}(N_L+1)}{V_o^2D'^2}\right)>1$	$\frac{R_d\left(\frac{T_sDV_g}{2L}\right)^2}{3}$

II. Steady-State and Stability Analyses of the Passive Solution

The design of the LFR for the five cases of Fig. 2 must consider the effect of the resistance R_d of the emulated resistor in the steady-state output voltage of both LFR and boost converter as well as in the resulting stability margin of the latter. This aspect must be complemented with the calculation of the minimum value of the required power for stabilization. The characteristic polynomial corresponding to the linearized averaged model of the boost converter in each of the five cases depicted in Fig. 2 is illustrated in Table I together with the resulting stability margin and the minimum power required for stabilization. It should be noted that the topologies (c), (d), and (e) introduce one reactive element to the plant, thereby increasing the order of the characteristic polynomial.

Notably, in these higher-order topologies, power dissipation is significantly lower than in Fig. 1b, Fig. 2a, and Fig. 2b because no DC current flows through the damping resistors, which means that dissipation is only produced by the ripple of the state variable being damped. Consequently, the minimum power for stabilization dissipated by R_d will depend on:

1) the RMS value of the ripple of v_o in case (c)
2) the RMS value of the ripple of i_{Ld} in case (d)
3) the RMS value of the ripple of i_L in case (e)

To estimate the minimum power losses in the dampers, a triangular approximation is considered in the ripple waveforms of the state variables, as represented in Fig. 3.

In the expressions of Table I , V_o is the DC value of the output voltage, P_{CPL} is the power demanded by the load, D is the duty cycle, C and L are the capacitor and inductor of the boost converter respectively, T_s is the switching period, and R_d, L_d and C_d are the respective resistance, inductance and capacitance of the damper. In addition, the ratio between damper capacitor and boost capacitor, and between damper inductor and boost inductor is defined as $N_C = C_d/C$ and $N_L = L_d/L$.

It can be observed that the value of R_d is comprised between upper and lower limits for stability in the purely resistive damping cases (a) and (b) of Fig. 2, and that the load power demand P_{CPL} establishes directly the minimum power for stabilization in both cases.

A. R_d in parallel with L

This proposal does not modify the steady-state DC waveforms of the boost converter. Nonetheless, the minimum power that the damper must process is $D \cdot P_{\mathrm{CPL}}$, which means that the required stabilizing converter must have a considerable power processing capability.

Furthermore, the resistive element is floating in the input mesh of the main bus and therefore the input voltage of the active damper would be discontinuous, this hindering the systematic implementation of the LFR by means of sliding-mode control [20].

B. R_d in parallel with C

This topology also does not affect the DC waveforms of the boost converter. However, the lower the value of R_d is, the more damped the dynamic behavior results. The use of this topology would imply that the minimum power processed by the damper is P_{CPL}, i.e. the stabilizing converter absorbs the same power as the main converter, and hence the input source v_g must provide at least $2 \cdot P_{\mathrm{CPL}}$. This drawback could be mitigated in an active implementation by reinjecting the stabilizing power into the input source.

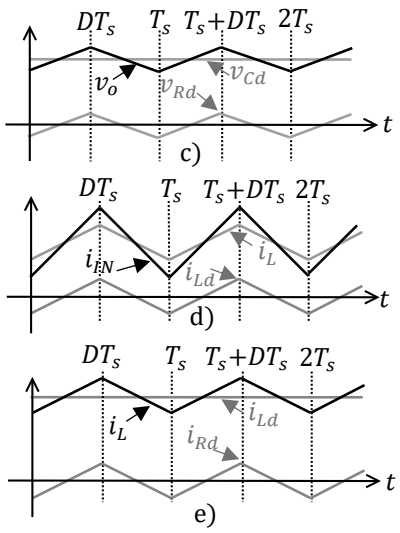

Fig. 3. Waveforms of the state variables involved in the damping filter (c) R_d-C_d in parallel with C (d) R_d-L_d in parallel with L (e) $R_d//C_d$ in series with L.

C. $R_d - C_d$ in parallel with C, $R_d - L_d$ in parallel with L, $R_d//L_d$ in series with L

Alternatively, in the cases (c), (d), (e) of Fig. 2, the stability region can be represented in the parametric plane $N - R_d$ for a fixed value of P_{CPL} and V_o, as indicated in Fig. 4, where the stability region of each topology is shown. Note that N corresponds to N_C in case (c) and to N_L in cases (d) and (e).
In particular, the $R_d - C_d$ in parallel with C topology presents the highest upper limit at R_d = 800 Ω. On the other hand, the

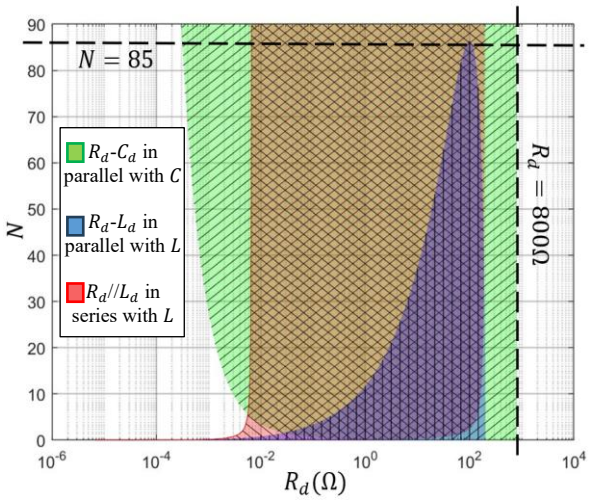

Fig. 4. Stability region of the system for the three proposed damping filters in the parametric plane defined by $N - R_d$ for $N = N_C = N_L$, L =160 μH, C =30 μF, D =0.5, P_{CPL}= 200 W and V_o= 400 V.

$R_d//L_d$ in series with L connection allows lower values of R_d, although with a marginally stable response.

Finally, for the $R_d - L_d$ in parallel with L damping network, the maximum value of N is around 85, which means that L_d can only be this number of times bigger than L. This topology allows values of N lower than 1 and in fact, for a fixed R_d, the lower the value of N is, the more damped the response results. By selecting one of the points within the defined region, the damping filter can be designed to ensure the system operation at a stable point.

III. Topological Selection of the Active Damper

In this section, we select the most appropriate candidate for the active implementation of the damping system.

In this framework, candidates (a) and (b) from Fig. 2 are discarded in advance due to their high stabilization power requirement in the damping circuit.

In addition, galvanic isolation between buses is considered an indispensable requirement in most of the multi-bus applications. For this reason, the LFR-based stabilizer must either be connected to the main circuit through a transformer or implemented in a converter topology with galvanic isolation. A priori, this second option requires high order topological circuits, and therefore it is also discarded.

The introduction of a transformer also increases the system's order and can severely disrupt the operation of the damped boost topologies proposed in Fig. 2 due to the impact of its parasitic inductances.

On the other hand, Figs 5a, 5b and 5c illustrate the resulting interconnection of the boost converter and the LFR emulating R_d in cases (c), (d), and (e) of Fig. 2 respectively. The connection of the damper by means of a transformer increases the dynamics order by one in Figs 5a and 5b. On the contrary, the order of the system is not affected in Fig. 5c, i.e. $R_d//L_d$ in series with L, in which the magnetizing inductance L_m of the transformer can play the role of the inductor L_d. For this reason, the $R_d//L_d$ in series with L topology is chosen as the candidate to be implemented.

IV. LFR-Based Damper Design

The sizing of the filter components can be calculated using the Middlebrook criterion [17]–[18]. The design has also to take into account the dynamic requirements of the system, as proposed in [21] together with the limitations of volume, weight and cost of the prototype. In this case considering the availability of components for the experimental prototype, it has been established a value of N = 14.38. Hence, R_d= 4.71 Ω has been chosen to ensure an overshoot under 30 %. Since the design must be versatile enough to supply a secondary bus or to reinject the damping power to another part of the system architecture, either the transformer ratio, the converter voltage DC gain, or both must be bigger than 1. We propose a 1:n transformer ratio and the boost topology also in the LFR stage as shown in Fig. 6, in which the power absorbed by the input port of the LFR is reinjected into a battery represented by a constant voltage source with open circuit voltage v_B and internal resistance R_B. The boost converter is chosen to implement the LFR because it is the simplest topology with a series inductor in the input port that can be used to emulate a resistor in that port by means of sliding-mode control (SMC) as discussed in [20]. The input inductor implies a continuous input current in the converter and therefore the direct use of that current in any SMC scheme. Note, however, that the output port of the damper is limited in this case to voltage step-up operation with respect to its input port. For that reason, the Ćuk or the non-isolated SEPIC, which also have a series input inductor, can be used if voltage step-down in the damper is required.

It is worth noting the presence of the diode rectifier bridge

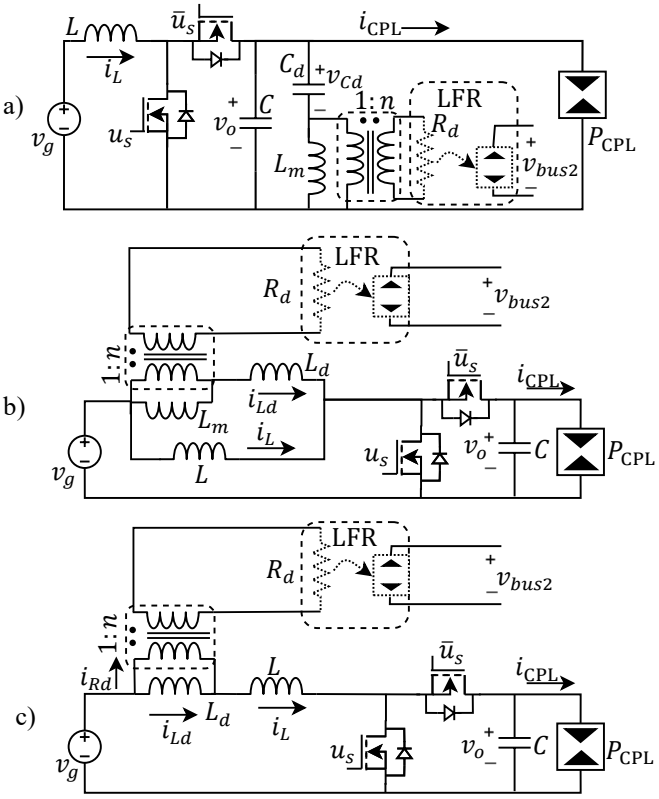

Fig. 5. Interconnection of the boost converter and the LFR emulating R_d (a) $R_d - C_d$ in parallel with C (b) $R_d - L_d$ in parallel with L (c) $R_d//L_d$ in series with L.

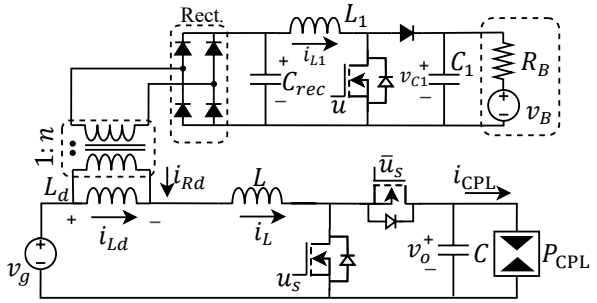

Fig. 6. Emulation of R_d by means of an LFR implemented with a boost converter that supplies a battery with open circuit voltage v_B and internal resistance R_B.

between the secondary port of the transformer and the LFR input, which is added to provide a current waveform with non-zero average value to the stabilizer input port. This modification does not alter the dynamics of the original system and allows the unidirectional behavior of the LFR converter. However, the converter emulating the resistance R_d must have a capacitor at its input port with enough capacitance to ensure a negligible voltage ripple at the LFR input. Based on the first harmonic approximation, the equivalent resistance R_d reflected in the primary side of the transformer will be (see Appendix I):

$$R_d = 2R_e \frac{D(1-D)\pi}{n^2} \frac{1}{\sqrt{2(1-\cos 2\pi D)}} \tag{1}$$

where R_e is the emulated resistance at the input of the LFR.

By particularizing the previous expression for a duty-cycle value of 0.5, one gets:

$$R_d|_{D=0.5} = R_e \frac{\pi}{4n^2} \tag{2}$$

If equality (2) is satisfied the behavior of the system will be the same as the one obtained with the passive network.

Therefore, the design of the LFR control loop must ensure that the damping converter is stable when emulating R_e at its input port.

V. Implementation of the LFR Boost Converter by Means of Sliding Mode Control

In this section, the implementation of the LFR boost converter, based on SMC (Fig. 7) is presented. The design uses the same procedure presented in [20], i.e. imposing proportionality between the voltage v_{Crec} at the input of the LFR and the current i_{L1} across the input port inductor, by applying an appropriate switching law and using a hysteresis comparator. The voltage V_{HYST} in Fig. 7 represents the hysteresis voltage of the controller; hence, the peak-to-peak input current ripple (scaled by R_e) will be equal to $2V_{HYST}$. It is worth noting that, unlike the approach in [14], the design of the LFR based on SMC does not require synchronization with the main boost converter or matching duty cycles as in [14]. This simplifies the implementation and enables variable switching frequency operation through the use of a hysteretic comparator.

As a result, the input port of the converter behaves as a resistor R_e and the output port as a power source, with voltage v_{C1} and current i_B.

$$v_{Crec} = R_e \cdot i_{L1} \tag{3}$$

$$v_{Crec} \cdot i_{L1} = v_{C1} \cdot i_B \tag{4}$$

Equation (3) is imposed by SMC while equality (4) expresses the power conservative nature of the converter [22].

A. Synthesizing LFR using SMC

Considering the boost converter of Fig. 7 operating in CCM, the differential equations describing the behavior of the converter are:

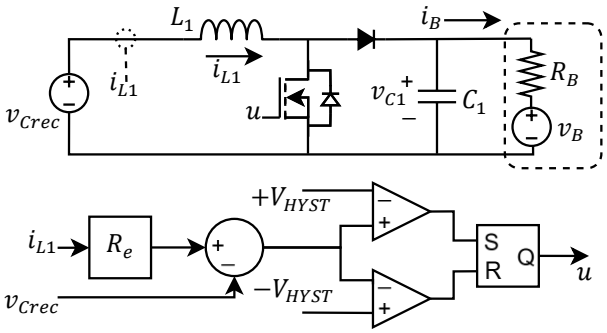

Fig. 7. Implementation of the SMC controller for the LFR of Fig. 6.

$$L_1 \frac{di_{L1}}{dt} = v_{Crec} - v_{C1}(1-u) \tag{5}$$

$$C_1 \frac{dv_{C1}}{dt} = i_{L1}(1-u) - \frac{v_{C1} - v_B}{R_B} \tag{6}$$

where u is a binary driving signal such that u = 1 during ON time duration and u = 0 during OFF time duration.

Assuming $S(x) = R_e i_{L1} - v_{Crec}$ and the switching law

$$u = 0 \text{ if } S(x) > 0; \quad u = 1 \text{ if } S(x) < 0 \tag{7}$$

we obtain

$$\frac{dS(x)}{dt} S(x) = R_e(R_e i_{L1} - v_{Crec}) \frac{V_{Crec} - v_{C1}(1-u)}{L_1} \tag{8}$$

If the condition $V_{Crec} - v_{C1} < 0$ is guaranteed in the boost converter, it can be deduced that if $S(x) > 0$ and $u = 0$ then $S(x) \cdot \frac{dS(x)}{dt} < 0$. Under the same condition, the same result is obtained for $S(x) < 0$ and $u = 1$. Therefore, the existence of sliding dynamics in the converter of Fig. 7 is confirmed with the selected switching function $S(x)$ and the associated switching law.

B. Equilibrium point of the system

The invariance condition $\frac{dS(x)}{dt} = 0$ results in an equivalent control $u_{eq} = 1 - v_{Crec}/v_{C1}$. By introducing the condition $S(x) = 0$ into the differential equations of the system and replacing u by u_{eq}, the following ideal sliding dynamics equations are obtained:

$$C_1 \frac{dv_{C1}}{dt} = \frac{v_{Crec}^2}{R_e \cdot v_{C1}} - \frac{v_{C1} - v_B}{R_B} \coloneqq g(v_{C1}) \tag{9}$$

$$i_{L1} = \frac{v_{Crec}}{R_e}$$

In steady-state, $v_{C1} = V_{C1}^*, i_{L1} = I_{L1}^*, v_{Crec} = V_{Crec}, v_B = V_B$ and $\frac{dv_{C1}}{dt} = 0$ which leads to the equilibrium point (10)

$$V_{C1}^* = \frac{1}{2}\left(V_B + \sqrt{V_B^2 + 4\frac{R_B}{R_e}V_{Crec}^2}\right); \; I_{L1}^* = \frac{V_{Crec}}{R_e} \tag{10}$$

C. Stability of the equilibrium point

The ideal sliding dynamic behavior is described by the nonlinear differential equation (9), which can be linearized around the equilibrium point resulting in $\frac{d\hat{v}_{C1}}{dt} = \alpha\hat{v}_{C1}$, where α is the single pole of the system given by

$$\alpha = \frac{1}{C_1}\cdot\frac{\partial g(v_{C1})}{\partial v_{C1}}\bigg|_{v_{C1}=V_{C1}^*} = -\frac{V_{Crec}^2}{C_1\cdot R_e\cdot V_{C1}^{*2}} - \frac{1}{C_1\cdot R_B} \qquad (11)$$

Notice that considering (11), the equilibrium point given in (10) is stable, since $\alpha < 0$. From expression (11), it is worth highlighting that the location of the system pole is determined by steady-state voltages, the capacitance C_1, and the emulated resistance, which is a controller parameter. Variations in the inductance only cause minor ripple changes, whereas variations in the capacitance affect the dynamics of the output voltage. Nevertheless, the overall system stability is primarily governed by the effectiveness of the emulated resistance at the converter input port, rather than by the specific dynamics of v_{C1}. Consequently, the SMC closed-loop dynamics remain essentially unaffected by parametric changes. Note that expressions (10) and (11) were already disclosed in [23], where an LFR supplying a generic nonlinear static load was analyzed.

VI. Simulation Results

This section presents simulation results of the system operating with the main converter supplying CPLs of 40 W and 200 W, powered by 20 V and 200 V sources, respectively. In the first test, shown in Fig. 8, the input current ripple is 2.5 A with a duty cycle of 0.35, resulting in an average output current of 0.5 A at the diode bridge. In the second test (Fig. 9), the ripple in the main converter increases to 4 A with a duty cycle of 0.5, and the current at the damper input reaches 1 A. In both cases, the damper supplies a constant voltage load that emulates a 12 V secondary battery.

Figs. 8 and 9 show the stabilizing effect of the proposed LFR-based damper for the set of parameter values given in Table II. In Fig. 8, the unstable behavior of the open-loop boost converter with a CPL is observed, leading to oscillations in the system variables. At t = 16 ms the damping system is activated resulting in stabilization of the converter at the desired operating point and supplying the LFR with 0.5 A current at its input. Note that the resulting output voltage in the main bus is

TABLE II
THE USED PARAMETER VALUES IN SIMULATION AND EXPERIMENTAL MEASUREMENTS

	Fig.8	Fig. 9		Fig.8	Fig. 9
L	160 µH		R_d	2.36 Ω	5 Ω
C	10 µF	30 µF	n	1	
f_s	15 kHz	160 kHz	C_{rec}	60 µF	
V_g	20 V	200 V	L_1	60 µH	
P_{CPL}	34 W	200 W	C_1	10 µF	
L_d	2300 µH		V_B	12 V	
D	0.35	0.5	R_B	1 Ω	

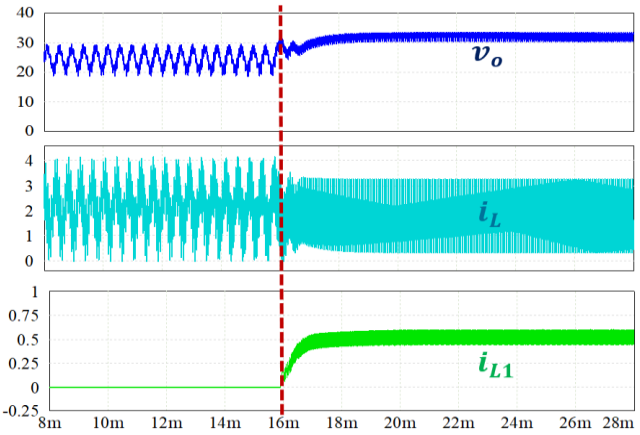

Fig. 8. Stabilizing effect of the proposed LFR-based damper which is applied at $t = 16$ ms to the open-loop boost converter with CPL operating in CCM.

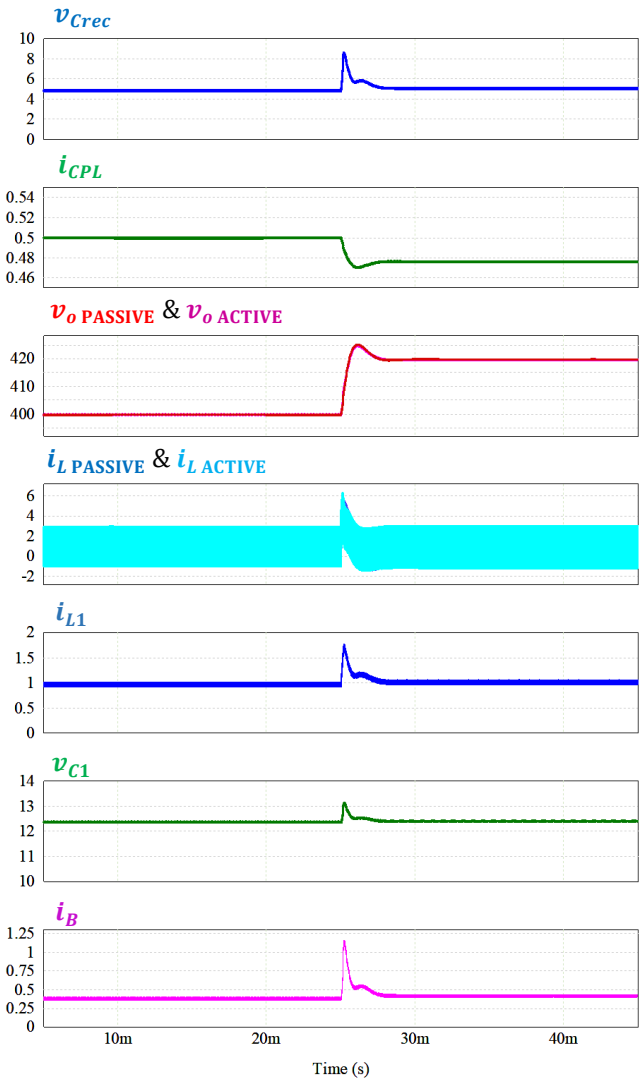

Fig. 9. Simulated response of the system to a 10 V voltage step change at the input in cases of active and passive damping.

exactly the same value predicted in the case of a passive damper.

The first test is conducted at a lower power level, requiring a different set of parameter values. Since this test is designed to demonstrate the damper's stabilizing capability, the system's unstable behavior is intentionally displayed. For safety reasons, the open-loop prototype output voltage was limited to 30 V with a load demand of 34 W.

The second test is carried out with an output voltage of 400 V and with a CPL power of 200 W. Fig. 9 shows the corresponding simulation result with a 10 V step change at the input of the main converter. The key feature highlighted in this figure is that the output voltage and input current waveforms of the actively damped system and the passively damped one match perfectly. This can be clearly observed in the figure by the perfect overlapping between $v_{o\,\mathrm{PASSIVE}}$ which corresponds to a passive damper, and $v_{o\,\mathrm{ACTIVE}}$ corresponding to an active one. The same occurs in the case of the currents $i_{L\,\mathrm{PASSIVE}}$ and $i_{L\,\mathrm{ACTIVE}}$. This fact demonstrates that the proposed LFR damper, in conjunction with the diode bridge and the high-frequency transformer, faithfully reproduces the behavior of a physical resistor.

The emulated resistance R_e is 6 Ω, which results in a damping resistance R_d of 4.71 Ω as predicted by expression (2), ensuring an overshoot of less than 30%. As in Fig. 8, the dynamic response of the state variables not only matches the passive damping case but also shows that the active solution introduces no changes in the main bus voltage waveform.

These results therefore confirm both the stabilizing effect and the correct emulation of a damping resistor by the proposed LFR active damper.

VII. Experimental Results

In order to validate the obtained theoretical and simulated results, an experimental prototype has been implemented. The values of the parameters used in the power circuits are summarized in Table II. C3M0120090D MOSFETS have been used in both converters. The used diode rectifier bridge has was implemented using C4D02120A device. On the other hand, the control stage has been implemented using LF347N operational amplifiers, AD633JNZ multiplier, LM319 comparator, CD4027BE flip-flop and IR2110 and TC4427 drivers for the main bus and for the stabilizer respectively.

The experimental setup includes a Kepco BOP 72-14MG power supply for the power stage and two Elektro-Automatik electronic loads: one EA-EL 9750-75 HP and one EA-EL 3400-25, which allow emulating the CPL and the constant voltage load v_B. Two Tektronix MD0314 Mixed Signal Oscilloscopes were also used to obtain the waveforms of both converters simultaneously and finally, a EL302RT DC source was employed to supply the control boards.

A picture of the experimental setup is shown in Fig. 10, providing a clear view of the hardware arrangement.

First, the nominal parameter values were selected to match those in Fig. 8, where a lower power level was used to ensure safe operation of the prototype. Fig. 11 shows the evolution of the state variables of the open-loop boost converter feeding a

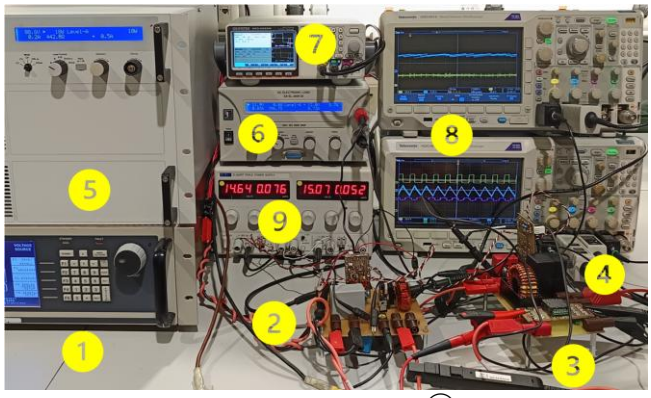

Fig. 10. Experimental setup containing: ① - The main power supply; ② - The main boost converter; ③ - The High frequency transformer; ④ - The LFR damper; ⑤ - The CPL; ⑥ - The Constant voltage load; ⑦ - The Wave function generator; ⑧ - Oscilloscopes; ⑨ - Control power supply.

CPL where the stabilizing effect of the proposed damper after $t = 16$ ms can be observed. The open-loop boost converter initially exhibits unstable behavior when supplying a CPL. The input voltage source, which is connected through a diode, is set at 18 V. The resulting oscillations match the simulation results presented in Fig. 8. As can be seen, these oscillations are eliminated after applying the LFR-based damper which is inserted in series with a secondary voltage source with a slightly higher voltage than the initial one (19 V). When it is connected, the first voltage source is disabled and current flows through the damping system, effectively blocking the current path through the input diode of the first source and redirecting all current through the damped branch. Once the system is supplied via the damper, the converter is stabilized, steady-state operation is reached within 2 ms, and the secondary converter receives an input current of 0.5 A. It is worth noting that the resulting output voltage and input current dynamics on the main bus closely match the predicted behavior. Minor discrepancies are observed due to the forward voltage drop of the diodes, though these are not significant.

Next, Fig. 12 illustrates the effect of a 10 V voltage step change in the input voltage of the primary bus. The system works initially at the same operating point of Fig. 9 and then evolves to a new equilibrium point following a transient behavior in response to the voltage change at the input. Note that the results show a remarkable agreement with the simulated behavior in Fig. 9 hence validating the theoretical predictions carried in the previous sections. The minor mismatches are due to the non-idealities in the rectifier bridge which are not modeled in the simulated scenario. This is the case of the voltage v_{Ld} at the input of the rectifier bridge, which is not perfectly square but is still in phase with current i_{Rd} as predicted in the Appendix. On the other hand, the power processed by the damper is approximately 6 W and represents 3% of the total power supplied by the voltage source v_g for the set of parameters listed in Table II. With a traditional passive damping network, the 6 W dissipated power would be lost. However, with the active approach, this power is effectively

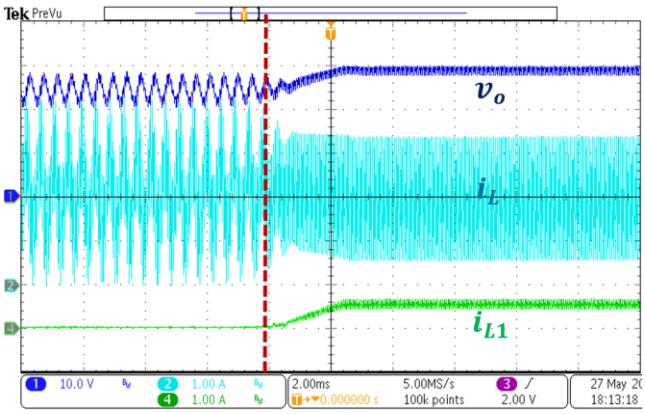

Fig. 11. Experimental validation of the stabilizing effect of the proposed damper after $t = 16$ ms in the open-loop boost converter with CPL.

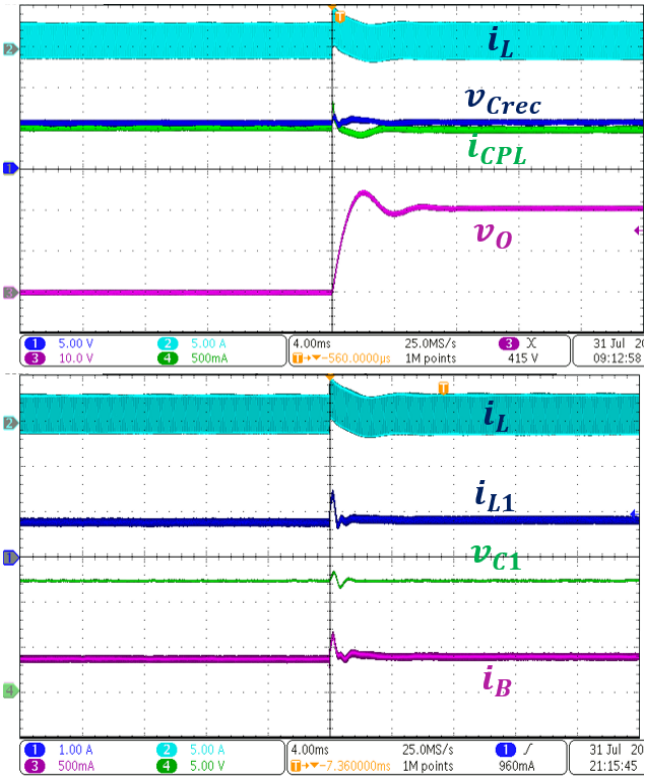

Fig. 12. Transient response of the experimental prototype to a step change in the input voltage using the LFR active damper.

harvested, improving the overall efficiency from 93% to 96% while maintaining the desired dynamic behavior. This value can be affected by variations in the input current ripple, which depends on switching frequency f_s, inductance L and the nominal value of v_g. Another factor to consider in the calculation of the damping power is a variation in the dynamic requirements, and therefore, in the damping resistance R_d.

Finally, Fig. 13 shows the steady-state waveforms of the two interconnected power converters. It can be seen that the synchronism between the switching frequency of the two systems and the matching of the two duty-cycles are not

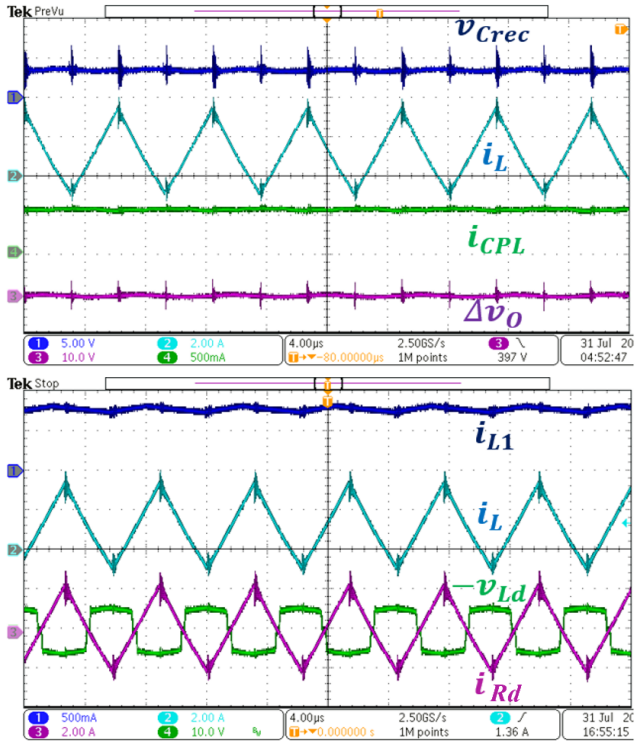

Fig. 13. Steady-state waveforms of the experimental prototype working in the operating point described in Table II.

necessary. This feature is visible in the input currents i_L and i_{L1} of both converters which are not synchronized, so the absence of this constraint represents a remarkable improvement over the SLFR-based active damper proposed in [14], where identical switching frequencies and duty-cycles for the main converter and the damper were indispensable. It should be also noted that the input current and voltage of the LFR are proportional while their reflected values in the primary side of the transformer are in phase, thus validating the analysis in both Section V and Appendix.

VIII. Discussion

Additional simulations have been performed to assess the scalability and versatility of the proposed LFR-based active damping method, and to highlight its improvements over previous implementations such as the SLFR stabilizer described in [14].

In [14], active damping was achieved by inserting the emulated resistor of the LFR in series with the inductor of elementary converters (buck, boost, and buck–boost). This configuration, known as SLFR, successfully emulated a damping resistance but presented several practical limitations. Specifically it required both the damper and the main converter to share the same switching frequency and duty cycle, which restricted the control strategy to fixed-frequency schemes to synthetize an LFR such as peak current mode control (PCMC).

Moreover, because the damping resistor processed the total current through the inductor, DC voltage drops and higher stabilization losses were unavoidable.

The proposed LFR architecture overcomes these limitations by introducing a parallel active damping topology, in which the emulated resistor at the input port of the LFR and the inductor L_d are connected in parallel and placed in series with the main inductor of the converter. In this configuration, the active damper only processes the AC ripple component of the current, thereby preserving the DC gain of the undamped converter and significantly reducing the power processed by the damper.

Furthermore, the new LFR design decouples the input current paths of the damper and the main converter, removing the synchronization constraint of [14] and enabling the possibility of using different switching frequencies and duty cycles. This flexibility allows the application of more advanced and robust control techniques such as SMC with its inherent variable switching frequency, while maintaining stability under CPL conditions. To validate these theoretical advantages, additional simulations have been carried out.

First, to evaluate adaptability to multi-bus configurations, the original setup was extended by adding a third tightly regulated bus in parallel with the main one, as illustrated in Fig. 14. This scenario replicates the stability challenges typically found in cascaded converter systems with tight voltage regulation. The simulation results shown in Fig. 15 confirm that the proposed approach remains effective in complex power distribution networks including more than two buses.

The third bus is supplied by a boost converter with parameters $L_3 = 600\ \mu H$, $C_3 = 20\ \mu$F, feeding a resistive load of $R_3 = 600\ \Omega$. This additional bus subtracts 600 W from the main bus and is regulated through two feedback loops: one maintaining the output voltage at v_{bus3} = 600 V and another ensuring an input current of i_{L3} =1.5 A. To emphasize the independent operation of each subsystem, different switching frequencies have been assigned; namely, 50 kHz for the main converter, 200 kHz for the parallel bus, and 75 kHz for the active damper.

The results demonstrate that the active damping network accurately reproduces the behavior of a resistive stabilizer under small-signal perturbations in the load power demand. In this context, each additional bus connected in parallel can be interpreted as an increment of the CPL demand, confirming the applicability of the LFR-based stabilization strategy to more complex power architectures.

Secondly, the scalability in power was studied by adapting the system parameters to an electric vehicle (EV) powertrain application. In this setup, a 300 V battery feeds a boost converter that steps up the voltage to 600 V, supplying an inverter–motor set modeled as a 50 kW CPL. This condition emulates the constant mechanical power operation of an EV under steady torque and speed, where the traction system behaves as a CPL from the perspective of the DC bus. Other system parameters are $L = 55\ \mu H$, $C = 90\ \mu$F, $R_d = 0.7\pi/4\ \Omega$ and a magnetizing inductance of 2.3 mH.

The results confirm that the proposed active damping approach preserves stability and reproduces the dynamics of a resistive stabilizer under 1% step-change in the CPL in a much higher power system.

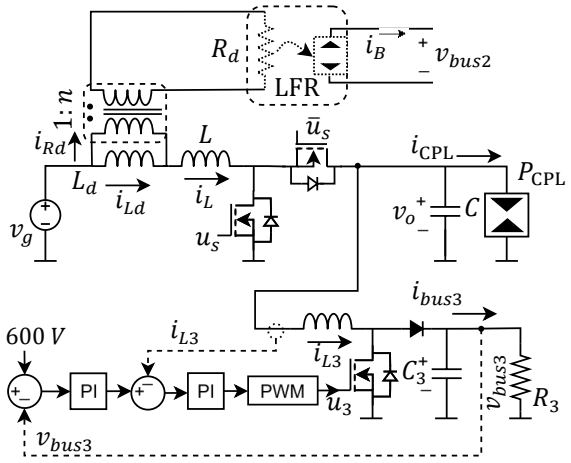

Fig. 14. Three-bus system made up of a 400 V main bus supplying a 200 W CPL, an LFR-based active damper feeding a 12 V battery, and a third parallel bus with a 600 V resistive load.

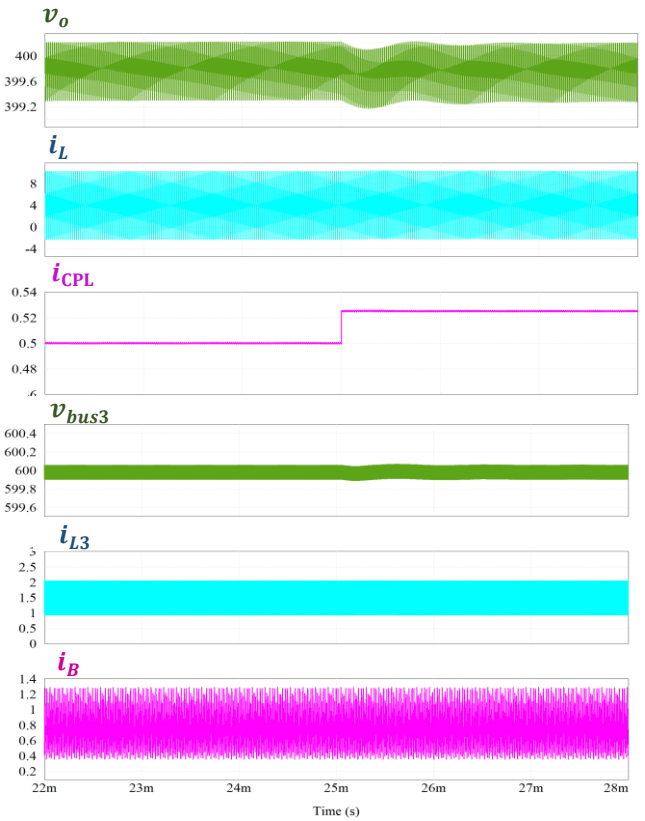

Fig. 15. Simulation results for a 1% transient of CPL power demand in the system described in Fig. 14.

IX. Conclusions

Active damping methods reported in the literature are based on the emulation of a passive element through an appropriate control strategy. This implies the design of the closed-loop control of the power system that benefits from the damping, which is appropriately introduced in the control strategy.

Unlike the closed-loop control damping methods, the solution proposed here has been based on the insertion of a two-port circuit in the topology of the power converter supplying a CPL

to stabilize the open-loop operation of the power converter and recycle the required energy for stabilization to other uses in a multi-bus system. The first proposal in the design of this type of active damper consisted in the insertion of the emulated resistor of the LFR in series with the inductance of the elementary converters buck, boost and buck-boost, which originated a new notion of SLFR [14].

This paper has extended the methodology of replacing the passive damping resistor with the emulated resistance at the input port of an LFR to other damping topologies. The main advantage of this active approach is the significant reduction in power losses compared to the passive solutions. Additionally, this active implementation enables the emulation of an adjustable resistor that can dynamically adapt to variations in the power demanded by the load, as well as to changes in the input/output voltage or any other set-point modification. As a result, it ensures that the system's operating point remains within the stability region, while keeping the open-loop dynamics of the main converter as invariant as possible.

Considering a boost converter in the main bus, the most appropriate candidate for active damping has been selected in a comparative analysis among five possible networks. The analysis has taken into account both the minimum power required for stabilization and the minimum increment of the dynamic order resulting from the transformation. The chosen passive damping topology consists of a resistor R_d in parallel with an inductor L_d. This network is placed in series with the inductor L of the main boost converter. Unlike the approach in [14], this topology preserves the DC gains of the undamped converter since the damping resistor only processes the AC current ripple of the input inductor. As a result, the minimum power dissipation required for stabilization is significantly reduced, and the suppression of the DC voltage drop in series with the main inductor improves the overall operation of the system. However, this improvement comes at the cost of increasing the system's order due to the addition of L_d.

The resulting damper is implemented using a boost converter whose input port is connected to the main bus through a high-frequency transformer and a full-wave rectifier, providing galvanic isolation and ensuring unidirectional energy flow. As a result, the proposed architecture is modular and the operating point of the required power stages is decoupled, which not only simplifies the prototype integration but also enhances its potential scalability across a wide range of applications and parameter sets. The damper can be designed independently of the main converter, making it suitable for plug-and-play deployment. Despite introducing an additional converter, the overall system cost remains low, as the damper also supplies power to a secondary bus. In multi-bus systems, each bus inherently requires its own converter, and the proposed architecture does not add extra converters to a two-bus system but rather redefines their interconnection. This reconfiguration improves both stability and dynamic performance without compromising modularity or requiring redesign of existing subsystems.

The experiments have demonstrated that the power required for stabilization can be successfully reinjected into a battery in a secondary bus. This possibility could be further explored in future work to develop constant power–constant voltage battery charging protocols, as reported in [24].

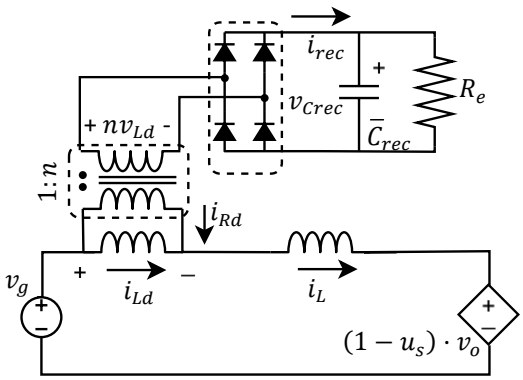

Fig. 16. Equivalent circuit model of the interconnection of the input port of the LFR based damper and the main converter.

APPENDIX

The equivalent resistance R_d reflected in the primary side of the transformer can be approximated by the ratio of the amplitude $V_{Ld\,1}$ of the first harmonic of the voltage v_{Ld} and the amplitude $I_{Rd\,1}$ of the first harmonic of the current i_{Rd} represented in Fig. 16.

$$R_d = \frac{V_{Ld\,1}}{I_{Rd\,1}} \tag{A1}$$

The assumption of constant voltage in C_{rec} in Fig. 16 implies a square wave signal v_{Ld} with two regions of equal absolute value $\frac{V_{Crec}}{n}$ but different sign, and a duration of half switching period each one at the input of the transformer as illustrated in Fig. 16. This discontinuous voltage modifies the waveform of voltage v_L in inductor L creating two different subintervals in both ON and OFF intervals. Thus, the ideal inductor current slope m_1 of the ON interval is substituted by slopes m_{11} and m_{12} during the corresponding subintervals introduced by the effect of v_{Ld}.

$$m_1 = \frac{V_g}{L},\ \ m_{11} = \frac{V_g + \frac{V_{Crec}}{n}}{L},\ \ m_{12} = \frac{V_g - \frac{V_{Crec}}{n}}{L} \tag{A2}$$

Similarly, the ideal inductor current slope m_2 of the OFF interval is substituted by slopes m_{21} and m_{22}.

$$m_2 = \frac{V_g - V_o}{L}$$
$$m_{21} = \frac{V_g - V_o - \frac{V_{Crec}}{n}}{L},\ \ m_{22} = \frac{V_g - V_o + \frac{V_{Crec}}{n}}{L} \tag{A3}$$

On the other hand, the waveform of i_{Ld} has two intervals of slope m_A and m_B as depicted in the upper part of Fig. 17.

$$m_A = -\frac{V_{Crec}}{nL_d},\ \ m_B = \frac{V_{Crec}}{nL_d} \tag{A4}$$

Therefore, the current i_{Rd} will present the four sub-regions shown at the bottom of Fig. 17 with the slopes

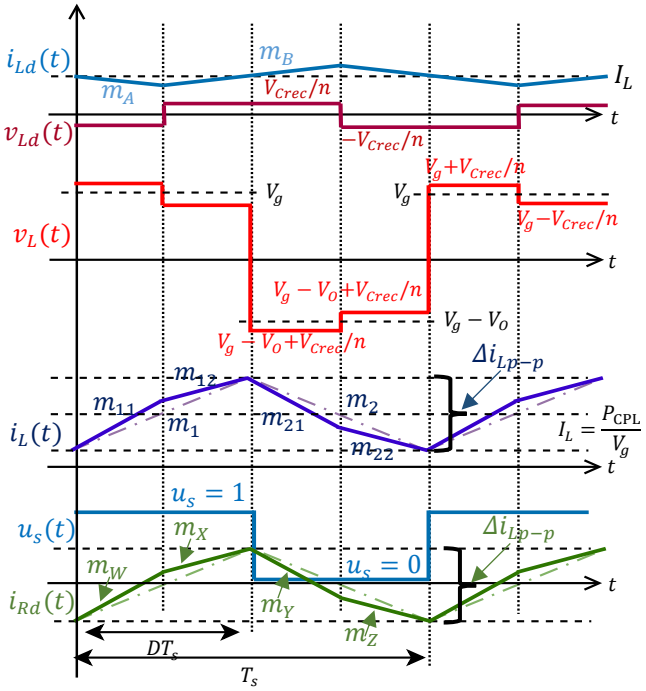

Fig. 17. Ideal waveforms in the input of the LFR based active damper.

$$m_W=\frac{V_g+\frac{V_{Crec}}{n}}{L}+\frac{V_{Crec}}{nL_d},\ m_X=\frac{V_g-\frac{V_{Crec}}{n}}{L}-\frac{V_{Crec}}{nL_d}$$
$$m_Y=\frac{V_g-V_o-\frac{V_{Crec}}{n}}{L}-\frac{V_{Crec}}{nL_d} \quad \text{(A5)}$$
$$m_Z=\frac{V_g-V_o+\frac{V_{Crec}}{n}}{L}+\frac{V_{Crec}}{nL_d}$$

The slopes m_W and m_X can be approximated by m_1; and m_Y and m_Z by m_2 if the following inequality is satisfied by design.

$$V_g \gg -\frac{V_{Crec}}{n}\left(1+\frac{L}{L_d}\right) \quad \text{(A6)}$$

The latter approximation results in a triangular waveform representation of i_{Rd} whose peak-to-peak ripple is exactly the peak-to-peak ripple Δi_{Lp-p} of inductor current i_L. Moreover, zero crossings of i_{Rd} coincide with those of v_{Ld} and their corresponding first harmonics are in phase.

In addition, since i_{rec} is the absolute value of i_{Rd} divided by n, voltage V_{Crec} will be given by the product of the dc value of i_{rec} and the emulated resistance R_e.

$$V_{Crec}=\frac{\Delta i_{Lp-p}R_e}{4n} \quad \text{(A7)}$$

Note that the high-frequency ripple amplitude in the capacitor C_{rec} will be given by

$$\Delta v_{Crec}=\frac{T_s}{16nC_{rec}}\Delta i_{Lp-p} \quad \text{(A8)}$$

From (A7) and (A8) the following expression for the relative ripple can be deduced.

$$\frac{\Delta v_{Crec}}{V_{Crec}}=\frac{T_s}{4R_eC_{rec}} \quad \text{(A9)}$$

Hence, the assumption of constant value for the voltage of capacitor C_{rec} will be valid if the switching period T_s is significantly smaller than the time constant R_eC_{rec}.

In addition, the amplitude of the first harmonic of v_{Ld} and i_{Rd} are given by

$$V_{Ld\,1}=\frac{4V_{Crec}}{n\pi}=\frac{\Delta i_{Lp-p}.R_e}{\pi n^2} \quad \text{(A10)}$$
$$I_{Rd\,1}=\frac{\Delta i_{Lp-p}}{2D(1-D)\pi^2}\sqrt{2(1-\cos(2D\pi))} \quad \text{(A11)}$$

Finally, from (A1), (A10) and (A11) we obtain

$$R_d=2R_e\frac{D(1-D)\pi}{n^2}\frac{1}{\sqrt{2(1-\cos(2\pi D))}} \quad \text{(A12)}$$

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M. Sebastià-Rullo received B.S. degrees in Electrical Engineering and Industrial Electronics and Automation Engineering, as well as an M.Eng. in Electric Vehicle Technologies from Universitat Rovira i Virgili, Spain, in 2020 and 2021. He joined the Automatic Control and Industrial Electronics Research Group (GAEI) as a Research Technician in 2021 and completed his Ph.D. with the same group in 2025. His research focuses on DC–DC converters, power converters stabilization, and renewable energy systems.

A. Cid-Pastor (Member, IEEE) received the Graduate degree in ingeniero técnico industrial en electrònica industrial and the degree in ingeniero en automàtica y electrònica industrial from Universitat Rovira i Virgili, Tarragona, Spain, in 1999 and 2002, respectively, the M.S. degree in design of microelectronics and microsystems circuits from Institut National des Sciences Appliquées, Toulouse, France, in 2003, and the joint Ph.D. degree from Universitat Politècnica de Catalunya, Barcelona, Spain, and Institut National des Sciences Appliquées, LAAS-CNRS, Toulouse, in 2005 and 2006, respectively. He is currently an Associate Professor with Departament d'Enginyeria Electrònica Elèctrica i Automàtica, Escola Tècnica Superior d'Enginyeria, Universitat Rovira i Virgili. His research interests are in the field of power electronics, power conditioning for electric vehicles, and renewable energy systems. He is a member of the Research Group in Automatic Control and Industrial Electronics (GAEI). He currently serves as a Subject Editor for Electronics Letters, Journal of Power Electronics, Energy Conversion, and Sustainability.

H. Valderrama-Blavi (Member, IEEE) received the M.S. degree in ingeniero de telecomunicación and the Ph.D. degree from Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1994 and 2001, respectively. In 2001, he got a post-doctoral research position with Laboratoire d'Analyse et Architecture des Systèmes of the Centre National de la Recherche Scientifique (LAAS-CNRS), Toulouse, France, where he remained for one year. Since 2003, he has been an Associate Professor with the Department of Electrical, Electronics, and Automatic Control Engineering (DEEEA), Universitat Rovira i Virgili, Tarragona, Spain. From February 2018 to February 2022, he was the academic responsible of the master of electric vehicle technologies. He is currently the Director of the Electronic Engineering and Automatic Control Department (DEEEA). Since 2003, he has been a main Researcher (IP) of five research projects financed by Spanish Ministry of Science and Technologies, he has coauthored more than 40 journal articles and has got a Full Professor accreditation from ANECA, since June 2022. He is working interests are power electronics for renewable energy and distributed generation systems, efficient lighting, high voltage gain conversion, applications for silicon carbide devices, nonlinear control for power converters, active stabilization networks based on loss free resistor (LFR), multifrequency AC-buses, and fast chargers and battery modeling for electrical vehicles.

A. El Aroudi (Senior Member, IEEE) received the bachelor's degree in physical science from Faculté des Sciences, Université Abdelmalek Essaadi, Tetouan, Morocco, in 1995, and the Ph.D. degree (Hons.) in applied physical science from Universitat Politècnica de Catalunya, Barcelona, Spain, in 2000. He is currently a Full Professor with the Department of Electronics, Electrical Engineering and Automatic Control, Rovira i Virgili University, Tarragona, Spain. His research interests include the field of dynamics, design and control of power conditioning for electric vehicles and renewable energy applications, power factor correction, and battery modeling. He was an Associate Editor of the IET Circuits, Devices & Systems, the IET Power Electronics, and the IET Electronics Letters. He was also a Guest Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS ON CIRCUITS AND SYSTEMS in 2015, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS in 2018, and Energies from 2018 to 2019. From 2019 to 2023, he was a Topic Editor of Energies. He currently serves as an Associate Editor for International Journal of Circuit Theory and Applications.

L. Martínez-Salamero (Life Senior Member, IEEE) received the ingeniero de telecomunicación degree in 1978 and the Ph.D. degree in 1984, both from Universidad Politécnica de Cataluña, Barcelona, Spain. He was given the Doctor Honoris Causa degree in 2024 from Université Toulouse III Paul Sabatier, France. From 1978 to 1992, he taught circuit theory, analog electronics and power processing in the Escuela Técnica Superior de Ingenieros de Telecomunicación in Barcelona, Spain. From 1992 to 1993, he was a Visiting Professor with the Center for Solid State Power Conditioning and Control, Department of Electrical Engineering, Duke University, Durham, NC, USA. From 2003 to 2004, from 2010 to 2011, and from March 2018 to September 2018, he was a Visiting Scholar with the Laboratory of Architecture and Systems Analysis (LAAS), National Agency for Scientific Research (CNRS), Toulouse, France. Since 1995, he has been a Full Professor with the Department of Electrical Electronic and Automatic Control Engineering, School of Electrical and Computer Engineering, Rovira i Virgili University, Tarragona, Spain, where he managed the Research Group in Automatic Control and Industrial Electronics (GAEI) (1998–2018). His research interests include structure and control of power conditioning systems, namely, electrical architecture of satellites and electric vehicles, nonlinear control of converters and drives, and power conditioning for renewable energy. He has published a large number of papers in scientific journals and conference proceedings in the fields of modeling, simulation, and control of power converters; and holds a U.S. patent on dual voltage electrical distribution in vehicles. He was a Guest Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS Special Issue on Simulation, Theory and Design of Switched-Analog Networks in August 1997. He organized in cooperation with European Space Agency (ESA) the Fifth European Space Power Conference (ESPC-98) in Tarragona and served during two terms (1996–2002) as the Dean of the School of Electrical and Computer Engineering. He was the President of Spanish Joint Chapter of the IEEE Power Electronics and Industrial Electronics Societies from 2005 to 2008 and a Distinguished Lecturer of the IEEE Circuits and Systems Society (2001–2002). He is currently a Distinguished Professor of Rovira i Virgili University.